Functional Safety Information

TPS4141-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for the TPS4141-Q1 (11 DWQ package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the functional block diagram of TPS4141-Q1 for reference.

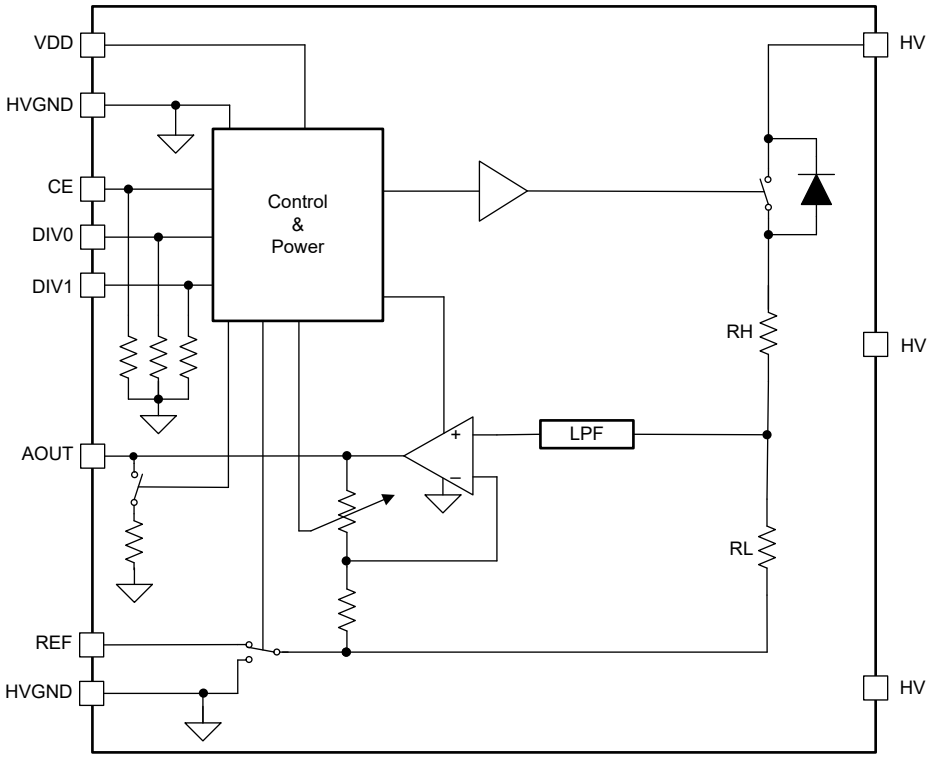

Figure 1-1. TPS4141-Q1 Functional Block Diagram

TPS4141-Q1 was developed using a quality-managed development process, but was not developed in accordance with IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the TPS4141-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	22
Die FIT rate	4
Package FIT rate	18

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 200mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog or mixed	30 FIT	75°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS4141-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Switch partially ON when enabled	40.46
Primary side ON – current higher than the specification	7.12
Switch stuck OFF	5.76
High leakage	35.36
Incorrect HV measurement	11.3

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS4141-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (HVGND) (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to adjacent pin (see Table 4-4)
- Pin short-circuited to VDD (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the TPS4141-Q1 pin diagram package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS4141-Q1 datasheet.

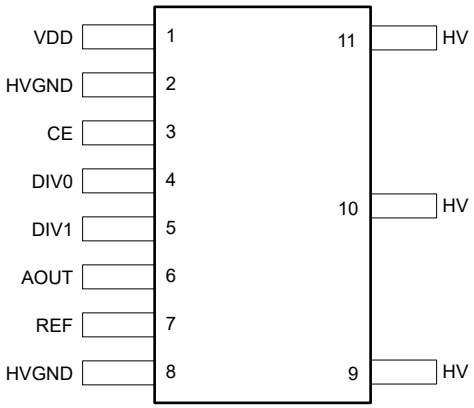

Figure 4-1. TPS4141-Q1 Pin Diagram

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Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	The device is in the OFF state (UVLO). The switch is in the OFF state.	B
HVGND	2	There is no effect on the device.	D
CE	3	The device is in the OFF state. The switch is in the OFF state.	B
DIV0	4	The fault condition can potentially modify the divider ratio (DIV_{NOM}) selection.	B
DIV1	5	The fault condition can potentially modify divider ratio (DIV_{NOM}) selection.	B
AOUT	6	If the AOUT pin is the driving pin, additional current can potentially occur. If the AOUT pin is high, there can be large current flow and the AOUT buffer is potentially damaged.	A
			B
REF	7	If the REF pin is tied to the HVGND pin in application, the device operates normally; otherwise, the functionality of the device is effected.	C
			D
HVGND	8	There is no effect on the device.	D
HV	9	There is no effect on the device. The pin is isolated from the die pad.	D
HV	10	There is no effect on the device. The pin is isolated from the die pad.	D
HV	11	The device measures the V_{HV} - V_{REF} voltage.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	The device is in the OFF state (UVLO). The switch is in the OFF state.	B
HVGND	2	There is no effect on the device.	C
CE	3	The device is in the OFF state. The switch is in the OFF state.	B
DIV0	4	The fault condition can potentially modify the divider ratio (DIV_{NOM}) selection.	B
DIV1	5	The fault condition can potentially modify the divider ratio (DIV_{NOM}) selection.	B
AOUT	6	There is no effect on the device.	D
REF	7	This fault condition results in a HV measurement error if the device is operated in bi-directional mode.	B
HVGND	8	There is no effect on the device.	D
HV	9	This pin is not internally connected. There is no effect on the device.	D
HV	10	This pin is not internally connected. There is no effect on the device.	D
HV	11	The device measures the V_{REF} voltage or 0V.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	2	The device is in the OFF state (UVLO). The switch is in the OFF state.	B
HVGND	2	3	The device is in the OFF state. The high-voltage switch is in the OFF state.	B
CE	3	4	The divider settings are limited. If the CE pin is low, the device shuts down, and the switch remains open.	B
				D
DIV0	4	5	The fault condition modifies the divider ratio (DIV_{NOM}) selection.	B
DIV1	5	6	If the DIV1 pin is driven higher than 6V, the AOUT pin buffer is potentially damaged.	A
				B
AOUT	6	7	When the device is enabled, the AOUT buffer drives the REF pin so large current potentially flows and causes damage to the AOUT buffer.	A
				B
REF	7	8	The device performs uni-directional measurement if the REF pin shorts to the HVGND.	B
HV	9	10	There is no effect on the device. TI recommends this connection.	D

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Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to Pin No.	Description of Potential Failure Effects	Failure Effect Class
HV	10	11	There is no effect on the device. TI recommends this connection.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VDD	1	There is no effect on the device.	D
HVGND	2	The device is in the OFF state (UVLO). The switch is in the OFF state.	B
CE	3	The device is always enabled.	B
DIV0	4	The fault condition modifies the divider ratio (DIV_{NOM}) selection.	B
DIV1	5	The fault condition modifies the divider ratio (DIV_{NOM}) selection.	B
AOUT	6	If the voltage at the drain (VDD) is greater than 6V, there is potentially damage to the device. If VDD is less than 6V, and the AOUT pin is being driven low, a large current flows and potential damages the AOUT buffer.	A B
REF	7	If VDD is above 4.5V, there is potentially damage to the device.	A B
HVGND	8	The device is in the OFF state (UVLO). The switch is in the OFF state.	B
HV	9	If the HV pin exceeds the VDD absolute maximum, damage to the device potentially occur.	A
HV	10	If the HV pin exceeds the VDD absolute maximum, damage to the device potentially occur.	A
HV	11	If the HV pin exceeds the VDD absolute maximum, damage to the device potentially occur.	A

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5 Revision History

DATE	REVISION	NOTES
July 2026	*	Initial Release

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