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Mr Nilkanth Pathak

Offenbach, 2026-04-27

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Translation: In any case the German version shall prevail

P R Ü F B E R I C H T
zur Information des Auftraggebers

Test Report for the Information of the applicant

Produkt / *Product*:

Microcontroller Selbstdiagnose Bibiliothek.
Microcontroller self-diagnostic library package

Version: 6.01.00

For Microcontroller device families

F28002x, F28004x, F2838x.

F28E12x, F280013x, F280015x, F28003x, F28P55x, F28P65x , F28P551x.

Dear Sirs,

dieser Prüfbericht enthält das Ergebnis einer einmaligen Untersuchung an dem zur Prüfung vorgelegten Erzeugnis. Ein Muster dieses Erzeugnisses wurde geprüft, um die Übereinstimmung mit den nachfolgend aufgeführten Normen bzw. Abschnitten von Normen festzustellen.
Die Prüfung wurde durchgeführt vom 2026-03-02 bis 2026-03-26.

This test report contains the result of a singular investigation carried out on the product submitted. A sample of this product was tested to found the accordance with the thereafter listed standards or clauses of standards resp. The testing was carried out from 2026-03-02 to 2026-03-26.

Der Prüfbericht berechtigt Sie nicht zur Benutzung eines Zertifizierungszeichens des VDE und berücksichtigt ausschließlich die Anforderungen der unten genannten Regelwerke.

The test report does not entitle for the use of a VDE Certification Mark and considers solely the requirements of the specifications mentioned below.

Wenn gegenüber Dritten auf diesen Prüfbericht Bezug genommen wird, muss dieser Prüfbericht in voller Länge an gleicher Stelle verfügbar gemacht werden.

Whenever reference is made to this test report towards third party, this test report shall be made available on the very spot in full length.

REMARK: VDE DETAIL TESTREPORT REFERENCE: VDE 340961-TL2-1

I – ANGEWENDETE STANDARDS / *STANDARDS APPLIED*

DIN EN 60335-1 (VDE 0700-1):2024-07
EN 60335-1:2012+AC+A11+A13+A1+A2+A14-A16:2023
ANHANG R; KLASSE R1 und *R2
ANNEX R; CLASS R1 and *R2

IEC 60335-1:2010, + COR1:2010 + COR2:2011 + A1:2013, + A1:2013/COR1:2014 + A2:2016 + A2:2016/COR1:2016
ANHANG R; KLASSE R1 und *R2
ANNEX R; CLASS R1 and *R2

DIN EN 60730-1 (VDE 0631-1):2025-05
ANHANG H; KLASSE B und *C
ANNEX H; CLASS B and *C

IEC 60730-1: 2022 +A11:2024

WEITERHIN/*FURTHERMORE*
IEC 60730-1:2013
IEC 60730-1:2013/AMD1:2015
IEC 60730-1:2013/AMD2:2020
ANHANG H; KLASSE B und *C
ANNEX H; CLASS B and *C

ANMERKUNG: Die Anforderungen der Normenreihe 60730-1 Anhang H für Klasse B & C, Ausgabedaten 2022 und 2020 sind vergleichbar.
REMARK: The requirements of 60730-1 annex H for class B and C are comparable between the 60730-1 versions of 2020 and 2022.

ANMERKUNG: Die Anforderungen der Normenreihe 60730-1 Tabelle H für Klasse B & C und der 60335-1 Tabelle R1 für Klasse R1 & R2 sind vergleichbar.
REMARK: The requirements of 60730-1 table H for class B and C are comparable to table R1 of 60335-1 for class R1 and R2.

*Anmerkung: Manche Typen der Familie verfügen über Co-Prozessoren oder 2 Kerne. Hier kommt ein Lockstep Test zum Einsatz der Anforderungen einer Klasse C erfüllen kann. Weiterhin kann reziproker Vergleich genutzt werden.
*Remark: Some devices covered by this test report have co processors or 2 cores, for such devices a lockstep test was provided, which can fulfil requirements of class C. Furthermore reciprocal comparison can be used.

*Types complying with Class C measures.
F280015x; F28002x; F2838x; F28003x; F28004x; F28P55x; F28P65x.

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II – SELBSTDIAGNOSE ROUTINEN / *SELF-DIAGNOSTIC ROUTINES*
ENGLISH DESCRIPTION ONLY

TABLE H.2 – MEASURES TO ADDRESS FAULT/ERRORS (Software Class B)			
Component	Fault/error	Declared measures	Verdict
1. CPU	-	-	-
1.1 Registers	Stuck at	Static register test (Pattern) Assembly language used. AA & 55 patterns	P
1.3 Program counter	Stuck at	Remark 1: watchdog timers may be used to supervise the program execution	P
2. Interrupt handling and execution	No interrupt	Remark 1: watchdog timers may be used to supervise the program execution	P
	Too frequent interrupt	Remark 1: watchdog timers may be used to supervise the program execution	P
3. Clock	Wrong frequency (for quartz synchronized clock: harmonics/ sub-harmonics only)	Comparison of 2 timers. DCC (Dual clock comparator)	P
4. Memory	-	-	-
4.1 Invariable memory	All single bit faults	CRC32Bit Remark: Additional integrated measure (ECC) is available.	P
4.2 Variable memory	DC fault	March 13N Test Remark: Additional integrated measures like ECC or Parity are available.	P
4.3. Addressing (relevant to variable and invariable memory)	Stuck at	March 13N Test Remark: Additional integrated measures like ECC or Parity are available.	P

5. Internal data path	-	-	-
5.1 Data	Stuck at	With measures acc. to clause 4	P
5.2 Addressing	Wrong address	With measures acc. to clause 4	P
6. External communication	-	-	-
6.1 Data	Hamming distance 3		N/A
6.2 Addressing	Wrong address		N/A
6.3 Timing	Wrong point in time		N/A
	Wrong sequence		N/A
7. Input/output periphery	-	-	-
7.1 Digital I/O	Fault conditions specified in Cl.H.13		N/A
7.2 Analog I/O	-	-	-
7.2.1 A/D and D/A-convertor	Fault conditions specified in Cl. H.13		N/A
7.2.2 Analog multiplexer	Wrong addressing		N/A
9. Custom chips e.g. ASIC, GAL, gate array	Any output outside the static and dynamic functional specification		N/A

TABLE H.2 – MEASURES TO ADDRESS FAULT/ERRORS (Software Class C)

Component	Fault/error	Declared measures	Verdict
1. CPU	-	-	-
1.1 Registers	DC fault	Lockstep & HW BIST Methodology. Reciprocal comparison.	P
1.2 Instruction decoding and execution	Wrong decoding and execution	Lockstep & HW BIST Methodology. Reciprocal comparison.	P
1.3 Program counter	DC fault	Lockstep & HW BIST Methodology. Reciprocal comparison.	P

1.4 Addressing	DC fault	Lockstep & HW BIST Methodology. Reciprocal comparison.	P
1.5 Data paths instruction decoding	DC fault	Lockstep & HW BIST Methodology. Reciprocal comparison.	P
	execution	Lockstep & HW BIST Methodology. Reciprocal comparison.	P
2. Interrupt handling and execution	No interrupt	Lockstep & HW BIST Methodology. Reciprocal comparison.	P
	Too frequent interrupt related to different sources	Lockstep & HW BIST Methodology. Reciprocal comparison.	P
3. Clock	Wrong frequency (for quartz synchronized clock: harmonics/ sub-harmonics only)	STL & HW BIST Reciprocal comparison. DCC (Dual clock comparator)	P
4. Memory	-	-	-
4.1 Invariable memory	99,6 % coverage of all information errors	Lockstep and reciprocal comparison. Reciprocal comparison Flash ECC.	P
4.2 Variable memory	DC fault	Lockstep and reciprocal comparison. Independent HW comparator	P
	Dynamic cross links	Lockstep and reciprocal comparison. Independent HW comparator	P
4.3 Addressing (relevant to variable and invariable memory)	DC fault	Lockstep and reciprocal comparison. Independent HW comparator	P
5. Internal data path	-	-	-
5.1 Data	DC fault	See clauses 4	P
5.2 Addressing	Wrong address	See clauses 4	P
	Multiple addressing	See clauses 4	P

6 External communication	-	-	-
6.1 Data	Hamming distance 4		N/A
6.2 Addressing	Wrong address		N/A
	Multiple addressing		N/A
6.3 Timing	Wrong point in time		N/A
	Wrong sequence		N/A
7. Input/output periphery	-	-	-
7.1 Digital I/O	Fault conditions specified in Cl.H.13		N/A
7.2 Analog I/O	-	-	-
7.2.1 A/D and D/A-convertor	Fault conditions specified in Cl. H.13		N/A
7.2.2 Analog multiplexer	Wrong addressing		N/A
8. Monitoring devices and comparators	Any output outside the static and dynamic functional specification		N/A
9 Custom chips e.g. ASIC, GAL, gate array	Any output outside the static and dynamic functional specification		N/A

III – TESTMETHODIK / *TEST METHODOLOGY*

Die vorliegenden Dokumente nach 60335-1 und 60730-1 wurden einem Review unterzogen.
Die vorgelegten Funktionen wurden unter Zuhilfenahme einer Testumgebung aus IN-CIRCUIT EMULATOR / DEBUGER und einem Evaluation Board geprüft, Reviews / Prüfungen fanden am 2026-04-06 und 2026-04-22 statt. Teilnehmende waren die maßgeblichen Entwickler der Fa. Texas Instruments und ein Experte des VDE Institutes.

The provided documents acc. to the requirements of 60335-1 / 60730-1 have been reviewed.
The provided functions have been tested using the IN-CIRCUIT EMULATOR / DEBUGGER and an evaluation board during a review / witness test sessions dated 2026-04-06 and 2026-04-22 participating development staff of Texas Instruments and an expert of VDE.

IV – ERGEBNIS / *RESULT*

Die unter II benannten Selbst-Diagnose-Routinen erfüllen die Anforderungen der unter I benannten Normen. Die unter II benannten Selbst-Diagnose-Routinen können zum Aufbau einer Selbst-Test-Bibliothek gemäß der unter I benannten Normen verwendet werden

The self-diagnostic routines mentioned under II fulfill the requirements of the standards mentioned under I. The self-diagnostic routines mentioned under II are suitable to be used to create a self-test library according the standards mentioned under I.

Anhang / Annex

Übersicht der Typen, die von diesem Testreport abgedeckt werden.
Overview of types covered by this test report.

Device comparison

	Technical Reference Manual	Safety Manual	stl_can_ram	stl_cpu_reg	stl_crc	stl_hwbist	stl_lcm	stl_march	stl_mcan_ram	stl_osc_ct	stl_osc_hr	stl_pie_ram	stl_sp
F280013x	link	link	X	X[1]	X[1]			X		X	X	X[2]	X
F280015x	link	link	X	X	X		X	X	X	X	X	X[2]	X
F28002x	link	link	X	X	X	X		X		X	X	X	
F28004x	link	link	X	X	X			X		X	X	X	
F2838x	link	link	X	X[3]	X	X[3]		X	X	X	X	X	
F28003x	link	link	X	X	X	X		X	X	X	X	X	
F28P65x	link	link	X	X[3]	X	X[3]	X	X	X	X	X	X	
F28P55x	link	link		X	X			X	X	X	X	X[2]	
F28E12x	link			X[1]	X[1]			X[4]		X		X[2]	X
F28P551x				X	X			X	X	X	X	X[2]	

1. Device does not have VCU instruction set extension
2. Device has vector table parity instead of redundant PIE RAM comparison
3. Device has FPU64 instruction set extension (additional FPU registers)
4. Device does not have ECC protected ram section

Best regards

VDE Testing- and Certification Institute

Ralf Schwab

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