Functional Safety Information

LM25192-Q1, LM5192-Q1, and LM5192 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for LM25192-Q1, LM5192-Q1, and LM5192 (RGY (VQFN, 19) package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

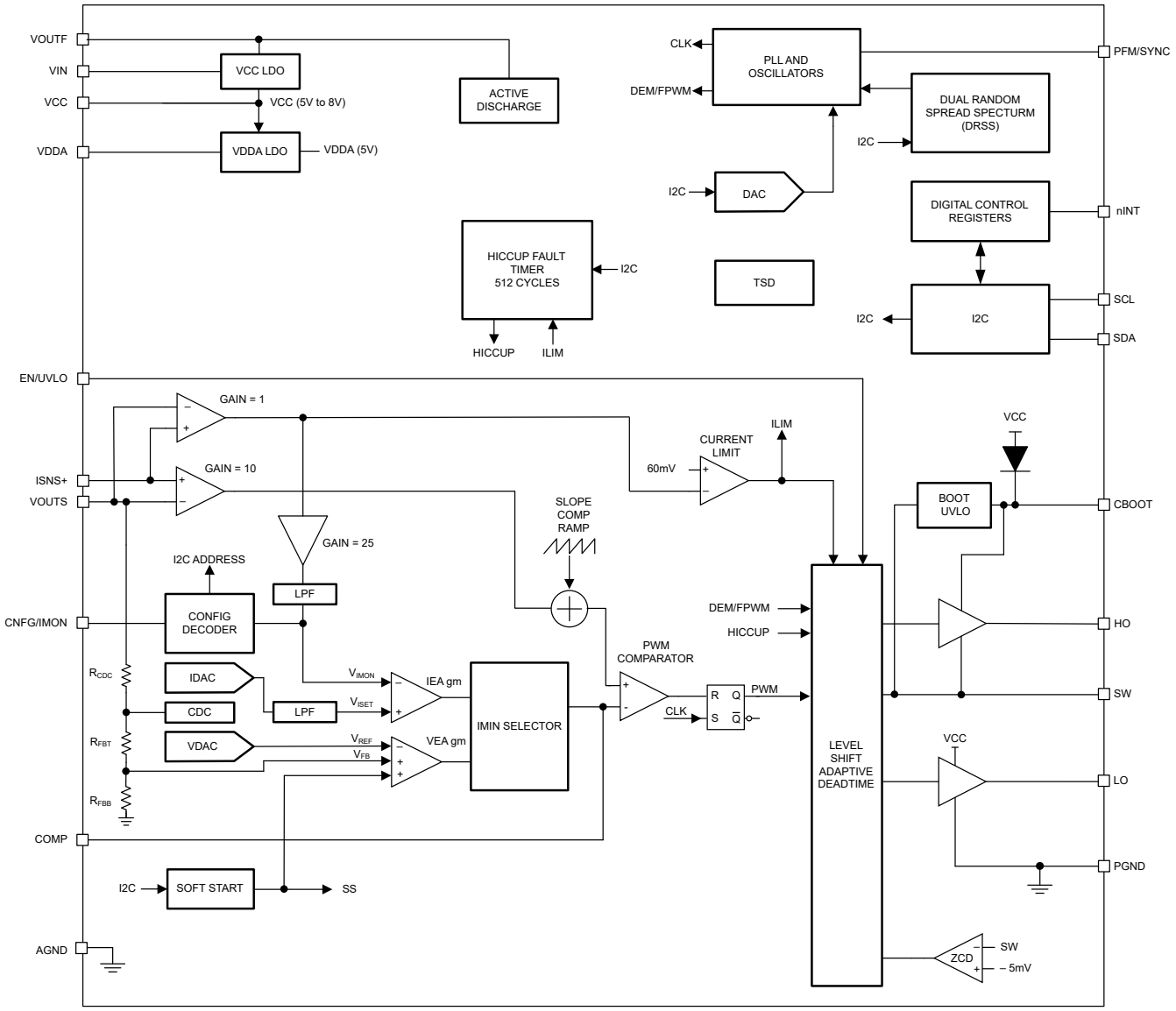

Figure 1-1. Functional Block Diagram

LM25192-Q1, LM5192-Q1, and LM5192 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 LM25192-Q1 FIT Rates

This section provides functional safety failure in time (FIT) rates for LM25192-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	16
Die FIT rate	7
Package FIT rate	9

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 750mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 LM5192-Q1 FIT Rates

This section provides functional safety failure in time (FIT) rates for LM5192-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	16
Die FIT rate	7
Package FIT rate	9

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 750mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	30 FIT	75°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.3 LM5192 FIT Rates

This section provides functional safety failure in time (FIT) rates for LM5192 based on two different industry-wide used reliability standards:

- Table 2-5 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-6 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-5. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	16
Die FIT rate	7
Package FIT rate	9

The failure rate and mission profile information in Table 2-5 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11 or figure 16
- Power dissipation: 750mW
- Climate type: World-wide table 8 or figure 13
- Package factor (lambda 3): Table 17b or figure 15
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-6. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	30 FIT	75°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-6 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM25192-Q1, LM5192-Q1, and LM5192 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No output voltage	40
Output voltage not in specification	45
HO or LO stuck on, off, or Hi-Z	5
nINT – false trip or fails to trip	5
No I2C communication	5

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LM25192-Q1, LM5192-Q1, and LM5192 (RGY (VQFN, 19) package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LM25192-Q1, LM5192-Q1, and LM5192 pin diagram. For a detailed description of the device pins, refer to the *Pin Configuration and Functions* section in the LM25192-Q1, LM5192-Q1, and LM5192 datasheet.

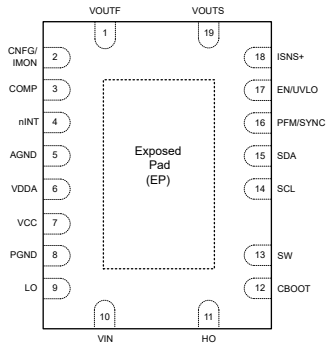

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The application circuit is used according to the LM25192-Q1, LM5192-Q1, and LM5192 datasheet.
- The PG pin is pulled up to the VDDA pin.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VOUTF	1	There is no BIAS functionality, which leads to lower efficiency and higher quiescent current.	B
CNFG	2	The I2C address and the functionality of IMON are potentially configured incorrectly.	C
EXTCOMP	3	VOUT = 0V.	B
nINT	4	There is a loss of the nINT indicator. In response, the USB controller potentially disables the LM5192 device.	B
AGND	5	AGND is GND. VOUT = Expected VOUT.	D
VDDA	6	VOUT = 0. No switching and loaded VCC output.	B
VCC	7	VOUT = 0. No switching and loaded VCC output.	B
PGND	8	PGND is GND. VOUT = Expected VOUT.	D
LO	9	The device switches without the low-side FET asynchronously. The low-side FET driver is potentially damaged.	A
VIN	10	VOUT = 0V.	B
HO	11	VOUT = 0V. No switching. The high-side FET driver is potentially damaged.	A
CBOOT	12	VOUT = 0V. The VCC regulator is loaded to current limit.	B
SW	13	VOUT = 0V. The high-side FET is shorted from VIN to GND.	A
SCL	14	The loss of I2C functionality prevents the USB controller from enabling the converter.	B
SDA	15	The loss of I2C functionality prevents the USB controller from enabling the converter.	B
PFM/SYNC	16	VOUT = Expected VOUT. No synchronization is available and the pin operates in FPWM mode.	C
EN/UVLO	17	VOUT = 0V since the device is in shutdown.	B
ISNS+	18	VOUT = 0V. The HO pin is damaged.	A
VOUT	19	The current limit is reached. VOUT = 0V.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VOUTF	1	There is no BIAS functionality or there is an output active discharge.	C
CNFG	2	The I2C address and the functionality of IMON is indeterminate.	B
EXTCOMP	3	VOUT oscillates. If VOUT oscillates to VIN, damage can occur if VIN > 60V.	A
nINT	4	There is a loss of the nINT indicator. In response, the USB controller potentially disables the LM5192 device.	B
AGND	5	VOUT is indeterminate.	B
VDDA	6	Poor noise immunity erratic switching.	B
VCC	7	VOUT = Expected VOUT, until damage occurs.	A
PGND	8	VOUT is indeterminate.	B
LO	9	The low-side FET is turned on capacitive through CGD; causes shoot-through current.	A
VIN	10	VOUT = 0V.	B
HO	11	The high-side FET gate is undefined. VOUT tracks HO.	A
CBOOT	12	VOUT = 0V.	A
SW	13	VOUT = 0V.	B
SCL	14	The loss of I2C functionality prevents the USB controller from enabling the converter.	B
SDA	15	The loss of I2C functionality prevents the USB controller from enabling the converter.	B
PFM/SYNC	16	Erratic CCM/DCM switching behavior at light loads.	C
EN/UVLO	17	The ON/OFF state of the device is indeterminate.	B
ISNS+	18	The OPEN ISNS+ pin blocks current limit and causes VOUT oscillations.	A
VOUT	19	No output sense causes VOUT to charge to VIN when switching.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
VOUTF	1	CNFG	The I2C address and the functionality of IMON are potentially configured incorrectly.	A
CNFG	2	EXTCOMP	There is a loss of voltage regulation.	B
EXTCOMP	3	NINT	High EXTCOMP voltage drives the part into current limit. There is a loss of voltage regulation.	B
nINT	4	AGND	There is a loss of the nINT indicator. In response, the USB controller potentially disables the LM5192 device.	B
AGND	5	VDDA	The VDDA pin is grounded. VOUT = 0V.	B
VDDA	6	VCC	The VDDA pin and circuitry are damaged due to high VCC. VOUT = 0V.	A
VCC	7	PGND	The VCC regulator is in current limit. Switching is disabled.	B
PGND	8	LO	The device switches without the low-side FET asynchronously. The low-side FET driver is potentially damaged.	A
LO	9	VIN	There is excess current from the VIN pin to ground. The part does not start-up. VOUT = 0V.	A
VIN	10	HO	SW, VOUT ≅ VIN, damage to low-side and high-side FETs due to shoot-through current.	A
HO	11	CBOOT	The high-side FET is always ON. VOUT ≅ VIN.	A
CBOOT	12	SW	The high-side switch never turns ON. VOUT = 0V.	B
SW	13	SCL	There is damage to the SCL pin.	A
SCL	14	SDA	The loss of I2C functionality prevents the USB controller from enabling the converter.	B
SDA	15	PFM/SYNC	This connection leads to erratic behavior of the PFM/FPWM pin. The pin potentially synchronizes to the I2C frequency.	B
PFM/SYNC	16	EN/UVLO	VOUT = Expected VOUT. If the voltage of the EN pin is greater than 6.5V, damage to the PFM pin potentially occurs.	A
EN/UVLO	17	ISNS+	The device remains ON and cannot be disabled.	B
ISNS+	18	VOUT	The current limit is disabled since the current limit resistor is shorted. VOUT cannot regulate (unstable) since current mode feedback is shorted.	A
VOUT	19	VOUTF	Shorted at the PCB level. The current limit is less accurate and degrades stability.	C

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
VOUTF	1	VIN > 50V leads to damage on the VOUTF pin. The active discharge circuitry is potentially damaged.	A
CNFG	2	The circuitry of the CONFIG pin is damaged by VIN voltages greater than 6.5V.	A
EXTCOMP	3	This pin brings VDD up. VOUT = 0V.	A
nINT	4	The pulldown device of the nINT pin is damaged due to excessive power dissipation.	A
AGND	5	VOUT = 0V.	B
VDDA	6	If VIN > 6.5V, the voltage exceeds the maximum ratings and the VDDA pin is damaged. VOUT = 0V.	A
VCC	7	If VIN > 12V, the voltage exceeds the maximum ratings and the VCC pin is damaged. VOUT = 0V.	A
PGND	8	VOUT = 0V.	B
LO	9	VOUT is shorted to GND. There is shoot-through current when the high-side FET turns on and this causes damage.	A
VIN	10	N/A	D
HO	11	VOUT ≅ VIN. There is damage to the low-side FET.	A
CBOOT	12	The voltage exceeds the maximum ratings and the CBOOT pin is damaged. There is HO bias damage. VOUT = 0V.	A
SW	13	VOUT = VIN. There is excess current from VIN through the low-side FET.	A
SCL	14	The loss of I2C functionality prevents the USB controller from enabling the converter.	A
SDA	15	The loss of I2C functionality prevents the USB controller from enabling the converter. The pulldown device of the SDA pin is potentially damaged due to high power dissipation.	A
PFM/SYNC	16	The voltage exceeds the maximum ratings and the PFM/SYNC pin is damaged. VOUT = Expected VOUT.	A
EN/UVLO	17	The part is always be enabled. VOUT = Expected VOUT.	B
ISNS+	18	If VIN > 60V, the voltage exceeds the maximum ratings and the ISNS+ pin is damaged. VOUT = VIN.	A
VOUT	19	If VIN > 60V, the voltage exceeds the maximum ratings and the VOUT pin is damaged. VOUT = VIN.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2026	*	Initial Release

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