Application Report
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TLV320AIC3104 Programming Made Easy

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ABSTRACT

The TLV320AIC3104 (AIC3104) is a versatile audio codec with multiple features. When first designing with the AIC3104, reading the entire data sheet and becoming familiar with the entire register set can be a daunting task. However, in many common configurations, it is possible to get the AIC3104 up and running while only writing to as few as 12 registers.

Although not intended to replace the data sheet, this document details several common configurations for the AIC3104. It gives a concise description of how to set up the codec and gives a script example that can be used to accelerate your design.

1 Controlling the AIC3104

All features of the AIC3104 are accessed by programmable registers. The registers can be programmed by an external microprocessor or DSP using I^{2}C™ protocol. The master clock (MCLK) is not required to be running while programming the AIC3104. The fixed 7-bit I^{2}C address for the AIC3104 is 001 1000 (0x30h to write, 0x31h to read). The AIC3104 supports I^{2}C data rates up to 400 kHz.

It is good practice to perform a hardware reset after initial power up to ensure that all registers are in their default states and that the AIC3104 is ready to be programmed.

2 Determining Sample Rate and Master Clock Frequency

The first task for any design using the AIC3104 is to determine the desired sample rate and master clock frequency. With the exception of register programming, all internal timing, including the sample rate, is ultimately derived from an external master clock. By default, the ADC and DAC sample rates are MCLK/256. For the common audio sample rates 44.1 ksps and 48 ksps, the most common MCLK frequencies are 11.2896 MHz (44.1 ksps $\times$ 256) and 12.288 MHz (48 ksps $\times$ 256). If you are using one of these two MCLK frequencies and sample rates, no register programming is needed to set the sample rate.

Table 1 shows two common audio MCLK frequencies and the settings required to obtain common sample rates.

Table 1. MCLK Frequencies and Settings

DESIRED SAMPLE RATE	REGISTER SETTINGS
MCLK = 11.2896 MHz	
44.1 ksps	None Required (use defaults)
MCLK = 12.288 MHz	
48 ksps	None Required (use defaults)
8 ksps	Register 2, Page 0 = 0xAA
16 ksps	Register 2, Page 0 = 0x44
32 ksps	Register 2, Page 0 = 0x11
96 ksps	Register 7, Page 0, D6 and D5 = 1

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If you do not have access to a common MCLK frequency, the AIC3104 also contains an internal PLL that can be used to set the timing. See the Audio Clock Generation section of the AIC3104 data sheet (SLAS510) for details on the usage of the PLL.

3 Selecting the Number of Bits and Digital Audio Format

Once the sample rate and MCLK have been selected, the number of bits and digital audio format can be selected. The default number of bits for the AIC3104 is 16 bits. The default digital audio format is I^2S with the AIC3104 being the slave (Bit Clock and Word Clock as inputs to the AIC3104). The serial data format and number of bits are selected through Page 0, Register 9, and master or slave mode can be selected through Page 0, Register 8.

Table 2. Page 0/Register 8: Audio Serial Data Interface Control Register A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Bit Clock Directional Control 0: BCLK is an input (slave mode). 1: BCLK is an output (master mode).
D6	R/W	0	Word Clock Directional Control 0: WCLK is an input (slave mode). 1: WCLK is an output (master mode).

Table 3. Page 0/Register 9: Audio Serial Data Interface Control Register B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D16	R/W	0	Audio Serial Data Interface Transfer Mode 00: Serial data bus uses I^2S mode. 01: Serial data bus uses DSP mode. 10: Serial data bus uses right-justified mode. 11: Serial data bus uses left-justified mode.
D5–D4	R/W	0	Audio Serial Data Word Length Control 00: Audio data word length = 16 bits 01: Audio data word length = 20 bits 10: Audio data word length = 24 bits 11: Audio data word length = 32 bits

4 Setting the Signal Path Through the AIC3104

The AIC3104 has been designed for low-power portable applications. As a result, when first powered up, the device defaults to a low-power mode with the codec largely powered down. The user must select a signal path through the AIC3104 and program the registers to enable the desired path.

The AIC3104 is versatile and has many different signal paths that can be selected. This application report covers only the most basic configurations. For a full description of the available signal paths, see the data sheet.

4.1 ADC

The ADC has two sets of stereo inputs, Line 1 Left and Right and Line 2 Left and Right. Line 1 Left and Right can be configured for single-ended or differential inputs (Figure 1). The default is single-ended with only the Plus (P) Inputs being used. Line 2 Left and Right are always single-ended. By default, none of the inputs is routed to the PGA. By default, both Left and Right PGAs are muted and the Left and Right ADCs are powered down.

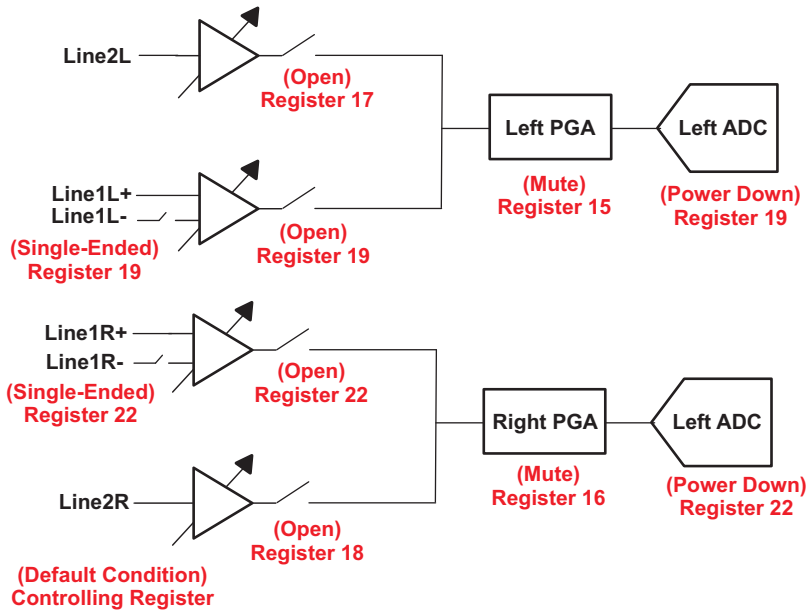

Figure 1. ADC Stereo Inputs

4.2 DAC

The Left and Right DACs each have an independent digital volume control. By default, the DACs are powered down, and the volume controls are muted.

The outputs of the DACs can be routed to any of the four high-power outputs or the stereo, differential line-outputs. By default, the DACs are not routed to any output. Each of the outputs has an independent analog amplifier with volume control. By default, these are muted and powered down.

Four high-power outputs can be used in pairs to drive two differential 16-Ω loads or independently to drive up to four single-ended, 16-Ω loads. By default, these are configured for differential outputs.

The line-outs are always fully differential and are designed to drive high-Z (10-kΩ) loads.

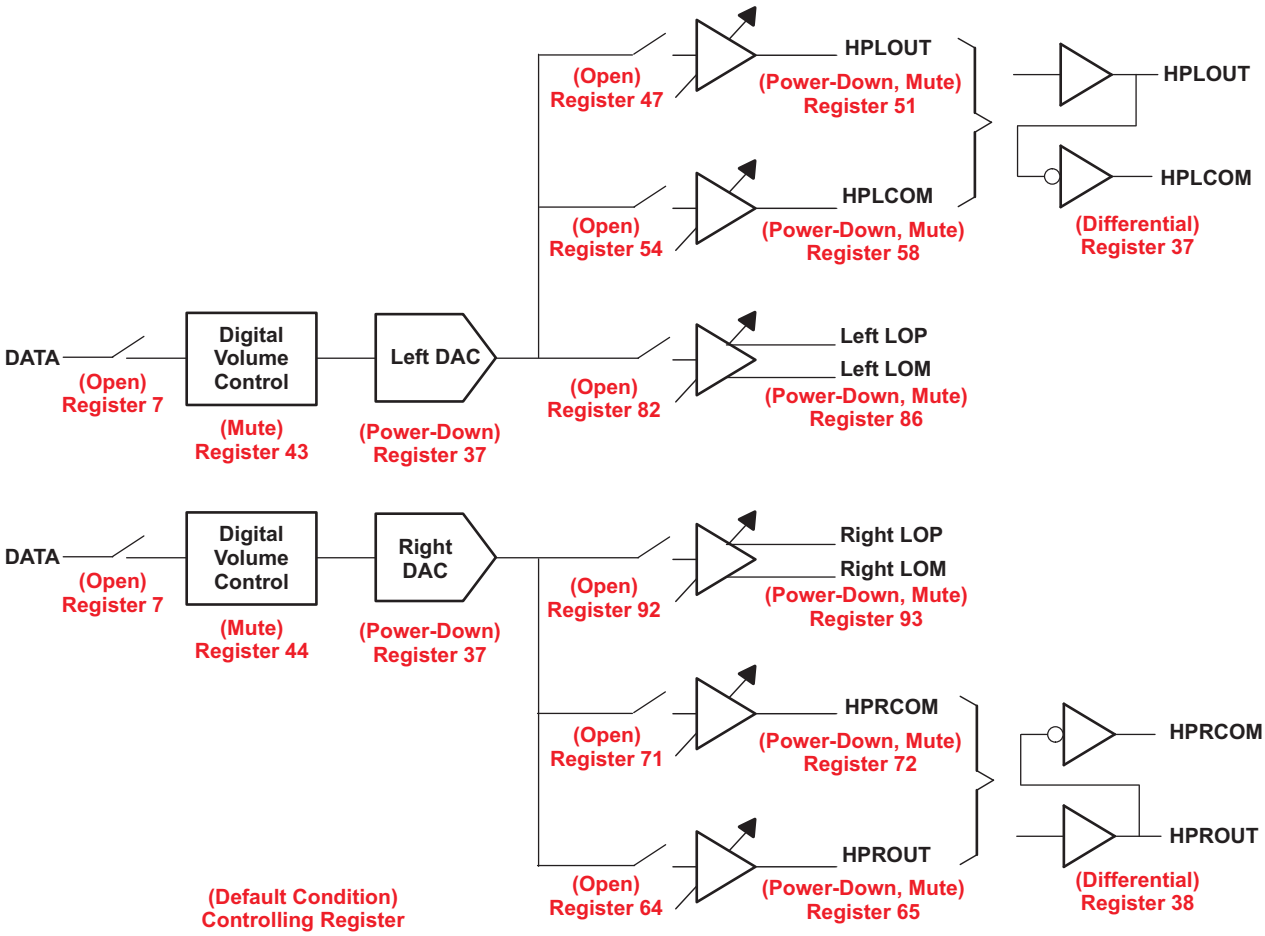

Figure 2. DAC Volume Control

5 Register Sequencing for Best Performance

In order to avoid unwanted audio artifacts associated with writing to the registers on the AIC3104, it is necessary to follow certain sequencing requirements. In some cases, the actual function of certain programming blocks depend on the register sequence to work properly.

Here are some guidelines:

- The ADC and DAC must be powered down when changing the sample rate.
- The PGAs must be muted before the ADC is powered down.
- When selecting an input, unmute the PGAs after routing the input and powering up the ADC.
- When selecting an output, power up and unmute the outputs after selecting the signal routing and powering up the DAC and unmuting the digital volume control.

6 Example Code

The following example code has been formatted to work with the AIC3104 EVM software GUI.

```
Format:
# Comment
w    30   01   08
^    ^    ^    ^
|    |    |    L Data in hex
|    |    L Register Address in hex
|    L Device I2C address in hex
L (W)rite or (R)ead
```

The following script makes maximum use of default settings to configure the AIC3104 for a single-ended stereo input into line 1 LP and RP, 16 bits, I^2C, slave mode, 48-ksps sample rate to differential stereo out on the line-outs:

```
# MCLK = 12.288 MHz
# reset
W 30 01 08
#  Route Line1LP to the Left ADC, Power up Left ADC
W 30 13 04
# Route Line1RP to the Right ADC, Power up Right ADC
W 30 16 04
# Unmute Left PGA, set gain to 0 dB
W 30 0F 00
# Unmute Right PGA, set gain to 0dB
W 30 10 00
# Route Left data to Left DAC, Route Right data to Right DAC
W 30 07 0A
# Power up Left and Right DAC's
W 30 25 C0
# Unmute Left digital volume control, set gain to 0 dB
W 30 2B 00
# Unmute Right digital volume control, set gain to 0 dB
W 30 2C 00
# Route Left DAC output to Left line outs
W 30 52 80
# Route Right DAC output to Right Line outs
W 30 5C 80
# Power up Left line out ± (differential), set gain to 0dB
W 30 56 09
# Power up Right line out ± (differential), set gain to 0 dB
W 30 5D 09
```

7 Summary

The AIC3104 is a versatile device with many features. In addition to the features discussed in this document, the AIC3104 has an onboard PLL, programmable filters, many bypass paths, and the ability to route and switch signals to almost anywhere a designer may want. This application report is not a replacement for the TLV320AIC3104 data sheet. A thorough understanding of the data sheet can ensure that you get the best performance from the AIC3104.

In spite of the complexity of the AIC3104, it can also be quite simple to set up and use for many standard configurations.

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