Application Note

MSPM0 G-Series MCUs Hardware Development Guide

ABSTRACT

The MSPM0 G-series microcontroller (MCU) portfolio offers a wide variety of 32-bit MCUs with ultra-low-power and integrated analog and digital peripherals for sensing, measurement, and control applications. This application note covers information needed for hardware development with MSPM0 G series MCUs, including detailed hardware design information for power supplies, reset circuitry, clocks, debugger connections, key analog peripherals, communication interfaces, GPIOs, and board layout guidance.

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1 MSPM0G Hardware Design Check List

Table 1-1 describes the main contents that needs to be checked during the MSPM0G hardware design process. The following sections provide more details.

Table 1-1. MSPM0G Hardware Design Check List

Pin	Description	Requirements
VDD	Power supply positive pin	Place 10µF and 100nF capacitors between VDD and VSS and keep those part close to VDD and VSS pins.
VSS	Power supply negative pin	
VCORE	Core voltage (typical: 1.35V)	Connect a 470nF capacitor to VSS. Do not supply any voltage or apply any external load to the VCORE pin.
NRST	Reset pin	Connect an external 47kΩ pullup resistor with a 10nF to 100nF pulldown capacitor. Adding a capacitor of appropriate capacitance to the reset pin can suppress transient interference caused by ESD, thereby reducing the risk of accidental reset.
ROSC	External reference resistor pin	• Connect an external 100kΩ/±0.1%, 25ppm resistor to VSS to enable high SYSOSC accuracy if needed. • Can be left open the application does not have high accuracy requirement for SYSOSC.
VREF+	Voltage reference power supply - external reference input	• When using VREF+ and VREF- to bring in an external voltage reference for analog peripherals such as the ADC, its output is directly tied to the VREF+ pin, and a decoupling capacitor must be placed on VREF+ to VREF-/GND with a capacitance based on the external reference source. • Leaving open is OK if the application does not need external voltage reference.
VREF-	Voltage reference ground supply - external reference input	
SWCLK	Serial wire clock from debug probe	Internal pulldown to VSS, does not need any external part.
SWDIO	Bidirectional (shared) serial wire data	Internal pullup to VDD, does not need any external part.
PA0, PA1	Open-drain I/O	Pullup resistor required for output high
PA18	Default BSL invoke Pin	Keep pulled down to avoid entering BSL mode after reset. (BSL invoke pin can be remapped.)
PAx (exclude PA0, PA1)	General-purpose I/O	Set corresponding pin functions to GPIO. (PINCMx.PF = 0x1)
Unused PAx (exclude PA0, PA1)	General-purpose I/O	Configure unused pins to output low or input with internal pullup or pulldown resistor.
Thermal Pad	Thermal pad on QFN package	The heat of the pad is transferred to the continuous copper plane (such as the GND Plane) of the PCB through the via. The larger the copper area, the better the heat dissipation effect.

Note

For any unused pin with a function that is shared with general-purpose I/O, follow the guidelines in Section 8.7.

TI recommends connecting a combination of a 10µF and a 0.1nF low-ESR ceramic decoupling capacitor to the VDD and VSS pins Higher-value capacitors can be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that for decouple (within a few millimeters).

The NRST reset pin is required to connect an external 47kΩ pullup resistor with a 10nF pulldown capacitor.

The SYSOSC frequency correction loop (FCL) circuit utilizes an external 100kΩ resistor, populated between the ROSC pin and VSS, to stabilize the SYSOSC frequency by providing a precision reference current for the SYSOSC. This resistor is not required if the SYSOSC FCL is not enabled.

For devices support external crystals, external bypass capacitors for the crystal oscillator pins are required when using external crystals.

A 0.47µF tank capacitor is required for the VCORE pin and need to be placed close to the device with minimum distance to the device ground.

For a 5-V-tolerant open drain (ODIO), a pullup resistor is required to output high, this is required for I2C and UART functions if the ODIO are used.

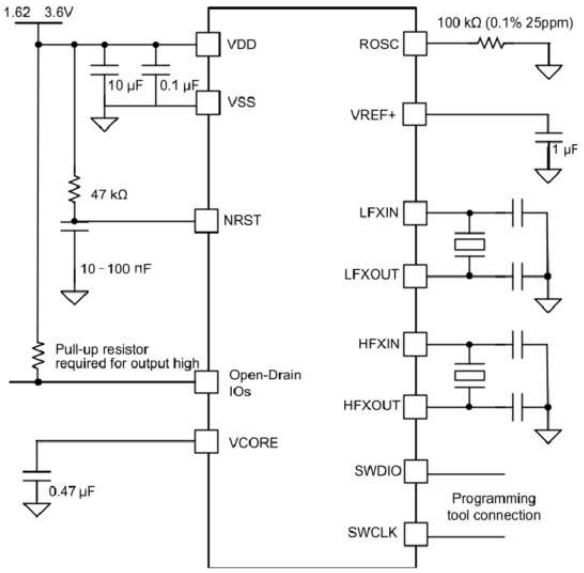

Figure 1-1. MSPM0G Typical Application Schematic

2 Power Supplies in MSPM0G Devices

Power is supplied to the device through the VDD and VSS connections. The device supports operation with a supply voltage of 1.62V to 3.6V and can start with a 1.62V supply. The power management unit (PMU) generates the regulated core supplies for the device and provides supervision of the external supply. This also contains a bandgap voltage reference used by the PMU and other analog peripherals. VDD is used directly to provide the IO supply (VDDIO) and the analog supply (VDDA). VDDIO and VDDA are internally connected to VDD so that additional power supply pins are not required (see the device data sheet for details).

2.1 Digital Power Supply

VCORE Regulator

An internal low-dropout linear voltage regulator generates a 1.35V supply rail to power the device core. In general, the core regulator output (VCORE) supplies power to the core logic, which includes the CPU, digital peripherals and the device memory. The core regulator requires an external capacitor (CVCORE) which is connected between the device VCORE pin and VSS (ground); see Figure 2-1. See the device-specific data sheet for the correct value and tolerance of C_{VCORE}. C_{VCORE} that needs to be placed close to the VCORE pin.

The core regulator is active in all power modes except for SHUTDOWN. In all other power modes (RUN, SLEEP, STOP, and STANDBY) the drive strength of the regulator is configured automatically to support the max load current of each mode. This reduces the quiescent current of the regulator when using low power modes, improving low power performance.

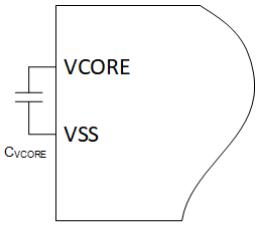

Figure 2-1. V_{CORE} Regulator Circuit

2.2 Analog Power Supply

Analog Mux VBOOST

The VBOOST circuit in the PMU generates an internal VBOOST supply that is used by the analog muxes in COMP, GPAMP, and OPA, if present on a device. The VBOOST circuit enables consistent analog mux performance across the external supply voltage (VDD) range.

Enabling and Disabling VBOOST

SYSCTL automatically manages the enable request for the VBOOST circuit based on the following parameters:

1. The COMP, OPA, and GPAMP peripheral PWREN settings.
2. The MODE setting of any COMP which is enabled (FAST vs. ULP mode).
3. The ANACPUMPCFG control bits in the GENCLKCFG register in SYSCTL.

VBOOST is disabled by default following a SYSRST. Use the application software to enable the VBOOST circuit before using the COMP, OPA, or GPAMP. When a COMP, OPA, or the GPAMP is enabled by application software, SYSCTL also enables the VBOOST circuit to support the analog peripheral.

Note

The VBOOST circuit has a startup time requirement (12µs typical) to transition from a disabled state to an enabled state. In the event that the startup time of the COMP, OPA, or GPAMP is less than the VBOOST startup time, the peripheral startup time is extended to account for the VBOOST startup time.

Bandgap Reference

The PMU provides a temperature and supply voltage stable bandgap voltage reference, which is used by the device for internal functions including:

- Driving the brownout reset circuit thresholds.
- Setting the output voltage for the core regulator.
- Driving the on-chip VREF levels for on-chip analog peripherals.

The bandgap reference is enabled in RUN, SLEEP, STOP modes. This operates in a sampled mode in STANDBY to reduce power consumption and is disabled in SHUTDOWN mode. SYSCTL manages the bandgap state automatically so that no user configuration is required.

2.3 Built-in Power Supply and Voltage Reference

The VREF module for the MSPM0G family is a shared voltage reference module that can be leveraged by a variety on on-board analog peripherals.

The VREF module features include:

- 1.4V and 2.5V user-selectable internal references.
- Support for receiving external reference on the VREF+ and VREF- device pins.
- Sample and hold mode support VREF operation down to STANDBY operating mode.
- Internal reference supports for ADC, COMP, and OPA.

When supplying the MCU with an external reference, TI recommends connecting a decoupling capacitor on the reference pins with a value based on the voltage source (see Figure 2-2).

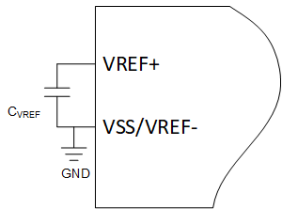

Figure 2-2. VREF Circuit

2.4 Recommended Decoupling Circuit for Power Supply

TI recommends connecting a combination of a 10µF plus a 100nF low-ESR ceramic decoupling capacitor to the DVCC pin (see Figure 2-3). Higher-value capacitors can be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that to decouple (within a few millimeters).

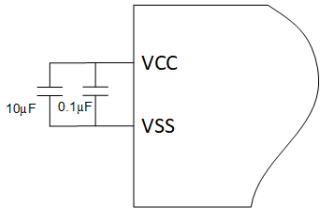

Figure 2-3. Power Supply Decoupling Circuit

3 Reset and Power Supply Supervisor

3.1 Digital Power Supply

The device has five reset levels:

- Power-on reset (POR)
- Brownout reset (BOR)
- Boot reset (BOOTRST)
- System reset (SYSRST)
- CPU reset (CPURST)

The details of the relationships between reset levels is described in the MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual (TRM).

After a cold start, the NRST pin is configured in NRST mode. The NRST pin must be high for the device to boot successfully. There is no internal pullup resistor on NRST. External circuitry (either a pullup resistor to DVCC or a reset control circuit) must actively pull NRST high for the device to start. A capacitor and an open button are needed for manual reset (see Figure 3-1). After the device is started, a low pulse on NRST that is <1 second in duration triggers a BOOTRST. If a low pulse on NRST longer than 1 second triggers a POR.

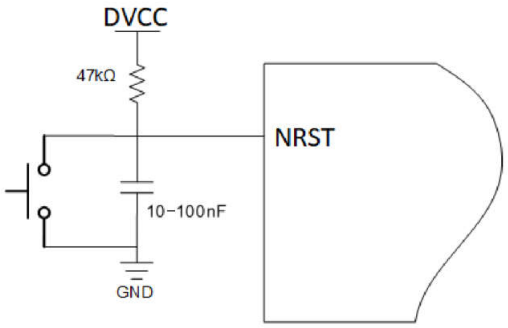

Figure 3-1. NRST Recommended Circuit

3.2 Power Supply Supervisor

Power-on Reset (POR) Monitor

The power-on reset (POR) monitor supervises the external supply (VDD) and asserts or deasserts a POR violation to SYSCTL. During cold power-up, the device is held in a POR state until VDD passes the POR+. Once VDD has passed POR+, the POR state is released and the bandgap reference and BOR monitor circuit are started. If VDD drops below the POR- level, then a POR- violation is asserted and the device is again held in a POR reset state.

The POR monitor does not indicate that VDD has reached a level high enough to support correct operation of the device. This is the first step in the boot process and is used to determine if the supply voltage is sufficient to power up the bandgap reference and BOR circuit, which are used to determine if the supply has reached a level sufficient for the device to run correctly. The POR monitor is active in all power modes including SHUTDOWN, and cannot be disabled. (The POR triggered waveform is shown in Figure 3-2).

Brownout Reset (BOR) Monitor

The brownout reset (BOR) monitor supervises the external supply (VDD) and asserts or deasserts a BOR violation to SYSCTL. The primary responsibility of the BOR circuit is to make sure that the external supply is maintained high enough to enable correct operation of internal circuits, including the core regulator. The BOR threshold reference is derived from the internal bandgap circuit. The threshold is programmable and is always higher than the POR threshold. During cold start, after VDD passes the POR+ threshold, the bandgap reference and BOR circuit are started. The device is then held in a BOR state until VDD passes the BOR0+ threshold. Once VDD passes BOR0+, the BOR monitor releases the device to continue the boot process, and the PMU is started. (The BOR triggered waveform is shown in Figure 3-2).

POR and BOR Behavior During Supply Changes

When the supply voltage (VDD) drops below POR-, the entire device state is cleared. Small variations in VDD which do not pass below the BOR0- threshold do not cause a BOR- violation, and the device continues to run. The BOR circuit is configured to generate an interrupt rather than immediately triggering a BOR reset.

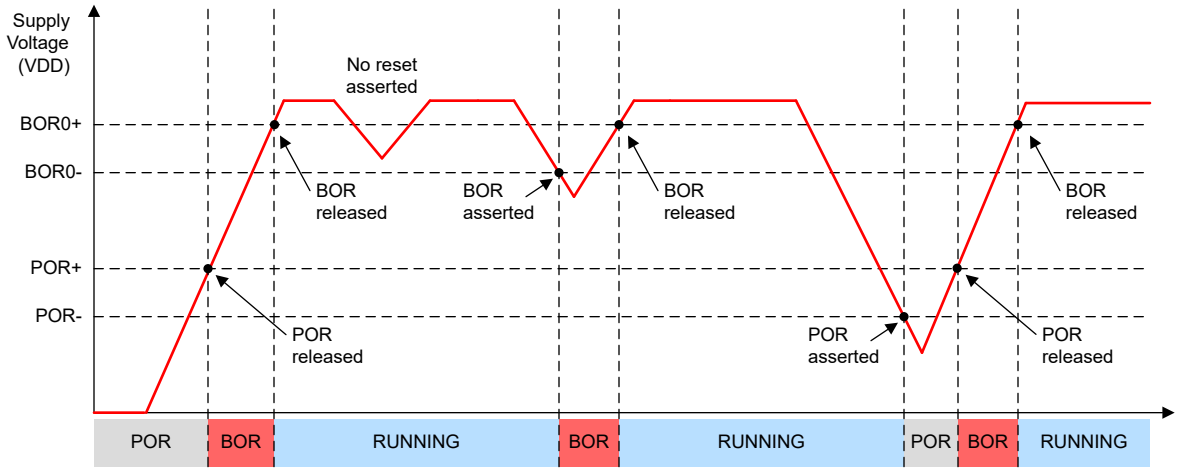

Figure 3-2. POR and BOR vs. Supply Voltage (VDD)

4 Clock System

The clock system of MSPM0G series contains the internal oscillators, the clock monitors, and the clock selection and control logic.

This section describes the clock resources on different MSPM0G family devices and the interaction with external signals or devices.

4.1 Internal Oscillators

Internal Low-Frequency Oscillator (LFOSC)

LFOSC is an on-chip low power oscillator that is factory trimmed to a frequency of 32.768kHz. This provides a low-frequency clock that can be used to help the system achieve low power consumption. The LFOSC can provide higher accuracy when used over a reduced temperature range. See the device-specific data sheet for details.

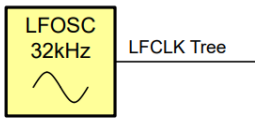

Figure 4-1. MSPM0G Series LFOSC

Internal System Oscillator (SYSOSC)

SYSOSC is an on-chip, accurate, and configurable oscillator with factory-trimmed frequencies of 32MHz (base frequency) and 4MHz (low frequency), as well as support for user-trimmed operation at either 24MHz or 16MHz. This provides a high frequency clock that allows the CPU to run at high speed for executing code and processing performance.

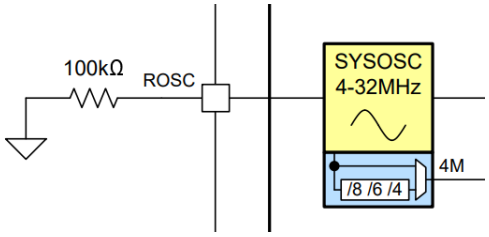

Figure 4-2. MSPM0G Series SYSOSC

SYSOSC Frequency Correction Loop

The additional hardware setting for this oscillator is an external resistor, populated between the ROSC pin and VSS, to increase SYSOSC from a base accuracy of ±2.5% across temperature.

The overall SYSOSC application accuracy is determined by combining the following error sources to determine the total error:

1. The ROSC reference resistor error (due to tolerance and temperature drift).
2. The SYSOSC circuit error in FCL mode (±0.75% for -40°C to 85°C or ±0.90% for -40°C to 125°C).

Table 4-1 shows how to calculate the SYSOSC application accuracy for two different ROSC resistor specs across two temperature ranges. For more details, see the device-specific TRM.

Table 4-1. SYSOSC Accuracy With FCL, by ROSC Tolerance, RSOC TCR, and Ambient Temperature (T_A)

Ambient Temperature (T_A)	-40 ≤ T_A ≤ 125°C		-40 ≤ T_A ≤ 85°C	
ROSC Resistor Parameters	**±0.1% 25ppm/°C**	**±0.5% 25ppm/°C**	**±0.1% 25ppm/°C**	**±0.5% 25ppm/°C**
Nominal ROSC resistance ($ROSC_{nom}$)	100kΩ			
Maximum ROSC resistance (at 25°C)	100.1kΩ	100.5kΩ	100.1kΩ	100.5kΩ
Minimum ROSC resistance (at 25°C)	99.9kΩ	99.5kΩ	99.9kΩ	99.5kΩ
ROSC resistor TCR	25ppm/°C			
ROSC temperature drift	-0.16% to 0.25%		-0.16% to 0.15%	
Maximum ROSC resistance (at high temperature) ($ROSC_{max}$)	100.35kΩ	100.75kΩ	100.25kΩ	100.65kΩ
Minimum ROSC resistance (at low temperature) ($ROSC_{min}$)	99.74kΩ	99.34kΩ	99.74kΩ	99.34kΩ
ROSC resistance error (high temperature) ($ROSC_{err+}$)	+0.35%	+0.75%	+ 0.25%	+0.65%
ROSC resistance error (low temperature) ($ROSC_{err-}$)	-0.26%	-0.66%	-0.26%	-0.66%
SYSOSC circuit error ($SYSOSC_{err}$)	±0.9%		±0.75%	
Total accuracy (TOT_{err-}, TOT_{err+})	-1.2% to +1.3%	-1.6% to +1.7%	-1.0% to +1.0%	-1.4% to +1.4%

System Phase-Locked Loop (SYSPLL)

SYSPLL is the system phase-locked loop with programmable frequency and is used to achieve the MSPM0G series highest speed (80MHz).

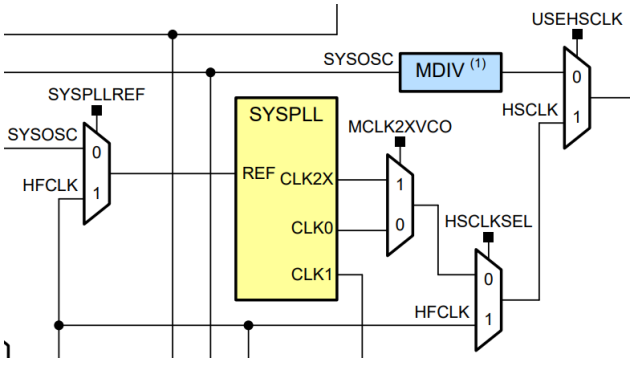

Figure 4-3. MSPM0G SYSPLL Circuit

4.2 External Oscillators

For applications that require even higher clock accuracy across devices and temperature, external oscillators can be used. LFXT can replace LFOSC, and HFXT can replace SYSOSC.

Low-Frequency Crystal Oscillator (LFXT)

The LFXT is an ultra-low power crystal oscillator that supports driving a standard 32.768kHz watch crystal. To use the LFXT, populate a watch crystal between the LFXIN and LFXOUT pins. Place loading capacitors on both LFXIN and LFXOUT pins to circuit ground (VSS). Size the crystal load capacitors according to the specifications of the crystal being used. A variety of crystal types are supported through a programmable drive strength mechanism. For the layout advice, refer to Section 9.

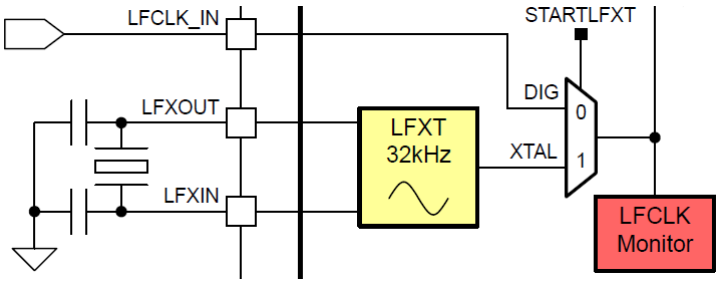

Figure 4-4. MSPM0G LFXT Circuit

LFCLK_IN (Digital Clock)

The LFXT circuit can be bypassed and a 32.76kHz typical frequency digital clock can be brought into the device to use as the LFCLK source. LFCLK_IN and LFXT are mutually exclusive and must not be enabled at the same time.

LFCLK_IN is compatible with digital square-wave CMOS clock inputs with a typical duty cycle of 50%. Users can check for a valid clock signal on LFCLK_IN by enabling the LFCLK monitor. By default, the LFCLK monitor checks LFCLK_IN if the LFXT was not started.

High-Frequency Crystal Oscillator (HFXT)

The high frequency crystal oscillator (HFXT) can be used with standard crystals and resonators in the 4 to 48MHz range to generate a stable high-speed reference clock for the system.

To use the HFXT, populate a crystal or resonator between the HFXIN and HFXOUT pins. Place loading capacitors on both pins to circuit ground (VSS). Size the crystal load capacitors according to the specifications of the crystal being used. A programmable HFXT startup time is provided with 64µs resolution. For layout advice, refer to Section 9.

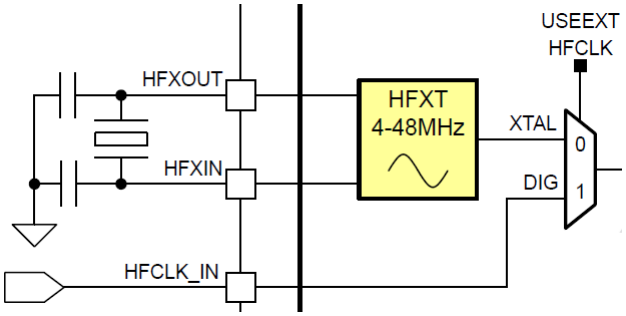

Figure 4-5. MSPM0G HFXT Circuit

HFCLK_IN (Digital clock)

Users can bypass the HFXT circuit and bring in a 4 to 48MHz typical frequency digital clock into the device to use as the HFCLK source instead of HFXT. HFCLK_IN and HFXT are mutually exclusive and must not be enabled at the same time.

HFCLK_IN is compatible with digital square wave CMOS clock inputs with a typical duty cycle of 50%.

4.3 External Clock Output (CLK_OUT)

A clock output unit can send digital clocks from the device to external circuits or to the frequency clock counter. This feature is useful for clocking external circuitry such as an external ADC that does not have a clock source. The clock output unit has a flexible set of sources to select, and includes a programmable divider.

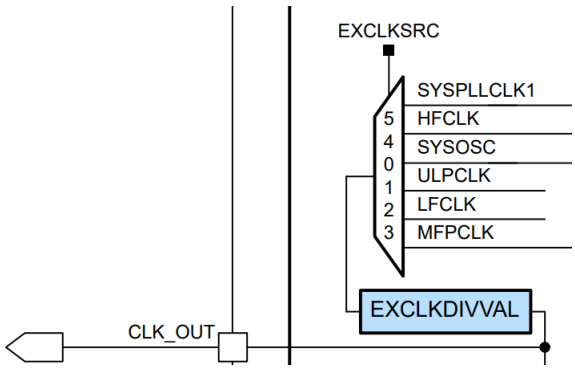

Figure 4-6. MSPM0G External Clock Output

Available clock sources for CLK_OUT:

- SYSPLLCLK1
- HFCLK
- SYSOSC
- ULPCLK
- MFCLK
- LFCLK

The selected clock source can be divided by 1, 2, 4, 8, 16, 32, 64, or 128 before being output to the pin or to the frequency clock counter.

4.4 Frequency Clock Counter (FCC)

The frequency clock counter (FCC) enables flexible in-system testing and calibration of a variety of oscillators and clocks on the device. The FCC counts the number of clock periods seen on the selected source clock within a known fixed trigger period (derived from a secondary reference source) to provide an estimation of the frequency of the source clock.

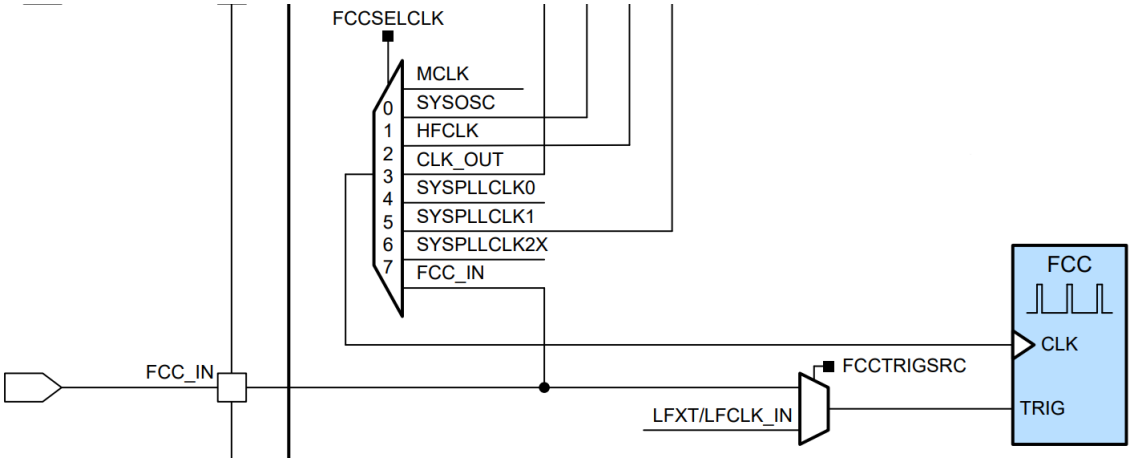

Figure 4-7. MSPM0G Frequency Clock Counter Block Diagram

Application software can use the FCC to measure the frequency of the following oscillators and clocks:

- MCLK
- SYSOSC
- HFCLK
- CLK_OUT
- SYSPLLCLK0
- SYSPLLCLK1
- SYSPLLCLK2X
- The external FCC input (FCC_IN)

Note

While the external FCC input (FCC_IN function) can be used as either the FCC clock source or the FCC trigger input, this cannot be used for both functions during the same FCC capture. This must be configured as either the FCC clock source or the FCC trigger.

5 Debugger

The debug subsystem (DEBUGSS) interfaces the serial wire debug (SWD) two-wire physical interface to multiple debug functions within the device. MSPM0G devices support debugging of processor execution, the device state, and the power state (using EnergyTrace technology).

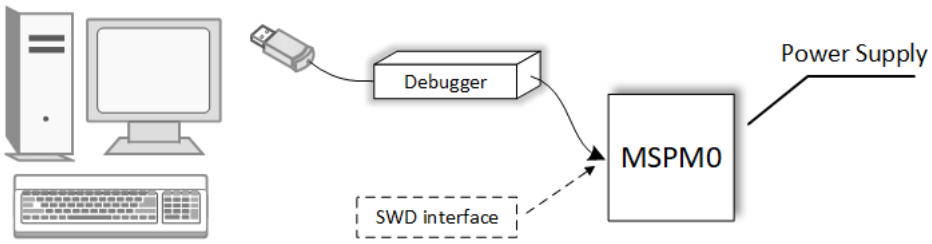

Figure 5-1. Host to Target Device Connection

5.1 Debug port pins and Pinout

The debug port contains SWCLK and SWDIO (see Table 5-1) which have internal pull-down and pull-up resistors (see Figure 5-2). The MSPM0G MCU family is offered in various packages with different numbers of available pins. See the data sheet for device-specific details.

Table 5-1. MSPM0G Debug Ports

DEVICE SIGNAL	DERECTION	SWD FUNCTION
SWCLK	Input	Serial wire clock from debug probe
SWDIO	Input/Output	Bi-directional (shared) serial wire data

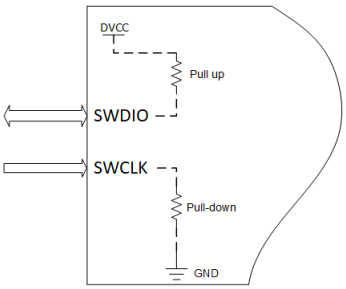

Figure 5-2. MSPM0G SWD Internal Pull

5.2 Debug Port Connection With Standard JTAG Connector

Figure 5-3 shows the connection between MSPM0G family MCU SWD debug port with the standard JTAG connector.

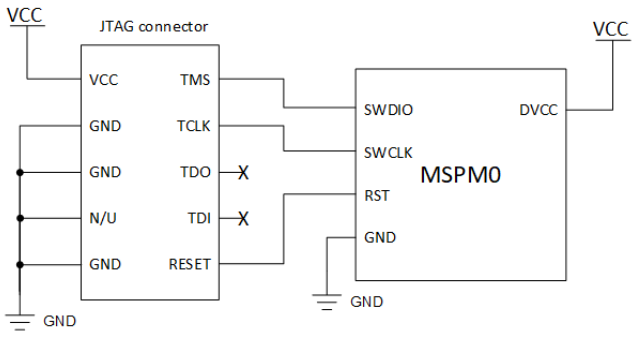

Figure 5-3. JTAG and MSPM0G Connection

For MSPM0G device, users can use XDS110 to implement debug or download function. This list the contents of the XDS110 and provides instruction on installing the hardware.

Standard XDS110

Users can purchase a standard XDS110 on ti.com. Figure 5-4 shows a high-level diagram of the major functional areas and interfaces of the XDS110 probe.

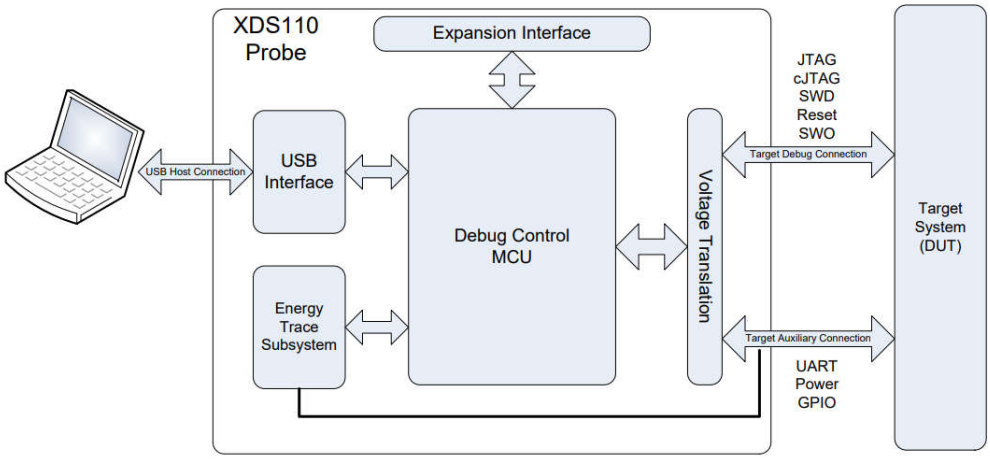

Figure 5-4. XDS110 Probe High-Level Block Diagram

For more XDS110 information, refer to the XDS110 Debug Probe User's Guide.

Lite XDS110 (MSPM0 LaunchPad Development Kit)

The MSPM0 LaunchPad kit includes a XDS110-ET (Lite) circuit. Users can use this debugger to download the firmware into MSPM0 device. Figure 5-5 shows XDS110-ET circuit.

There are two probes in XDS110-ET:

2.54mm probe: This port supports the SWD protocol and includes a 5V or 3.3V power supply. Users can connect SWDIO SWCLK 3V3 GND to the board and download firmware into an MSPM0G device.

This probe also supports **EnergyTrace** technology to measure power consumption precisely in real time.

For more information for EnergyTrace technology, refer to the EnergyTrace Technology tool page.

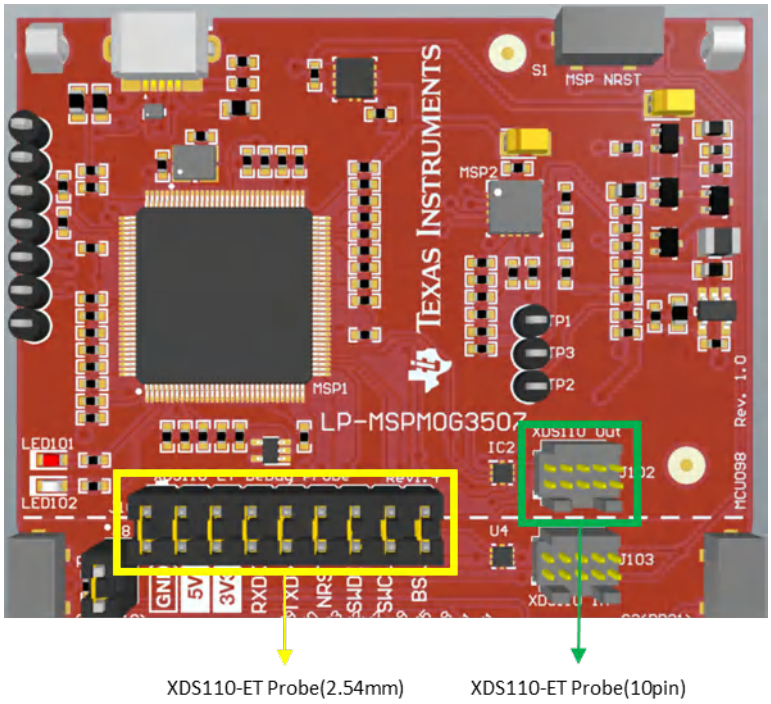

Figure 5-5. XDS110-ET Circuit

10-pin probe: This port supports the JTAG and SWD protocols and includes a 3.3V power supply. Users can use a 10-pin cable to connect the board and XDS110-ET and download firmware into an MSPM0G device. Figure 5-6 shows the 10-pin cable.

Figure 5-6. Arm Standard 10-Pin Cable

Note

- Standard XDS110 support level shift for debug ports, XDS110-ET just support 3.3v probe level.
- TI does not recommend using the XDS110 to power other devices except the MSPM0G MCU because the XDS110 integrates an LDO with limited current drive capability.
- XDS110-ET 2.54mm probe does not support JTAG protocol.
- XDS110-ET 10-pin probe does not support EnergyTrace technology.

6 Key Analog Peripherals

The MSPM0G series MCU includes analog peripheral resources that can provide many analog signal conditioning functions inside the chip. To maximize the use of the MSPM0G's analog peripheral performance, some considerations need to be made in the hardware design. This chapter discusses analog design considerations for many typical analog circuit configurations.

6.1 ADC Design Considerations

MSPM0G devices have a 12-bit, up to 4Msps, analog-to-digital converter (ADC). The ADC supports fast 12-, 10-, and 8-bit analog-to-digital conversions. The ADC implements a 12-bit SAR core, sample or conversion mode control, and up to 12 independent conversion-and-control buffers.

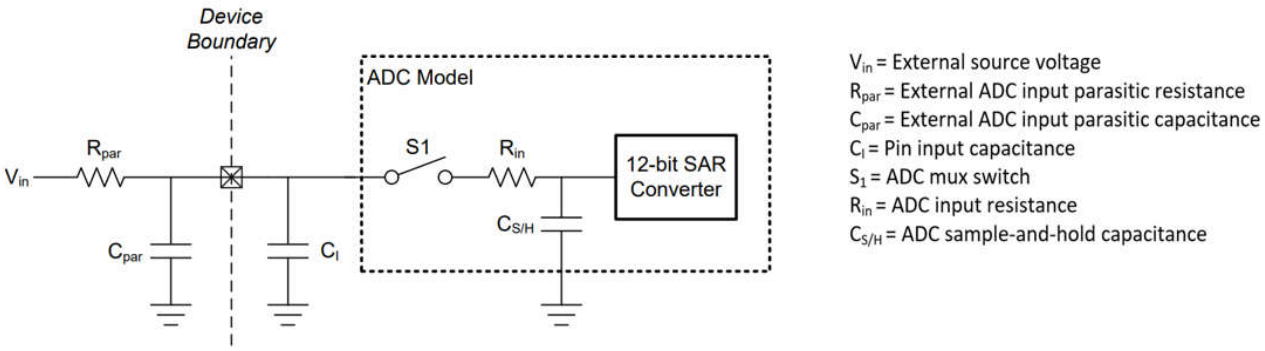

Figure 6-1. ADC Input Network

To achieve the desired conversion speed and keep high accuracy, make sure there is proper sampling time in hardware designs. Sampling (sample-and-hold) time determines how long to sample a signal before digital conversion. During sample time, an internal switch allows the input capacitor to be charged. The required time to fully charge the capacitor is dependent on the external analog front-end (AFE) connected to the ADC input pin. Figure 6-1shows a typical ADC model of an MSPM0G MCU. The Rin and CS/H values can be obtained from the device-specific data sheet. Understand the AFE drive capability and calculate the minimum sampling time required to sample the signal. The resistance of RPar and Rin affects tsample. Equation 1 can be used to calculate a conservative value of the minimum sample time tsample for an n-bit conversion:

$$t_{sample} \geq (R_{par} + R_{in}) \times \ln(2^{n+2}) \times (C_{S/H} + C_1 + C_{Par}) \quad (1)$$

To evaluate continuous high speed (4Msps) ADC performance, TI recommends adding an external buffer to make sure of sufficient signal source drive capability. As a design reference, see the LP-MSPM0G3507 hardware design, which includes a recommended external OPA.

6.2 OPA Design Considerations

The MSPM0G OPA is a zero-drift chopper stabilized operational amplifier with a programmable gain stage. The OPA can used for signal amplification and buffering and can work in general-purpose mode, buffer mode and PGA mode.

When using the OPA in general-purpose mode, add an external resistor and capacitor to create the amplifier circuit. The OPA can be configured through software for buffer mode. For PGA mode, software can configure the OPA up to 32x PGA gain.

Note

The PGA gain is only in the negative terminal.

When two or more OPAs are available on a device, the two can be combined to form a differential amplifier. The output equation for the differential amplifier is given by the V_{diff} equation in Figure 6-2.

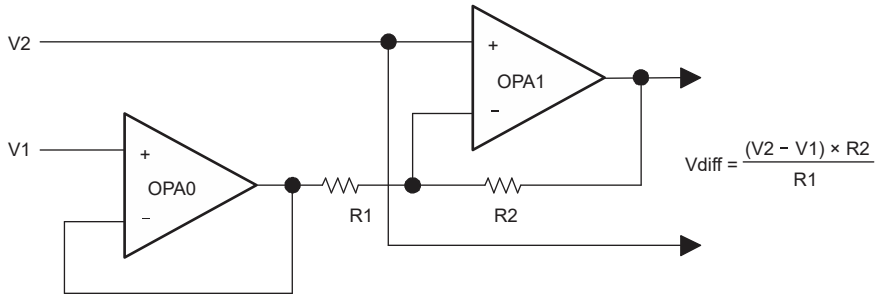

Figure 6-2. Two OPA Differential Amplifier Block Diagram and Equation

Alternately, two or more OPAs that are available on a device can be combined to form a multistage or cascaded amplifier. Using the programmable input muxes, all combinations of inverting and non-inverting multistage amplifiers can be implemented. The output equation for the noninverting to noninverting cascaded amplifier is given by the V_{out} equation in Figure 6-3.

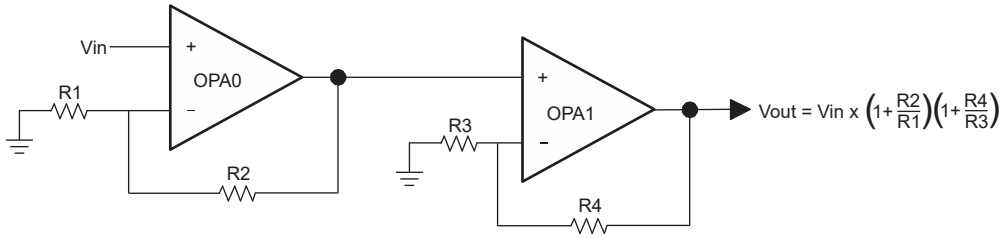

Figure 6-3. Two OPA Noninverting to Noninverting Cascade Amplifier Block Diagram and Equation

6.3 DAC Design Considerations

MSPM0G devices include two DAC modules: 8-bit and 12-bit. The DAC can be used as the reference voltage and also can work with the OPA to drive the output pad directly. 12-bit DAC modules include a buffer, thus this can output to pad directly. However, the 8-bit DAC module is normally used as internal reference voltage for OPA and COMP, therefore to output to an external pin, the OPA must be configured into buffer mode to improve the drive strength.

Not all devices include these two DAC modules. See the device-specific data sheet for details.

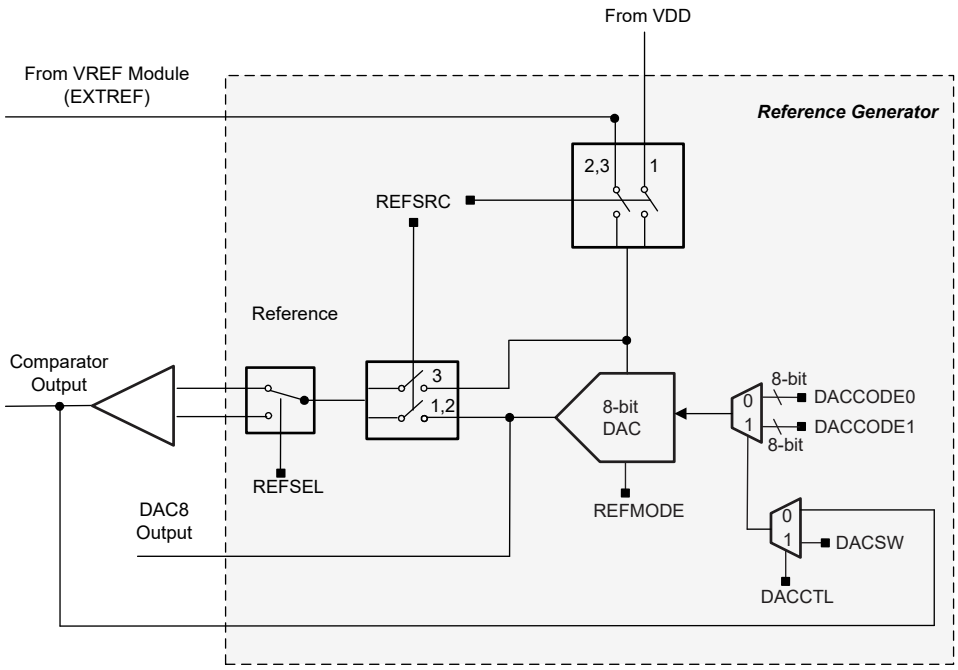

Figure 6-4. 8-Bit DAC Block Diagram

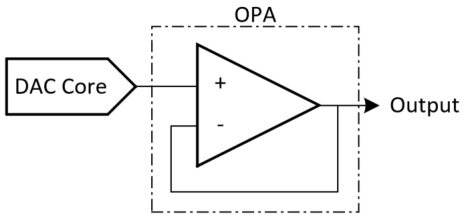

Figure 6-5. 8-Bit DAC and OPA Output Block Diagram

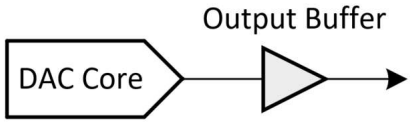

Figure 6-6. 12-bit DAC Output Block Diagram

6.4 COMP Design Considerations

The MSPM0G comparator module (COMP) is an analog voltage comparator with general comparator functionality.

The COMP module includes internal and external inputs that can be used to flexibly to process analog signals. An internal temperature sensor can be used as a direct input to the COMP.

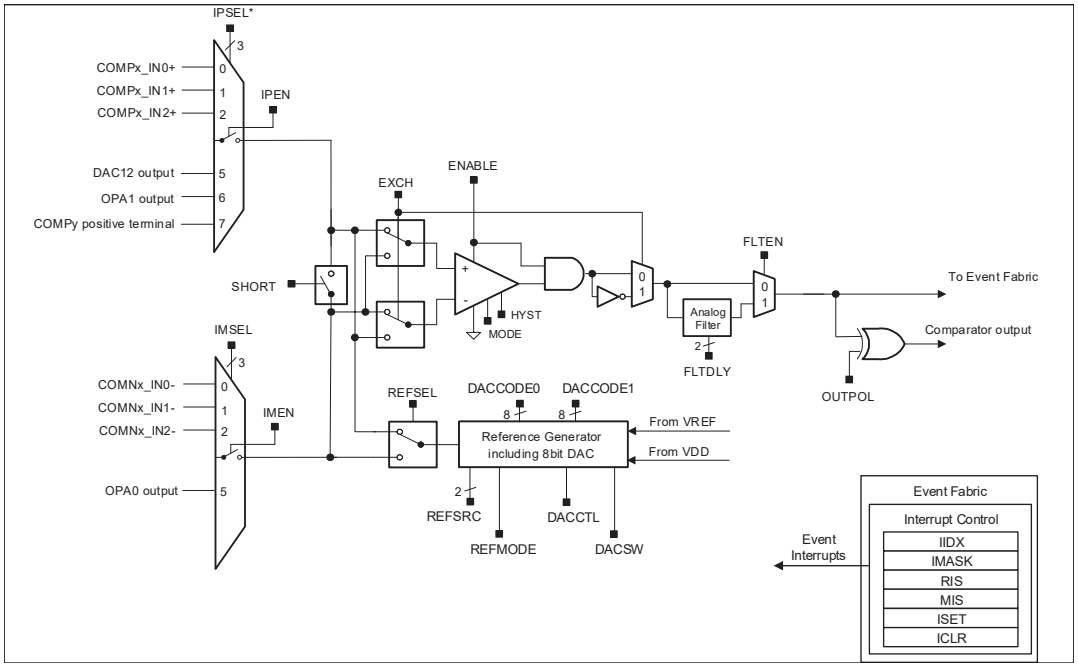

Figure 6-7. Comparator Diagram

The MSPM0G Comparator module also combine two COMP to implement a window comparator function. As shown in Figure 6-8, COMP0 and COMP1 can be configured together to create a window comparator. In this configuration, the input signal is connected to the positive terminal of the comparators connected together, and the upper and lower threshold voltages are connected to the negative terminal of the comparators.

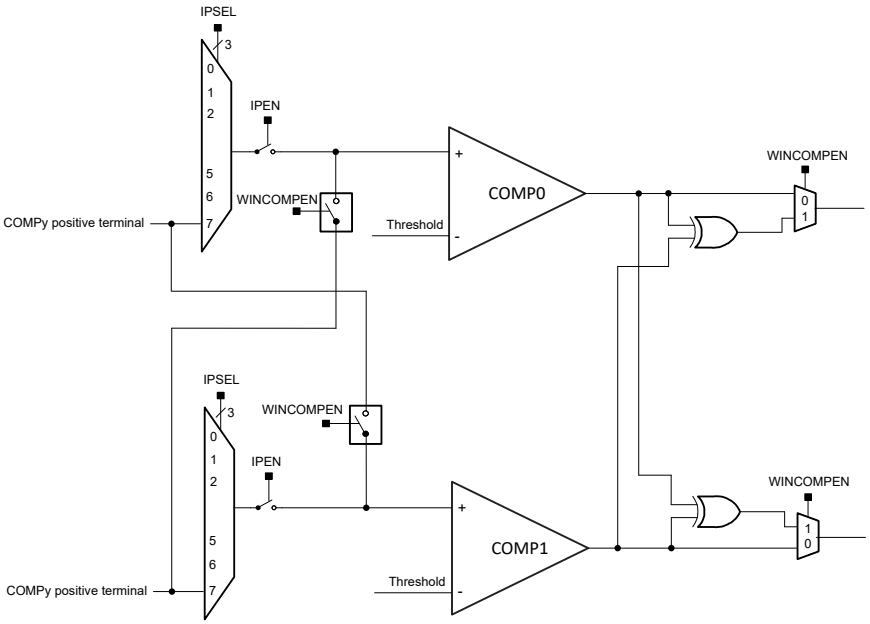

Figure 6-8. Window Comparator Mode

The COMP module also includes a SHORT switch that can be used to build a simple sample-and-hold for the comparator.

As shown in Figure 6-9, the required sampling time is proportional to the size of the sampling capacitor (CS), the resistance of the input switches in series with the short switch (R), and the resistance of the external source (RS). The sampling capacitor CS must be greater than 100pF. The time constant, Tau, to charge the sampling capacitor CS can be calculated with Equation 2.

$$T_{au} = (R_I + R_S)xC_S \quad (2)$$

Depending on the required accuracy, use 3 to 10 Tau as the sampling time. With 3 Tau, the sampling capacitor is charged to approximately 95% of the input signals voltage level. With 5 Tau, the sampling capacitor is charged to more than 99%, and with 10 Tau the sampled voltage is sufficient for 12-bit accuracy.

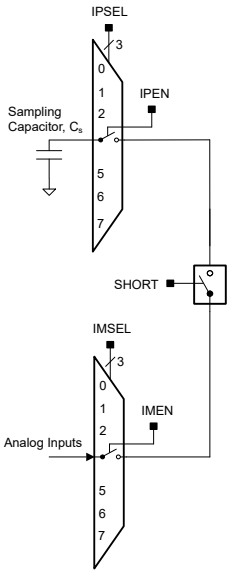

Figure 6-9. Comparator Short Switch

6.5 GPAMP Design Considerations

MSPM0G devices includes GPAMP (General Purpose Amplifier) modules that can used for signal amplification with some external resistors and capacitors, as seen in Figure 6-10.

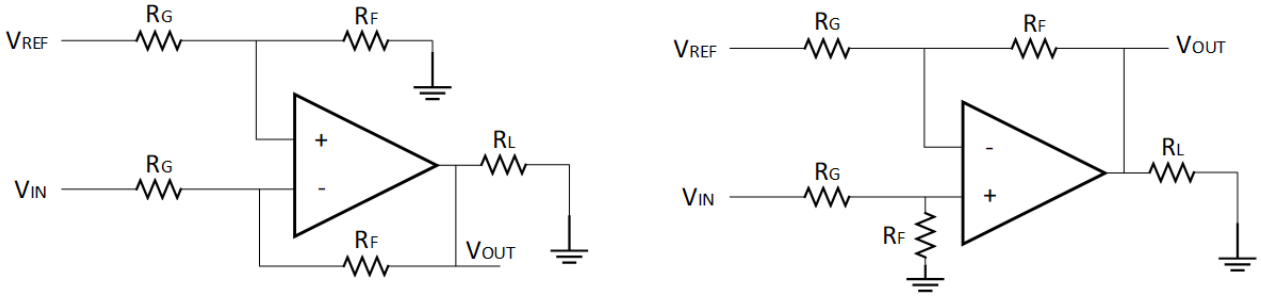

Figure 6-10. GPAMP Circuit in Amplify Mode

The GPAMP can also be used as a buffer for the internal ADC. Figure 6-11 shows an example of this configuration.

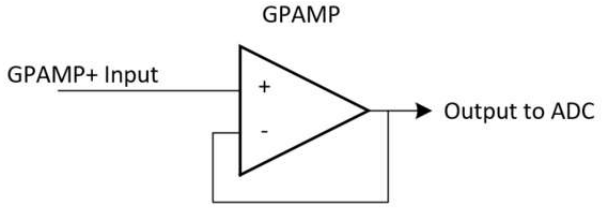

Figure 6-11. GPAMP Circuit in Buffer Mode

7 Key Digital Peripherals

The MSPM0G series MCU includes a wealth of digital peripheral resources, like Timer, UART, SPI, MCAN, LIN etc. which provide rich communication capabilities. To maximize the use of the MSPM0G's digital peripherals, some considerations need to be made in the hardware design. This chapter discusses design considerations for many typical digital peripheral configurations.

7.1 Timer Resources and Design Considerations

Timers are one of the most basic and important modules in any MCU, and this resource is used in all applications. This can be used to process tasks regularly, delay, output PWM waveforms to drive to devices, detect the width and frequency of external pulses, simulate waveform outputs, and more.

The MSPM0G series MCU includes two types of timer modules: advanced timer (TIMA) and general-purpose timer (TIMG). The TIMA and TIMG are timer counting modules that can be used for a variety of functions, including measuring the input signal edge and period (capture mode) or generating output waveforms (compare mode output) like PWM signals. However, TIMA adds additional features such as complementary PWM with dead band insertion. A summary of the different features and configurations of each timer is shown in Table 7-1 and Table 7-2.

Table 7-1. TIMA Instance Configuration

Instance	Power Domain	Counter Resolution	Prescaler	Repeat Counter	CCP Channels	Phase Load	Shadow Load	Pipelined CC	Dead band	Fault Handler	QEI
TIMA0	PD1	16-bit	8-bit	8-bit	4	Yes	Yes	Yes	Yes	Yes	-
TIMA1	PD1	16-bit	8-bit	-	2	Yes	Yes	Yes	Yes	Yes	-

Table 7-2. TIMG Instance Configuration

Instance	Power Domain	Counter Resolution	Prescaler	Repeat Counter	CCP Channels	Phase Load	Shadow Load	Shadow CCs	Dead band	Fault Handler	QEI/Hall Input Mode
TIMG0	PD0	16-bit	8-bit	-	2	-	-	-	-	-	-
TIMG1	PD0	16-bit	8-bit	-	2	-	-	-	-	-	-
TIMG2	PD0	16-bit	8-bit	-	2	-	-	-	-	-	-
TIMG3	PD0	16-bit	8-bit	-	2	-	-	-	-	-	-
TIMG4	PD0	16-bit	8-bit	-	2	-	Yes	Yes	-	-	-
TIMG5	PD0	16-bit	8-bit	-	2	-	Yes	Yes	-	-	-
TIMG6	PD1	16-bit	8-bit	-	2	-	Yes	Yes	-	-	-
TIMG7	PD1	16-bit	8-bit	-	2	-	Yes	Yes	-	-	-
TIMG8	PD0	16-bit	8-bit	-	2	-	-	-	-	-	Yes
TIMG9	PD0	16-bit	8-bit	-	2	-	-	-	-	-	Yes
TIMG10	PD1	16-bit	8-bit	-	2	-	-	-	-	-	Yes
TIMG11	PD1	16-bit	8-bit	-	2	-	-	-	-	-	Yes
TIMG12	PD1	32-bit	-	-	2	-	-	Yes	-	-	-
TIMG13	PD1	32-bit	-	-	2	-	-	Yes	-	-	-
TIMG14	PD0	16-bit	8-bit	-	4	-	-	-	-	-	-

- Look at the device-specific data sheet to check which TIMG instances are available on the device
- Check what features are available for each TIMG instance in the MSPM0 G-Series 80MHz Microcontrollers Technical Reference Manual

7.2 UART and LIN Resources and Design Considerations

The MSPM0G series of microcontrollers include Universal Asynchronous Receiver-Transmitter (UART). As shown in Table 7-3, UART0 through UART7 support the LIN, DALI, IrDA, ISO7816 Manchester Coding function.

Table 7-3. UART Features

UART Features	UART Extend	UART Main (Low-Power Mode Support)	UART Main
Instances	UART0, UART7	UART1, UART2	UART3-UART6
Active in Stop and Standby Mode	Yes	Yes	-
Separate transmit and receive FIFOs	Yes	Yes	Yes
Support hardware flow control	Yes	Yes	Yes
Support 9-bit configuration	Yes	Yes	Yes
Support LIN mode	Yes	-	-
Support DALI	Yes	-	-
Support IrDA	Yes	-	-
Support ISO7816 smart card	Yes	-	-
Support Manchester coding	Yes	-	-

The MSPM0G UART module can support up to 10MHz baud date in Power Domain1 for almost all UART applications.

Table 7-4. MSPM0G UART Specifications

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{UART}	UART input clock frequency	UART in Power Domain1			80	MHz
f_{UART}	UART input clock frequency	UART in Power Domain0			40	MHz
f_{BITCLK}	BITCLK clock frequency(equals baud rate in MBaud)	UART in Power Domain1			10	MHz
f_{BITCLK}	BITCLK clock frequency(equals baud rate in MBaud)				5	MHz
t_{SP}	Pulse duration of spikes suppressed by input filter	AGFSELx = 0		6		ns
		AGFSELx = 1		14	35	ns
		AGFSELx = 2		22	60	ns
		AGFSELx = 3		35	90	ns

Local Interconnect Network (LIN) is a commonly used low-speed network interface that consists of a commander node communicating with multiple remote responder nodes. Only a single wire is required for communication and is commonly included in the vehicle wiring harness.

The TLIN1021A-Q1 transmitter supports data rates up to 20kbps. The transceiver controls the state of the LIN bus by the TXD pin and reports the state of the bus on the open-drain RXD output pin. The device has a current-limited wave-shaping driver to reduce electromagnetic emissions (EME).

The TLIN1021A-Q1 is designed to support 12V applications with a wide input voltage operating range. The device supports low-power sleep mode and wake-up from low-power mode over LIN, the WAKE pin, or the EN pin. The device allows for system-level reductions in battery current consumption by selectively enabling the various power supplies that can be present on a node through the TLIN1021A-Q1 INH output pin. Figure 7-1 shows a typical interface implemented using the TI TLIN1021A LIN transceiver.

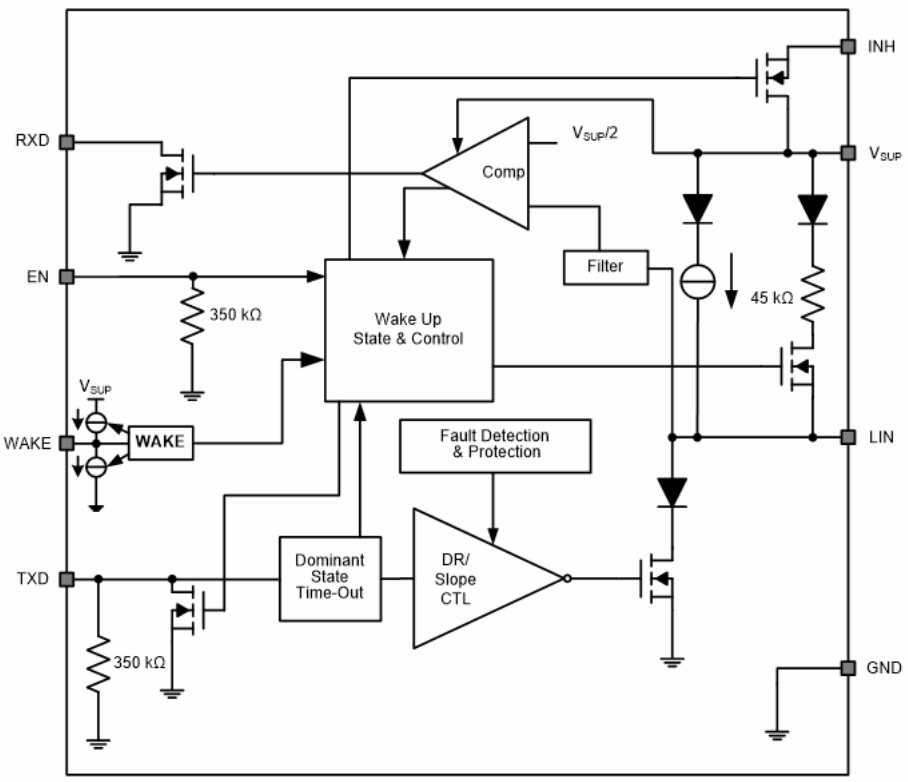

Figure 7-1. Typical LIN TLIN1021A Transceiver

Only a single wire is required for communication and is commonly included in the vehicle wiring harness. Figure 7-2 and Figure 7-3 show typical interfaces implemented using the TI TLIN1021A LIN transceiver. For more information, refer to the TLIN1021A-Q1 Fault-Protected LIN Transceiver with Inhibit and Wake data sheet.

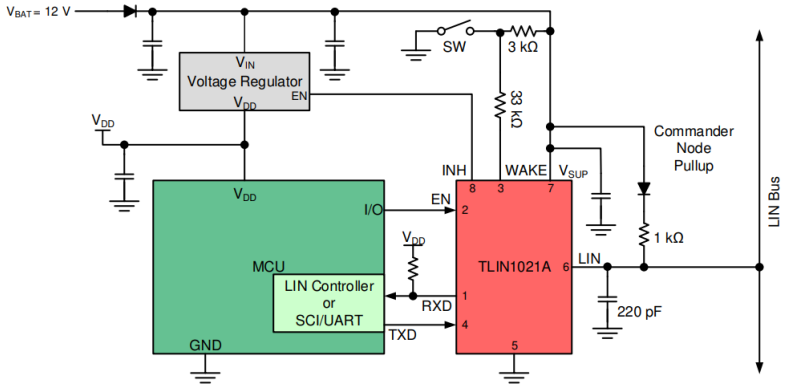

Figure 7-2. Typical LIN Application (Commander) With MSPM0G

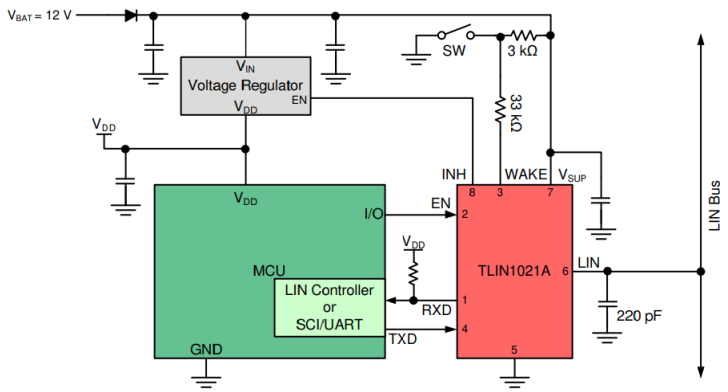

Figure 7-3. Typical LIN Application (Responder) With MSPM0G

7.3 MCAN Design Considerations

Controller Area Network (CAN) is a serial communications protocol that efficiently supports distributed real-time control with a high level of reliability. CAN has high immunity to electrical interference and the ability to detect various type of errors. In CAN, many short messages are broadcast to the entire network, which provides data consistency in every node of the system.

The MCAN module supports both classic CAN and CAN FD (CAN with flexible data-rate) protocols. The CAN FD feature allows higher throughput and increased payload per data frame. Classic CAN and CAN FD devices can coexist on the same network without any conflict, provided that partial network transceivers, which can detect and ignore CAN FD without generating bus errors, are used by the classic CAN devices. The MCAN module is compliant to ISO 11898-1:2015.

Some MSPM0G devices include MCAN and LIN modules. To connect to CAN and LIN buses normally, the device needs an external MCAN transceiver or LIN transceiver as shown in Figure 7-4.

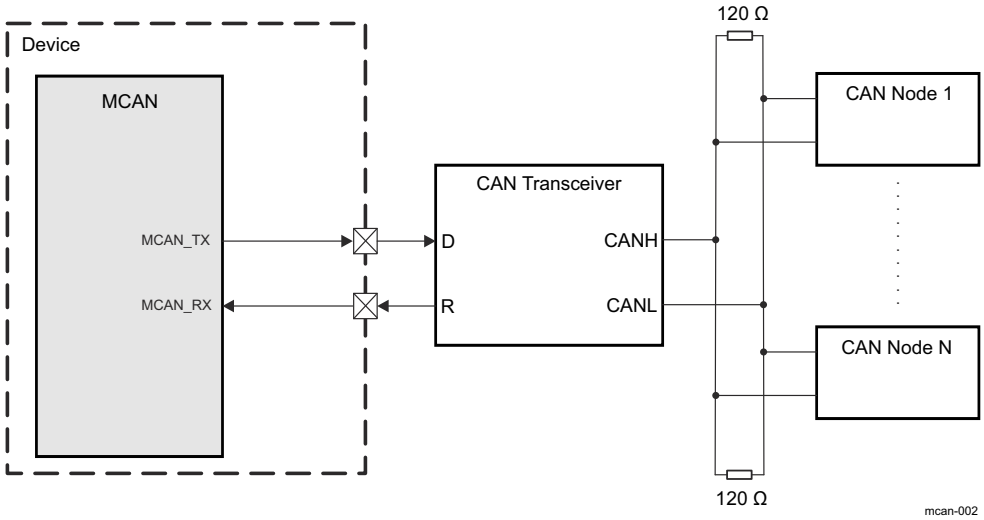

Figure 7-4. MCAN Typical Bus Wiring

TCAN1042GV is a CAN transceiver and meets the ISO11898-2 (2016) High Speed CAN (Controller Area Network) physical layer standard. This can be used in CAN FD networks up to 5Mbps (megabits per second) with the secondary power supply input for I/O level shifting the input pin thresholds and RXD output level. This device has a low-power standby mode with remote wake request feature. Additionally, this device includes many protection features to enhance device and network robustness. Figure 7-5 includes a reference design circuit. For more details, refer to the TCAN1042-Q1Automotive Fault Protected CAN Transceiver with CAN FD data sheet.

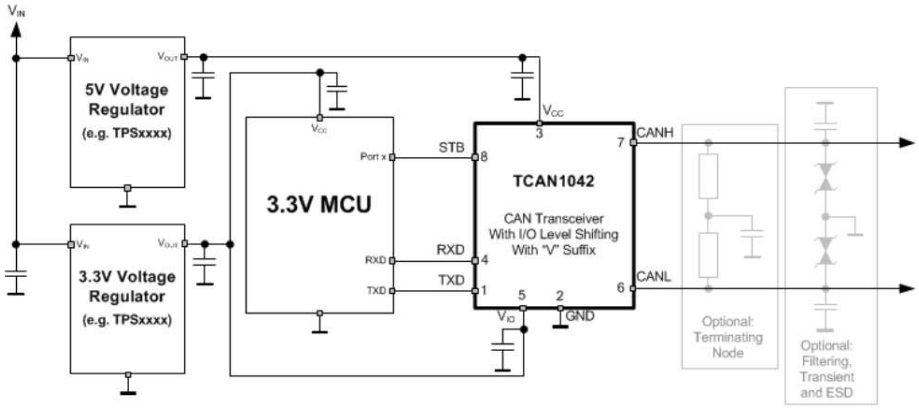

Figure 7-5. Typical CAN Bus Application With MSPM0G

7.4 I2C and SPI Design Considerations

SPI and I2C protocols are widely used in communication between devices or boards, such as data exchange between an MCU and a sensor. The MSPM0G series MCU includes up to 32MHz high-speed SPI, and support 3-wire, 4-wire, chip select, and command mode. See Figure 7-6 to design a system based on specific requirements.

Some SPI peripheral devices need PICO (Peripherals Input Controller Output) to keep high logic. Add a pullup resistor to the PICO pin if the external device requires.

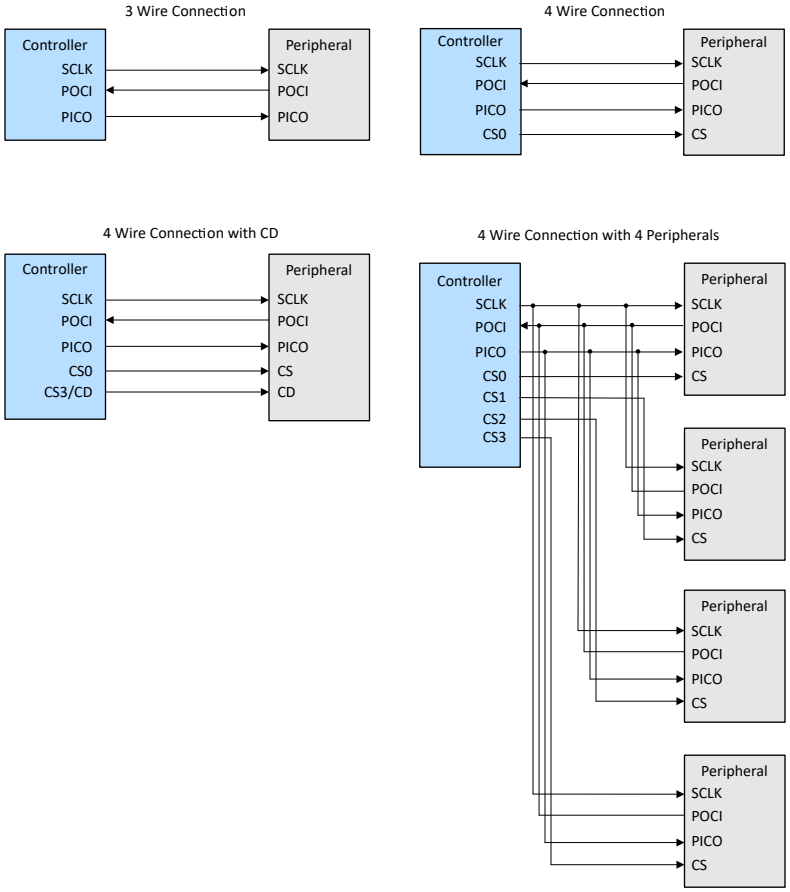

Figure 7-6. External Connections for Different SPI Configurations

For I2C bus, the MSPM0G device supports standard, fast and fast plus mode, as shown in the Table 7-5.

External pullup resistors are required when using I2C bus. The value of these resistors depends on the I2C speed; TI recommends 2.2k to support fast plus mode. For systems concerned with power consumption, large resistor values can be used. ODIO (see GPIOs) can be used to implement communication with a 5V device.

Table 7-5. MSPM0G I2C Characteristics

PARAMETERS		TEST CONDITIONS	Standard mode		Fast mode		Fast mode plus		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{I2C}	I2C input clock frequency	I2C in Power Domain0	2	32	8	32	20	32	MHz
f_{SCL}	SCL clock frequency			0.1		0.4		1	MHz
$t_{HD,STA}$	Hold time (repeated) START		4		0.6		0.26		us
t_{LOW}	LOW period of the SCL clock		4.7		1.3		0.5		us
t_{HIGH}	High period of the SCL clock		4		0.6		0.26		us
$t_{SU,STA}$	Setup time for a repeated START		4.7		0.6		0.26		us
$t_{HD,DAT}$	Data hold time		0		0		0		us
$t_{SU,DAT}$	Data setup time		250		100		50		us
$t_{SU,STO}$	Setup time for STOP		4		0.6		0.26		us
t_{BUF}	Bus free time between a STOP and START condition		4.7		1.3		0.5		us
$t_{VD;DAT}$	Data valid time			3.45		0.9		0.45	us
$t_{VD;ACK}$	Data valid acknowledge time			3.45		0.9		0.45	us

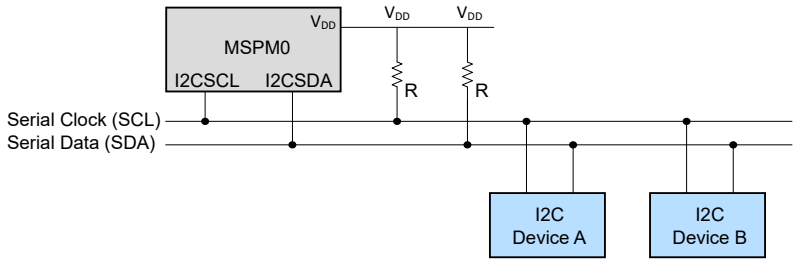

Figure 7-7. Typical I2C Bus Connection

8 GPIOs

MSPM0G series MCUs include standard-drive I/O (SDIO), high-drive I/O (HDIO), high-speed I/O (HSIO), and 5V-tolerant open-drain I/O (ODIO). Users can flexibly choose the appropriate I/O type based on actual requirements. The following characteristics need to be considered in hardware design.

8.1 GPIO Output Switching Speed and Load Capacitance

When using the GPIO as I/O, design considerations must be made to verify correct operation. As load capacitance becomes larger, the rise and fall time of the I/O pin increases. This capacitance includes pin parasitic capacitance (Ci = 5pF (typical)) and the effects of the board traces. I/O characteristics are available in the device-specific data sheet. Table 8-1 lists the I/O output frequency characteristics of the MSPM0G device.

Table 8-1. MSPM0G GPIO Switching Characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Port output frequency	SDIO	VDD ≥ 1.71V, C_L = 20pF			16	MHz
			VDD ≥ 2.7V, C_L = 20pF			32	
		HSIO	VDD ≥ 1.71V, DRV = 0, C_L = 20pF			16	
			VDD ≥ 1.71V, DRV = 1, C_L = 20pF			24	
			VDD ≥ 2.7V, DRV = 0, C_L = 20pF			32	
			VDD ≥ 2.7V, DRV = 1, C_L = 20pF			40	
		HDIO	VDD ≥ 1.71V, DRV = 0, C_L = 20pF			16	
			VDD ≥ 2.7V, DRV = 0, C_L = 20pF			20	
		ODIO	VDD ≥ 1.71V, FM^+, C_L = 20pF to 100pF			1	
t_r,t_f	Output rise or fall time	All output ports except ODIO	VDD ≥ 1.71V			0.3*f_{max}	s
t_f	Output fall time	ODIO	VDD ≥ 1.71V, FM^+, C_L = 20pF to 100pF	20*VDD/5.5		120	ns

Note

- The output voltage reaches at least 10% and 90% Vcc at the specified toggle frequency.
- The output rise time of open-drain I/Os is determined by pullup resistance and load capacitance.

8.2 GPIO Current Sink and Source

Table 8-2. MSPM0G GPIO Absolute Maximum Ratings

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	1.62		3.6	V
VCORE	Voltage on VCORE pin		1.35		V
C_{VDD}	Capacitor placed between VDD and VSS		10		uF
C_{VCORE}	Capacitor placed between VCORE and VSS		470		nF
T_A	Ambient temperature, T version	–40		105	°C
	Ambient temperature, S version	–40		125	
T_A	Ambient temperature, Q version	-40		125	°C
T_J	Max junction temperature, T version			125	°C
T_J	Max junction temperature, S and Q versions			130	°C
$f_{MCLK(PD1\ bus\ clock)}$	MCLK, CPUCLK, ULPCLK frequency with 2 flash wait state			80	MHz
	MCLK, CPUCLK, ULPCLK frequency with 1 flash wait state			48	
	MCLK, CPUCLK, ULPCLK frequency with 0 flash wait states			24	
$f_{ULPCLK(PD0\ bus\ clock)}$	ULPCLK frequency			40	MHz

Note

- The total current of I/O must be less than the maximum value of I_{VDD}.
- HDIO, HSIO and ODIO are patched in a fixed pin, see to the device data sheet.

SDIO and HSIO are able to sink or source a maximum current of 6mA (typical), which is sufficient to drive a typical LED. For larger current loading, use HDIO (maximum current of 20mA (typical)). However, the total combined current must be less than IVDD (80 mA typical).

8.3 High-Speed GPIOs (HSIO)

HSIO can support up to 40MHz frequency, and this speed is related to bus clock, supply voltage, and load capacitance. Users can also select the output max frequency via the DRV bit in the DIO register.

8.4 High-Drive GPIOs (HDIO)

HDIO are able to output 20mA current to drive a load, and the max source current is related to supply voltage.

8.5 Open-Drain GPIOs Enable 5V Communication Without a Level Shifter

ODIO are tolerant to 5V input. Because the ODIO are open drain, an external pullup resistor is required for the pin to be able to output high. This I/O can used for UART or I2C interfaces with different voltage levels. To limit the current, place a series resistor between the pin and the pullup resistor, and the R_{SERIES} must be no less than 250Ω. As shown in Figure 8-1, TI recommends 270Ω. The value of the pullup resistor depends on the output frequency (see Section 7.4).

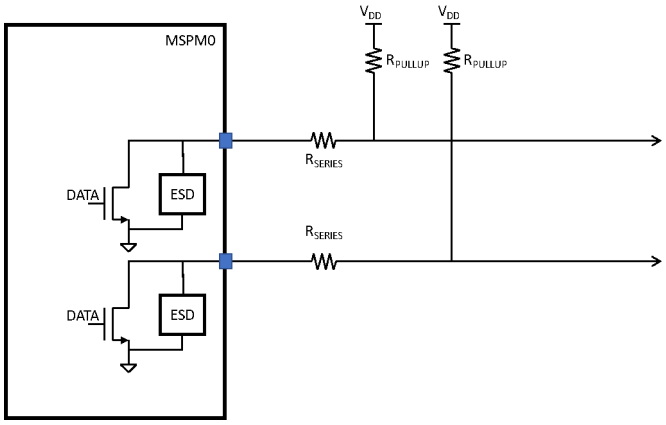

Figure 8-1. Suggested ODIO Circuit

8.6 Communicate With a 1.8V Device Without a Level Shifter

The MSPM0G series devices use a 3.3V logic level (excluding ODIO). If users need to communicate with 1.8V devices and do not use external level shifter devices, Figure 8-2 shows a suggested circuit for interfacing with a 1.8V device.

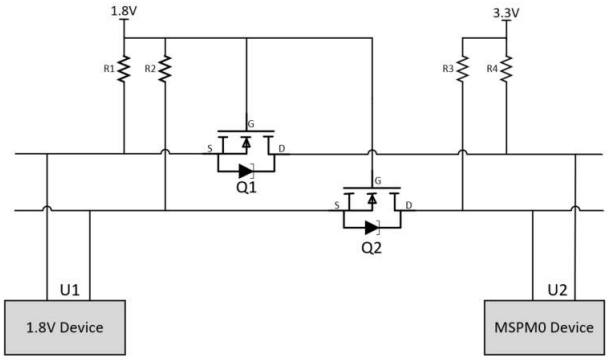

Figure 8-2. Suggested Communication Circuit With 1.8V Device

Two MOSFET are used in this circuit. Check the VGS to make sure this MOSFET can fully turn on with a low RDS(on). For a 1.8V device, use less than 1.8V VGS MOSFET. However, a too low VGS MOSFET can cause the MOSFET to turn on at a very small voltage (MCU logic judges as 0), resulting in a communication logic error.

U1 output and U2 input

1. U1 output *1.8v high*, Q1 VGS around 0, thus Q1 turn off, U2 reads *3.3v high* with R4.
2. U1 output *low*, Q1 VGS around 1.8v, thus Q1 turn on, U2 reads *low*.

U1 input and U2 Output

1. If the U2 output is *3.3V high*, then keep U1 at 1.8V with R1, and Q1 turn off, thus U1 reads *1.8V high*.
2. If the U2 output is *low*, then keep U1 at 1.8V with R1. But the diode inside MOSFET pulls down U1 to 0.7V (diode voltage drops) and causes VGS to be greater than the turn-on voltage; Q1 turns on, and U1 reads *low*.

8.7 Unused Pins Connection

All microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources. To increase EMC performance, unused clocks, counters or I/Os, must not be left free or floating. For example, set I/Os to 0 or 1 (pullup or pulldown enabled on the unused I/O pins) and disable unused features.

Table 8-3. Connection of Unused Pins

Pin	Potential	Comment
PAx	Open	Reserve corresponding pin functions to GPIO (PINCMx.PF = 0x0) as Hi-Z mode by default
OPAx_IN0-	Open	This pin is high-impedance.
NRST	VDD	NRST is an active-low reset signal and must be pulled high to VCC or the device cannot start.

Note

- To reduce leakage, TI recommends to keep IO unconfigured. IO is Hi-Z by default.
- BSL invoke pin must be pulled down to avoid entering BSL mode after reset.

9 Layout Guides

9.1 Power Supply Layout

Figure 9-1 shows the typical parts placement and routing for the power supply layout; you must modify this appropriately for your MSPM0G part. You can optionally connect a filter inductor in series with the VCC and MCU VDD pins. This inductor is used to filter the switching noise frequency of DCDC. For the value, please refer to the data sheet of DCDC vendor. C1/C2/C3 values and layout in the MSPM0G device data sheets.

Note

- Keep the smallest capacitance, closest to the MCU VDD pin (C1 < C2 < C3).
- Make all the traces direct without any vias.

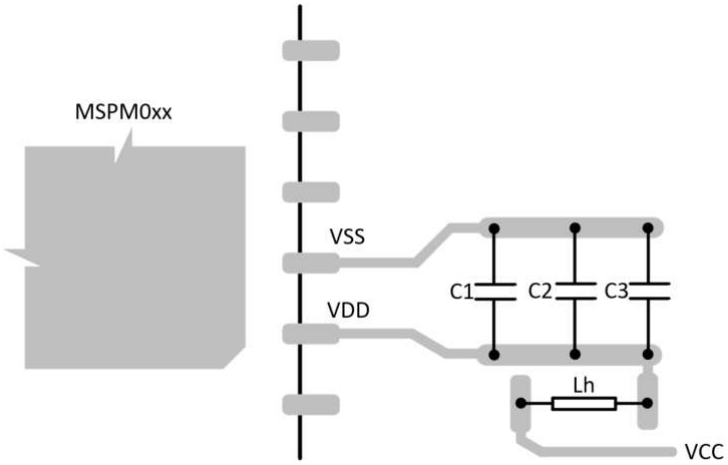

Figure 9-1. Suggested Power Supply Layout

9.2 Considerations for Ground Layout

System ground is the most critical area and foundation related to noise and EMI problems on the board. The most practical way to minimize these problems is to have a separate ground plane.

What is Ground Noise?

Each signal originating from a circuit (for example, a driver) has a return current flow to the source by ground path. As the frequency increases, or even for simple but high-current switching like relays, there is a voltage drop due to line impedance generating interference in the grounding scheme. The return path is always through the least resistance. For DC signals, that is the lowest resistive path. For high frequency signals, that is the lowest impedance path. This explains how a ground plane simplifies the issue and is the key to making sure of signal integrity.

TI does not recommend that the digital return signals propagate inside the analog return (ground) area; therefore, the designer must split the ground plane to keep all the digital signal return loops within the ground area. Splitting needs to be done carefully. Many designs use a single (common) voltage regulator to generate a digital and analog supply of the same voltage level (for example, 3.3V). Users need to isolate the analog rail and digital supply rails and the respective grounds from each other. Be careful while isolating the ground, as both grounds have to be shorted somewhere. Figure 9-2 shows how possible return paths for digital signals are not allowed to form a loop passing through the analog ground. On each design, decide the common point considering the component placements and so forth. Do not add any inductors (ferrite bead) or resistors (not even zero Ω) in the series with any ground trace. The impedance increases due to associated inductance at a high frequency, causing a voltage differential. Do not route a signal referenced to digital ground over analog ground or the other direction.

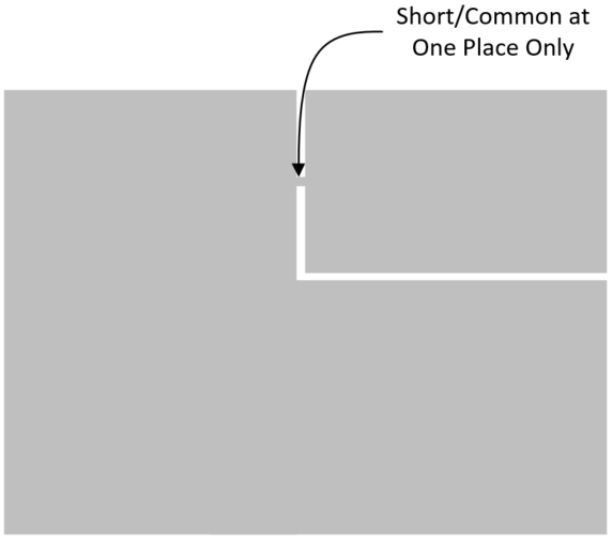

Figure 9-2. Digital and Analog Grounds and Common Area

9.3 Traces, Vias, and Other PCB Components

A right angle in a trace can cause more radiation. The capacitance increases in the region of the corner and the characteristic impedance changes. This impedance change causes reflections. Avoid right-angle bends in a trace and try to route them with at least two 45° corners. To minimize any impedance change, the best routing is a round bend, as shown in Figure 9-3.

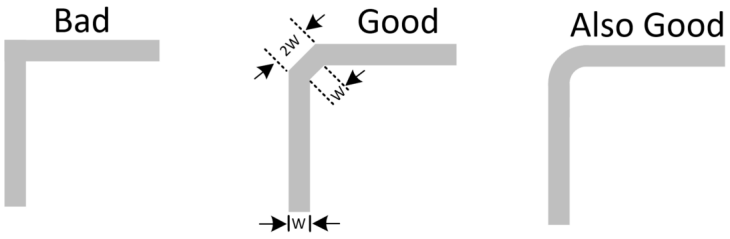

Figure 9-3. Poor and Correct Way of Bending Traces in Right Angle

To minimize crosstalk, not only between two signals on one layer but also between adjacent layers, route them 90° to each other. More complex boards need to use vias while routing; however, care must be taken when using vias as these add additional inductance and capacitance, and reflections occur due to the change in the characteristic impedance. Vias also increase the trace length. When using differential signals, use vias in both traces or compensate the delay in the other trace as well.

For signal traces, observe the impact of high-frequency pulse signals, especially on relatively small analog signals (like sensor signals). Too many crossovers couple the electromagnetic noise of the high-frequency signal to the analog signal, which results in a low signal-to-noise ratio of the signal and affect the signal quality. Therefore, avoid crossing when designing. But, if there is indeed an unavoidable intersection, then TI recommends to intersect vertically to minimize the interference of electromagnetic noise. Figure 9-4 shows how to reduce this noise.

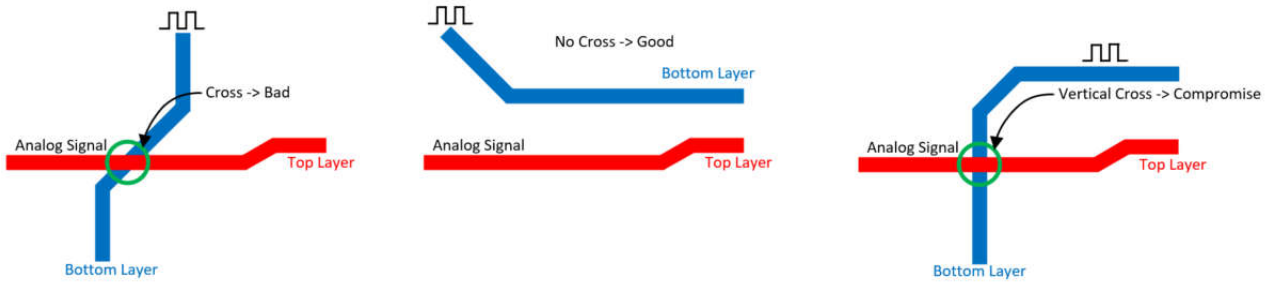

Figure 9-4. Poor and Correct Cross Traces for Analog and High-Frequency Signals

9.4 How to Select Board Layers and Recommended Stack-up

To reduce the reflections on high-speed signals, match the impedance between the source, sink and transmission lines. The impedance of a signal trace depends on the geometry and position with respect to any reference planes.

The trace width and spacing between differential pairs for a specific impedance requirement is dependent on the chosen PCB stack-up. As there are limitations in the minimum trace width and spacing which depend on the type of PCB technology and cost requirements, a PCB stack-up needs to be chosen which allows all the required impedances to be realized.

The minimum configuration that can be used is 2 stack-up. A 4- or 6-layer boards are required for very dense PCBs that have multiple high-speed signals.

The following stack-ups in Figure 9-5 are intended as 4-layer examples that can be used as a starting point for stack-up evaluation and selection. These stack-up configurations use a GND plane adjacent to the power plane to increase the capacitance and reduce the gap between GND and power plane. High-speed signals on the top layer have a solid GND reference plane that helps to reduce EMC emissions. Increasing the number of layers and having a GND reference for each PCB signal layer further improves the radiated EMC performance.

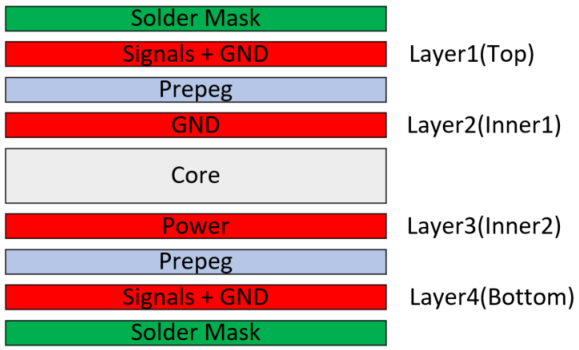

Figure 9-5. Four-Layer PCB Stack-up Example

If the system is not very complicated and there is no high-speed signal or some sensitive analog signal, then the 2 stack-up structure is sufficient.

10 Bootloader

10.1 Bootloader Introduction

A bootloader is a firmware IP (software shipped pre-programmed with the device) that can be used to program the SoC memories (flash and SRAM) using serial interfaces like UART or I2C. The bootloader is usually invoked after the bootcode has completed when the device is about to start the customer application. To support production programming use cases some bootloaders also offer more interfaces like SPI or CAN. A bootloader can also be used for in-field updates.

10.2 Bootloader Hardware Design Considerations

10.2.1 Physical Communication interfaces

The MSPM0G bootloader (BSL) is implemented on UART and I2C serial interfaces. In MSPM0G devices, the BSL can automatically select the interface used to communicate with the device. The BSL communication pins are predefined in the ROM based bootloader. The specific instance of the peripheral interfaces that is used depends on the selected device and can be found in the device-specific data sheet. Refer to the device data sheet to find which pin has been assigned for BSL communication function before the hardware design.

Note

The BSL invoke pin must be pulled down to avoid entering BSL mode after reset.

10.2.2 Hardware Invocation

The bootloader supports hardware invocation after a BOOTRST through the use of a GPIO. The BSL configuration in the NONMAIN flash memory contains the pad, pin, and polarity definition for the GPIO invocation. Devices come configured from TI for a specific GPIO and polarity, but software can change this default by modifying the GPIO pin configuration in the BSL configuration in NONMAIN flash memory. See the device specific data sheet to determine the default BSL invoke GPIO. Figure 10-1 shows an example for the GPIO pin PA18 with high level to trigger bootloader.

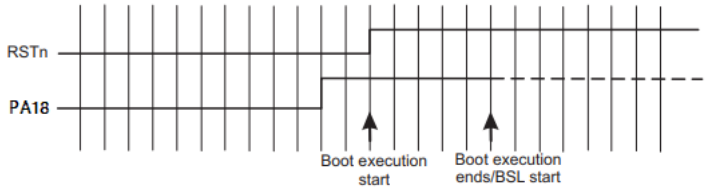

Figure 10-1. BSL Entry Sequence at Configured GPIO Pin

11 Summary

This application note cover every aspect of hardware development including power supplies, reset circuits, clocks, debugger connections, analog and digital peripherals, GPIO, and board layout guidelines. This document can help users to quickly start hardware designs by following the considerations shown in this application note.

12 References

1. Texas Instruments, MSPM0G350x Mixed-Signal Microcontrollers With CAN-FD Interface, data sheet
2. Texas Instruments, MSPM0 G-Series 80MHz Microcontrollers, technical reference manual
3. Texas Instruments, MSPM0 L-Series MCUs Hardware Development Guide, application note
4. Texas Instruments, TLIN1021A-Q1 Fault-Protected LIN Transceiver with Inhibit and Wake, data sheet
5. Texas Instruments, TCAN1042-Q1Automotive Fault Protected CAN Transceiver with CAN FD, data sheet

13 Revision History

Changes from Revision D (March 2026) to Revision E (April 2026) **Page**

- Updated Table 1-1 regarding VREF+ and VREF-..... 3
- Updated Table 8-3 regarding PAx unused pin configurations.....28

Changes from Revision C (May 2025) to Revision D (March 2026)	Page
• Updated Table 8-3	28

Changes from Revision B (June 2023) to Revision C (May 2025)	Page
• Updated VCORE cap value and NRST cap value in *MSPM0G Typical Application Schematic* figure	3
• Added unused pin description and thermal pad description.	3
• Changed the cap value on NRST in *MSPM0G Hardware Design Check List* table	3
• Updated NRST cap value in *Digital Power Supply* section	6
• Updated TIMAx description in *TIMA Instance Configuration* table	20
• Updated TIMGx description in *TIMG Instance Configuration* table	20
• Deleted TIMHx description in *MSPM0G UART Specifications* table	21
• Updated UART feature description in *UART Features* table	21
• Updated *MSPM0G I2C Characteristics* table with latest data sheet information	24
• Updated *MSPM0G GPIO Switching Characteristics* table with latest data sheet information	26

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