

## ***TFP401PZP Evaluation Module***

This document describes how to use and configure the TFP401PZPEVM board and describes some of the factors that should be considered in using this EVM.

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## 1 Overview

### 1.1 What is the TFP401?

The Texas Instruments TFP401 is a TI PanelBus™ flat-panel display product that is part of a comprehensive family of end-to-end DVI. The TFP401 has 1.0 compliant solutions and is targeted primarily at desktop LCD monitors and digital projectors. The TFP401 supports display resolutions up to 1080p and WUXGA in 24-bit true-color pixel format.

### 1.2 What is the TFP401PZPEVM?

The TFP401PZPEVM board is used to evaluate the performance and design of the TFP401 using a DVI source. This board receives DVI data from the input source through a standard DVI cable to a TFP401 which converts the data to a 24-bit parallel format.

This EVM can be used as a hardware reference design for any implementation using the TFP401. PCB design and layout files are provided upon request to aid PCB design with a TFP401 component.

The board is designed and optimized to support high-speed operation. The board impedance should be controlled as closely as possible to  $50\ \Omega$ . Impedance mismatches should be kept to a minimum by designing the component pad size to be as close as possible to the width of the connecting transmission line. In addition, to reduce board skew, trace lengths should be matched as closely as possible.

Some features offered by this board include:

- PCB designed for high-speed signal integrity.
- High-speed output signals that all have differential test point accessibility.

### 1.3 What is Included in the TFP401PZPEVM?

The major components of the EVM include:

- TFP401
- DVI connector
- Two 56-Pin Headers

### 1.4 What Does This EVM Look Like?

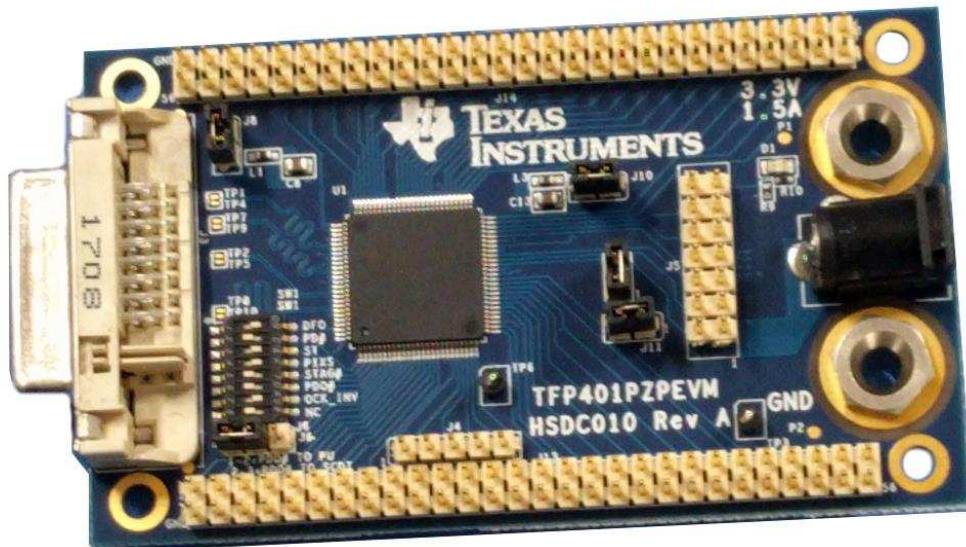


Figure 1. TFP401PZPEVM

## 2 Hardware Description

### 2.1 EVM Board Configuration and Operation

Operation of the DVI EVM board requires the following equipment:

- DVI source (Programmable Video Signal Generator)
- DVI cable
- 5-V wall power adapter capable of 1 A or 3.3-V power supply capable of 1 A with connecting cables

### 2.2 Installation

The TFP401PZPEVM board requires the following steps to operate:

1. Connect a 5-V wall power adapter to J12 of the board or a 3.3-V DC power supply to P1 (+) and P2 (-).
2. Connect a DVI cable from the DVI source to J3 of the board (typically 2m cable).
3. Power on the supply.

The TFP401PZPEVM board has various options for different modes of operation, selectable by jumpers and switches. When shipped, the board is fully operational and all jumpers are in the default positions. See the configuration tables if the board configuration has been changed.

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**NOTE:** When handling boards, standard ESD protection is required.

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### 2.3 Power Supply

The TFP401PZPEVM has two options to provide voltage:

1. A plug (J12) to accept a 5-V wall power adapter.
2. Two banana jacks (P1 (+) and P2 (-)) to connect an external regulated power supply of 3.3-V DC taking care to observe marked polarity.

The supply should have a current rating of approximately 1 A. Take care to ensure a clean power supply when minimum ripple is used, as supply noise can manifest itself on the DVI output.

### 2.4 High-Speed Data Line Probe Point

The high-speed data lines are monitored on an oscilloscope with a high-bandwidth differential scope probe through probe points on the EVM board. Although small, scope probe loading may disrupt operation of the DVI signal during probing. [Table 1](#) describes the test point function for the high-speed DVI signals.

**Table 1. High Speed Test Points**

Connector Reference Designator	Test Point
TP1	RX2P
TP2	RX0N
TP4	RX2N
TP5	RX0P
TP7	RX1P
TP8	RXCP
TP9	RX1N
TP10	RXCN

### 2.5 Switch Functions

[Table 2](#) shows the function and default configuration of the switches on the TFP401PZPEVM board. See the data sheet for specific pin functions.

**Table 2. Switch 1 Function and Default Settings**

SW1 Switch Section	Label	Function	Default Position
1	DFO	RX device DFO select	ON (0 V)
2	PD/	RX device PD/ select	OFF (3.3 V)
3	ST	RX device ST select	ON (0 V)
4	PIXS	RX device PIXS select	ON (0 V)
5	STAG	RX device STAG select	OFF (3.3 V)
6	PDO/	RX device PDO/ select	OFF (3.3 V)
7	OCK_INV	RX device OCK_INV select	ON (0 V)
8	N/C	Not used	ON (0 V)

## 2.6 Jumper Functions

**Table 3** shows the function of jumper positions on the TFP401PZPEVM with the default location of shunt. See the data sheet for specific pin functions. Jumpers are listed in order of appearance rather than in numeric order for easier comparison to the board.

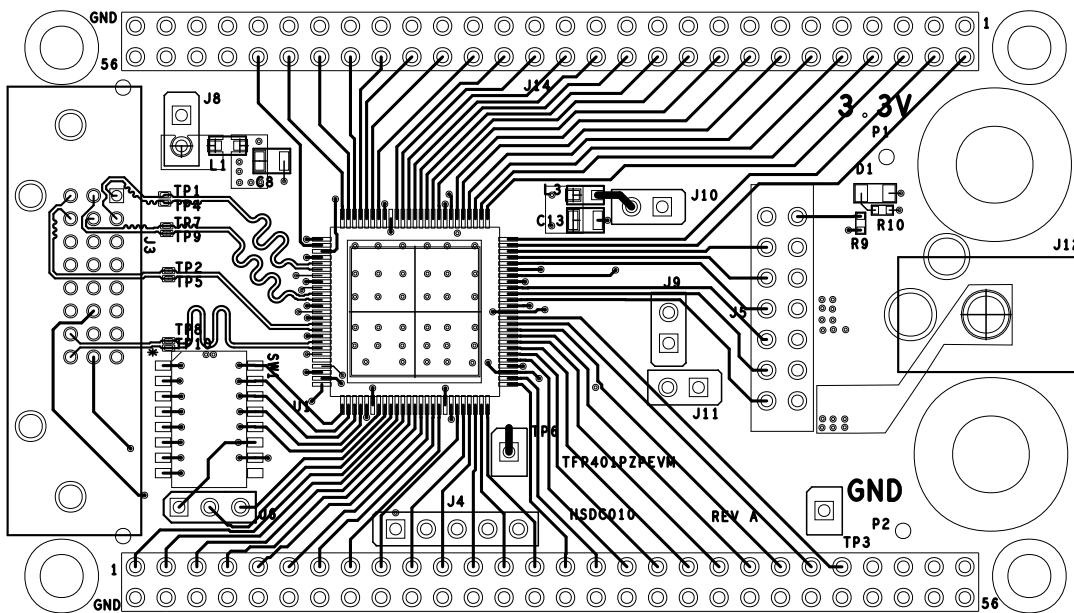
**Table 3. Jumper Function and Default Shunt Position**

Jumper Reference Designator	Description	Default Shunt Position
J8	AVDD supply	Installed
J9	DVDD supply	Installed
J10	OVDD supply	Installed
J11	PVDD supply	Installed
J6	PDO/ control	Installed on pin 1–2

### 3 Physical Description

This section describes the physical characteristics and PCB layout of the EVM and lists the components used on the module. The EVM schematics are also included.

### 3.1 EVM Board Diagram



**Figure 2. TFP401PZPEVM Top**

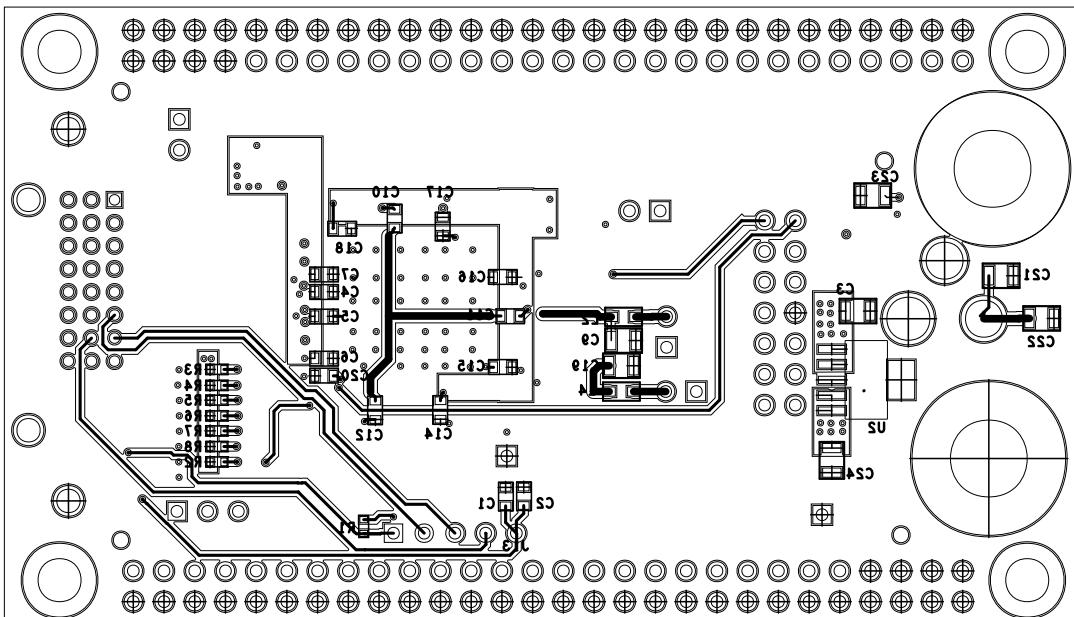


Figure 3. TFP401PZPEVM Bottom

## 4 TFP401PZPEVM Bill of Materials

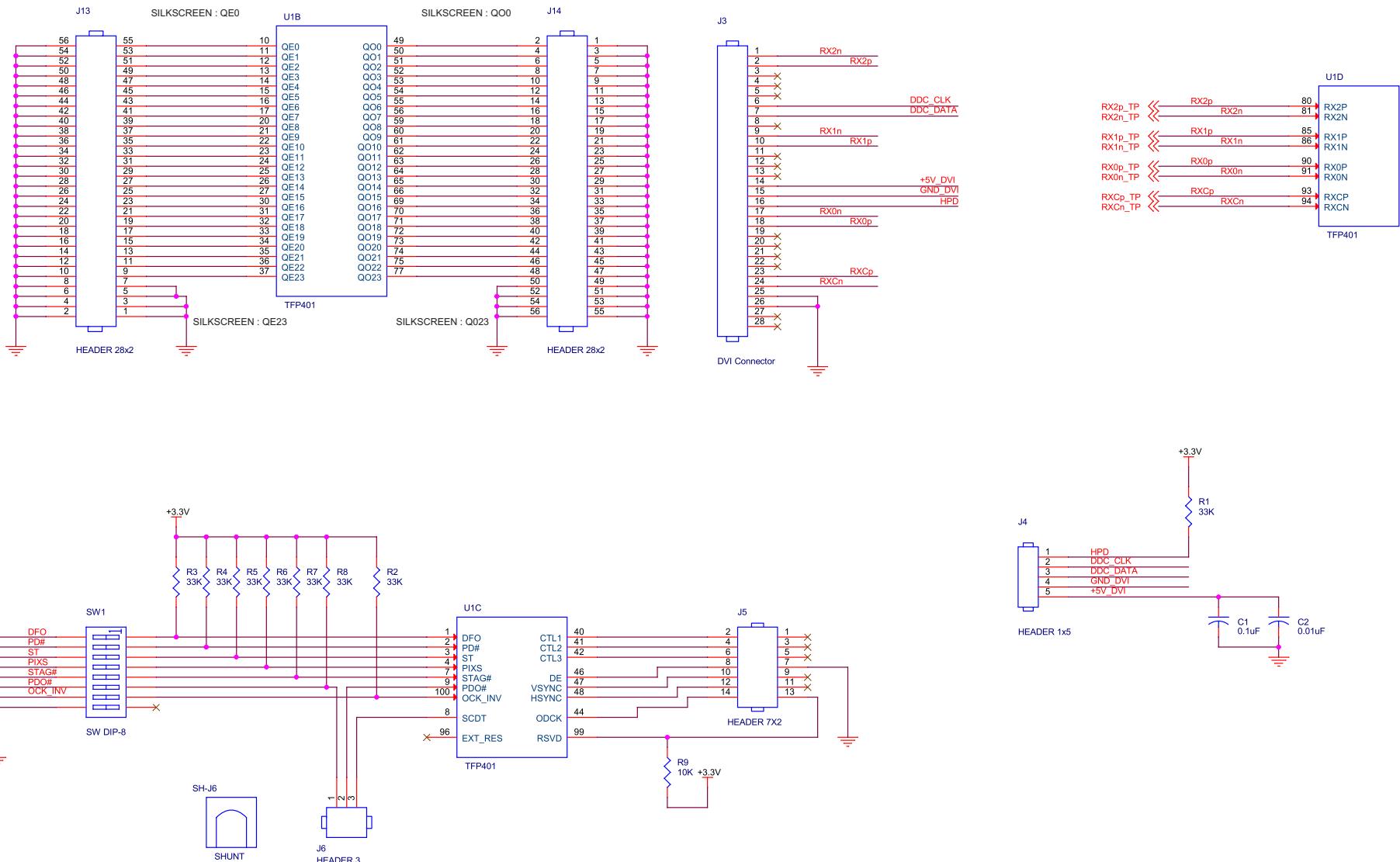
**Table 4. Bill of Materials**

Item	Quantity	Reference	Part	FootPrint	Manufacturer	Manufacturer Part Number	Description
1	14	C1,C4,C5,C6,C7,C10,C11,C12,C14,C15,C16,C17,C18,C20	0.1uF	cc0603	KEMET	C0603C104K8RACTU	CAP CER 0.1UF 10V X7R 0603
2	1	C2	0.01uF	cc0603	Murata	GRM1857U1A103JA44D	CAP CER 10000PF 10V U2J 0603
3	2	C3,C23	10uF	cc0805	Yageo	CC0805ZKY5V6BB106	CAP CER 10UF 10V Y5V 0805
	3	C21,C22,C24	10uF	cc0805	Taiyo Yuden	EMK212BJ106KG-T	CAP CER 10UF 16V X5R 0805
4	4	C8,C9,C13,C19	22uF	cc0805	Murata Electronics North America	GRM21BR61A226ME51L	CAP CER 22UF 10V X5R 0805
5	1	D1	LED Green 0805	r0805	Lumex	LTST-C170KGKT	LED GREEN CLEAR 0805 SMD
6	1	J3	DVI Connector	DVI_conn_01	Molex, LLC	743204004	Description DVI-D, Dual Link Receptacle Connector 24 Position Panel Mount, Through Hole, Right Angle
7	1	J4	HEADER 1x5	berg1x5	TE Connectivity AMP Connectors	7-104878-1	05/06 MODII HDR SRST B/A .100
8	1	J5	HEADER 7X2	berg2x7	Amphenol FCI	67996-114HLF	14 Positions Header Connector 0.100" (2.54mm) Through Hole Gold or Gold, GXT™
9	1	J6	HEADER 3	hdr_thvt_1x3_10_0	Harwin Inc.	M20-9990345	3 Positions Header, Cuttable Connector 0.100" (2.54mm) Through Hole Gold
10	4	J8,J9,J10,J11	JUMPER	berg1x2	FCI	68001-402HLF	2 Positions Header Connector 0.100" (2.54mm) Through Hole Tin
11	1	J12	2.1mm x 5.5mm	PJ-202AH	CUI Inc.	PJ-202A	CONN PWR JACK 2X5.5MM KINKED PIN
12	2	J13,J14	HEADER 28x2	header2x28	Sullins Connector Solutions	PRPC028DAAN-RC	56 Positions Header, Breakaway Connector 0.100" (2.54mm) Through Hole Gold
13	4	L1,L2,L3,L4	BLM18RK601SN1D	CAP0603	Murata	BLM18RK601SN1D	FERRITE BEAD 600 OHM 0603 1LN
14	2	P1,P2	Banana-Jack	Banana_Jack_25_0mil	Cinch Connectivity Solutions Johnson	108-0740-001	CONN JACK BANANA UNINS PANEL MOU
15	8	R1,R2,R3,R4,R5,R6,R7,R8	33K	r0402	Yageo	RC0402JR-0733KL	RES SMD 33K OHM 5% 1/16W 0402
16	1	R9	10K	r0402	Yageo	RC0402JR-0710KL	RES SMD 10K OHM 5% 1/16W 0402
17	1	R10	330	r0402	Yageo	RC0402JR-07330RL	RES SMD 330 OHM 5% 1/16W 0402
18	1	SW1	SW DIP-8	TDA08H0SK1	C&K	TDA08H0SB1R	SWITCH SLIDE DIP SPST 25MA 24V
19	8	TP1,TP2,TP4,TP5,TP7,TP8,TP9,TP10	TEST POINT - DNI	TestPointSMT_1			OPEN PADS

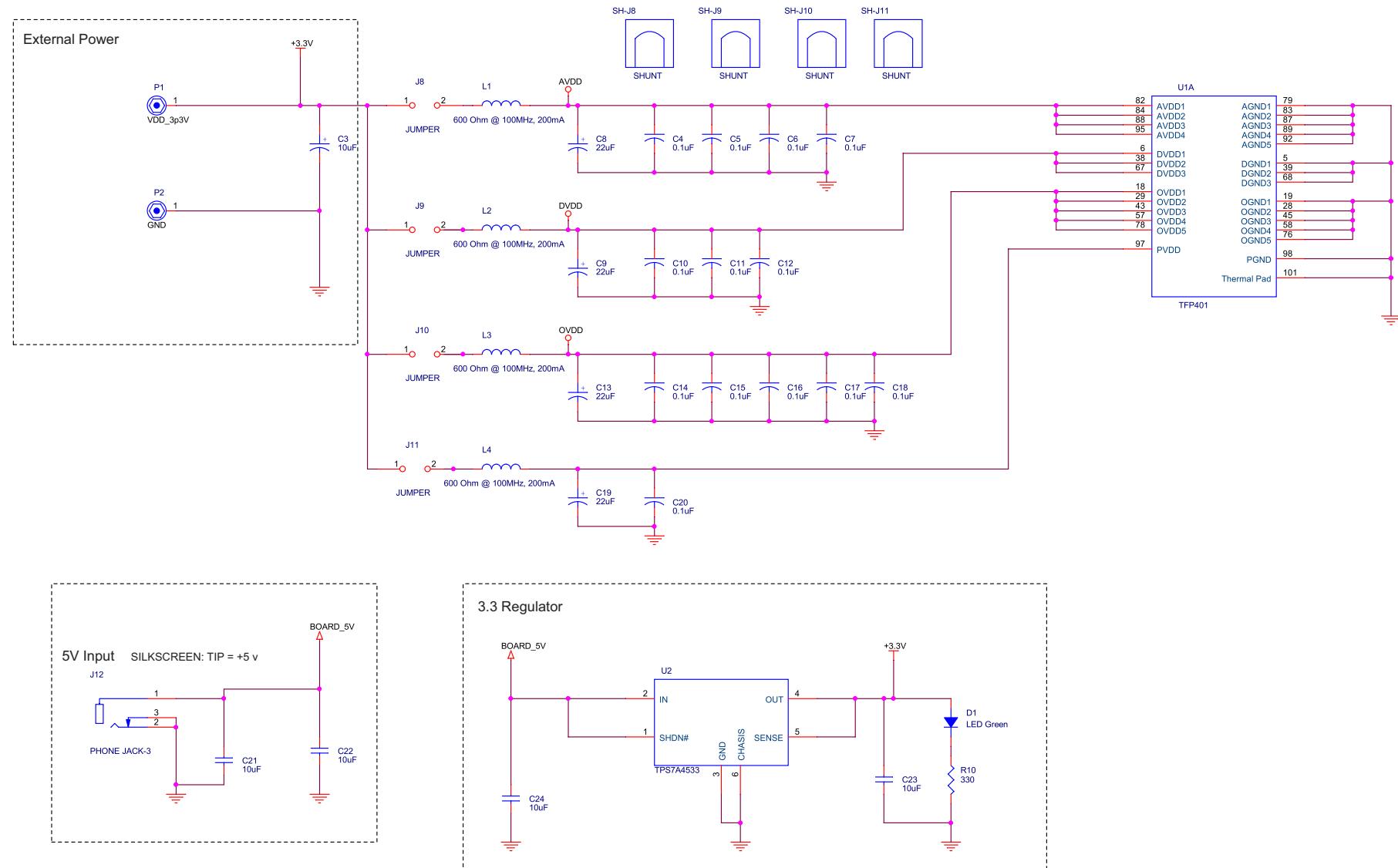
**Table 4. Bill of Materials (continued)**

Item	Quantity	Reference	Part	FootPrint	Manufacturer	Manufacturer Part Number	Description
20	2	TP3,TP6	TEST POINT	berg1x1	Keystone Electronics	5011	TEST POINT PC MULTI PURPOSE BLK
20	1	U1	TFP401	pzp-s-pqfp-g100	Texas Instruments	TFP401PZP	165 MHz PanelBus™ TMDS DVI Receiver/Deserializer
21	1	U2	TPS7A4533	dcq_r-pdso-g6	Texas Instruments	TPS7A4533DCQT	Low-Noise Fast-Transient-Response 1.5-A LDO Regulator
22	1	PCB	TFP401PZPEVM		ANY	HSDC010	TFP401PZPEVM HSDC010

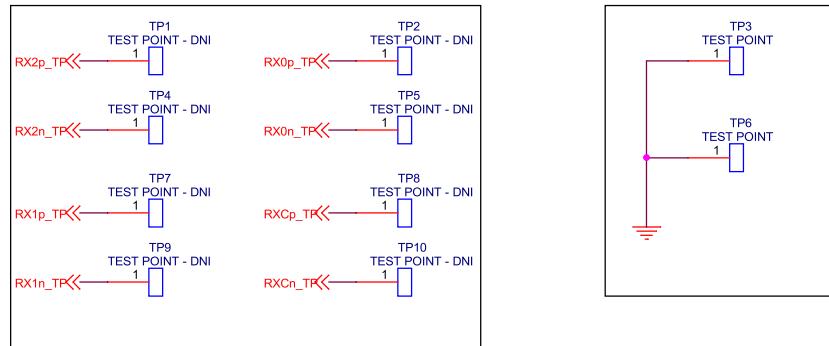
## 5 TFP401PZPEVM Schematic



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##### 3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

#### **CAUTION**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

#### **FCC Interference Statement for Class A EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

#### FCC Interference Statement for Class B EVM devices

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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###### **Concerning EVMs Including Radio Transmitters:**

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Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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