Application Report
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ISO72x Digital Isolator Magnetic-Field Immunity

Kevin Gingerich *High-Performance Linear/Interface Products*

ABSTRACT

The purpose of this analysis is to estimate the immunity of the ISO72x family of digital isolators to magnetic fields.

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Trademarks

1 Introduction

The expected application environment of a digital isolator includes close proximity to large motors and other magnetic-field-generating equipment. Data errors due to exposure to such fields are a concern. This is especially so because TI is applying a novel capacitive-coupled isolation barrier.

The ISO72x isolators transfer the data signals differentially across the isolation barrier through two capacitors formed with a metal top plate and conductive silicon bottom plate on each side of a SiO2 dielectric. The drive circuits reside on one substrate and the capacitors and receiving circuits reside on another substrate. Figure 1 shows the bond wires between the two substrates that complete the circuit. The electromotive force (emf) from time-varying magnetic fields in these differential circuits is the subject of this analysis. A noise budget is developed and Faraday's Law applied to estimate the magnetic flux density necessary to exceed the budget. Pulse magnetic field test results per CEI IEC 61000-4-9 offer empirical validation of the analysis.

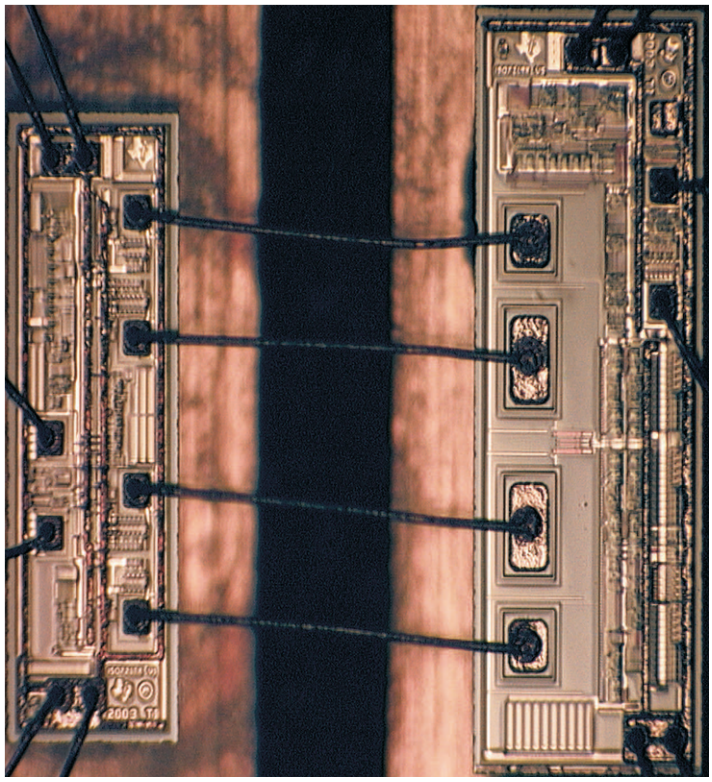


Figure 1. ISO721 Inter-Die Bonds

2 Differential Noise Budget

Figure 2 shows a basic model of the circuit path across the isolation barrier of the ISO72x. V_I is the output of a CMOS totem-pole driver operating from V_{CC1} and v_n represents differential noise. The isolation capacitors differentiate v_I and v_n such that only time-varying and amplitude information is presented to the receiver inputs. The receiver, operating from VCC2, amplifies the differential signal for level comparison, latching, validation, and presentation to the output.

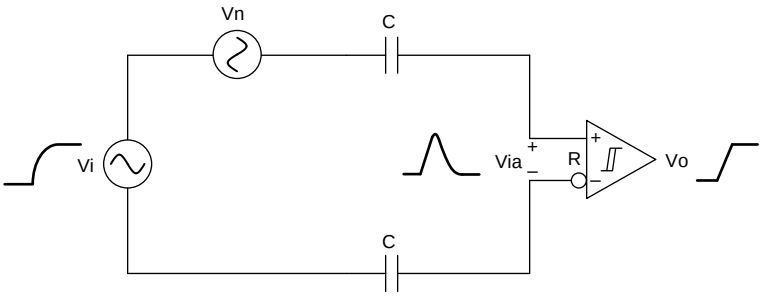


Figure 2. Equivalent Barrier Differential Circuit Schematic

In the absence of differential noise and during the steady state, there is no differential voltage across the inputs of the receiver, and the output is the last state latched. When the differential voltage v_{ia} exceeds the receiver positive-going or negative-going threshold voltage for a sufficient period, a state change occurs at the output of the receiving circuitry. Preferably, the state change is from v_I and not v_n. To prevent state changes from noise, the input voltage from v_n must remain below the positive-going threshold and above the negative-going threshold of the receiver during the steady state.

The lowest positive-going differential input voltage threshold of the ISO72x receiver is 10 mV, and the highest negative-going threshold is –10 mV. These thresholds apply over its recommended operating conditions and sinusoidal frequencies up to approximately 30 MHz. Above this frequency, the gain of the receiver decreases requiring more input voltage to cross the threshold and raising the input threshold magnitude. Therefore, it can be postulated that no steady-state errors occur if the magnitude of v_{ia} due to v_n is less than 10 mV for noise frequencies up to 30 MHz. Circuit simulation predicts a 100-MHz minimum noise threshold magnitude of 16.7 mV.

The input and output voltage of the circuit in the frequency domain is related by the system function H(ω) such that

$$V_{ia}(\omega) = V_n(\omega)H(\omega),$$

where

$$H(\omega) = \frac{j\omega}{j\omega + \frac{2}{RC}}$$

The requirement is that the magnitude of via be less than the minimum receiver threshold which is identified as VIT(ω) and |via(ω)|<|VIT(ω)|. Making the substitutions and rearranging gives:

$$|v_n(\omega)H(\omega)| < |V_{IT}(\omega)| \quad (2)$$

and

$$|v_n(\omega)| < \frac{\left|V_{IT}(\omega)\right|\sqrt{\omega^2 + \frac{4}{(RC)^2}}}{\omega} \quad (3)$$

The value of RC is approximately 43.8 ps, giving sufficient information to calculate differential noise margins.

Two primary sources of differential noise in the circuit are emf and common-mode-to-differential voltage conversion. Conservatively, one-half of the differential noise margin is allocated to each source giving the equation for the emf noise margin as shown in Equation 4.

$$|v_n(\omega)| < \frac{|V_{IT}(\omega)|\sqrt{\omega^2 + \frac{4}{(RC)^2}}}{2\omega} \quad (4)$$

3 emf Calculation

An electromotive force is merely a voltage that arises from conductors moving in a magnetic field or from changing magnetic fields. Faraday's Law for electromagnetic induction in a nonmoving circuit states that the emf induced is proportional to the time rate of change of the magnetic flux linked with the circuit. For stationary circuits, this law may be stated as shown in Equation 5.

$$\text{emf} = \oint \vec{E} \cdot d\vec{l} = -\frac{d}{dt}\int_{surface} \vec{B} \cdot d\vec{s} = -\int \frac{\partial \vec{B}}{\partial t} \cdot d\vec{s}$$

where

- E is the electric field intensity along a path length dl.
- B is the magnetic flux density normal to the surface ds. (5)

Assume a B field of $B_0 \sin\omega_0 t$ normal to and uniform over the surface. Taking the time partial derivative gives:

$$\text{emf} = -B_0\omega_0 \cos\omega_0 t \int_{surface} d\vec{s} \quad (6)$$

Of course, the surface integral of ds is simply the area enclosed by the loop, S, giving:

$$\text{emf}(t) = -B_0\omega_0 S \cos \omega_0 t \quad (7)$$

Each channel of the ISO72x has high-speed and low-speed isolated signals. The high-speed signal transfers input state changes whereas the low-speed signal transfers low-frequency, internally generated signals used to keep the input and output in the same state. (The loop nearest to the top of the page in Figure 1 is the high-speed circuit.) The two circuits are electrically the same but slightly differ in physical layout.

The differential circuit areas for integration are approximately rectangular, and the centers of the bond pads used to connect the inter-die wires define the corners. The nominal length of the inter-die bond wires is 954E-06 m. The distance between differential bond pads are the same on both die and 360E-06 m for the high-speed circuit and 990E-06 m for the low-speed circuit. This gives areas of 343E-09 m^2 for the high-speed differential loop and 944E-09 m^2 for the low-speed circuit. Because the largest area gives the greatest emf, the low-speed loop area is used.

Substituting this gives $emf(t) = -B_0\omega_0 944\times10^{-9} \cos \omega_0 t$ and, because the concern is only with magnitudes, emf becomes:

$$emf = B_0\omega_0 944 \times 10^{-9} \text{ V}. \tag{8}$$

4 Magnetic Field Sensitivity

Now, the maximum magnetic flux density can be calculated by bounding the magnitude of the emf with the emf noise margin or Equation 9

$$B_0\omega_0 944 \times 10^{-9} < \frac{\left|V_{IT}(\omega)\right| \sqrt{\omega^2 + \frac{4}{(RC)^2}}}{2\omega} \tag{9}$$

Solving the inequality for B_0 at ω_0 gives:

$$B_0 < \frac{\left|V_{IT}(\omega_0)\right| \sqrt{\omega_0^2 + \frac{4}{(RC)^2}}}{2\times944\times10^{-9}\omega_0^2} \text{ Wb / m}^2 \tag{10}$$

Table 1 solves Equation 4, Equation 8, and Equation 10 at different noise frequencies ($\omega = 2\pi f$).

Table 1. Solutions to Equations

f	$\lvert V_{IT}\rvert$	emf	B_O
0.001 MHz	10 mV	72,700 V	12.3E+6 Wb/m^2
0.01	10	7,270	122.6E+3
0.1	10	727	1.2E+3
1	10	72.7	12.3E+0
10	10	7.27	122.6E-3
30	10	2.4	13.6E-3
100	16.7	1.2	2.0E-3

For perspective, the magnetic flux density produced by a current element I 0 dl may be interpreted as shown in Equation 11.

$$\mathbf{B} = \oint \frac{\mu_O dl}{4\pi r^2} = \frac{\mu_O I}{4\pi r^2} \tag{11}$$

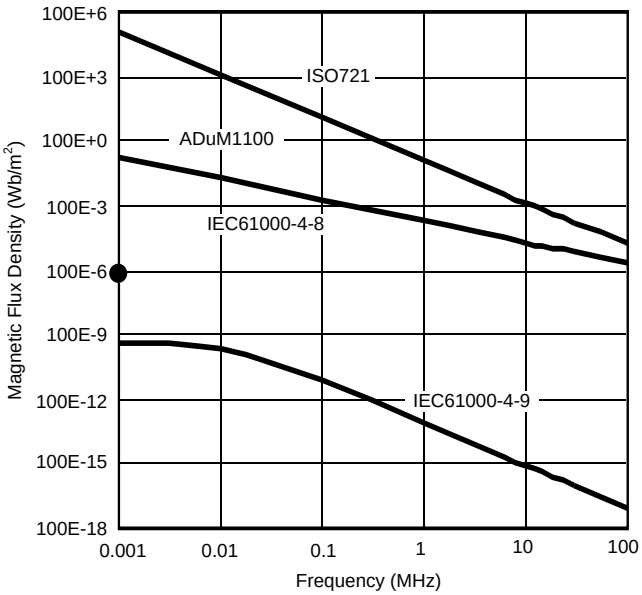
where

- $4\pi r^2$ is the surface area of a sphere of radius r positioned at each point along the conductor of length l.

If a 0.1-m differential current element is assumed as the source and $\mu = \mu_0$ and r = 0.1 m, the current would need to be in excess of ten million amperes to produce a magnetic flux density of 12.3 Wb/m^2 and exceed the 1-MHz limit.

The unshielded ISO721 has successfully passed the Class-5 magnetic field immunity requirements of IEC 61000-4-8 power-frequency fields up to 100 A/m (125.6×10^{-6} Wb/m^2) and IEC 61000-4-9 pulsed fields to 1000 A/m (1.256×10^{-3} Wb/m^2). The standard defines Class 5 as applying to severe industrial environments characterized by conductors, bus bars, medium-voltage lines, or high-voltage lines carrying tens of kA; ground conductors of the lightning protection system or high structures (like the line towers) carrying the whole lightning current. Switchyard areas of heavy industrial plants and power stations may be representative of this environment.

Figure 3 graphically compares the calculated magnetic field immunity thresholds of the ISO721 and Analog Device's ADuM1100(1) along with the Class-5 (highest) test levels of IEC 61000-4-8 and IEC 61000-4-9 (2).



(1) Data was taken from Figure 8 of revision E of the ADuM1100 data sheet and converted to comparable units.

(2) Assumes the permeability of free space and approximates the IEC 61000-4-9 pulse shape as 304 / [(jω + 78.7 × 10^3) (ω + 10^5)].

Figure 3. Magnetic Flux Density vs Frequency Magnetic Field Immunities and Test Thresholds

5 Conclusions

Magnetic coupling in the differential circuit of the low-speed signal of the ISO72x exceeding the noise budget requires a magnetic flux density greater than 12.3 Wb/m^2 (123 kGauss) at 1 MHz. This would be the field generated by over ten million amperes in a 0.1-m conductor 0.1 m away from the device. It is unlikely that this will occur in nature or any manufactured equipment. If it did, it is more likely that surrounding circuitry would fail before the barrier circuit of the ISO72x.

We currently recommend the ISO7710 from our newest ISO77xx family of digital isolators with improved isolation ratings.

6 References

- Fink, Donald G., *Electronic Engineers' Handbook*, McGraw-Hill, 1975
- Hayt, William H., Jr., *Engineering Electromagnetics, McGraw-Hill*, 1974
- McGillem, Clare D. and Cooper, George R., *Continuous and Discrete Signal and System Analysis*, Holt, Rinehart and Winston, Inc., 1974
- *Electromagnetic Interference Test Report for the ISO721 HIGH-SPEED DIGITAL ISOLATOR*, Southwest Research Institute, Document no. EMCR 05/019 rev. 00, August 2005

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (February 2006) to B Revision	Page
• Added the reference to the ISO7710 device in the *Conclusions*	5

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