

PowerPAD™ Thermally Enhanced Package

Steven Kummerl

ABSTRACT

The PowerPAD™ thermally enhanced package provides greater design flexibility and increased thermal efficiency in a standard size device package. The PowerPAD package’s improved performance permits higher clock speeds, more compact systems and more aggressive design criteria. PowerPAD™ packages are available in several standard surface mount configurations. They can be mounted using standard printed-circuit board (PCB) assembly techniques, and can be removed and replaced using standard repair procedures. To make optimum use of the thermal efficiencies designed into the PowerPAD™ package, the PCB must be designed with this technology in mind. In order to leverage the full thermal performance benefits offered from the PowerPad™ package, the exposed pad must be soldered to the board. This document focuses on the specifics of integrating a PowerPAD™ package into the PCB design.

Contents

1	Introduction	2
2	Installation and Use	3
3	Assembly	12
4	Repair	15
5	Summary	16
Appendix A	Definitions and Modeling	17
Appendix B	Rework Process for Heat Sink TQFP and TSSOP PowerPAD™ Packages - from Air-Vac Engineering	24
Appendix C	PowerPAD™ Process Rework Application Note from Metcal	28

List of Figures

1	Cross Section of PowerPAD™ Package Mounted to PCB and Resulting Heat Transfer	2
2	Bottom and Top View of the 20-Pin TSSOP PowerPAD™ Package	3
3	64 Pin, 14 × 14 × 1.0 mm Body TQFP PowerPAD™ Package	3
4	Package and PCB Land Configuration for a Single Layer PCB	4
5	Package and PCB Land Configuration for a Multi-Layer PCB	5
6	64-Pin TQFP Package with PowerPAD™ Implemented, Bottom View	6
7	PCB Thermal Land Design Considerations for Thermally-Enhanced TQFP Packages	7
8	Impact of the Number of Thermal Vias vs Chip Area (Die Area)	8
9	Impact of the Number of 0.33 mm (0.013 inch) Diameter Thermal Vias vs Chip Area (Die Area)	8
10	Example Thermal Land Size and Thermal Via Patterns for PowerPAD™ Layout	9
11	Sample Land Pattern and Stencil Design for Thermally Enhanced TQFP Packages	11
12	Thermal Modeling of 20 DWP Effects of Varying Solder Coverage and Standoff Height on θ_{JA}	12
13	Thermal Modeling of 100 PZP Effects of Varying Solder Coverage on θ_{JA}	12
14	Range of Reflow Temperatures per JSTD-020C	13
15	Moisture Sensitivity Labeling	14
16	Thermal Resistance Diagram	17
17	Texas Instruments Example Jedec Board Design (Side View)	18
18	Thermal Pad and Lead Attachment to PCB Using the PowerPAD™ Package	19
19	General Leadframe Drawing Configuration	21
20	PowerPAD™ θ_{JP} Measurement	22

21	Standard Package θ_{JC} Measurement	22
22	Comparison of θ_{JA} for Various Packages.....	23
23	DRS22C Reworking Station	24
24	Reworking Nozzles of Various Sizes	25
25	Reworking Nozzles of Various Sizes	25
26	Nozzle Configuration.....	25
27	Air-Vac Vision System	26

List of Tables

1	Typical Power-Handling Capabilities of PowerPAD™ Packages	3
2	Center PowerPAD™ Solder Stencil Opening	7
3	Classification Reflow Profiles	14
4	PowerPAD™ Package Template Description	20
5	Metcal Conduction Tips	28

Trademarks

PowerPAD is a trademark of Texas Instruments.
 All other trademarks are the property of their respective owners.

1 Introduction

The PowerPAD™ concept is implemented in a standard epoxy-resin package material. The integrated circuit die is attached to the leadframe die pad using a thermally conductive epoxy. The package is molded so that the leadframe die pad is exposed at a surface of the package. This provides an extremely low thermal resistance (θ_{JP}) path between the device junction and the exterior of the case. Because the external surface of the leadframe die pad is on the PCB side of the package, it can be attached to the board using standard reflow soldering techniques. This allows efficient attachment to the board, and permits board structures to be used as heat sinks for the IC. Using vias, the leadframe die pad can be attached to an internal copper plane or special heat sink structure designed into the PCB. Check the respective product data sheet to verify which signal, power, or ground plane the device should be soldered to. For the first time, the PCB designer can implement power packaging without the constraints of extra hardware, special assembly instructions, thermal grease or additional heat sinks.

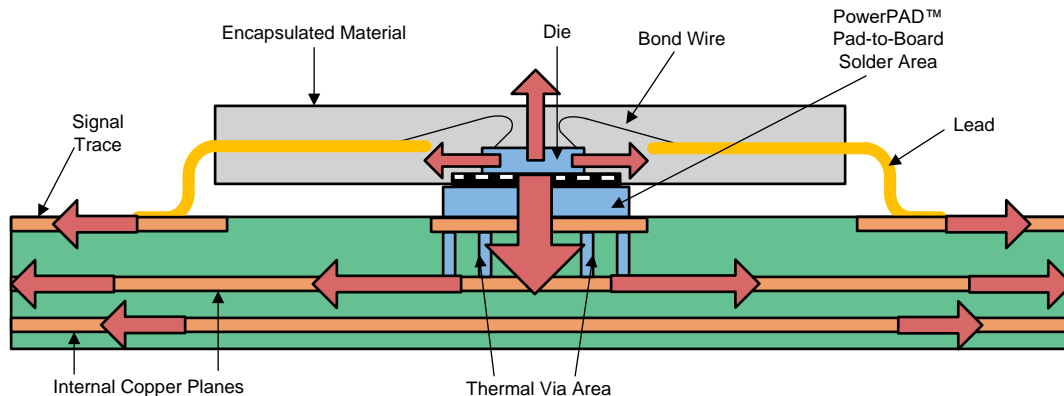


Figure 1. Cross Section of PowerPAD™ Package Mounted to PCB and Resulting Heat Transfer

Because the exact thermal performance of any PCB is dependent on the details of the circuit design and component installation, exact performance figures cannot be given here. However, representative performance is very important in making design decisions. The data shown in [Table 1](#) is typical of the performance that can be expected from the PowerPAD™ package.

Table 1. Typical Power-Handling Capabilities of PowerPAD™ Packages⁽¹⁾

PACKAGE TYPE	PIN COUNT	POWER HANDLING (W)	
		STANDARD PACKAGE	PowerPAD™ PACKAGE
SSOP	20	0.75	3.25
TSSOP	24	0.55	2.32

⁽¹⁾ Assumes +150°C junction temperature (T_J) and +80°C ambient temperature. Values are calculated from θ_{JA} figures shown in Appendix A.

For example, the user can expect 3.25 W of power-handling capability for the PowerPAD™ version of the 20-pin SSOP package. The standard version of this package can handle only 0.75 W. Details for all package styles and sizes are given in Appendix A.

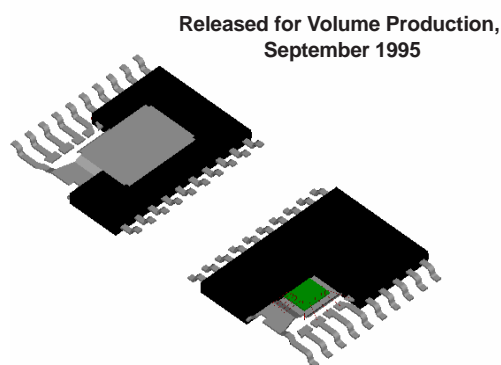
The standard package used in this example is a fully encapsulated device, whereas the PowerPAD™ package has an exposed die mounting pad which is soldered directly to the PCB. The PowerPAD™ package is not designed to be used without the exposed pad being soldered to the PCB.

2 Installation and Use

2.1 PCB Attachment

Proper thermal management of the PowerPAD™ package requires PCB preparation. This preparation is not difficult, nor does it use any extraordinary PCB design techniques, however it is necessary for proper heat removal. The PowerPAD™ package with exposed pad down is designed to be soldered to the PCB. Texas Instruments does not recommend the use of a PowerPAD™ package without soldering it to the PCB due to the risk of lower thermal performance and mechanical integrity.

Pad-Up PowerPAD™ packages should have appropriately designed heat sinks attached. Because of the variation and flexible nature of this type of heat sink, additional details should come from the specific manufacturer of the heat sink.



Released for Volume Production,
September 1995

Figure 2. Bottom and Top View of the 20-Pin TSSOP PowerPAD™ Package

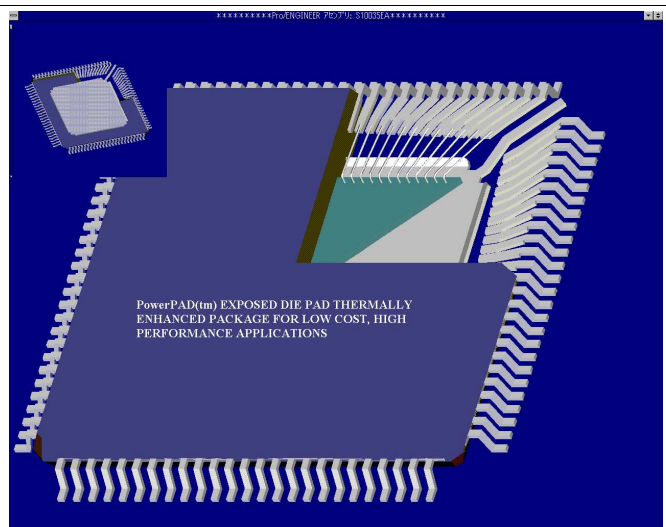


Figure 3. 64 Pin, 14 x 14 x 1.0 mm Body TQFP PowerPAD™ Package

All of the thermally enhanced packages incorporate features that provide a very low thermal resistance path for heat removal from the integrated circuit - either to and through a printed-circuit board (in the case of zero airflow environments), or to an external heatsink. The TI PowerPAD™ implementation does this by creating a leadframe where the bottom of the die pad is exposed, as opposed to the case where a heat slug is embedded in the package body. (See Figure 2 and Figure 3).

2.2 PCB Design Considerations

The printed-circuit board used with PowerPAD™ packages must have features included in the design to create an efficient thermal path to remove the heat from the package. As a minimum, there must be an area of solderable copper underneath the PowerPAD™ package. This area is called the thermal land. As detailed below, the thermal land varies in size depending on the PowerPAD™ package being used, the PCB construction and the amount of heat that needs to be removed. In addition, this thermal land may or may not contain thermal vias depending on PCB construction. The requirements for thermal lands and thermal vias are detailed below.

2.3 Thermal Lands

A thermal land is required on the surface of the PCB directly underneath the body of the PowerPAD™ package. During normal surface mount reflow solder operations, the leadframe on the underside of the package is soldered to this thermal land creating a very efficient thermal path. Normally, the PCB thermal land has a number of thermal vias within it that provide a thermal path to internal copper planes (or to the opposite side of the PCB) that provide for more efficient heat removal. The size of the thermal land should be as large as needed to dissipate the required heat.

For simple, double-sided PCBs, where there are no internal layers, the surface layers must be used to remove heat. Shown in Figure 4 is an example of a thermal land for a 24-pin package. Details of the package, the thermal land and the required solder mask are shown. Refer to the device-specific data sheet for detailed dimensions of the exposed pad on the package. If the PCB copper area is not sufficient to remove the heat, the designer can also consider external means of heat conduction, such as attaching the copper planes to a convenient chassis member or other hardware connection.

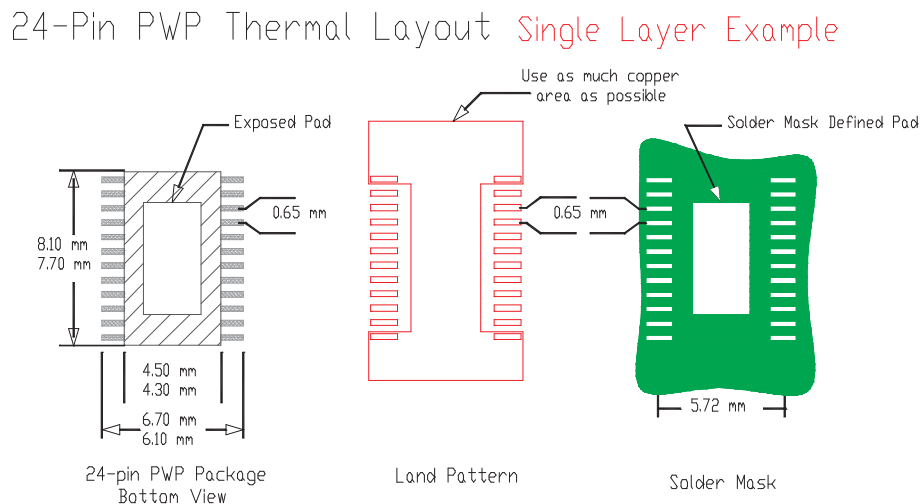


Figure 4. Package and PCB Land Configuration for a Single Layer PCB

In the PWP-24 example shown in Figure 4, the copper area is maximized on the surface of the board with a soldermask defined pad designed onto the copper area. The PCB's solder mask defined pad should be designed to the maximum exposed pad size shown in the respective device's product data sheet.

NOTE: Refer to the device-specific data sheet for the exact pad dimensions for the used device.

For multilayer PCBs, the designer can take advantage of internal copper layers (such as the ground plane) for heat removal. Check the respective device's product data sheet to verify which signal, power, or ground plane the device should be soldered to. The external thermal land on the surface layer is still required, however the thermal vias can conduct heat out through the internal power or ground plane. Shown in Figure 5 is an example of a thermal land used for multilayer PCB construction. In this case, the primary method of heat removal is down through the thermal vias to an internal copper plane.

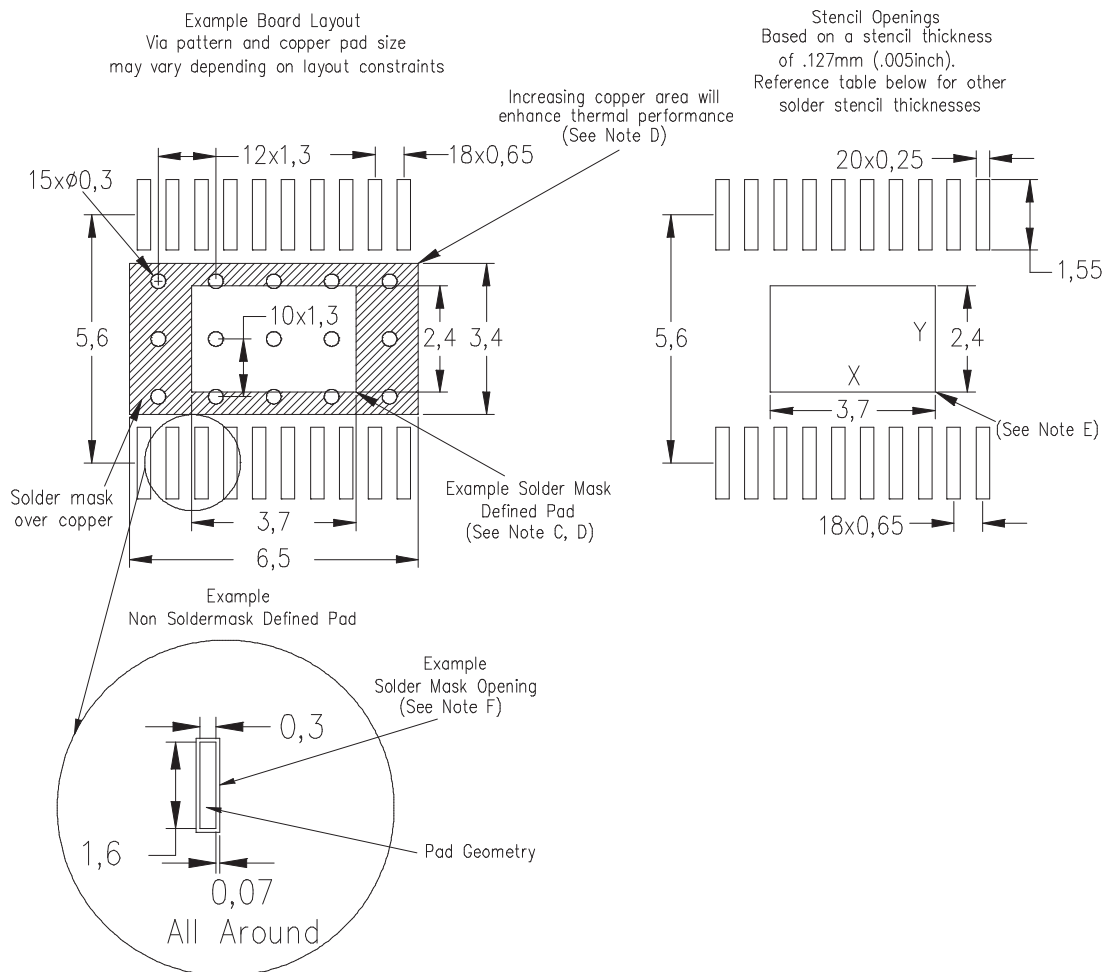


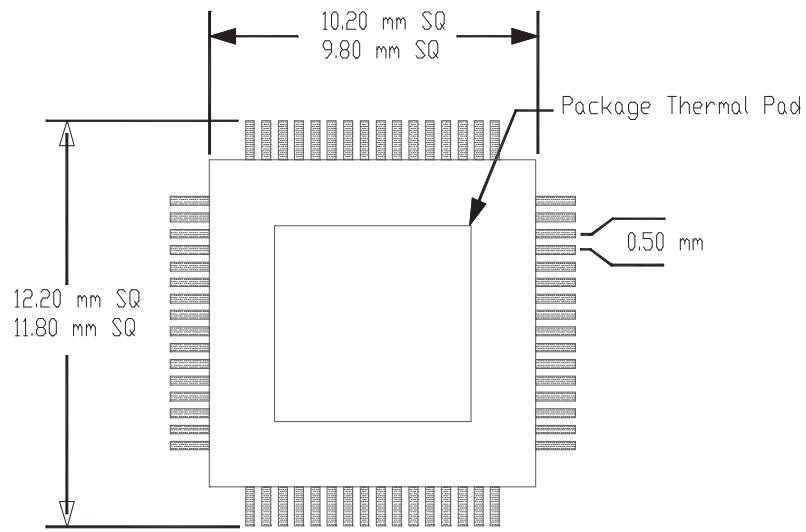
Figure 5. Package and PCB Land Configuration for a Multi-Layer PCB

NOTE: The dimensions of the 24-pin PWP package shown in [Figure 5](#) is for reference only. Refer to the device-specific data sheet for exact package dimensions for your device.

The details of a 64-pin TQFP PowerPAD™ package are shown in [Figure 6](#) . The recommended PCB thermal land for this package is shown in [Figure 7](#) . The maximum copper land size for TQFP packages is the package body size minus 2.0 mm. A solder mask defined pad is then placed onto the copper land sized to the maximum exposed pad size listed in the respective product data sheet.

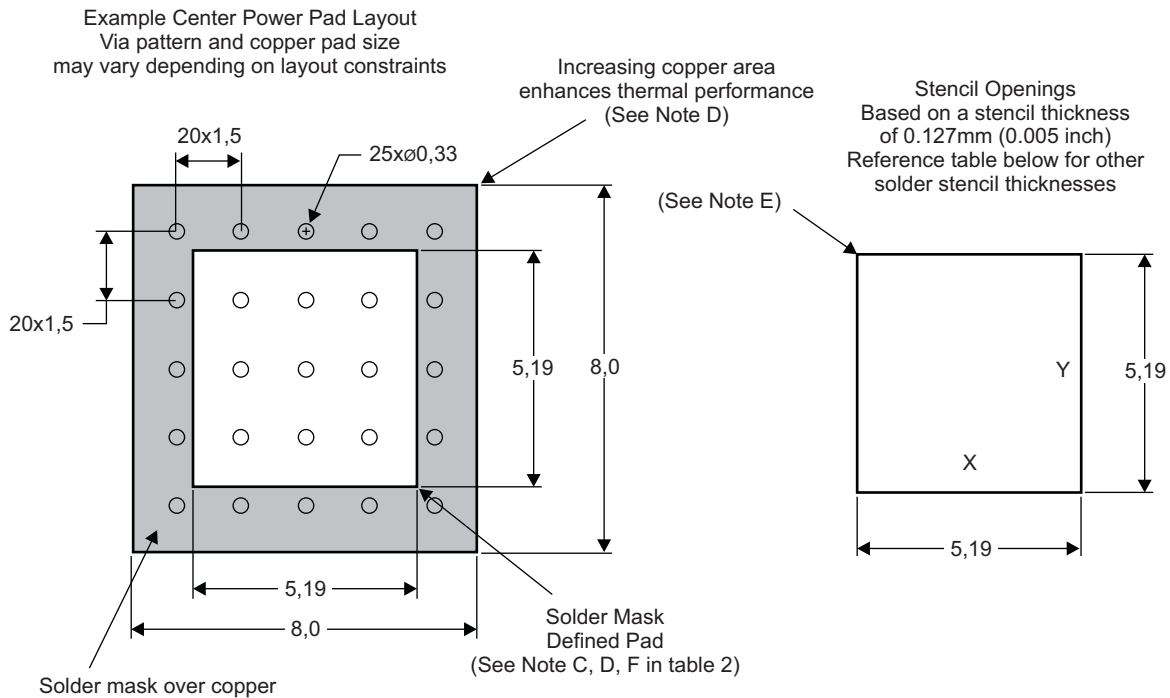
Note that the PowerPAD™ package land patterns are device specific with the exposed pad size shown in the product data sheet. This land is normally attached to the PCB for heat removal, but can be configured to take the heat to an external heat sink. This is preferred when airflow is available.

64-PAP PowerPAD(™) PACKAGE



64-Pin PAP Package
Bottom View

Figure 6. 64-Pin TQFP Package with PowerPAD™ Implemented, Bottom View



STENCIL THICKNESS (mm)	PLANE COORDINATE	
	X	X
0.1	5.55	5.55
0.127	5.19	5.19
0.152	4.90	4.90
0.178	4.60	4.60

Figure 7. PCB Thermal Land Design Considerations for Thermally-Enhanced TQFP Packages

Table 2. Center PowerPAD™ Solder Stencil Opening

STENCIL THICKNESS (mm)	PLANE COORDINATE	
	X	X
0.1	5.55	5.55
0.127	5.19	5.19
0.152	4.90	4.90
0.178	4.60	4.60

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defines pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPAD™ Thermally-Enhanced Package, Texas Instruments Literature Number [SLMA004](#), and also the product data sheets for specific thermal information via requirements and recommended board layout. These documents are available at <http://www.ti.com>. Publication IPC-7351 is recommended for alternative designs.
- E. Laser cutting apertures with trapezoidal walls and also rounded corners offer better past relief. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

- F. Contact the board fabrication site for recommended soldermask tolerances.
- G. Copper area under soldermask can be altered to accommodate via requirements for signal leads.

NOTE: The dimensions of the 64-pin PAP package shown in [Figure 6](#) and [Figure 7](#) are for reference only. Refer to the device-specific data sheet for exact package dimensions for your device.

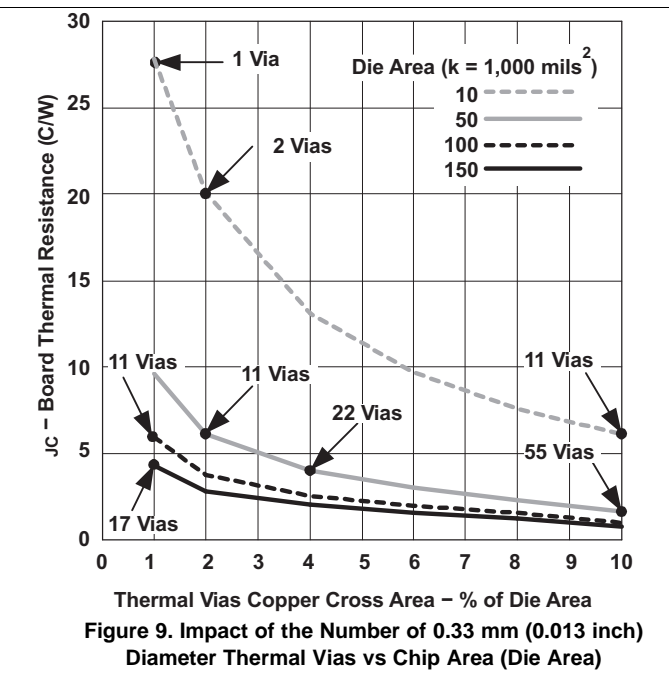
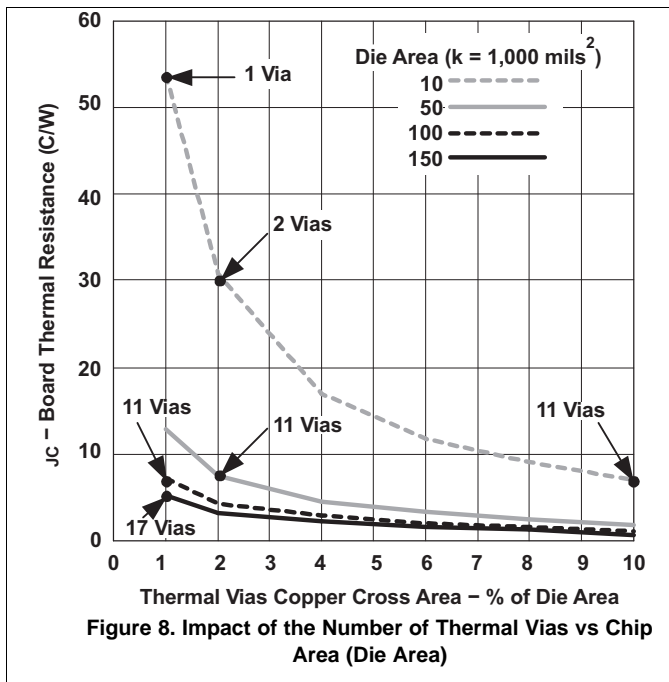
2.4 Thermal Vias

Thermal vias are the primary method of heat transfer from the PCB thermal land to the internal copper planes or to other heat removal sources. The number of vias used, the size of the vias and the construction of the vias are all important factors in both the PowerPAD™ package thermal performance and the package-to-PCB assembly. Recommendations and guidelines for thermal vias follow.

Shown in [Figure 8](#) and [Figure 9](#) are the effects on PCB thermal resistance of varying the number of thermal vias for various sizes of die for 2- and 4-layer PCBs. As can be seen from the curves, there is a point of diminishing returns where additional vias does not significantly improve the thermal transfer through the board. For a small die, having from five to nine vias should prove adequate for most applications. For larger die, a higher number may be used simply because there is more space available under the larger package. Shown in [Figure 10](#) are examples of ideal thermal land size and thermal via patterns for PowerPAD™ packages using 0.33 mm (13 mil) diameter vias plated with 1 oz. copper. This thermal via pattern set represents a copper cross section in the barrel of the thermal via of approximately 1% of the total thermal land area. Fewer vias may be used and still attain a reasonable thermal transfer into and through the PCB as shown in [Figure 8](#) and [Figure 9](#).

The number of thermal vias varies with each product being assembled to the PCB, depending on the amount of heat that must be moved away from the package, and the efficiency of the system heat removal method. Characterization of the heat removal efficiency versus the thermal via copper surface area should be performed to arrive at an optimum value for a given board construction. Then the number of vias required can be determined for any new design to achieve the desired thermal removal value.

The incorporation of thermal vias in the PCB is intended for efficient heat removal from the device package. The effectiveness of the thermal vias depends on soldering the exposed pad of the package to the PCB. Failure to solder the package to the PCB results in insufficient heat removal; and therefore, negatively impacts device performance and reliability.



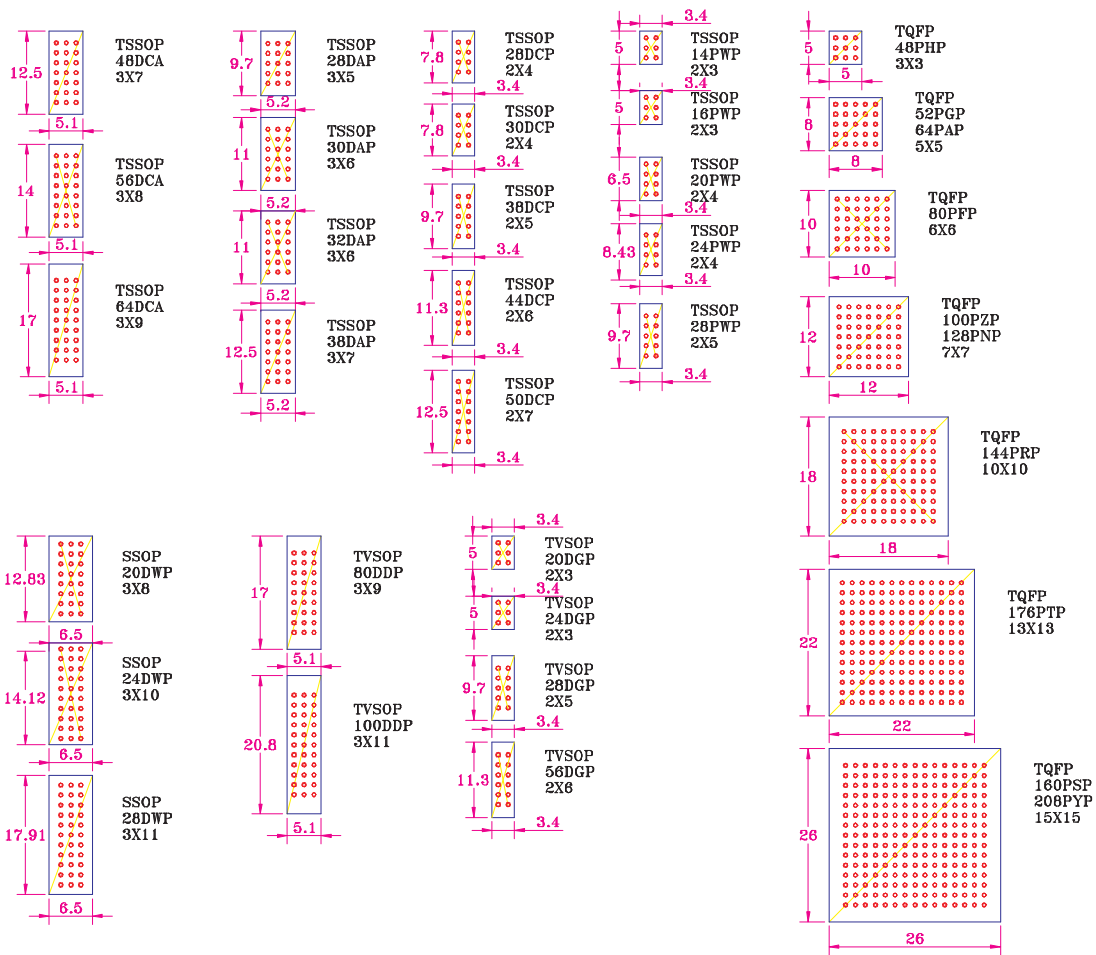


Figure 10. Example Thermal Land Size and Thermal Via Patterns for PowerPAD™ Layout

NOTE: Check the device-specific data sheet for exposed pad dimensions and for thermal via recommendations. The maximum exposed pad size listed in the data sheet should be used to design the solder mask defined pad. Solder mask defined pads are recommended to prevent shorting between exposed pad and package leads.

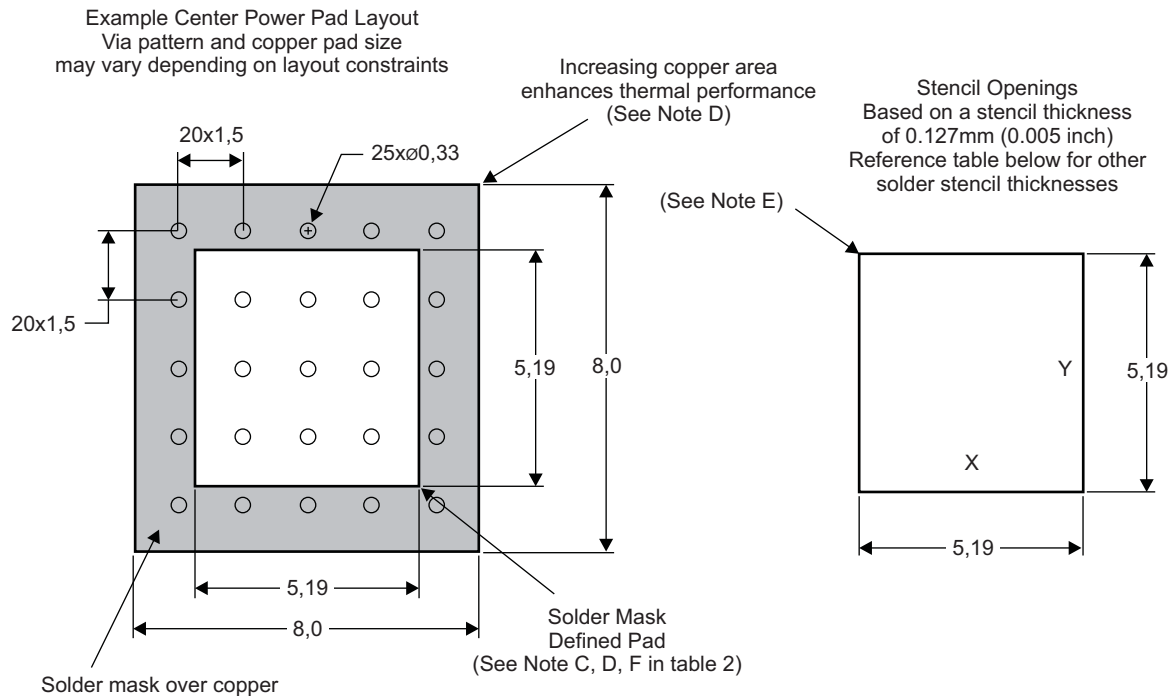
Thermal vias connect the thermal land to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole does not wick excessive solder volume from the solder deposited on the thermal pad. Minimizing the via hole size reduces the amount of solder wicking away from the interface between the package body and the thermal land on the surface of the board during solder reflow. The experiments conducted jointly with Solectron Texas indicate that a via drill diameter of 0.33 mm (13 mils) or smaller works well when 1 ounce copper is plated at the surface of the board and simultaneously plating the barrel of the via. As an alternative, if the thermal vias are not plugged when the copper plating is performed, then a solder mask material should be used to cap the vias on the component side with a dimension equal to the via diameter + 0.1 mm minimum. If vias are tented from the opposite side of the board instead of the preferred component side, an increase in the amount of voiding is seen in x-ray inspection due to flux out gassing and air entrapment post reflow. In addition, by tenting vias from the component side the solder is prevented from being wicked through the thermal via and potentially creating a solder void in the region between the package bottom and the thermal land on the surface of the PCB due to insufficient metal fill.

To assure the optimum thermal transfer through the thermal vias to internal planes or the reverse side of the PCB, the thermal vias used in the thermal land should not use web construction techniques also called a thermal relief via design which resembles a wagon wheel. Thermal relief construction on PCB vias is a standard technique used in most PCBs today to facilitate soldering, by constructing the via so that it has a high thermal resistance. This is not desirable for heat removal from the PowerPAD™ package. Therefore it is recommended that all vias used under the package make internal connections to the planes using a continuous connection completely around the hole diameter. Thermal relief construction for thermal vias is not recommended.

2.5 Solder Stencil Determination

The Joint Electronic Devices Engineering Council (JEDEC) specification for the standoff height of TSSOP and TQFP is in the range of 0.05 to 0.15mm (1.97 to 5.91mils), and is an acceptable range to successfully process PowerPad™ devices.

When a stencil thickness of 5 mils is designed, a 1:1 stencil aperture ratio to board pad must be used to maximize available paste to promote a complete solder joint to form. Thinner stencils may require growing the aperture size to increase the amount of the metal fill possible. Without adequate metal fill, an increase in the amount of voiding may result. In the example given in Figure 11, a solder paste with metal loading of 50% by volume was used. This is a typical land pattern and stencil design for the center thermal pad. Note that the exposed pad geometries may change between different devices. Therefore, consult the back of the datasheet for specific land pattern geometries because this document is intended to familiarize the reader to the standard format.



STENCIL THICKNESS (mm)	PLANE COORDINATE	
	X	X
0.1	5.55	5.55
0.127	5.19	5.19
0.152	4.90	4.90
0.178	4.60	4.60

Figure 11. Sample Land Pattern and Stencil Design for Thermally Enhanced TQFP Packages

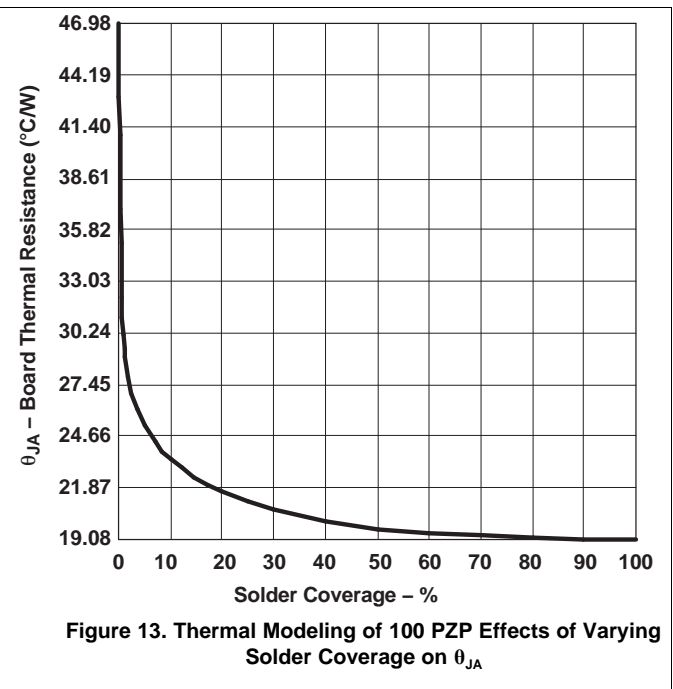
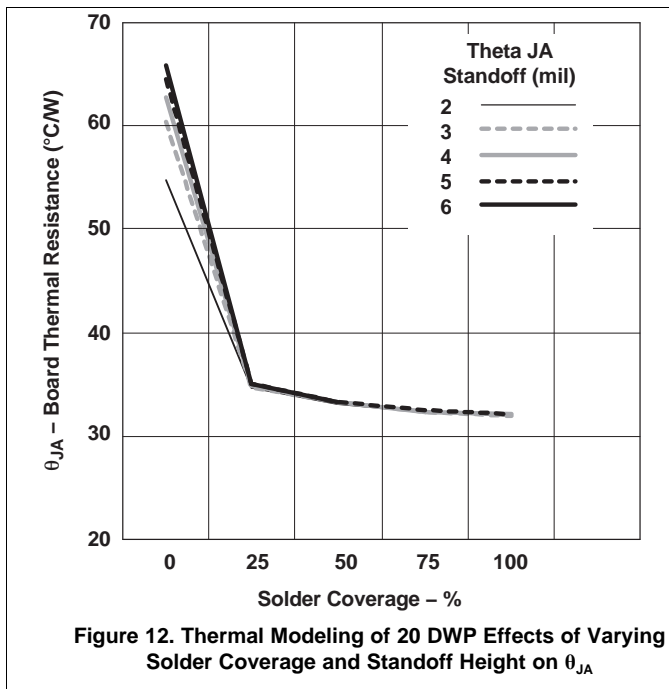
3 Assembly

3.1 Introduction

Solder joint inspection in the attachment area of the thermal pad of the thermally enhanced packages to the thermal land on the PCB is difficult to perform with the best option to date being x-ray inspection. Tests performed within Texas Instruments and during the joint PCB experiments with Solectron-Texas indicate that x-ray inspection allows detection of voiding within the solder joint and could be used either in a monitor mode, or for 100% inspection if required by the application.

Based on experimental and modeling data (Figure 12 and Figure 13), Texas Instruments recommends a minimum solder joint area of 50% of the package thermal pad area when the part is assembled on a PCB. The results of the PCB assembly study conducted with Solectron-Texas indicate that standard board assembly processes and materials normally achieves greater than 80% solder joint area without any attempt to optimize the process for thermally enhanced packages. A characterization of the solder joint achieved with a given process should be conducted to assure that the results obtained during testing apply directly to the customer application, and that the thermal efficiency in the customer application is similar to the thermal test board results for the power level of the packaged component. If the heat removal is not at the efficiency desired, then either additional thermal via structures needs to be added to the PCB construction, or additional thermal removal paths needs to be defined (such as direct contact with the system chassis).

Should a nonsolder attach method be used, the customer must validate the performance of the package by collecting empirical data for the device.



3.2 Solder Reflow Profile Suggestion

The reflow profile for board assembly using the Texas Instruments PowerPAD™ packages does not have to change from that used with conventional plastic packaged parts. The construction of the package does not add thermal mass, and the only new thermal load is due to the increased solder area between the package thermal pad and the thermal land on the PCB. A typical reflow oven profile for fine pitch surface mount packages is shown in Figure 14. Nitrogen purged, convection reflow is advantageous for this part to PCB assembly to minimize the possibility of solder ball formation under the package body.

Figure 14 represents JSTD-020 range of reflow profiles which are compatible with TI components. Peak temperatures can be located on the respective device's moisture sensitivity label. TI recommends following the solder paste supplier's recommendations to optimize flux activity and also to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20 and not exceeding the devices moisture sensitivity level. Figure 14 of this document illustrates a range of temperatures that our packages are capable of withstanding without risk to package reliability but TI prefers parts to be processed with the lowest peak temperature possible. The exact profile would depend on the solder paste manufacturer's recommendation, complexity of the PWB, and capability of the reflow equipment to be confirmed by the SMT assembly operation.

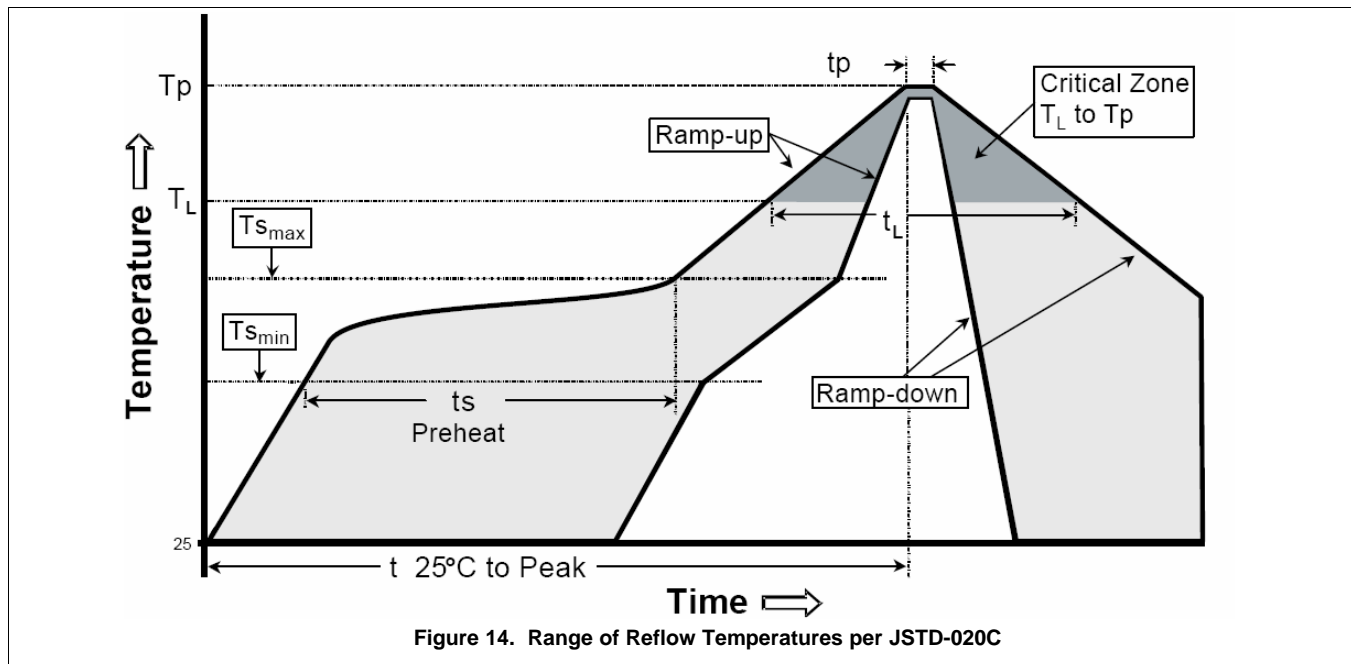
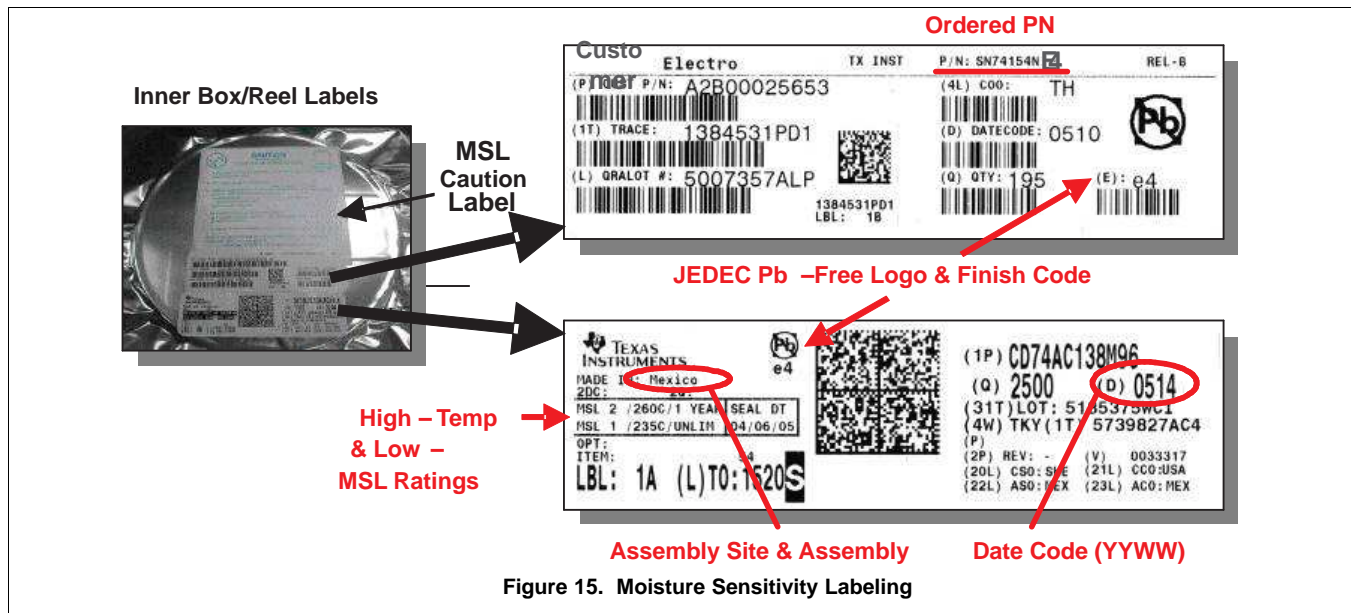


Figure 14. Range of Reflow Temperatures per JSTD-020C

Table 3. Classification Reflow Profiles⁽¹⁾

	Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
$T_{S(max)}$ to T_P	Maximum average ramp-up rate	3°C/second	3°C/second
PREHEAT			
$T_{S(min)}$	Minimum temperature	+100°C	+150°C
$T_{S(max)}$	Maximum temperature	+150°C	+200°C
$t_{s(min)}$ to $t_{s(max)}$	Preheat time	60 - 120 seconds	60 - 180 seconds
TIME MAINTAINED			
T_L	Temperature	+183°C	+217°C
t_L	Time	60 - 150 seconds	60 - 150 seconds
T_P	Peak/classification temperature		
	Maximum ramp-down rate	6°C/second	6°C/second
	Maximum time +25°C to peak temperature	6 minutes	8 minutes

⁽¹⁾ All temperatures refer to the topside of the package, measured on the package body surface.



3.3 Installation and Assembly Summary

The PowerPAD™ package families can be attached to printed-circuit boards using conventional solder reflow techniques that are standard in the industry today without changing the reflow process used for normal fine pitch surface mount package assembly. A minimum solder attachment area of 50% of the package thermal pad area is recommended to provide efficient heat removal from the semiconductor package, with the heat being carried into or through the PCB to the final thermal management system. This attachment can be achieved either by the use of solder for the joining material. Typical PCB thermal land pattern definitions have been provided that have been shown to work with 4 and 8 layer PCB test boards, and can be extended for use by other board structures.

4 Repair

4.1 Overview

Reworking thermally enhanced packaged semiconductors that have been attached to PCB assemblies through the use of solder can present significant challenges, depending on the point at which the re-work is to be accomplished. Tests of re-work procedures to date indicate that part removal from the PCB is successful with all of the conventional techniques used in the industry today. The challenge is part replacement on the board due to the combined thermal enhancement of the PCB itself, and the addition of thermal removal enhancement features to the semiconductor package. The traditional steps in the rework or repair process can be simply identified by the following steps for solder attached components:

1. Unsolder old component from the board
2. Remove any remaining solder from the part location
3. Clean the PCB assembly
4. Tin the lands on the PCB and leads, or apply solder paste to the lands on the PCB
5. Target, align, and place new component on the PCB
6. Reflow the new component on the PCB
7. Clean the PCB assembly

4.2 Part Removal From PCBs

Almost any removal process works to remove the device from the PCB, even with the thermal pad of the package soldered to the PCB. Heat is easily transferred to the area of the solder attachment either from the exposed surface thermal land of the PCB (single layer example), or through the thermal vias in the PCB (multi-layer example) from the backside of the PCB.

Re-work has been performed for both the TSSOP and TQFP PowerPAD™ style packages using METCAL removal irons and hot air. The specific example of a 20-pin TSSOP PowerPAD™ part removal is discussed in detail.

A 750-W METCAL removal iron was used in conjunction with hot air to verify the removal method efficiency to take 20-pin PowerPAD™ TSSOP packages off of assembly test boards. The hot air method is recommended as it subjects the PCB and surrounding components to less thermal and mechanical stress than other methods available, and has been proven to be much easier to control than some of the hot bar techniques. Use of the hot air method may require assemblers to acquire tools specifically for the smaller packages since most assemblers use a hot bar method for packages of this size. (Note: This same tool is also needed for part re-attachment to the PCB when the hot air method is employed). A tool with an integrated vacuum pick up tip is an advantage in the part removal process so the part can be physically removed from the board as soon as the solder reaches liquidus. Preheating of the local area of the PCB to a temperature of approximately 160 degrees centigrade can make the part removal easier. This is especially helpful in the case of larger packages such as 56-pin TSSOP or 100-pin TQFP style packages. This preheat is required in the thermal removal method if the semiconductor package is a heat slug package rather than the TI PowerPAD™ package version. Some experimentation is required to find the optimum procedure to use for any specific PCB construction and thermally enhanced package version.

After the part has been removed from the PCB, conventional techniques to clean the area of the part attachment - such as solder wicking - is needed to prepare the location for subsequent attachment of a new component.

4.3 Attachment of a Replacement Component to the PCB

Preparation of the PCB for attachment of a new component follows normal industry practice with respect to the lands on the board and the leads of the package. Both may be tinned, and/or solder paste applied to the lands for new component attachment. In addition, when solder is used to re-attach the thermal pad of the package to the thermal land on the PCB, solder paste needs to be applied to the surface of the thermal land on the board. This may be in the form of stripes of solder paste with sufficient volume to achieve the desired solder coverage, or a solder preform may be applied to the location for attachment. In a factory environment, the component is then placed in the desired location and alignment, and processed through a reflow oven to re-establish the desired solder joints. This is the most desirable process and is normally the easiest to accomplish.

When a manual or off-line attachment and reflow procedure is to be used, the challenge of supplying sufficient heat to the components and solder becomes a greater concern. In most cases, the corner leads of the package being attached is tack soldered to hold the component in alignment so the balance of the leads and the thermal pad to thermal land solder reflow can be accomplished without causing part movement from its desired location. As in the part removal case, it is advisable to pre-heat the board or the specific device location to a temperature below the melting point of the solder to minimize the amount of heat that must be provided by the reflow device as the part is being attached. A good starting point is to pre-heat to approximately 160°C. A hot gas reflow tool can then be used to complete the solder joint formation both at the leads and for the connection of the thermal pad to the thermal land of the PCB. Care must be taken at this operation to avoid blowing solder out from the thermal pad to thermal land interface and causing solder balling under the package or creating lead to lead or thermal land to lead shorts. The thermal enhancement of the package and the PCB requires a higher temperature gas or higher gas flow to reach solder liquidus than would be needed with an assembly lacking these enhancements. The tool should be specifically sized to the part being reworked to minimize possible damage to surrounding components or the PCB itself.

Note that Texas Instruments PowerPAD™ packages are easier to rework at the board level than other semiconductor packages utilizing metal slugs for the thermal path between the chip and the PCB. This is due to the additional requirement for heating the total mass of the slug to reflow temperatures versus heating the thermal pad of the PowerPAD™ package. The hot gas temperature and/or flow becomes critical for effective joining of the components without causing damage to the adjacent components or the PCB. In either case, the use of flux paste makes the rework task easier and more reliable to perform in a manual repair environment.

During solder joint repair and/or device replacement, Device MSL Floor life and maximum temperature exposures need to be considered.

5 Summary

An overview of the design, use and performance of the Texas Instruments PowerPAD™ package has been presented. The package is simple to use and can be assembled and repaired using existing assembly and manufacturing tools and techniques. Package performance is outstanding. By exposing the leadframe on the package bottom, extremely efficient thermal transfer between the die and the PCB can be achieved.

The simplicity of the PowerPAD™ package not only makes for a low cost package, but there is no additional cost in labor or material for the customer using standard surface mount assembly techniques. The only preparation needed to implement a PowerPAD™ design is at the PCB design stage. Simply by including a thermal land and thermal vias on the PCB the design can use the PowerPAD™ package effectively.

Definitions and Modeling

A.1 Thermal Resistance Definition

Thermal Resistance is defined as the temperature drop from the packaged chip to its primary heat sink per watt of power dissipated in the package. The primary heat sink may be the ambient air, the PWB itself, or a heat sink that is mounted on the package. Thermal resistance is denoted by the symbol θ_{Jx} (or Theta-Jx) where 'x' denotes the external reference point where the temperature is measured

- θ_{JA} is junction-to-ambient air thermal resistance
- θ_{JC} is junction-to-case thermal resistance
- θ_{JP} is junction-to-pad thermal resistance
- θ_{JB} is junction-to-board thermal resistance

Thermal Parameter is different from a thermal resistance in that the referenced external temperature is not the ultimate heat sink for the package. A thermal parameter can be used to estimate junction temperatures for a device in its end-use environment. A thermal parameter is denoted by the symbol ψ_{Jx} (or Psi-Jx) where 'x' denotes the referenced point where the temperature is measured. The thermal parameters are measured during the ψ_{JA} test only. Currently defined thermal parameters include the following:

- ψ_{JT} is the junction-to-package top center thermal parameter. A thermocouple is attached to the top center of the package in order to measure the surface temperature
- ψ_{JB} is the junction-to-board thermal parameter. A thermocouple is attached to a trace on the board at the middle of the long side of the package to measure the PWB temperature.

Common Uses

- θ_{JA} rough comparison
- θ_{JB} , θ_{JC} , θ_{JAP} system model
- ψ_{JB} , ψ_{JT} probing on board

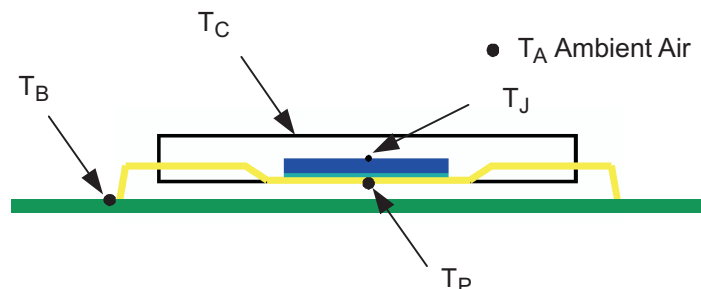


Figure 16. Thermal Resistance Diagram

where

- T_A is the ambient temperature
- T_J is the device junction temperature
- T_C is the case temperature
- T_B is the board temperature at lead
- T_P is the exposed pad temperature

A.2 General Information

Thermal modeling is used to estimate the performance and capability of device packages. From a thermal model, design changes can be made and thermally tested before any time is spent on manufacturing. It can also be determined what components have the most influence on the heat dissipation of a package. Models can give an approximation of the performance of a package under many different conditions. In this case, a thermal analysis was performed in order to approximate the improved performance of a PowerPAD™ thermally enhanced package to that of a standard package.

A.3 Modeling Considerations

Only a few differences exist between the thermal models of the standard packages and models for the PowerPAD™ package. The geometry of both packages was essentially the same, except for the location of the lead frame bond pad. The pad for the thermally enhanced PowerPAD™ package is deep downset, so its location is further away from the lead fingers than a standard package lead frame pad. Both models used the maximum pad and die size possible for the package, as well as using a lead frame that had a gap of one lead frame thickness between the pad and the lead fingers. The lead frame thickness was:

- TQFP/LQFP: 0.127 mm, or 5 mils
- TSSOP/TVSOP/SSOP: 0.147 mm, or 5.8 mils

In addition, the board design for the standard package is different from that of the PowerPAD™ package. One of the most influential components on the performance of a package is board design. In order to take advantage of the PowerPAD™ package's heat dissipating abilities, a board must be used that acts similarly to a heat sink and allows for the use of the exposed (and solderable) deep downset pad. This is Texas Instruments' recommended board for the PowerPAD™ device (see [Figure 17](#)). A summary of the board geometry is included below.

A.4 Texas Instruments Example Jedec Board Design for PowerPAD™ Packages

- 0.062" thick
- 3" x 3" (for packages <27 mm long)
- 4" x 4" (for packages >27 mm long)
- 2 oz. copper traces located on the top of the board (0.071 mm thick)
- Copper areas located on the top and bottom of the PCB for soldering
- Power and ground planes, 1 oz. copper (0.036 mm thick)
- Thermal vias, 0.3 mm diameter, 1.5 mm pitch
- Thermal isolation of power plane

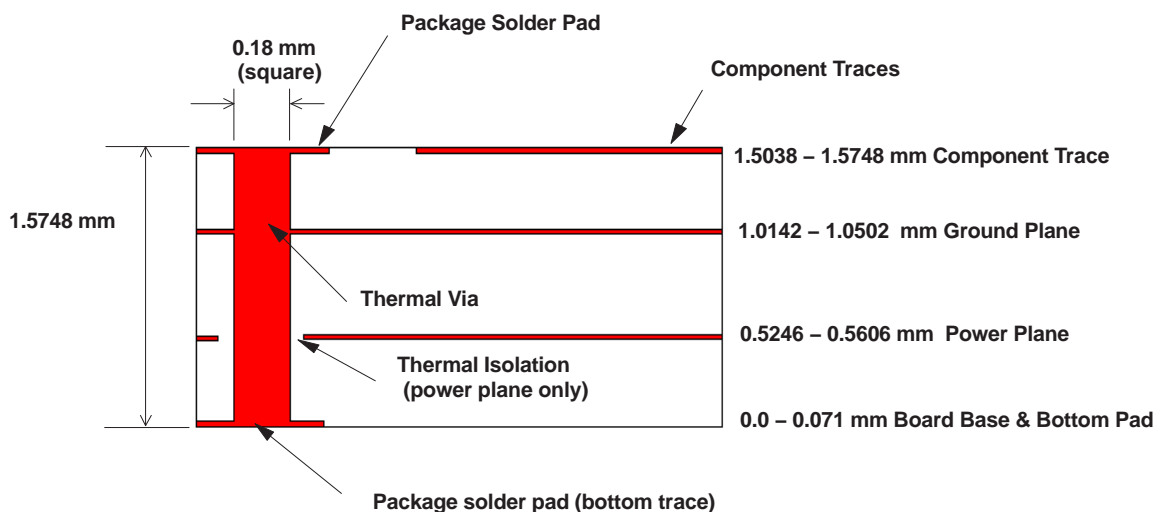


Figure 17. Texas Instruments Example Jedec Board Design (Side View)

The standard packages were placed on a board that is commonly used in the industry today, following the JEDEC standard. It does not contain any of the thermal features that are found on the Texas Instruments recommended board. It only has component traces on the top of the board. A summary of the standard is located below:

A.5 JEDEC Low Effective Thermal Conductivity Board (Low-K)

- 0.062" thick
- 3" x 3" (for packages <27 mm long)
- 4" x 4" (for packages >27 mm long)
- 1 oz. copper traces located on the top of the board (0.036 mm thick)

These boards were used to estimate the thermal resistance for both PowerPAD™ and the standard packages under many different conditions. The PowerPAD™ package was modeled on the JEDEC low-k board for comparison purposes only. It is recommended that it be used on the Texas Instruments heat dissipating board design. It allows for the exposed pad to be directly soldered to the board, which creates an extremely low thermal resistance path for the heat to escape.

A general modeling template was used for each PowerPAD™ package, with variables dependent on the package size and type. The package dimensions and an example of the template used to model the packages are shown in Figure 17 and Table 4. While only 1/4 of the package was modeled (in order to simplify the model and to lessen the calculation time), the dimensions shown are those for a full model.

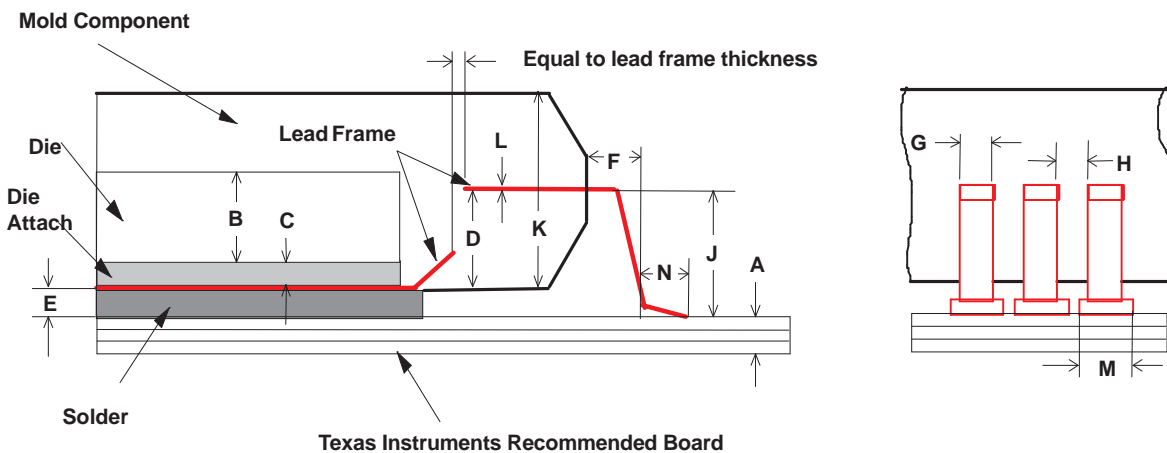


Figure 18. Thermal Pad and Lead Attachment to PCB Using the PowerPAD™ Package

Table 4. PowerPAD™ Package Template Description

Component Designator	Component Description	Size (mm)
A	PCB Thickness	1.5748
	PCB Length	76.2 ⁽¹⁾
	PCB Width	76.2 ⁽¹⁾
B	Chip Thickness	0.381
	Chip Length	⁽²⁾
	Chip Width	⁽²⁾
C	Die Attach Thickness	0.0127
D	Lead Frame Downset	⁽³⁾
	Tie Strap Width	⁽³⁾
E	PCB to Package Bottom	0.09
G	Shoulder Lead Width	⁽³⁾ ⁽⁴⁾ ⁽⁵⁾
H	Shoulder Lead Space	⁽³⁾ ⁽⁵⁾
J	Shoulder to PCB Dist.	⁽⁶⁾
K	Package Thickness	⁽³⁾
	Package Length	⁽³⁾
	Package Width	⁽³⁾
L	Pad Thickness	0.147 ⁽⁷⁾
	Pad Length	⁽³⁾
	Pad Width	⁽³⁾
	PCB Trace Length	25.4
	PCB Trace Thickness	0.071
	PCB Backplane Thickness	0.0 ⁽⁸⁾
	PCB Trace Width	0.254
M	Foot Width	⁽⁴⁾
N	Foot Length on PCB	⁽³⁾

⁽¹⁾ 99.6 mm for packages > 27 mm maximum length

⁽²⁾ Chip size is 10 mils smaller than the largest pad size (5 mils from each side)

⁽³⁾ Dependent on package size and type

⁽⁴⁾ Foot width was set equal to shoulder lead width for model efficiency

⁽⁵⁾ Lead pitch is equal to the shoulder lead width plus the shoulder lead space (pitch = G + H)

⁽⁶⁾ The shoulder to board distance is equal to the downset plus the board to package bottom distance (J = D + E)

⁽⁷⁾ The pad thickness for TQFP/LQFP is equal to 0.127 mm

⁽⁸⁾ The recommended board requires the addition of two internal copper planes, solder pads, and thermal vias

In addition to following a template for the dimensions of the package, a simplified lead frame was used. A description of the lead frame geometry is seen in Figure 19.

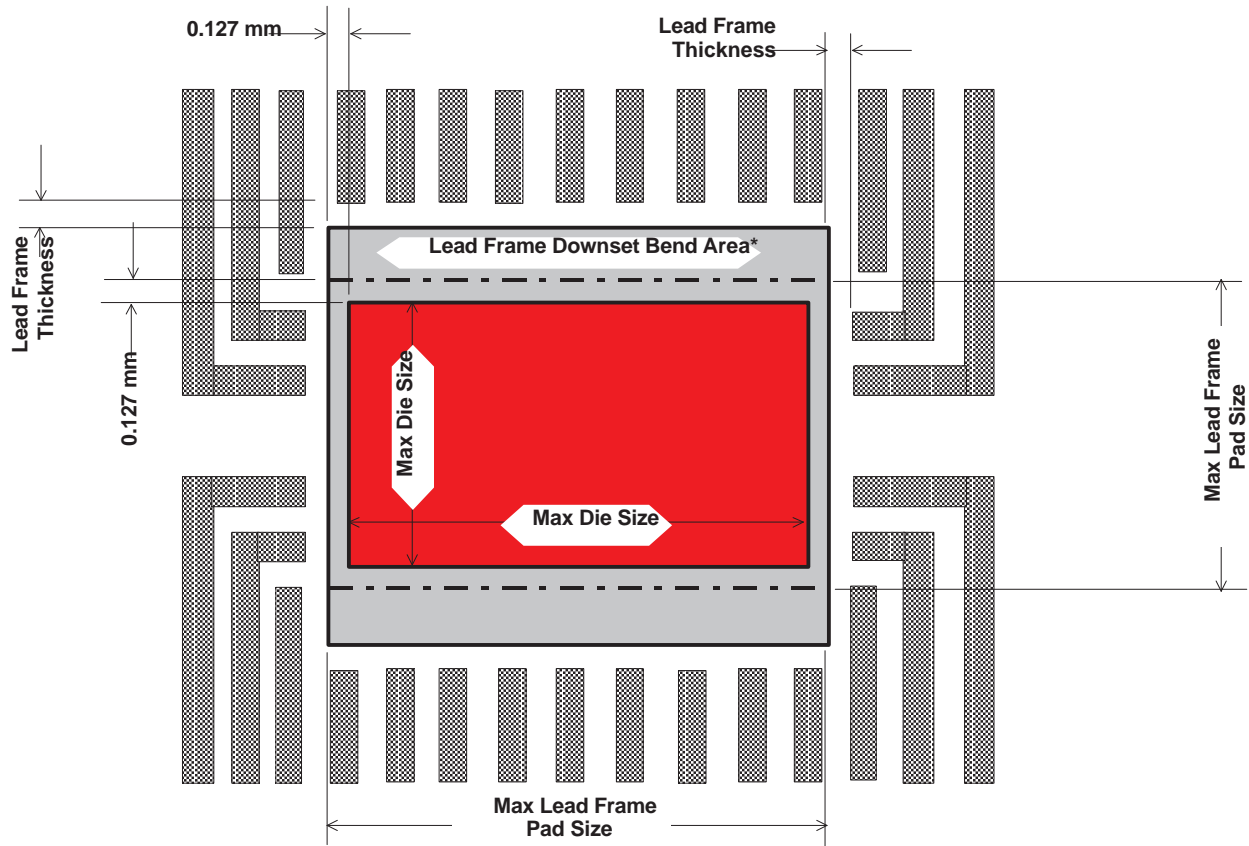


Figure 19. General Leadframe Drawing Configuration

NOTE: The leadframe downset bend area = 20 mils (leadframe thickness). For SSOP, TSSOP, and TVSOP packages, add the bend area to the width of the pad. For TQFP and LQFP, add the bend area to both the width and length of the pad.

A.6 Boundary Considerations

The junction-to-ambient (θ_{JA}), junction-to-pad (θ_{JP}), and junction-to-top of package (ψ_{JT}) thermal resistances were calculated using a Texas Instruments finite difference program. This program uses assumptions in order to simplify the calculation time, but is still accurate to within 10% of the actual measured number. Of course, the model conditions must be approximately the same as the test conditions for this to be true. Below is a summary of the analysis boundary conditions.

Junction-to-ambient (θ_{JA})

- Software calculated convection coefficients
- No radiation inputs
- +25°C ambient temperature

Junction-to-top of package (ψ_{JT})

- (Highest Device Temp. – Highest Package Surface Temp.)/Power
- Extracted graphically from θ_{JA} solution

Junction-to-pad (θ_{JP})

- For the PowerPAD™ package, the board was removed and the bottom of the pad set to a fixed temperature of +25°C. (See [Figure 20](#)).

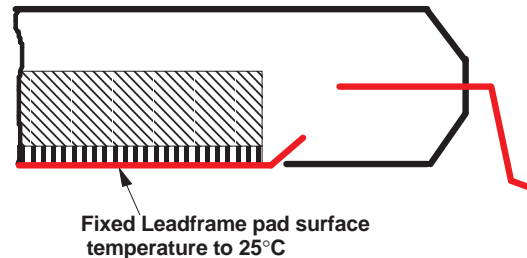


Figure 20. PowerPAD™ θ_{JP} Measurement

For the standard package, the board was removed and the top of the package was set to 25°C. (See [Figure 21](#)).

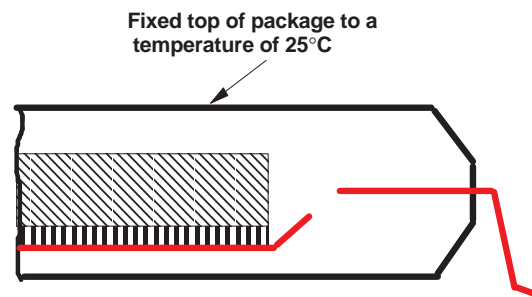


Figure 21. Standard Package θ_{JC} Measurement

A.7 Results

The purpose of the thermal modeling analysis was to estimate the increase in performance that could be achieved by using the PowerPAD™ package over a standard package. For this package comparison, several conditions were examined.

1. PowerPAD™ package soldered to the TI-recommended board.
2. A standard package configuration on a Low-K board
3. A standard package on the TI recommended board

The first two cases show a comparison of PowerPAD™ packages on the recommended board to standard packages on a board commonly used in the industry. From these results, it was shown that the PowerPAD™ package, as soldered to the TI recommended board, performed 73% cooler than a standard package on a low-k board.

For the final case, a separate analysis was performed in order to show the difference in thermal resistance when the standard and the thermally enhanced packages are used on the same board. The results showed that the PowerPAD™ package, as soldered, performed an average of 44% cooler than the standard package (See [Figure 22](#)).

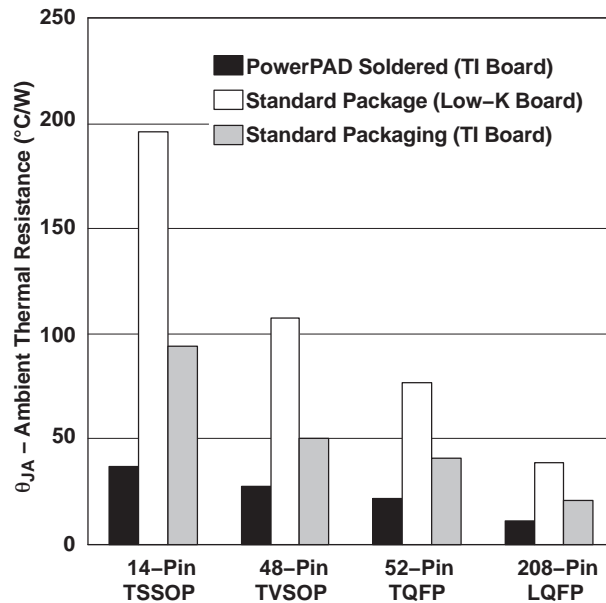


Figure 22. Comparison of θ_{JA} for Various Packages

A.8 Conclusions

The deep downset pad of a PowerPAD™ package allows for an extensive increase in package performance. Standard packages are limited by using only the leads to transport a majority of the heat away. The addition of a heat sink improves standard package performance, but greatly increases the cost of a package. The PowerPAD™ package improves performance, but maintains a low cost. The results of the thermal analysis showed that the PowerPAD™ package directly to a board designed to dissipate heat, thermal performance increased approximately 44% over the standard packages used on the same board.

Rework Process for Heat Sink TQFP and TSSOP PowerPAD™ Packages - from Air-Vac Engineering

B.1 Introduction

The addition of bottom side heat sink attachment has enhanced the thermal performance of standard surface mounted devices. This has presented new process requirements to effectively remove, redress, and replace (rework) these devices due to the hidden and massive heat sink, coplanarity issues, and balance of heat to the leads and heat sink. The following is based on rework of the TQFP100 and TSSOP20/24 pin devices.



Figure 23. DRS22C Reworking Station

B.2 Equipment

The equipment used was the Air-Vac Engineering DRS22C hot gas reflow module. The key requirements for the heat sink applications include: stable PCB platform with sufficient bottom side preheat, alignment capabilities, very accurate heat control, and proper nozzle design.

PCB support is critical to reduce assembly sagging and to provide a stable, flat condition throughout the process. The robust convection-based area heater provides sufficient and accurate bottom side heat to reduce thermal gradient, minimize local PCB warpage, and compensate for the heat sink thermal characteristics. The unique pop-up feature allows visible access to the PCB with multiple easy position board supports.



Figure 24. Reworking Nozzles of Various Sizes

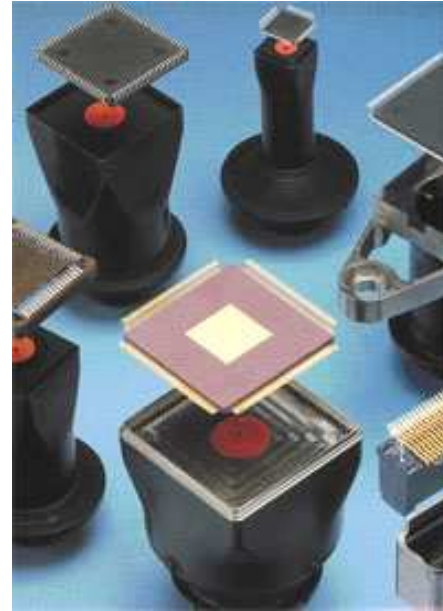


Figure 25. Reworking Nozzles of Various Sizes

During removal, alignment, and replacement, the device is held and positioned by a combination hot gas/hot bar nozzle. Built-in nozzle tooling positions the device correctly to the heat flow. A vacuum cup holds the component in place. Hot gas is applied to the top of the device while hot gas/hot bar heating is applied to the component leads. The hot bar feature also insures bonding of the fine pitch leads.

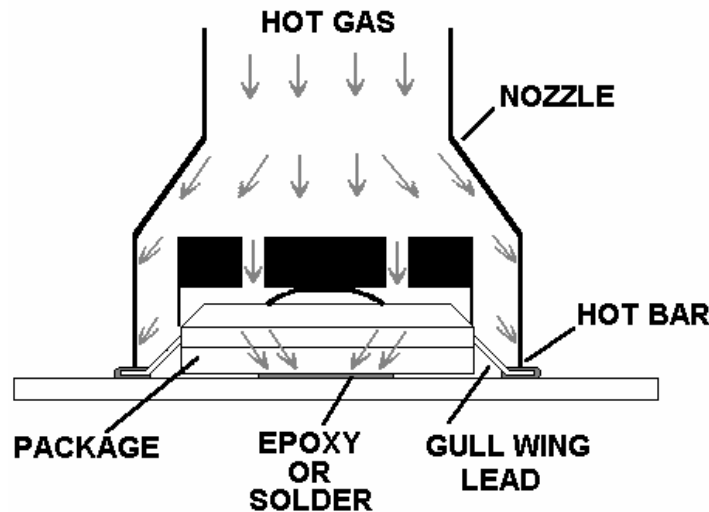


Figure 26. Nozzle Configuration

B.3 Profile

The gas temperature, flow, and operator step-by-step instructions are controlled by an established profile. This allows complete process repeatability and control with minimal operator involvement. Very accurate, low gas flow is required to insure proper temperature control of the package and to achieve good solder joint quality.

B.4 Removal

The assembly is preheated to 75°C. While the assembly continued to preheat to 100°C, the nozzle is preheated. After the preheat cycle, the nozzle is lowered and the device is heated until reflow occurs. Machine settings: TSSOP 20/24 - 220°C at 0.39 scfm gas flow for 50 seconds (preheat) above board level, 220°C at 0.39 scfm for 10 seconds. TQFP 100 - 240°C at 0.10 scfm for 60 seconds (preheat) above board level, 250°C at 0.65 scfm for 15 seconds. The built in vacuum automatically comes on at the end of the cycle and the nozzle is raised. The time to reach reflow was approximately 15 seconds. The component is released automatically allowing the part to fall into an appropriate holder.

B.5 Site Redress

After component removal the site must be cleaned of residual solder. This may be done by vacuum desoldering or wick. The site is cleaned with alcohol and lint-free swab. It is critical that the heat sink area be flat to allow proper placement on the leads on new device. Stenciling solder paste is the preferred method to apply new solder. Solder dispensing or reflowing the solder bumps on the pads for the leads may also be an alternative, but reflow (solid mass) of solder to the heat sink is not.



Figure 27. Air-Vac Vision System

B.6 Alignment

A replacement device is inserted into the gas nozzle and held by vacuum. The device is raised to allow the optical system to be used. The optical system used for alignment consists of a beam-splitting prism combined with an inspection quality stereo microscope or camera/video system. The leads of the device are superimposed over the corresponding land pattern on the board. This four sided viewing allows quick and accurate operator alignment.

B.7 Replacement

Once aligned, the x/y table is locked and the optical system retracts away from the work area. The preheat cycle is activated. The device is then lowered to the board. An automatic multi-step process provides a controlled reflow cycle with repeatable results. Machine settings for TSSOP 20/24: 160°C at 0.39 scfm gas flow for 40 seconds (preheat), 220°C at 0.39 scfm for 60 seconds above board level, 220°C at 0.39 scfm for 10 seconds. For TQFP 100: 100°C at 0.78 scfm for 40 seconds (preheat), 240°C at 0.10 scfm for 90 seconds above board level, 250°C at 0.65 scfm for 15 seconds (2 stages).

B.8 Conclusion

Rework of heat sink devices, TQFP and TSSOP, can be successful with attention to the additional issues they present. With respect to proper thermal profiling of the heat sink, die, and lead temperatures, the correct gas nozzle and profile can be developed to meet the requirements of the device and assembly. Existing equipment and nozzle design by Air-Vac can provide the tools and process knowledge to meet the heat sink TQFP and TSSOP rework application.

NOTE: This process was provided by one supplier. Texas Instruments encourages the user to work with other rework equipment suppliers to get their recommendations as well.

PowerPAD™ Process Rework Application Note from Metcal

C.1 Introduction

The following report references six of Texas Instruments' fine pitch, surface mount prototype packages (TSOP20, TSOP56, TSOP24, TQFP100, and TQFP64). The shapes and sizes are not new to the circuit board industry. Normally, you could use Metcal conduction tools to simply remove and replace these components. However, these packages are unique because all packages include a 'dye lead' on the underside of the package. This dye lead cannot be accessed by contact soldering. Therefore, convection rework methods are necessary for component placement.

NOTE: Conduction tools can be used for removal. But convection rework techniques are required for placement, and recommended for removal.

C.2 Removal

Conduction (optional): All packages can be removed with Metcal conduction tips. Use the following tips.

Table 5. Metcal Conduction Tips

Component	Metcal Tip Cartridge	OK Nozzle
TSOP20	SMTC-006	N-S16
TSOP56	SMTC-166	N-TSW32
TSOP24	SMTC-006	N-S16
TQFP100	SMTC-0118	N-P68
TQFP64	SMTC-112	N-P20

The dye lead, which is not in contact with the Metcal tip, easily reflows as heat passes through the package.

C.3 Conduction Procedure

1. Tin the tip, contact all perimeter leads simultaneously, and wait 3-5 seconds for the leads to reflow
2. Lift the package off the board (surface tension holds it in the tip cartridge). Dislodge the component from the tip by wiping the tip cartridge on a damp sponge.

C.4 Convection Procedure

1. Flux the leads. Preferably, use a liquid RMA/rosin flux. Pre-heat the board at 100°C. Use a convection or IR preheater, like the SMW-2201 from OK Industries. The settings 2-4 generally heats a heavy board to 100°C in 60 seconds.
2. Remove the component with the OK Industries FCR hot air system. Use a nozzle that matches the size and shape of the component (see above). With the preheat still on, heat the top of the board for 30-45 seconds on a setting of 3-4 (depending on board thickness and amount of copper in board).

Since convection is *necessary* for placement, convection is recommended for removal.

C.5 Placement Procedure

1. Pads can be tinned by putting solder paste on the pads and reflowing with hot air. Simply apply a fine bead of solder paste (pink nozzle, 24AWG) to the rows of pads. Be sure to apply very little paste. Excessive paste causes bridging, especially with fine pitch components.
2. Once the pads are tinned, apply gel flux (or liquid flux) to the pads. RMA flux is preferable. Be sure to apply gel flux to the dye pad as well. It is important that your pads not be OVER tinned. If too much solder has formed on the dye pad, the component sits above the perimeter leads, causing co-planarity problems. The gel flux is tacky and helps with manual placement. The joints require very little solder, so stenciling is not necessary. The pads are so thin that a minimal amount of solder is needed to form a good joint. Use a hot air nozzle for the FCR system. Pre-heat the board and (setting 3 to 5). Use low air flow (5 to 10 liters/minute) and topside heat (setting 3-4) for about 30 to 45 seconds.

NOTE: The quality of the dye lead's solder joint cannot be visually inspected. An X-ray machine, cross sectioning, or electrical testing is required. The vias on the test board are not solder masked very well which causes some bridging and solder wicking.

Specific board and component temperatures varies from board to board and from nozzle to nozzle. Larger nozzles require a higher setting because the heat must travel farther away from the heat source. There is a slight convection cooling effect from pushing hot air through long flutes, and depending on how wide the nozzle is. However, as a rule, keep the board temperature at 100°C (as thermocoupled from the TOP). You can regulate the board temperature by setting the temperature knob on the bottom side pre-heater. Apply a HIGHER topside heat from the FCR heating head. As a rule, use a maximum of 200°C to 210°C for a short peak period (10 seconds). Look for the flux to burn off. For board profiling purposes, you can visually inspect the condition of the solder joints during the removal process. Note the time allotted for reflow and set the system to Auto Remove or Auto Place at the same time designation for good repeatability. Be sure not to overheat the joints. Excessive heat can cause board delamination and discoloration. Alignment self-corrects once all the solder has reflowed. Tap board lightly. Remove any solder bridges with solder braid. Also, limit the board's heating cycles to a minimum. Excessive heat shock may warp the board or cause cracking in the solder joints.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from D Revision (October, 2008) to E Revision	Page
• Revised third paragraph of Section 4.3 ; changed <i>use of thermally conductive epoxy materials to flux paste</i>	16
• Added title to Appendix A.....	17

Changes from E Revision (July 2010) to F Revision	Page
• Changed section 2.5 with new text and added Figure 11	11

Changes from F Revision (August 2010) to G Revision	Page
• Changed Figure 11	11

Changes from G Revision (January 2011) to H Revision	Page
• Changed the Die Area From: (k) To: (k = 1,000 mils ²) in Figure 8 and Figure 9	8
• Changed section A.4 title From: <i>Texas Instruments Recommended Board for the PowerPAD™ Package</i> To: <i>Texas Instruments Example Jedec Board Design for PowerPAD™ Packages</i>	18
• Changed the first list item in section A.4 From: 0.622" thick To: 0.062" thick	18
• Changed the title of Figure 17 From: <i>Texas Instruments Recommended Board (Side View)</i> To: <i>Texas Instruments Example Jedec Board Design (Side View)</i>	18

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>), [evaluation modules](#), and [samples](http://www.ti.com/sc/docs/sampterm.htm) (<http://www.ti.com/sc/docs/sampterm.htm>).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated