Application Report
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PSE Controller Interface Control

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ABSTRACT

Texas Instruments provides POE solutions for both the powered devices (PDs) as well as power sourcing equipment (PSE). The TPS2384 is a 4-channel device for PSEs that manages and delivers power to PDs. Advanced functionality from this device is available when accompanied by a MSP430 microcontroller to manage and control functions such as power management, ac disconnect and legacy device detection. This document specifies the interface requirements for the MSP430 for use with the TPS2384 PSE.

Contents

1 Overview

The MSP430 is a microcontroller that supports manual mode operation of Texas Instruments' TPS2384 PSE. The MSP430 has available an application that supports manual mode operation on POE enabled systems with between 4 and 48 ports, using the TPS2384 PSE.

In order for the POE firmware in the MSP430 to function correctly, a system designer needs to ensure that several criteria are followed on the board design with the MSP430 and TPS2384 devices. These criteria include peripheral requirements, clock, power and ground, etc.

This interface control document specifies each of these to enable a POE enabled system using the MSP430 controller and TPS2384 PSEs.

1.1 System Architecture

The power management subsystem in an Ethernet Switch includes the MSP430 controller as well as between 1 and 12 TPS2384 PSEs, which can provide between 4 and 48 port POE-enabled Ethernet ports.

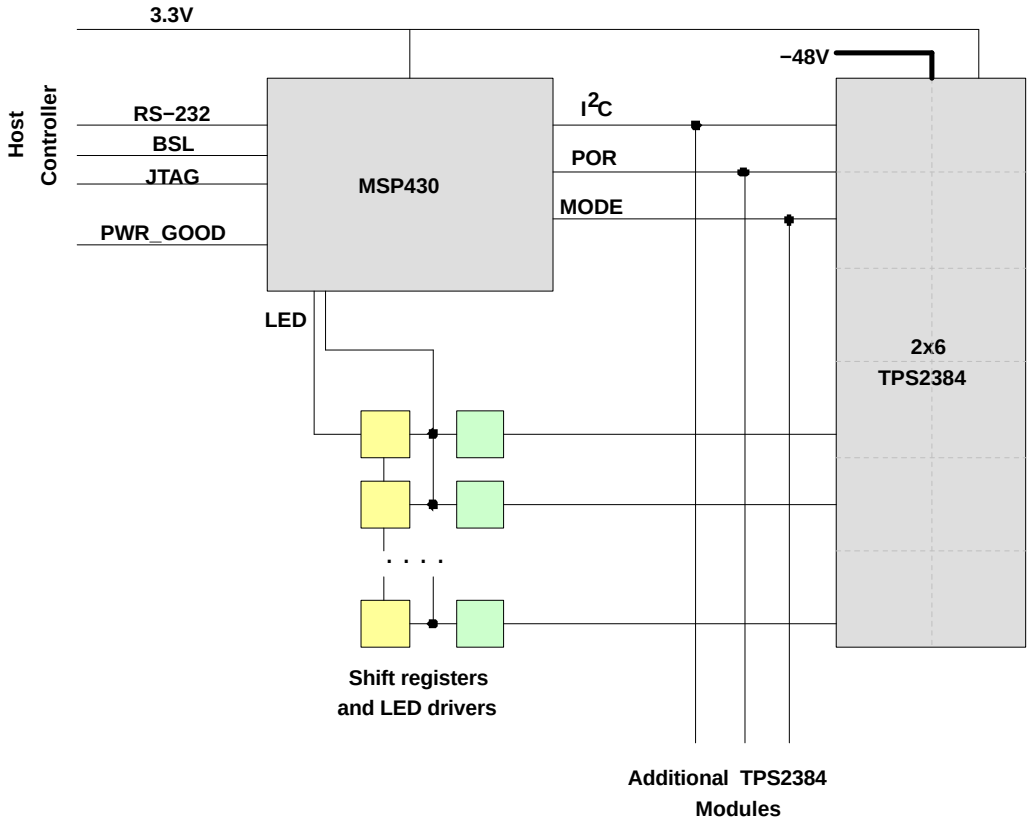

Figure 1. System Architecture Block Diagram

The MSP430 interfaces to a host controller (or PC running a test program or GUI) via a standard RS-232 interface, implemented using one of the UARTs in the MSP430. The MSP430 manages the TPS2384 devices by mastering a single I^2C interface. Many TPS2384 devices or modules containing TPS2384 devices should be put on the same I^2C bus, and each device should be given its own unique I^2C address on this bus. See the section in this document on device addressing for recommendations.

An MSP430 based system supports up to 2 LEDs per port, for up to 48 ports. The LEDs are managed through a separate set of signals using a clock, data and latch mechanism. The MSP430 also supports a debugging interface (JTAG) that can be used to download new code images to the controller, as well as for debugging using an integrated development environment (IDE). Since JTAG is not implemented in all systems in the field, there is also a dedicated interface for programming the MSP430 with new firmware images called the bootstrap loader (BSL). There are also signals used for power, ground and clock.

1.2 Controller Overview

The MSP430 controller is a 16-bit low-power mixed-signal microcontroller with flash memory. This program can be updated at any time over either JTAG or BSL. The specific controller that is used for this application is the MSP430F1481 from Texas Instruments.

For detailed information that isn't covered in this document about this controller such as packaging information, detailed operation, pinout and other device characteristics, see the MSP430F1481 data sheet, (TI literature number SLAS272F), on the Texas Instruments web site.

2 Controller Interface

The following section defines the interface to the MSP430 controller for this application. To successfully design a system which the MSP430 works, these guidelines should be followed to ensure that the device works in your system without changes. The MSP430 has a collection of interfaces to the device that range from peripherals, power and ground, mode selection and so on.

The interfaces that this controller specifies requirements around are:

- Host communications interface (RS-232)
- Host programming interface (BSL)
- PSE communications interface (I2C)
- Debugging interface (JTAG)
- LED interface
- Power monitoring interface
- Clock
- Power and ground
- Power-on reset
- Mode selection

These sections are detailed below in terms of their schematic and pin descriptions. See the section on Electrical Characteristics for information on all digital signals on the MSP430.

2.1 Host Communications Interface (RS-232)

The host communications interface is an asynchronous serial protocol with RS-232 signal levels. This interface is implemented on the MSP430 using a hardware UART with the settings of one start bit, one stop bit and no parity. This is typically the interface to a host processor's serial channel. This interface is used for both configuration and control communications, as well as upgrading the MSP430 firmware. In a prototype environment, this interface can be used with a DB-9 connector and level shifters to adapt to the signaling requirements of the MSP430.

The host communications interface is used for the host to manage the POE subsystem through configuration commands and status requests. The host can also receive status notifications through this interface from the MSP430 about the state of the Ethernet channels it is managing.

In order to ensure that this interface works properly, make sure to use the signals for the UART specified in the diagram below. The schematic details a design used to connect this interface to a serial channel on a host processor. The user's guide (TI Literature Number SLVU126) has added buffers for each of the signals, to accommodate for longer signal traces on the PCB.

2.1.1 Schematic

The following is the schematic for the Interface between the RS-232 on the MSP430 and system host.

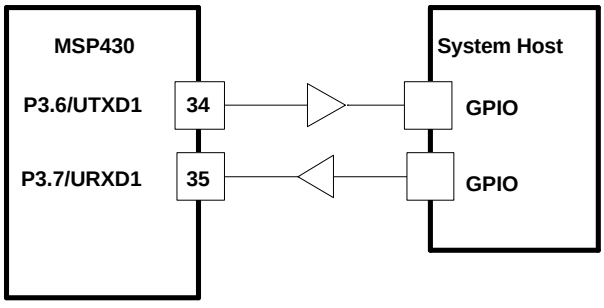

Figure 2. Host Communications Interface (RS-232) Schematic

2.1.2 Terminal Functions

The terminal functions for the RS-232 host communications interface are shown below.

Table 1. Host Communications Interface Terminal Functions

NAME	NUMBER	I/O	DESCRIPTION
P3.6/UTXD1	34	I/O	This is a general purpose digital I/O pin on the MSP430. Even though it can technically be used for input or output, the program on the MSP430 uses this pin strictly for output, to transmit data to the serial RS-232 interface.
P3.7/URXD1	35	I/O	This is a general purpose digital I/O pin on the MSP430. Even though it can technically be used for input or output, the program on the MSP430 uses this pin strictly for output, to receive data from the RS-232 serial interface for processing by the POE application.

2.2 Host Programming Interface (BSL)

The MSP430 has a feature that allows a new image to be loaded into flash memory through a hardware mechanism, without intervention of the CPU in the MSP430. This can be useful in the event that the flash image gets corrupted or some other soft failure in the device occurs. TI recommends that systems be designed with either the JTAG or BSL interfaces, so that updates can be performed in the field, in the event that the RS-232 host interface is not available.

The BSL is invoked and managed through 4 dedicated pins on the MSP430. The RST and TCK signals are used to invoke the BSL mechanism to have the host push a new firmware image to the MSP430. The URXD and UTXD signals are used to move the data to the device.

For complete details on the BSL function include application notes on how to design your board to support the BSL, see the MSP430F1481 data sheet (TI literature number SLAS272F) on the Texas Instrument's web site.

2.2.1 Terminal Functions

Table 2. BSL Interface Terminal Functions

NAME	NUMBER	I/O	DESCRIPTION
TCK	57	I	Test clock. TCK is the clock input port for device programming test and bootstrap loader start.
NMI/RST	58	I	Bootstrap loader start.
URXD/P1.1/TA0	13	I/O	This is a general purpose digital I/O pin on the MSP430. Even though it can technically be used for input or output, the program on the MSP430 uses this pin strictly for input, to receive data from the RS-232 serial interface for processing during the BSL function.
UTXD/P2.2/CAout/TA0	22	I/O	This is a general purpose digital I/O pin on the MSP430. Even though it can technically be used for input or output, the program on the MSP430 uses this pin strictly for output, to transmit data to the RS-232 serial interface for processing by system host during the BSL function.

2.3 PSE Communications Interface (I^2C)

The MSP430 communicates with all TPS2384 devices (either as a set of discrete devices, in modules or on DIMMs or SIPs) through a standard I^2C bus. The MSP430 masters a two-wire I^2C bus, but can work with 3-wire implementations on slave devices, by tying together the SDA-IN and SDA-OUT signals on the board.

All TPS2384 slave devices are expected to have unique I^2C addresses on this bus and address 0 cannot be used. This bus runs at between 360 kHz and 400 kHz, which is a function of the speed of execution of the firmware on the MSP430. All devices and modules should be on this same bus, by tying all the SCL and SDA signals together on the board.

See device addressing below for more requirements and recommendations how TPS2384 PSEs should be addressed in the system.

This interface is used for all communication with the TPS2384 PSEs in a system and provides memory mapped access to all registers within the TPS2384 PSEs. The only functions that are not available in the TPS2384 through this bus are LED control, power-on reset and TPS2384 mode selection.

2.3.1 Schematic

The following is the schematic for the PSE communications interface on the MSP430.

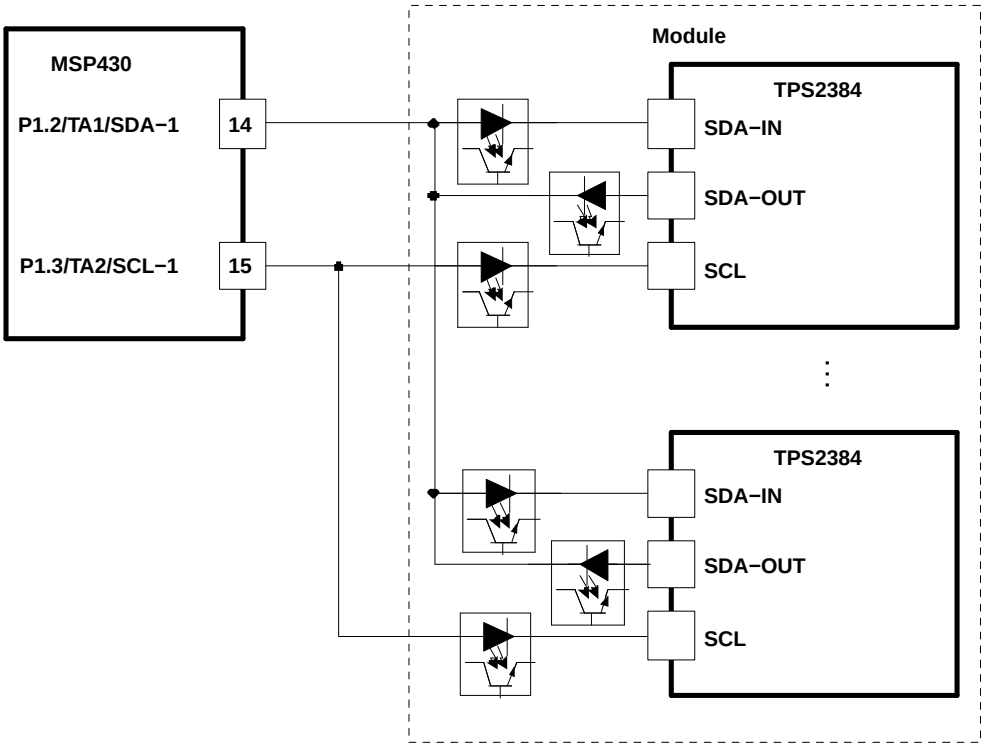

Figure 3. PSE Communications Interface (I^2C) Schematic

NOTE: Note that the I^2C bus requires opto-isolation between the MSP430 and TPS2384 devices for all three signals (SDA-IN, SDA-OUT and SCL). This isolation should be supplied in the module if possible. If a solution with discrete components is provided, then the isolation will have to be on the PCB.

2.3.2 Terminal Functions

Table 3. PSE Communications Terminal Functions

NAME	NUMBER	I/O	DESCRIPTION
SDA_IN_1/SDA_O_1/P1.2	14	I/O	This is a general purpose digital I/O pin on the MSP430. This signal is used for I^2C data (both input and output) and is mastered by the MSP430.
SCL/P1.3	15	I/O	This is a general purpose digital I/O pin on the MSP430. Even though it can technically be used for input or output, the program on the MSP430 uses this pin strictly for output, as the serial clock for the mastered I^2C interface to the PSE.

2.4 Debugging Interface (JTAG)

The MSP430 also supports a JTAG interface for code download and debugging. This is the only interface that can be used for debugging of a program on the MSP430. This is a proprietary JTAG interface and is required by the IDE for debugging of a program and can also be used to download new firmware images to flash memory on the MSP430.

JTAG is implemented with the TMS, TCK, TDI, TDO/TDI and RST/NMI signals in the MSP430.

2.4.1 Schematic

The following is the schematic for the JTAG interface on the MSP430. Note that the NMI/RST signal is pulled high since its active low state will reset the MSP430.

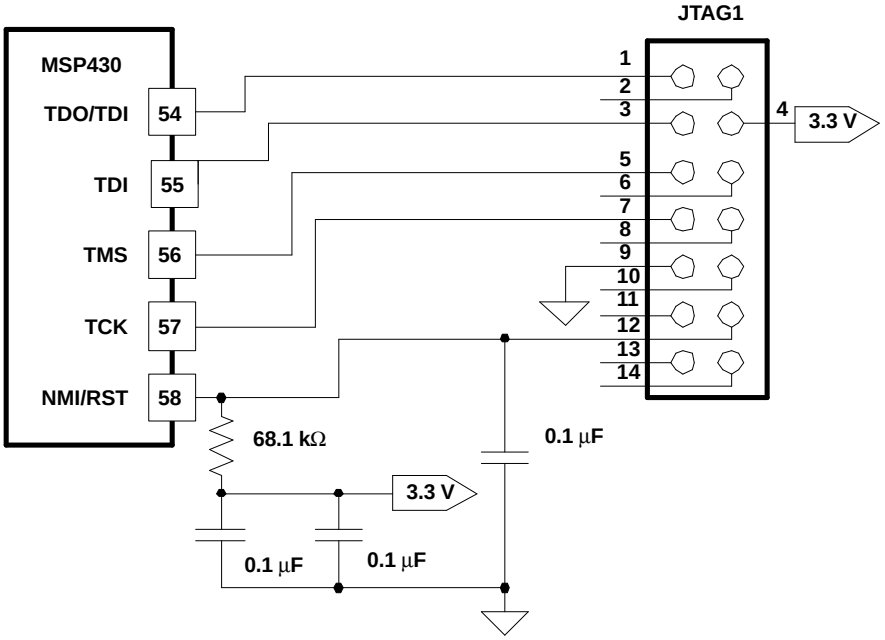

Figure 4. JTAG Interface Schematic

2.4.2 Terminal Functions

Table 4. JTAG Terminal Functions

NAME	NUMBER	I/O	DESCRIPTION
TDO/TDI	54	I/O	Test data output port. TDO/TDI data output or programming data input terminal.
TDI	55	I	Test data input. TDI used as a data input port. The device protection fuse is connected to TDI.
TMS	56	I	Test mode select. TMS is used as an input port for device programming and test.
TCK	57	I	Test clock. TCK is the clock input port for device programming test.
NMI/RST	58	I/O	Reset input, nonmaskable interrupt input port.

2.5 LED Interface

The program that runs on the MSP430 has the capability to control two LEDs per Ethernet port. The LEDs are used during program operation to indicate that power is being applied to the port or if some type of fault condition exists. For details on how the program on the MSP430 uses these two LEDs, see the TPS2384 software user's guide.

The LEDs are manipulated by the program in the MSP430 through a set of data, clock and latch signals. Data is fed through a set of shift registers for each of the ports that are daisy chained together. When all the data is shifted into the registers, the firmware running on the MSP430 will latch the data in parallel to a set of latches behind the shift registers. This enacts any changes to the LEDs all at once.

For Ethernet switches that do not wish for the power subsystem to control the LEDs on the board or module, the designer should not connect the clock, data and latch signals below and the LEDs can then be driven from the host or Ethernet PHYs on the PCB.

2.5.1 LED Ordering

The firmware program that runs on the MSP430 manages the LEDs according to an algorithm that assumes the shift registers are in sequential order, starting with the register and latch representing port 1.

The firmware shifts out a bit string with the most significant bits first, for up to 48 ports. As long as the system designer daisy-chains the shift registers and latches together as shown below, the same firmware can support any port configuration without changes.

Of course, if the system designer does not want to use the LEDs in this manner, then they can have the option of not connecting the DATA, CLK and LATCH signals.

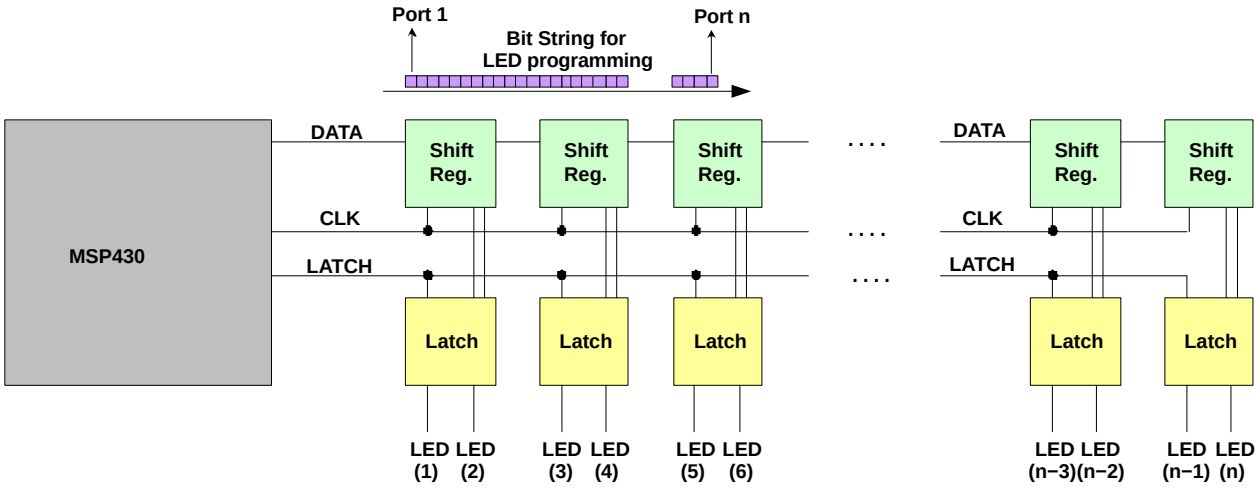

Figure 5. LED Shift Register and Latch Ordering

2.5.2 Schematic

The following schematic shows how a single Ethernet port's two LEDs are connected to MSP430 via a shift register and latch. Only 8 ports are shown. Additional ports can be supported by daisy chaining additional shift registers and latches.

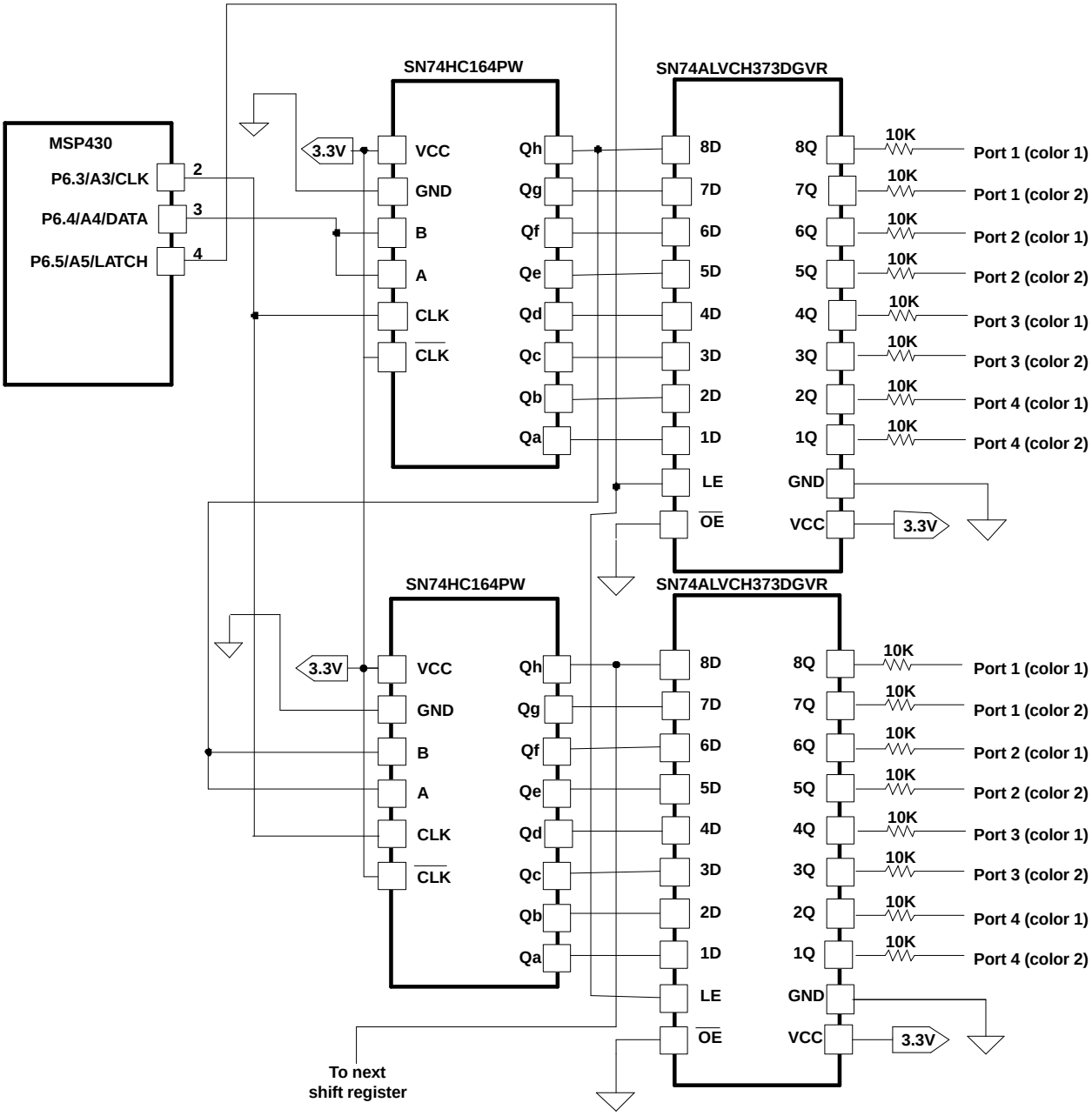

Figure 6. LED Interface Schematic

2.5.3 Terminal Functions

Table 5. LED Terminal Functions

NAME	NUMBER	I/O	DESCRIPTION
CLK/P6.3/A3	2	I/O	This is a general purpose digital I/O pin on the MSP430. Even though it can technically be used for input or output, the program on the MSP430 uses this pin strictly for output. The program uses this to clock out the data to the shift registers for LED control.
DATA/P6.4/A4	3	I/O	This is a general purpose digital I/O pin on the MSP430. Even though it can technically be used for input or output, the program on the MSP430 uses this pin strictly for output. The program on the MSP430 uses this signal to push out the data to the shift registers that represents the on/off state of each of the LEDs for all of the Ethernet channels.
LATCH/P6.5/A5	4	I/O	This is a general purpose digital I/O pin on the MSP430. Even though it can technically be used for input or output, the program on the MSP430 uses this pin strictly for output. The program on the MSP430 asserts this signal once all of the data has been clocked out to the shift registers to latch it to the LED drivers, to apply changes to the LEDs for each of the Ethernet channels.

2.6 Power Monitoring Interface

One of the powerful features of the MSP430 POE program is power management.

Power management is a sophisticated algorithm that allows efficient use of up to two power supplies for all the Ethernet channels. Power management also manages the POE subsystem in the event of a power supply going down, or coming online.

To perform this function, the MSP430 uses two input signals to represent the state of two power supplies in the system. These fault active signals are referred to as AC-PW-GOOD and DC-PW-GOOD, although they don't necessarily have to be an ac and dc supply.

These signals are checked in the POE program to manage any changes in power delivery during system operation.

2.6.1 Schematic

The following is the schematic for the two power good signals from the two power supplies. Note that these two signals are active high and pulled up to 3.3 V.

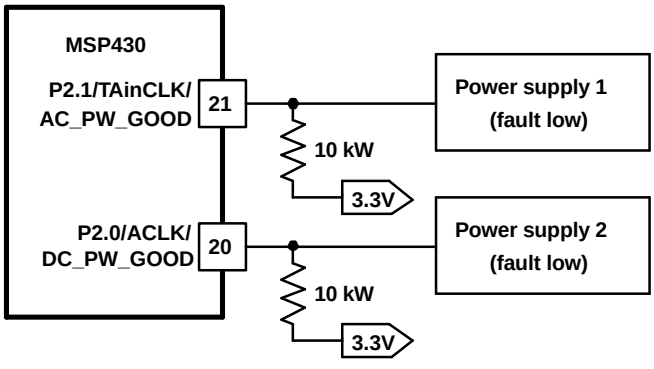

Figure 7. Power Supply Monitoring Schematic

2.6.2 Terminal Functions

The terminal functions for the power monitoring interface are shown below.

Table 6. Host Communications Interface Terminal Functions

NAME	NUMBER	I/O	DESCRIPTION
P2.1/TAinCLK/AC-PW-GOOD	21	I/O	This is a general purpose digital I/O pin on the MSP430. Even though it can technically be used for input or output, the program on the MSP430 uses this pin strictly for input, to indicate that power supply 1 is delivering power to the system.
P2.0/ACLK/DC-PW-GOOD	20	I/O	This is a general purpose digital I/O pin on the MSP430. Even though it can technically be used for input or output, the program on the MSP430 uses this pin strictly for input, to indicate that power supply 2 is delivering power to the system.

2.7 Clock Interface

The MSP430's clock can be driven with either an 8-MHz crystal or oscillator.

When using an 8-MHz crystal, two signals must be connected to the MSP430; an input and an output. Only standard crystals can be used. When using an 8MHz oscillator source, only the input needs to be connected to the MSP430.

An 8-MHz source (crystal or oscillator) is required for the program on the MSP430 to operate correctly and support applications up to 48 ports. Note that a bypass capacitor should be used if the device manufacturer requires.

2.7.1 Schematic

The following is the schematic for the clock input to the MSP430 implemented with a crystal.

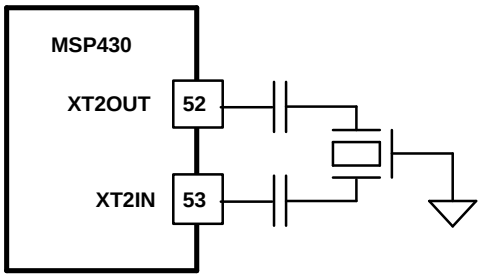

Figure 8. Clock Circuit Interface

2.7.2 Terminal Functions

Table 7. Clock Terminal Functions

NAME	NUMBER	I/O	DESCRIPTION
XT2OUT	52	O	Output terminal of crystal oscillator.
XT2IN	53	I	Input port for crystal oscillator XT2.

2.8 Power and Ground

The MSP430 has both analog and digital power and ground signals that must be tied together as shown below in the schematic. The MSP430 is a mixed-signal controller so it has both analog and digital power and ground signals.

2.8.1 Schematic

The following is the schematic for the power and ground signals on the MSP430. Note that the analog and digital grounds are tied directly together. The analog and digital VCC are also tied together with small coupling capacitors for noise filtering.

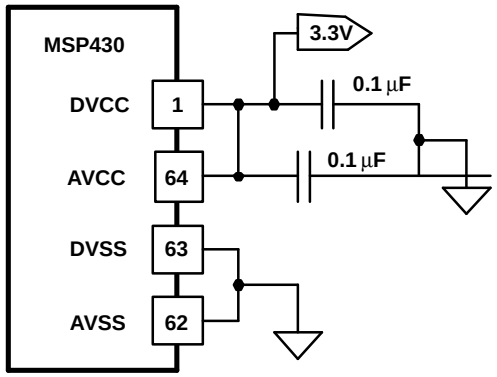

Figure 9. Power and Ground Schematic

2.8.2 Terminal Functions

The terminal functions for the power and ground signals are shown below.

Table 8. Clock Terminal Functions

NAME	NUMBER	I/O	DESCRIPTION
AVSS	62		Analog supply voltage, negative terminal.
DVSS	63		Digital supply voltage, negative terminal.
AVCC	64		Analog supply voltage, positive terminal.
DVCC	1		Digital supply voltage, positive terminal.

2.9 Power-On Reset

The power-on reset signal (POR) is an output from the MSP430 to the TPS2384 PSE. This signal asserts a hardware reset of the PSE in response to a command received from the host communications interface on the MSP430, or during system reset.

2.9.1 Schematic

The following is the schematic for the power-on reset circuit interface from the MSP430. Note that this signal requires opto-isolation between the MSP430 and the TPS2384. This signal is pulled high because PORB is active low from the MSP430.

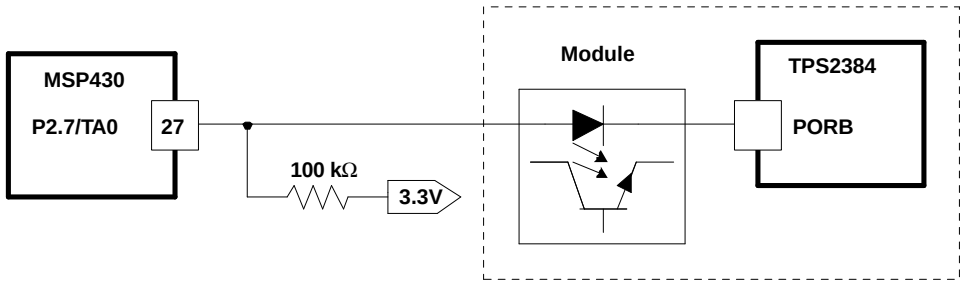

Figure 10. Power-On Reset Circuit Interface

2.9.2 Terminal Functions

The terminal function for the power-on reset pin is shown below.

Table 9. POR Terminal Functions

NAME	NUMBER	I/O	DESCRIPTION
P2.7/TA0/PORB	27	I/O	Asserts power-on reset signal to TPS2384 PSE(s). Even though this pin can be used for input as well as output, the program on the MSP430 only uses this pin to output this signal to the PSE.

2.10 Device Mode

The TPS2384 PSE supports two modes of operation: auto mode or manual mode.

Auto mode does not require intervention of a micro-controller. It supports basic IEEE 802.3af operation (detection, classification, power-up and dc disconnect) without the intervention of a micro-controller. Manual mode requires the MSP430 controller to operate the TPS2384 and allows additional functionality that auto mode does not support.

The device mode in the TPS2384 is set to auto mode by holding the mode select signal low when the device is released from reset. Manual mode is selected when the signal is held high when releasing the TPS2384 from reset. The MSP430 controller sets the TPS2384 device(s) to manual mode as a part of its normal program execution.

2.10.1 Schematic

The following is the schematic for the mode select circuit interface to the MSP430. Note that this signal requires opto-isolation between the MSP430 and the TPS2384. This signal is pulled up to 3.3 V, since the TPS2384 runs in manual mode when this signal is pulled high.

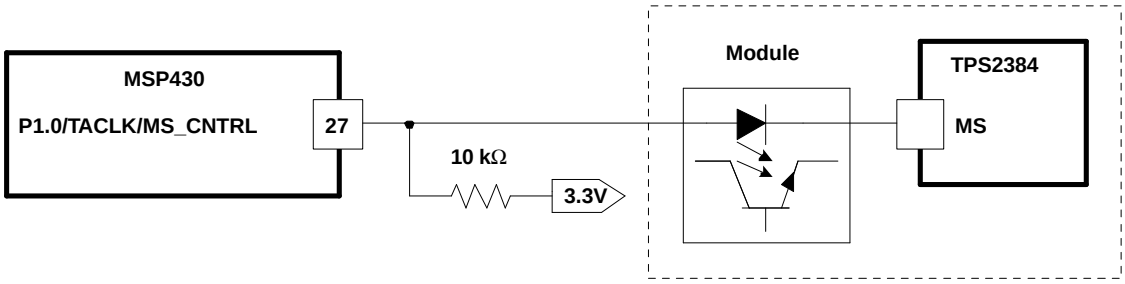

Figure 11. Mode Select Interface

2.10.2 Terminal Functions

Table 10. Mode Select Terminal Functions

NAME	NUMBER	I/O	DESCRIPTION
P1.0/TACLK/MS_CNTRL	12	I/O	This is a general purpose digital I/O pin on the MSP430. The program on the MSP430 uses this strictly as an output to the TPS2384 to select auto or manual mode when that device is released from reset.

3 Electrical Characteristics

The MSP430F1481 is a 16-bit, low-power mixed signal micro-controller from Texas Instruments. Unless otherwise stated, all electrical characteristics can be found in the MSP430F1481 data sheet (TI literature number SLAS272F) located on the Texas Instrumnets web site.

4 Device Addressing

Many TPS2384 devices can be supported by a single MSP430 controller. These devices can be discrete components, included in Ethernet modules or included in DIMMs or SIPs. All TPS2384 PSE devices must have a unique address on the I^2C bus and the address '0' cannot be used.

The firmware in the MSP430 provides a method for binding TPS2384 devices to I^2C addresses, but the following table is a recommended mapping that system designers are encouraged to follow, in order to lower the risk that a particular addressing strategy won't work.

In the table below, the I^2C address for a particular device is shown as a binary string with the format: A5-A4-A3-A2-A1 where A<n> represents the value of that address pin on the TPS2384 PSE. Note that in all cases, it is recommended that the A4 and A5 address pins be tied to either 3.3 V or ground on the board. This allows the board to be able to assign unique I^2C addresses for multiple modules on the same I^2C bus.

Table 11. TPS2384 I^2C Addressing Recommendations

Port Configuration	TPS2384 Device Address					
	DEVICE 0	DEVICE 1	DEVICE 2	DEVICE 3	DEVICE 4	DEVICE 5
2x4 module, 8 port DIMM, 2 x TPS2384	xx001	xx010	N/A	N/A	N/A	N/A
2x6 module, 12 port DIMM, 3 x TPS2384	xx001	xx010	xx011	N/A	N/A	N/A
2x8 module, 16 port DIMM, 4 x TPS2384	xx001	xx010	xx011	xx100	N/A	N/A
20 port DIMM, 5 x TPS2384	xx001	xx010	xx011	xx100	xx101	N/A
24 port DIMM, 6 x TPS2384	xx001	xx010	xx011	xx100	xx101	xx110

5 Reference Design Schematics

The complete reference design schematic for the TPS2384 is shown below.

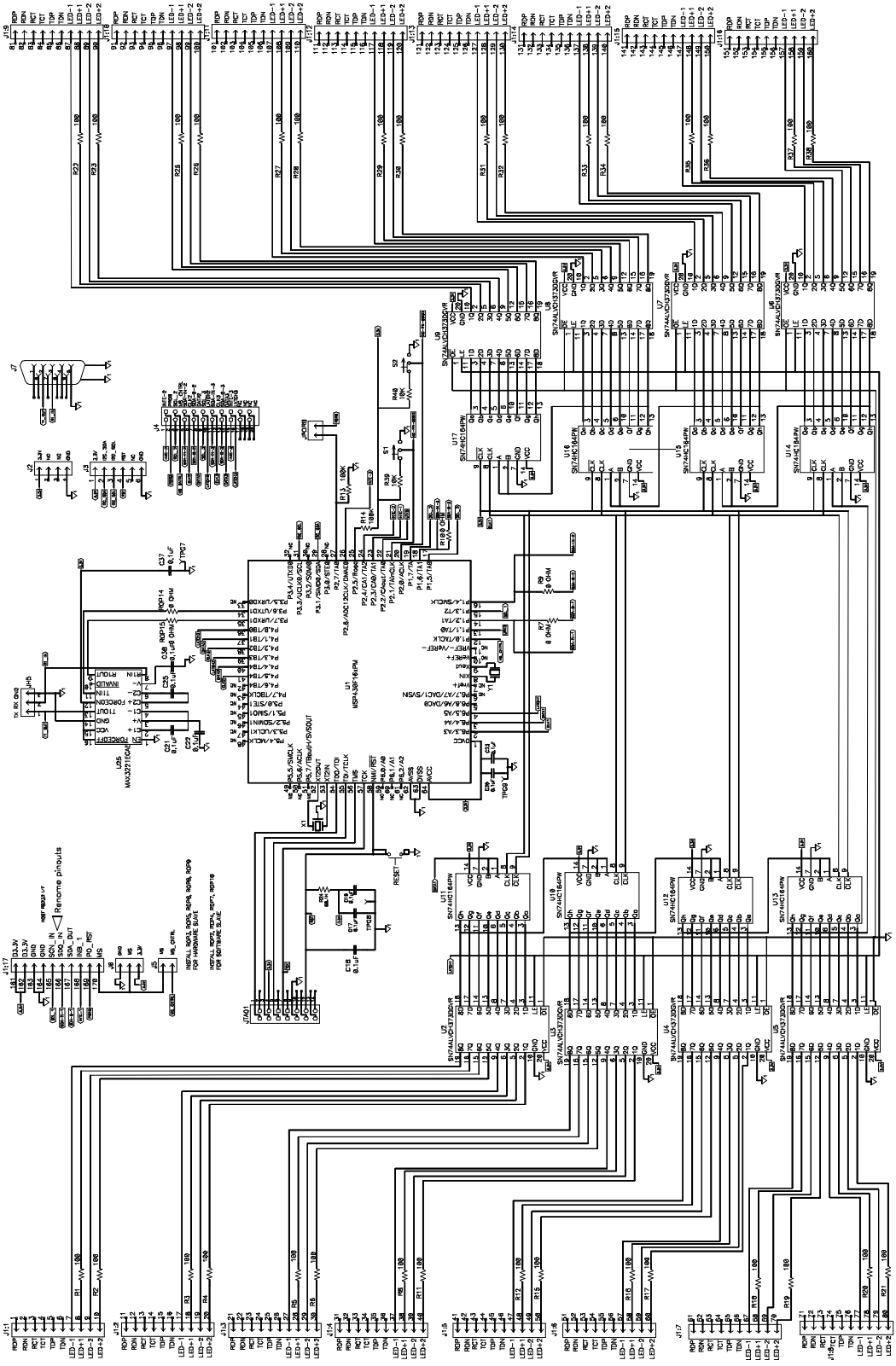

Figure 12. TPS2384 Reference Design Schematic

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