

Programmer's Guide

LMK3H2108A05 Configuration Guide



ABSTRACT

This document provides the configuration information for the LMK3H2108A05 device. For the default configuration of the LMK3H2108 device, refer to the [LMK3H2108 data sheet](#).

Table of Contents

1 Configuration Overview	1
1.1 LMK3H2108A05 Configuration Information.....	1
2 Revision History	6

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1 Configuration Overview

This section provides an overview of the critical device settings of the configurations.

1.1 LMK3H2108A05 Configuration Information

Table 1-1. LMK3H2108A05 Frequency Configuration

OTP Page	OUT0 (MHz)	OUT1 (MHz)	OUT2 (MHz)	OUT3 (MHz)	OUT4 (MHz)	OUT5 (MHz)	OUT6 (MHz)	OUT7 (MHz)
OTP Page 0	0	0	0	0	0	0	0	0
OTP Page 1	0	0	0	0	0	0	0	0
OTP Page 2	0	0	0	0	0	0	0	0
OTP Page 3	0	0	0	0	0	0	0	0

Table 1-2. LMK3H2108A05 I2C Configuration

OTP Page	I2C Configuration
OTP Page 0	I2C Address: 0x6c 1 Byte Register Addressing
OTP Page 1	I2C Address: 0x6c 1 Byte Register Addressing
OTP Page 2	I2C Address: 0x6c 1 Byte Register Addressing
OTP Page 3	I2C Address: 0x6c 1 Byte Register Addressing

OTP Page 0

Table 1-3. LMK3H2108A05 GPI Settings, OTP Page 0

GPI Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPI0	GPI	Inverted	Enabled	Disabled
GPI1	GPI	Inverted	Enabled	Disabled
GPI2	GPI	Inverted	Enabled	Disabled
GPI3	GPI	Inverted	Enabled	Disabled
GPI4	GPI	Inverted	Enabled	Disabled
GPI5	GPI	Inverted	Enabled	Disabled

Table 1-4. LMK3H2108A05 GPIO Settings, OTP Page 0

GPIO Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPIO0	GPI	Inverted	Enabled	Disabled
GPIO1	Dynamic OTP	Normal	Enabled	Disabled
GPIO2	Dynamic OTP	Normal	Enabled	Disabled
GPIO3	Global OE	Inverted	Enabled	Disabled
GPIO4	GPI	Inverted	Enabled	Disabled

Table 1-5. LMK3H2108A05 Input Settings, OTP Page 0

Input	Powered Up/Down	Input Format	Input Termination
IN_0	Powered Up	Differential IN0	None, DC
IN_1	Powered Down	Differential IN1	None, DC
IN_2	Powered Down	Differential IN2	None, DC

Table 1-6. LMK3H2108A05 Output Settings, OTP Page 0

Output	Frequency (MHz)	Format	Clock Source	Output State	OE Group	SSC Behavior
OUT0	0	85 Ω LP-HCSL	IN_0	Enabled	Global OE Only	Disabled
OUT1	0	85 Ω LP-HCSL	IN_0	Enabled	Global OE Only	Disabled
OUT2	0	85 Ω LP-HCSL	IN_0	Enabled	Global OE Only	Disabled
OUT3	0	85 Ω LP-HCSL	IN_0	Enabled	Global OE Only	Disabled
OUT4	0	85 Ω LP-HCSL	IN_0	Enabled	Global OE Only	Disabled
OUT5	0	85 Ω LP-HCSL	IN_0	Disabled	Global OE Only	Disabled
OUT6	0	85 Ω LP-HCSL	IN_0	Disabled	Global OE Only	Disabled
OUT7	0	85 Ω LP-HCSL	IN_0	Disabled	Global OE Only	Disabled

OTP Page 1

Table 1-7. LMK3H2108A05 GPI Settings, OTP Page 1

GPI Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPI0	GPI	Inverted	Enabled	Disabled
GPI1	GPI	Inverted	Enabled	Disabled
GPI2	GPI	Inverted	Enabled	Disabled
GPI3	GPI	Inverted	Enabled	Disabled
GPI4	GPI	Inverted	Enabled	Disabled
GPI5	GPI	Inverted	Enabled	Disabled

Table 1-8. LMK3H2108A05 GPIO Settings, OTP Page 1

GPIO Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPIO0	GPI	Inverted	Enabled	Disabled
GPIO1	Dynamic OTP	Normal	Enabled	Disabled
GPIO2	Dynamic OTP	Normal	Enabled	Disabled
GPIO3	Global OE	Inverted	Enabled	Disabled
GPIO4	GPI	Inverted	Enabled	Disabled

Table 1-9. LMK3H2108A05 Input Settings, OTP Page 1

Input	Powered Up/Down	Input Format	Input Termination
IN_0	Powered Up	Differential IN0	None, DC
IN_1	Powered Down	Differential IN1	None, DC
IN_2	Powered Down	Differential IN2	None, DC

Table 1-10. LMK3H2108A05 Output Settings, OTP Page 1

Output	Frequency (MHz)	Format	Clock Source	Output State	OE Group	SSC Behavior
OUT0	0	85 Ω LP-HCSL	IN_0	Enabled	Global OE Only	Disabled
OUT1	0	85 Ω LP-HCSL	IN_0	Enabled	Global OE Only	Disabled
OUT2	0	85 Ω LP-HCSL	IN_0	Enabled	Global OE Only	Disabled
OUT3	0	85 Ω LP-HCSL	IN_0	Enabled	Global OE Only	Disabled
OUT4	0	85 Ω LP-HCSL	IN_0	Enabled	Global OE Only	Disabled
OUT5	0	85 Ω LP-HCSL	IN_0	Disabled	Global OE Only	Disabled
OUT6	0	85 Ω LP-HCSL	IN_0	Disabled	Global OE Only	Disabled
OUT7	0	85 Ω LP-HCSL	IN_0	Disabled	Global OE Only	Disabled

OTP Page 2

Table 1-11. LMK3H2108A05 GPI Settings, OTP Page 2

GPI Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPI0	GPI	Inverted	Enabled	Disabled
GPI1	GPI	Inverted	Enabled	Disabled
GPI2	GPI	Inverted	Enabled	Disabled
GPI3	GPI	Inverted	Enabled	Disabled
GPI4	GPI	Inverted	Enabled	Disabled
GPI5	GPI	Inverted	Enabled	Disabled

Table 1-12. LMK3H2108A05 GPIO Settings, OTP Page 2

GPIO Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPIO0	GPI	Inverted	Enabled	Disabled
GPIO1	Dynamic OTP	Normal	Enabled	Disabled
GPIO2	Dynamic OTP	Normal	Enabled	Disabled
GPIO3	Global OE	Inverted	Enabled	Disabled
GPIO4	GPI	Inverted	Enabled	Disabled

Table 1-13. LMK3H2108A05 Input Settings, OTP Page 2

Input	Powered Up/Down	Input Format	Input Termination
IN_0	Powered Down	Differential IN0	None, DC
IN_1	Powered Down	Differential IN1	None, DC
IN_2	Powered Up	Differential IN2	None, DC

Table 1-14. LMK3H2108A05 Output Settings, OTP Page 2

Output	Frequency (MHz)	Format	Clock Source	Output State	OE Group	SSC Behavior
OUT0	0	85 Ω LP-HCSL	IN_2	Enabled	Global OE Only	Disabled
OUT1	0	85 Ω LP-HCSL	IN_2	Enabled	Global OE Only	Disabled
OUT2	0	85 Ω LP-HCSL	IN_2	Enabled	Global OE Only	Disabled
OUT3	0	85 Ω LP-HCSL	IN_2	Enabled	Global OE Only	Disabled
OUT4	0	85 Ω LP-HCSL	IN_2	Enabled	Global OE Only	Disabled
OUT5	0	85 Ω LP-HCSL	IN_2	Disabled	Global OE Only	Disabled
OUT6	0	85 Ω LP-HCSL	IN_2	Disabled	Global OE Only	Disabled
OUT7	0	85 Ω LP-HCSL	IN_2	Disabled	Global OE Only	Disabled

OTP Page 3

Table 1-15. LMK3H2108A05 GPI Settings, OTP Page 3

GPI Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPI0	GPI	Inverted	Enabled	Disabled
GPI1	GPI	Inverted	Enabled	Disabled
GPI2	GPI	Inverted	Enabled	Disabled
GPI3	GPI	Inverted	Enabled	Disabled
GPI4	GPI	Inverted	Enabled	Disabled
GPI5	GPI	Inverted	Enabled	Disabled

Table 1-16. LMK3H2108A05 GPIO Settings, OTP Page 3

GPIO Pin	Pin Behavior	Polarity	Internal Pull-Down	Internal Pull-Up
GPIO0	GPI	Inverted	Enabled	Disabled
GPIO1	Dynamic OTP	Normal	Enabled	Disabled
GPIO2	Dynamic OTP	Normal	Enabled	Disabled
GPIO3	Global OE	Inverted	Enabled	Disabled
GPIO4	GPI	Inverted	Enabled	Disabled

Table 1-17. LMK3H2108A05 Input Settings, OTP Page 3

Input	Powered Up/Down	Input Format	Input Termination
IN_0	Powered Down	Differential IN0	None, DC
IN_1	Powered Down	Differential IN1	None, DC
IN_2	Powered Up	Differential IN2	None, DC

Table 1-18. LMK3H2108A05 Output Settings, OTP Page 3

Output	Frequency (MHz)	Format	Clock Source	Output State	OE Group	SSC Behavior
OUT0	0	85 Ω LP-HCSL	IN_2	Enabled	Global OE Only	Disabled
OUT1	0	85 Ω LP-HCSL	IN_2	Enabled	Global OE Only	Disabled
OUT2	0	85 Ω LP-HCSL	IN_2	Enabled	Global OE Only	Disabled
OUT3	0	85 Ω LP-HCSL	IN_2	Enabled	Global OE Only	Disabled
OUT4	0	85 Ω LP-HCSL	IN_2	Enabled	Global OE Only	Disabled
OUT5	0	85 Ω LP-HCSL	IN_2	Disabled	Global OE Only	Disabled
OUT6	0	85 Ω LP-HCSL	IN_2	Disabled	Global OE Only	Disabled
OUT7	0	85 Ω LP-HCSL	IN_2	Disabled	Global OE Only	Disabled

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2025	*	Initial Release

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