User's Guide

LMK3H2108 Configuration Summary

ABSTRACT

This document provides high-level information on the configurations available for the LMK3H2108 devices. For a detailed breakdown of the settings on each OTP page, refer to the configuration guide document for the desired OPN. For the full register settings, refer to the register map document for the desired OPN.

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Trademarks

1 Introduction

This configuration summary helps designers understand each configuration offered for the LMK3H2108 devices at a high level. Each LMK3H2108Axx and LMK3H2108Txx part number is a different configuration, with potentially different frequencies and output formats. Use this guide to determine if one of the released configurations meets application requirements.

2 LMK3H2108 Configuration Summary

2.1 LMK3H2108A01

LMK3H2108A01 Configuration Guide

LMK3H2108A01 Register Map

Table 2-1. LMK3H2108A01 Configuration Summary

OTP Page	OUT0 Config	OUT1 Config	OUT2 Config	OUT3 Config	OUT4 Config	OUT5 Config	OUT6 Config	OUT7 Config
Page 0	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	Disabled
Page 1	IN1 100Ω LP-HCSL	IN1 100Ω LP-HCSL	IN1 100Ω LP-HCSL	IN1 100Ω LP-HCSL	IN1 100Ω LP-HCSL	IN1 100Ω LP-HCSL	IN1 100Ω LP-HCSL	Disabled
Page 2	100MHz 100Ω LP-HCSL -0.5% down-spread SSC	100MHz 100Ω LP-HCSL -0.5% down-spread SSC	100MHz 100Ω LP-HCSL -0.5% down-spread SSC	100MHz 100Ω LP-HCSL -0.5% down-spread SSC	100MHz 100Ω LP-HCSL -0.5% down-spread SSC	100MHz 100Ω LP-HCSL -0.5% down-spread SSC	100MHz 100Ω LP-HCSL -0.5% down-spread SSC	Disabled
Page 3	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled

2.2 LMK3H2108A03

LMK3H2108A03 Configuration Guide

LMK3H2108A03 Register Map

Table 2-2. LMK3H2108A03 Configuration Summary

OTP Page	OUT0 Config	OUT1 Config	OUT2 Config	OUT3 Config	OUT4 Config	OUT5 Config	OUT6 Config	OUT7 Config
Page 0	Disabled	24MHz In-Phase LVCMOS	24MHz In-Phase LVCMOS	24MHz In-Phase LVCMOS	24MHz In-Phase LVCMOS	50MHz In-Phase LVCMOS	50MHz In-Phase LVCMOS	50MHz In-Phase LVCMOS
Page 1	Disabled	24MHz In-Phase LVCMOS	24MHz In-Phase LVCMOS	24MHz In-Phase LVCMOS	24MHz In-Phase LVCMOS	50MHz In-Phase LVCMOS	50MHz In-Phase LVCMOS	50MHz In-Phase LVCMOS
Page 2	Disabled	24MHz In-Phase LVCMOS	24MHz In-Phase LVCMOS	24MHz In-Phase LVCMOS	24MHz In-Phase LVCMOS	50MHz In-Phase LVCMOS	50MHz In-Phase LVCMOS	50MHz In-Phase LVCMOS
Page 3	Disabled	24MHz In-Phase LVCMOS	24MHz In-Phase LVCMOS	24MHz In-Phase LVCMOS	24MHz In-Phase LVCMOS	50MHz In-Phase LVCMOS	50MHz In-Phase LVCMOS	50MHz In-Phase LVCMOS

2.3 LMK3H2108A04

LMK3H2108A04 Configuration Guide

LMK3H2108A04 Register Map

Table 2-3. LMK3H2108A04 Configuration Summary

OTP Page	OUT0 Config	OUT1 Config	OUT2 Config	OUT3 Config	OUT4 Config	OUT5 Config	OUT6 Config	OUT7 Config
Page 0	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Page 1	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Page 2	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL
Page 3	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL

2.4 LMK3H2108A05

LMK3H2108A05 Configuration Guide

LMK3H2108A05 Register Map

Table 2-4. LMK3H2108A05 Configuration Summary

OTP Page	OUT0 Config	OUT1 Config	OUT2 Config	OUT3 Config	OUT4 Config	OUT5 Config	OUT6 Config	OUT7 Config
Page 0	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	Disabled	Disabled	Disabled
Page 1	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	Disabled	Disabled	Disabled
Page 2	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	Disabled	Disabled	Disabled
Page 3	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	Disabled	Disabled	Disabled

2.5 LMK3H2108A06

LMK3H2108A06 Configuration Guide

LMK3H2108A06 Register Map

Table 2-5. LMK3H2108A06 Configuration Summary

OTP Page	OUT0 Config	OUT1 Config	OUT2 Config	OUT3 Config	OUT4 Config	OUT5 Config	OUT6 Config	OUT7 Config
Page 0	Disabled	Disabled	IN2 85Ω LP-HCSL	Disabled	Disabled	Disabled	Disabled	Disabled
Page 1	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Page 2	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	Disabled	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL
Page 3	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	Disabled	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL

2.6 LMK3H2108A07

LMK3H2108A07 Configuration Guide

LMK3H2108A07 Register Map

Table 2-6. LMK3H2108A07 Configuration Summary

OTP Page	OUT0 Config	OUT1 Config	OUT2 Config	OUT3 Config	OUT4 Config	OUT5 Config	OUT6 Config	OUT7 Config
Page 0	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	Disabled
Page 1	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	Disabled
Page 2	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	Disabled
Page 3	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	Disabled

2.7 LMK3H2108A0D

LMK3H2108A0D Configuration Guide

LMK3H2108A0D Register Map

Table 2-7. LMK3H2108A0D Configuration Summary

OTP Page	OUT0 Config	OUT1 Config	OUT2 Config	OUT3 Config	OUT4 Config	OUT5 Config	OUT6 Config	OUT7 Config
Page 0	IN0 85Ω LP-HCSL	IN1 85Ω LP-HCSL	IN1 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	Disabled	100MHz 85Ω LP-HCSL	IN0 85Ω LP-HCSL
Page 1	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	Disabled	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL
Page 2	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	Disabled	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL
Page 3	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	Disabled	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL

2.8 LMK3H2108A0E

LMK3H2108A0E Configuration Guide

LMK3H2108A0E Register Map

Table 2-8. LMK3H2108A0E Configuration Summary

OTP Page	OUT0 Config	OUT1 Config	OUT2 Config	OUT3 Config	OUT4 Config	OUT5 Config	OUT6 Config	OUT7 Config
Page 0	IN0 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL
Page 1	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL
Page 2	100MHz 85Ω LP-HCSL -0.25% down-spread SSC	100MHz 85Ω LP-HCSL -0.25% down-spread SSC	100MHz 85Ω LP-HCSL -0.25% down-spread SSC	100MHz 85Ω LP-HCSL -0.25% down-spread SSC	100MHz 85Ω LP-HCSL -0.25% down-spread SSC	100MHz 85Ω LP-HCSL -0.25% down-spread SSC	100MHz 85Ω LP-HCSL -0.25% down-spread SSC	100MHz 85Ω LP-HCSL -0.25% down-spread SSC
Page 3	100MHz 85Ω LP-HCSL -0.5% down-spread SSC	100MHz 85Ω LP-HCSL -0.5% down-spread SSC	100MHz 85Ω LP-HCSL -0.5% down-spread SSC	100MHz 85Ω LP-HCSL -0.5% down-spread SSC	100MHz 85Ω LP-HCSL -0.5% down-spread SSC	100MHz 85Ω LP-HCSL -0.5% down-spread SSC	100MHz 85Ω LP-HCSL -0.5% down-spread SSC	100MHz 85Ω LP-HCSL -0.5% down-spread SSC

2.9 LMK3H2108A0F

LMK3H2108A0F Configuration Guide

LMK3H2108A0F Register Map

Table 2-9. LMK3H2108A0F Configuration Summary

OTP Page	OUT0 Config	OUT1 Config	OUT2 Config	OUT3 Config	OUT4 Config	OUT5 Config	OUT6 Config	OUT7 Config
Page 0	100MHz 100Ω LP-HCSL	25MHz Differential LVCMOS	25MHz Differential LVCMOS	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	Disabled	156.25MHz DC-LVDS	156.25MHz DC-LVDS
Page 1	100MHz 100Ω LP-HCSL	25MHz Differential LVCMOS	25MHz Differential LVCMOS	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	Disabled	156.25MHz DC-LVDS	156.25MHz DC-LVDS
Page 2	100MHz 100Ω LP-HCSL	25MHz Differential LVCMOS	25MHz Differential LVCMOS	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	Disabled	156.25MHz DC-LVDS	156.25MHz DC-LVDS
Page 3	100MHz 100Ω LP-HCSL	25MHz Differential LVCMOS	25MHz Differential LVCMOS	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	Disabled	156.25MHz DC-LVDS	156.25MHz DC-LVDS

2.10 LMK3H2108A11

LMK3H2108A11 Configuration Guide

LMK3H2108A11 Register Map

Table 2-10. LMK3H2108A11 Configuration Summary

OTP Page	OUT0 Configuration	OUT1 Configuration	OUT2 Configuration	OUT3 Configuration	OUT4 Configuration	OUT5 Configuration	OUT6 Configuration	OUT7 Configuration
Page 0	IN0 100Ω LP-HCSL	IN0 100Ω LP-HCSL	IN0 100Ω LP-HCSL	IN0 100Ω LP-HCSL	IN0 100Ω LP-HCSL	IN0 100Ω LP-HCSL	IN0 100Ω LP-HCSL	IN0 100Ω LP-HCSL
Page 1	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL
Page 2	100MHz 100Ω LP-HCSL -0.2% down-spread SSC	100MHz 100Ω LP-HCSL -0.2% down-spread SSC	100MHz 100Ω LP-HCSL -0.2% down-spread SSC	100MHz 100Ω LP-HCSL -0.2% down-spread SSC	100MHz 100Ω LP-HCSL -0.2% down-spread SSC	100MHz 100Ω LP-HCSL -0.2% down-spread SSC	100MHz 100Ω LP-HCSL -0.2% down-spread SSC	100MHz 100Ω LP-HCSL -0.2% down-spread SSC
Page 3	100MHz 85Ω LP-HCSL -0.3% down-spread SSC	100MHz 85Ω LP-HCSL -0.3% down-spread SSC	100MHz 85Ω LP-HCSL -0.3% down-spread SSC	100MHz 85Ω LP-HCSL -0.3% down-spread SSC	100MHz 85Ω LP-HCSL -0.3% down-spread SSC	100MHz 85Ω LP-HCSL -0.3% down-spread SSC	100MHz 85Ω LP-HCSL -0.3% down-spread SSC	100MHz 85Ω LP-HCSL -0.3% down-spread SSC

2.11 LMK3H2108A14

LMK3H2108A14 Configuration Guide

LMK3H2108A14 Register Map

Table 2-11. LMK3H2108A14 Configuration Summary

OTP Page	OUT0 Configuration	OUT1 Configuration	OUT2 Configuration	OUT3 Configuration	OUT4 Configuration	OUT5 Configuration	OUT6 Configuration	OUT7 Configuration
Page 0	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Page 1	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL
Page 2	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL
Page 3	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled

2.12 LMK3H2108A15

LMK3H2108A15 Configuration Guide

LMK3H2108A15 Register Map

Table 2-12. LMK3H2108A15 Configuration Summary

OTP Page	OUT0 Configuration	OUT1 Configuration	OUT2 Configuration	OUT3 Configuration	OUT4 Configuration	OUT5 Configuration	OUT6 Configuration	OUT7 Configuration
Page 0	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	Disabled	IN0 85Ω LP-HCSL	IN0 85Ω LP-HCSL	IN1 85Ω LP-HCSL	IN1 85Ω LP-HCSL	IN0 85Ω LP-HCSL
Page 1	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	Disabled	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL	IN2 85Ω LP-HCSL
Page 2	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
Page 3	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled

2.13 LMK3H2108A16

LMK3H2108A16 Configuration Guide

LMK3H2108A16 Register Map

Table 2-13. LMK3H2108A16 Configuration Summary

OTP Page	OUT0 Configuration	OUT1 Configuration	OUT2 Configuration	OUT3 Configuration	OUT4 Configuration	OUT5 Configuration	OUT6 Configuration	OUT7 Configuration
Page 0	156.25MHz 100Ω LP-HCSL	156.25MHz 100Ω LP-HCSL	156.25MHz 100Ω LP-HCSL	156.25MHz 100Ω LP-HCSL	156.25MHz 100Ω LP-HCSL	156.25MHz 100Ω LP-HCSL	156.25MHz 100Ω LP-HCSL	156.25MHz 100Ω LP-HCSL
Page 1	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL	100MHz 100Ω LP-HCSL
Page 2	156.25MHz 85Ω LP-HCSL	156.25MHz 85Ω LP-HCSL	156.25MHz 85Ω LP-HCSL	156.25MHz 85Ω LP-HCSL	156.25MHz 85Ω LP-HCSL	156.25MHz 85Ω LP-HCSL	156.25MHz 85Ω LP-HCSL	156.25MHz 85Ω LP-HCSL
Page 3	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL

2.14 LMK3H2108A17

LMK3H2108A17 Configuration Guide

LMK3H2108A17 Register Map

Table 2-14. LMK3H2108A17 Configuration Summary

OTP Page	OUT0 Configuration	OUT1 Configuration	OUT2 Configuration	OUT3 Configuration	OUT4 Configuration	OUT5 Configuration	OUT6 Configuration	OUT7 Configuration
Page 0	100MHz 85Ω LP-HCSL	100MHz LVCMOS P	Disabled	100MHz 85Ω LP-HCSL	Disabled	100MHz LVCMOS P	100MHz 85Ω LP-HCSL	Disabled
Page 1	100MHz 85Ω LP-HCSL -0.5% down-spread SSC	100MHz LVCMOS P -0.5% down-spread SSC	Disabled	100MHz 85Ω LP-HCSL -0.5% down-spread SSC	Disabled	100MHz LVCMOS P -0.5% down-spread SSC	100MHz 85Ω LP-HCSL -0.5% down-spread SSC	Disabled
Page 2	100MHz 85Ω LP-HCSL -0.3% down-spread SSC	100MHz LVCMOS P -0.3% down-spread SSC	Disabled	100MHz 85Ω LP-HCSL -0.3% down-spread SSC	Disabled	100MHz LVCMOS P -0.3% down-spread SSC	100MHz 85Ω LP-HCSL -0.3% down-spread SSC	Disabled

Table 2-14. LMK3H2108A17 Configuration Summary (continued)

OTP Page	OUT0 Configuration	OUT1 Configuration	OUT2 Configuration	OUT3 Configuration	OUT4 Configuration	OUT5 Configuration	OUT6 Configuration	OUT7 Configuration
Page 3	100MHz 85Ω LP-HCSL -0.25% down-spread SSC	100MHz LVCMOS P -0.25% down-spread SSC	Disabled	100MHz 85Ω LP-HCSL -0.25% down-spread SSC	Disabled	100MHz LVCMOS P -0.25% down-spread SSC	100MHz 85Ω LP-HCSL -0.25% down-spread SSC	Disabled

2.15 LMK3H2108A18

LMK3H2108A18 Configuration Guide

LMK3H2108A18 Register Map

Table 2-15. LMK3H2108A18 Configuration Summary

OTP Page	OUT0 Configuration	OUT1 Configuration	OUT2 Configuration	OUT3 Configuration	OUT4 Configuration	OUT5 Configuration	OUT6 Configuration	OUT7 Configuration
Page 0	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL	100MHz 85Ω LP-HCSL
Page 1	100MHz 85Ω LP-HCSL -0.25% down-spread SSC	100MHz 85Ω LP-HCSL -0.25% down-spread SSC	100MHz 85Ω LP-HCSL -0.25% down-spread SSC	100MHz 85Ω LP-HCSL -0.25% down-spread SSC	100MHz 85Ω LP-HCSL -0.25% down-spread SSC	100MHz 85Ω LP-HCSL -0.25% down-spread SSC	100MHz 85Ω LP-HCSL -0.25% down-spread SSC	100MHz 85Ω LP-HCSL -0.25% down-spread SSC
Page 2	100MHz 85Ω LP-HCSL -0.3% down-spread SSC	100MHz 85Ω LP-HCSL -0.3% down-spread SSC	100MHz 85Ω LP-HCSL -0.3% down-spread SSC	100MHz 85Ω LP-HCSL -0.3% down-spread SSC	100MHz 85Ω LP-HCSL -0.3% down-spread SSC	100MHz 85Ω LP-HCSL -0.3% down-spread SSC	100MHz 85Ω LP-HCSL -0.3% down-spread SSC	100MHz 85Ω LP-HCSL -0.3% down-spread SSC
Page 3	100MHz 85Ω LP-HCSL -0.5% down-spread SSC	100MHz 85Ω LP-HCSL -0.5% down-spread SSC	100MHz 85Ω LP-HCSL -0.5% down-spread SSC	100MHz 85Ω LP-HCSL -0.5% down-spread SSC	100MHz 85Ω LP-HCSL -0.5% down-spread SSC	100MHz 85Ω LP-HCSL -0.5% down-spread SSC	100MHz 85Ω LP-HCSL -0.5% down-spread SSC	100MHz 85Ω LP-HCSL -0.5% down-spread SSC

3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

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