Hotswap Design using TPS2490/91 and MOSFET Transient Thermal Response

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ABSTRACT

Hotswap circuits rely on the thermal capacitance of the series-limiting MOSFET to dissipate the large transient energy under current- or power-limit operation. The peak junction temperature must be controlled in order to achieve a robust design. The constant-power MOSFET protection of the TPS2490 provides a simple method to use information provided by MOSFET manufacturers to determine peak junction temperature. This application report provides a review of the fundamentals and information commonly available to the designer along with several design examples. This report assumes familiarity with hotswap circuit considerations, thermal design, and the TPS2490/1.

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Introduction

A hotswap circuit must use a series-limiting device such as a power MOSFET to control inrush and fault currents. The limiting MOSFET momentarily dissipates a large amount of power, because the limiting action simultaneously imposes large voltage and current on it. Inrush or fault-limiting power dissipation is often an order of magnitude more than steady-state operation. An important, but often ignored, MOSFET requirement is the ability to safely absorb this thermal impulse. A successful design must limit the junction-temperature rise to a safe level.

This report demonstrates the use of published and measured data to validate the thermal design of hotswap switches using several practical examples.

Background

A successful design meets the system specifications while keeping the junction temperature of the limiting MOSFET below the manufacturer's absolute-maximum rating. The introduction of the TPS2490/91, a hotswap controller with constant-power limiting, greatly simplifies the design of hotswap circuits, allowing the designer to directly control junction temperature in an optimal fashion. Linear foldback methods only approximate optimal protection, because the MOSFET power stress varies throughout the limiting region. The constant power-limiting feature of the TPS2490/91 allows a robust design without using an oversized MOSFET.

Design and selection of the limiting element can be broken into two classical modes of operation; static and dynamic. Static operation includes the familiar thermal design based on the worst-case ambient temperature, the $I^2 \times R$ loss, the static thermal properties of the MOSFET, and heatsink parameters. Dynamic operation comes into play during a start-up or a fault-protection event. Dynamic stresses often are an order of magnitude greater than the static stresses. The ability of the MOSFET to withstand dynamic stresses has always been assumed, but rarely verified in hotswap design. The TPS2490/91's constant power foldback simplifies the use of available resources to validate a particular design.

Thermal Capacitance – Basic Concept

A power MOSFET is a composite assembly of a number of elements, each having its own size, shape, and thermal properties. Conceptually, these components are depicted in Figure 1.

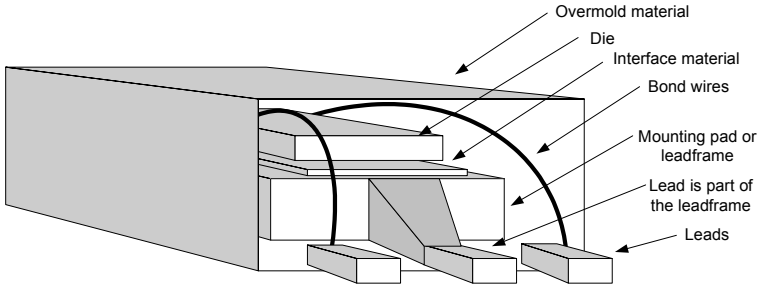


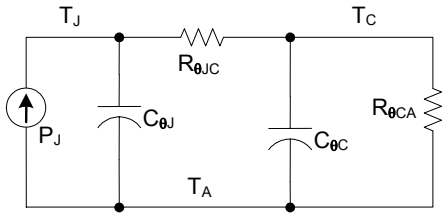
Figure 1. MOSFET Conceptual Construction

Heat dissipated within the die travels through multiple parallel paths radiating outward. Many packages expose a portion of the mounting pad to enhance thermal dissipation. Some of the leads may be an extension of the mounting pad to improve thermal and electrical performance, as is the case in the thermally-enhanced SO-8 package.

The heat flow within each element is limited by the material characteristics and geometry. Each element also has a thermal capacitance that is determined by its specific heat and mass. These properties allow the thermal performance of the mechanical assembly to be modeled.

Conceptual Thermal Model

A simplified thermal circuit, suitable for TO-220, D2PAK, and DPAK packages is shown in Figure 2. Table 1 describes each variable in the model. This model is based on the $R_{\theta JC}$ and $R_{\theta JA}$ parameters provided by the MOSFET manufacturer and supplemented by thermal capacitance to account for transient behavior. A more elaborate model would include a distinct R-C section for every thermal interface. For example, a TO-220 package bolted to a heatsink could be modeled with the series R representing the thermal resistance of the mounting interface and the C representing the thermal capacitance of the heatsink. Some designers prefer an alternate model consisting of a series of parallel thermal R-C sections.



$R_{\theta CA} = R_{\theta JA} – R_{\theta JC}$

Figure 2. MOSFET Thermal Model

Table 1. Thermal Model Parameters

Element	Description	Units
T_A	Ambient temperature or heatsink temperature	°C
T_J	Die temperature	°C
T_C	Case temperature – Often measured on a MOSFET at a central point on the mounting pad surface	°C
$R_{\theta JC}$	Lumped thermal-resistance model between the die and the case or lead measurement point	°C/W
$R_{\theta CA}$	Lumped model of the thermal resistance between the case and the ambient	°C/W
P_J	Power dissipated in the junction	W
$C_{\theta J}$	Die thermal mass	°C/J
$C_{\theta C}$	Thermal mass of the pad, leads, and plastic case	°C/J

The junction thermal capacitance of TO-220, D2PAK, and DPAK devices is often much smaller than the case capacitance. The transient thermal-impedance data provided by manufacturers typically excludes case effects because the test method maintains the case at a constant temperature. Figure 2 shows how thermal-model parameters relate to a device with weak thermal coupling between the silicon and the external connection point, such as a SOT-223 package.

Table 2. SOT-223 Thermal Model

Element	Description	Units
$R_{\theta JC}$	Converts to $R_{\theta JL,}$ the thermal resistance from junction to lead	°C/W
$R_{\theta CA}$	Represents the thermal resistance of the case and circuit-board pads, and board to ambient	°C/W
$C_{\theta J}$	Die and pad thermal mass	°C/J
$C_{\theta C}$	Represents the thermal mass of the copper device-mounting pad and board to ambient	°C/J

Hotswap Transient Junction Temperature Calculations

The transient thermal-impedance and safe-operating-area (SOA) curves published by MOSFET manufacturers can be used in a number of ways, depending on the package style and the application.

Transient Thermal Impedance

Many manufacturers give the transient thermal impedance of either the junction-to-case ($Z_{\theta JC}$), the junction-to-ambient ($Z_{\theta JA}$), or the junction-to-lead ($Z_{\theta JL}$) interface. The familiar $R_{\theta JA}$ is simply the steady-state value of $Z_{\theta JA}$, which is sometimes presented as normalized to $R_{\theta JA}$. Although Z_θ is used as a variable, it is not a complex impedance, but is a factor that relates the peak junction temperature to the dissipation of a rectangular power impulse or train of impulses. Figure 3 provides a typical example.

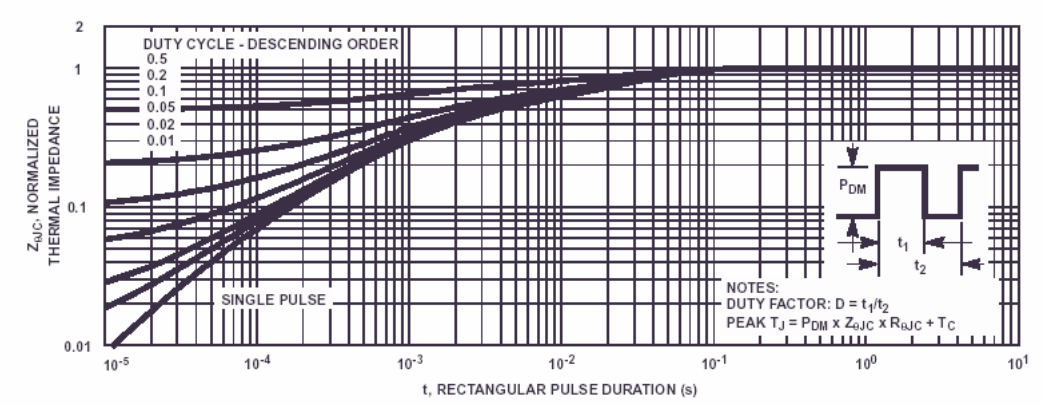


Figure 3. $Z_{\theta JC}$ Example, Fairchild FDD3682[4]

Devices mounted in packages with large metallic slugs, such as the D^2PAK and the DPAK, are characterized by $Z_{\theta JC}$, which is measured with a constant case temperature. Much larger amounts of heat can be absorbed by the case and connected heatsink if their temperature is allowed to rise.

Manufacturers of devices mounted in smaller packages, such as the TO-223 and the SO-8, provide $Z_{\theta JA}$ or $Z_{\theta JL}$. Often the $R_{\theta JC}$ or $R_{\theta JL}$ is an order of magnitude greater in these packages than a D^2PAK, which tends to thermally decouple the internals of TO-223/SO-8 devices from external heatsinking. The test methods for these packages, by necessity, include significant heating of the internal pad or leadframe.

Transient thermal impedance is provided in the form of a graph that gives the thermal impedance versus power pulse duration and duty cycle. The graph's single-pulse data is appropriate for many hotswap applications. The TPS2491 has an automatic retry duty cycle of only 0.75% which may result in a Z_θ similar to the single pulse value. Use the hotswap protection maximum time-out value as the time period to determine Z_θ from the graph, and multiply by R_θ if it is normalized. Calculate the peak junction temperature as

$$T_{JPEAK} = (P_D \times Z_{\theta JX}) + T_X$$

where X denotes the reference point (e.g., case, lead, or ambient) and T_X was the thermal-reference-point temperature immediately before the transient. The TPS2490 simplifies the use of this resource because the power dissipation is constant when the device is in foldback mode.

Safe Operating Area

The safe operating area (SOA) curves provided by manufacturers are also of some benefit. These SOA curves usually assume a junction-temperature rise from a 25°C ambient to 150°C or 175°C. System-level thermal requirements often require operation at higher starting temperatures, and so data from the graph must be adjusted for lower temperature rise. The first source[1] listed in the References section provides a methodology for scaling SOA curves as

$$SOA_T = SOA_{JMAX} \times \frac{T_{JMAX} - T}{T_{JMAX} - T_A}$$

where SOA_T represents the SOA capability at arbitrary temperature T, SOA_{JMAX} represents the capability at a specific point on the manufacturer's SOA curves, and T_{JMAX} and T_A represent the peak and ambient junction temperatures assumed on the curves (e.g., 175°C and 25°C). SOA curves tend to mix die-heating and pad- or leadframe-heating effects. They do provide a quick way of verifying a design, if the curves for the expected fault duration are provided.

Hotswap Calculations

Devices with Exposed Backside Thermal Pads

When considering a package with a low $R_{\theta JC}$ (1 - 2°C/W) such as D^2PAK or DPAK that specifies $Z_{\theta JC}$, the calculation for T_{JMAX} is relatively simple if T_C is assumed to remain constant. Ignoring the effects of $C_{\theta J}$, then

$$T_J = T_C + (P_D \times R_{\theta JC})$$

where P_D is the power dissipated, and $R_{\theta JC}$ is given by the data sheet. P_D is controlled by the TPS2490 so as to be constant when in power-limit mode, so this calculation is a simple task. T_C is the case temperature prior to an inrush or fault, which in most cases is at maximum ambient and load. The maximum junction temperature must be less than the manufacturer's specification and it is prudent to allow a safety margin of 10°C - 25°C.

The thermal capacitance of the package and heatsink must be known to check if the constant case temperature assumption is correct. The packages discussed in this presentation were measured, and the tabulated results provided below. To calculate the case temperature rise, assume that the dissipation is constant power, the package and heatsink capacitance dominate the junction capacitance, and that little energy is lost over the fault period to convection. The case temperature rise can be calculated as

$$\Delta T_C = \frac{P_D \times t_L}{C_{\theta C}}$$

where t_L is the power-pulse duration, which is equal to the maximum fault timer period.

Example 1

Create a design using the TI Design Tool[2] with the following entries and results:

- Use V_{CCMAX} = 48 V, C_{OUT} = 100 µF, and I_{MAX} = 4 A. The maximum ambient temperature is 68°C, which is entered further down the spreadsheet.
- Choose R_S = 10 mΩ and skip the section on undervoltage lockout.
- Use Eff_{MIN} = 99% which yields $R_{DS(ON)\_MAX}$ = 77 mΩ.
- Select FDD3682, which is in a DPAK, by researching vendor catalogs. R_{DSON} is 36 mΩ at 25°C with a 1.6 multiplier at 110°C (= 56 mΩ). Thermal resistances are $R_{\theta JC}$ = 1.58°C/W, and $R_{\theta JA}$ = 52°C/W (on a 1-in^2 pad).
- Use T_{JMAX} = 175°C, T_{AMAX} = 68°C, $R_{\theta JA}$ = 52°C/W, $R_{\theta JC}$ = 1.58°C/W, and $R_{DSONMAX}$ = 56 mΩ.
- The calculated T_{JMAX} = 115°C, and P_{MAX} = 16.314 W. The junction temperature assumption used for the R_{DSON} value was close enough as chosen, but its value could be refined by iteration.
- The calculated t_{ON} = 7.094 ms, and C_{TMIN} = 0.082 µF.
- Select a value of C_T = 0.1 µF.

The P_{MAX} shown in the spreadsheet is reduced by 30% to account for the TPS2490 tolerance. P_{MAX} can be as high as 21.2 W. To determine the maximum fault-timer period that the TPS2490 would yield using a 0.1 µF capacitor, refer to the TPS2490 data sheet. The minimum timer charge current of 15 µA to a 4-V trip point, using a 10% tolerance capacitor would yield a period of:

$$I = C \times \frac{\Delta V}{\Delta T}$$

$$\Delta T = C \times \frac{\Delta V}{I} = (0.1\,\mu F \times 1.1) \times \frac{4V}{15\,\mu A} = 29.3\ ms$$

Calculate:

- T_{JMAX} = (115°C + (21.2 W × 1.58°C/W)) = 148.5°C
- ΔT_C = ((21.2 W × 0.029 s)/ 0.37 J/°C) = 1.66°C
  (See Table 4 for thermal capacitance values)

This is a solid design with margin for additional, unaccounted stress factors.

To compare this result to the $Z_{\theta JC}$ approach, get $Z_{\theta JX}$ from the manufacturer's graph (refer to Figure 3), using the maximum power dissipation allowed by the TPS2490/91 and the maximum fault timer period.

- The normalized $Z_{\theta JC}$ at 30 mS, is approximately 0.8 for a net value of 1.26.
- T_{JMAX} = (115°C + (21.2 W × 1.26°C/W)) = 141.7°C.

The results from the two methods compare well considering the difference in methodology and the required accuracy; however, the former is considerably simpler as the next example shows. The $Z_{\theta JC}$ value of 0.8 indicates that the $C_{\theta J}$ was nearly charged, and if an output capacitor greater than 100µF was used, the two methods would have resulted in even closer results.

Devices Without Exposed Thermal Pads

When considering a package with a high $R_{\theta JC}$ (10°C/W – 20°C/W), such as a TO-223 or SO-8, the $Z_{\theta JC}$ method yields the best results. If T_L doesn't change much over the fault period,

$$T_{JPEAK} = (P_D \times Z_{\theta JL}) + T_{L\_INITIAL}$$

where $Z_{\theta JL}$ is the single-pulse thermal impedance (from the MOSFET data sheet) for the maximum fault timer period. $T_{L\_INITIAL}$ is the expected lead temperature prior to an inrush or fault, which in most cases occurs with maximum ambient temperature and load. Power is absorbed by the distributed thermal capacitance of the leadframe, but little is transmitted to the heatsink during the transient due to the relatively high $R_{\theta JL}$.

Example 2

Create a design using the TI Design Tool[2] with the following entries and results:

- Use V_{CCMAX} = 48 V, C_{OUT} = 100 µF, and I_{MAX} = 4 A. The maximum ambient temperature is 50°C, which is entered further down the spreadsheet.
- Choose R_S = 10 mΩ and skip the section on undervoltage lockout.
- Use Eff_{MIN} = 99% which yields $R_{DS(ON)MAX}$ = 77 mΩ.
- Select Si4484EY, which is in an SO-8 package, by researching vendor catalogs. R_{DSON} is 34 mΩ at 25°C with a 1.6 multiplier at 100°C (= 54.4 mΩ). Thermal resistances are $R_{\theta JL}$ = 21°C/W, and $R_{\theta JA}$ = 85°C/W (on a 1-in^2 pad), but assume that this reduces to 50°C/W with forced air cooling.
- Use T_{JMAX} = 175°C, T_{AMAX} = 50°C, $R_{\theta JA}$ = 50°C/W, $R_{\theta JC}$ = 21°C/W, and $R_{DSONMAX}$ = 54.4 mΩ.
- The calculated $T_{J(OPERATING)}$ = 93.5°C, and P_{MAX} = 2.492 W. Typical TimerOut time is 108 ms using a 0.68 µF, and assuming about 75% tolerance, the maximum time is approximately 189 ms.
- Iterate by going to the data sheet graph for $Z_{\theta JL}$ in Figure 4 (189 ms, single pulse) and obtain an adjusted value for $R_{\theta JC}$ of $0.44 \times 21 = 9.24$°C/W; then substitute this value into the spreadsheet.
- The calculated $T_{J(OPERATING)}$ = 93.5°C, and P_{MAX} = 4.888 W, TimerOut time typical is 52.5 ms using a 0.33-µF capacitor, and assuming about 75% tolerance the maximum time is approximately 92.4 ms. $T_{J(OPERATING)}$ doesn't change because it is based on $R_{\theta JA}$.
- Iterate several times until a solution is found with values similar to C_T = 0.1 µF, TimerOut time = 16 ms (worst case is 28 ms), $Z_{\theta JL} = 0.15 \times 21 = 3.15$°C/W, t_{ON} = 8.78 ms, and P_{MAX} = 13.16 W.

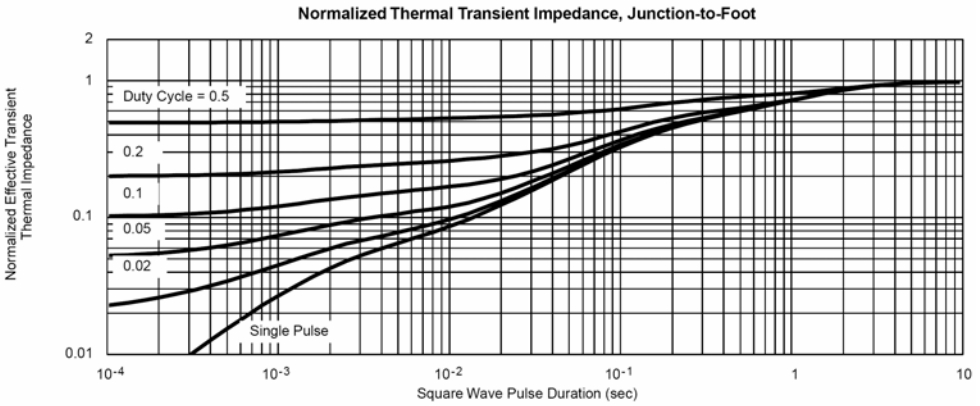


Figure 4. Si4484EY Transient Thermal Impedance[3]

P_{MAX} is derated by 30% in the spreadsheet to account for the TPS2490 tolerance, resulting in a worst case dissipation of 17.18 W maximum.

T_{JMAX} = (93.5°C + (17.18 W × 3.15°C/W)) = 148°C

This example was similar to Example 1, but a few changes were neccessary, notably a reduction in the ambient temperature and an assumed reduction in thermal resistance due to forced air. The smaller package has a reduced ability to sink power from the die to a larger $R_{\theta JL}$ and also has a higher $R_{\theta JA}$.

This design process is more difficult due to the external graphical data and required iteration.

SOA Derating Example

Assume that we want to see if the FDD3682 can withstand a fault with the following conditions: P_J = 20.5 W, pulse width = 29 ms, operating junction temperature = 116°C, T_{JMAX} = 175°C, and V_{IN_MAX} = 56 V.

1. Using Figure 5, determine that at 56 V, for a period of between 10 ms and continuous (DC), a power of 56 W and a current of 1 A are allowed.
2. Calculate:

$$SOA_T = SOA_{JMAX} \times \frac{T_{JMAX} - T}{T_{JMAX} - T_A}$$

$$SOA_T = (56\ V \times 1\ A) \times \frac{175\ C - 116\ C}{175\ C - 25\ C} = 22\ W$$

3. The result is that the device will survive the fault with a little margin.

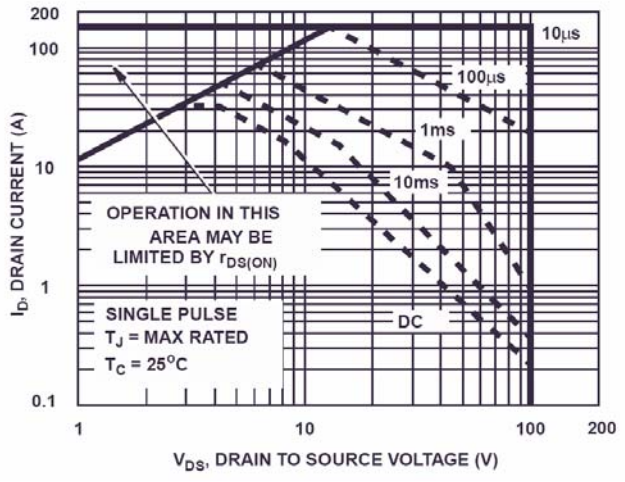


Figure 5. FDD3682[4] SOA Curve

$R_{\theta JC}$ or $R_{\theta JL}$ Comparison Table

The application note listed at the end of this report[5] gives a broad guideline of thermal resistances $R_{\theta JC}$ or $R_{\theta JL}$ in Appendix B which is quoted here:

Table 3. Thermal Resistance Comparison

Package	$R_{\theta JX}$ °C/W
D^2PAK	1
DPAK	5
SOT-223	7.4
SO-8	20.8

These numbers only represent a guideline and examples can easily be found that show large differences from these values.

Tabulated Thermal Capacitance Test Results

A number of packages were tested for $R_{\theta JA}$ and C_θ to assist the designer. The testing was performed on devices suspended in air with only test leads soldered to the pins. $R_{\theta JA}$ results vary somewhat from the published data because the mounting was different, and the relatively heavy test leads offered an unconventional heat path. C_θ represents the total package thermal capacitance. These results were obtained using the inherent diode junction to heat the device and then monitor temperature as the device cooled. The junction forward voltage versus temperature was characterized to allow determination of junction temperature for $R_{\theta JA}$ calculation. Given the time constant and $R_{\theta JA}$, the package capacitance was computed.

Table 4. Tabulated Thermal Properties

Device	Package	τ (s)	$R_{\theta JA}$ (°C/W)	$C_{\theta C}$ (°C/J)
IRF540NS	D^2PAK	60	55.2	1.09
IRFR3411	DPAK	25	67.4	.37
IRF7307	SO-8	10.8	94.7	.11
IRFL014	SOT-223	10.0	96.1	.10

Design Verification

Not all MOSFETs are equally able to handle the high stress levels associated with the inherent active control of hotswap. This capability is not always evident from data-sheet SOA curves, as vendors sometimes construct these curves based on projections of pulsed operation. Some MOSFET designs may exhibit a negative temperature coefficient when driven with gate voltage slightly above the threshold voltage, with a resultant spot heating and failure[6]. One study reports linear-operation problems with some Trench FET designs[7]. However this weakness may not be a problem for all voltage ranges, specific devices, and applications. Ultimately, the design should be tested to validate both the thermal design and to determine the suitability of a particular device to the application.

Conclusion

This report has shown how to use the available MOSFET SOA and transient thermal impedance data to design hotswap circuits, and why transient thermal data is the more useful of the two for design. Cases using several classes of power MOSFET packaging were covered.

The TPS2490 makes MOSFET selection and thermal design easier because it implements constant power limiting. Constant power limiting, along with transient thermal data, makes it possible to account for peak junction temperature across many operating points with a single calculation.

References

[1] Fairchild Semiconductor, *Safe Operating Area Without a Heat Sink*, AN-7516, August 1994.

[2] Texas Instruments, *TPS2490 / TPS2491 Design-In Calculation Tool*, SLVC033

[3] Vishay – Siliconix, *Si4484EY*, Document Number 71189S-03951 Rev. C, May 2003

[4] Fairchild Semiconductor, *FDD3682*, *FDD3682 Rev B*, September 2002

[5] Fairchild Semiconductor, *Maximum Power Enhancement Techniques for SOT-223 Power MOSFETs*, AN-1028, August 1998.

[6] Alan Ball, Hot-swap MOSFET reliability, *EDM Magazine,* April 2004

[7] Jeffrey A. Ely, Are Trench FETS too Fragile for Linear Applications, *Power Electronics Technology*, January 2004

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Texas Instruments, Positive High-Voltage Power-Limiting Hotswap Controller, TPS2490/91 Data Sheet, SLVS503, November 2003

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