User's Guide

TPS54202 Step-Down Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains background information for the TPS54202 as well as support documentation for the TPS54202EVM-716 evaluation module (PWR716-001). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54202EVM-716.

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1 Introduction

This user's guide contains background information for the TPS54202 as well as support documentation for the TPS54202EVM-716 evaluation module (PWR716-001). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54202EVM-716.

1.1 Background

The TPS54202 dc/dc converter is designed to provide up to a 2-A output from an input voltage source of 8 V to 28 V. Rated input voltage and output current range for the evaluation module are given in Table 1-1. In order to reduce EMI, the TPS54202 introduces frequency spread spectrum. The jittering span is ±6% of the switching frequency with 1/512 swing frequency. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS54202 regulator. The switching frequency is internally set at a nominal 500 kHz. The high-side and low-side MOSFETs are incorporated inside the TPS54202 package along with the gate-drive circuitry. The low drain-to-source on resistance of the MOSFETs allow the TPS54202 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are integrated to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54202 provides an adjustable undervoltage lockout input. The absolute maximum input voltage is 30 V for the TPS54202EVM-716.

Table 1-1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS54202EVM-716	V_{IN} = 8 V to 28 V	0 A to 2 A

1.2 Performance Specification Summary

A summary of the TPS54202EVM-716 performance specifications is provided in Table 1-2. Specifications are given for an input voltage of V_{IN} = 24 V and an output voltage of 5.0 V, unless otherwise specified. The TPS54202EVM-716 is designed and tested for V_{IN} = 8 V to 28 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

Table 1-2. TPS54202EVM-716 Performance Specification Summary

Specification	Test Conditions		MIN	TYP	MAX	Unit
V_{IN} operating voltage range			8	24	28	V
V_{IN} start voltage				6.74		V
V_{IN} stop voltage				5.83		V
Output voltage set point				5		V
Output current range	V_{IN} = 8 V to 28 V		0		2	A
Line regulation	I_O = 1 A, V_{IN} = 8 V to 28 V			±0.5%		
Load regulation	V_{IN} = 12 V, I_O = 0 A to 2 A			±0.5%		
Load transient response	I_O = 0.5 A to 1.5 A	Voltage change		–150		mV
		Recovery time		150		µs
	I_O = 1.5 A to 0.5 A	Voltage change		150		mV
		Recovery time		150		µs
Input ripple voltage	I_O = 2 A			400		mV_{PP}
Output ripple voltage	I_O = 2 A			<30		mV_{PP}
Output rise time				5		ms

Table 1-2. TPS54202EVM-716 Performance Specification Summary (continued)

Specification	Test Conditions	MIN	TYP	MAX	Unit
Center operating frequency			500		kHz
Maximum Efficiency	TPS54202EVM-716, V_{IN} = 12 V, I_O = 1 A		94.06%		

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54202. Some modifications can be made to this module.

1.3.1 Output Voltage Set Point

The voltage divider, R2 and R3, is used to set the output voltage. To change the output voltage of the EVM, it is necessary to change the value of resistor R3. Changing the value of R3 can change the output voltage above 0.596 V. The value of R3 for a specific output voltage can be calculated using Equation 1. Use 100 kΩ for R2.

$$R3 = \frac{R2 \times 0.596\ V}{V_{OUT} - 0.596\ V} \quad (1)$$

Table 1-3 lists the R2 and R3 values for some common output voltages. Note that V_{IN} must be in a range so that the minimum on-time is greater than 150 ns. The values in Table 1-3 are standard values, not the exact value calculated using Equation 1.

Table 1-3. Recommended Component Values

V_{OUT} (V)	L (µH)	C_{OUT} (µF)	R2 (kΩ)	R3 (kΩ)	C8 (pF)
1.8	5.6	66	100	49.9	47
2.5	8.2	44	100	31.6	33
3.3	10	44	100	22.1	56
5	15	44	100	13.3	75
12	22	44	100	5.23	100

1.3.2 Output Capacitor and Feed-Forward Capacitor

Considering the loop stability and the effect of the internal parasitic parameters, choose a crossover frequency less than 40 kHz, without considering the feed-forward capacitor. A simple estimation for the crossover frequency without feed-forward capacitor C8 is shown in Equation 2, assuming C_{OUT} has small ESR.

$$f_o = \frac{3.95}{V_{OUT} \times C_{OUT}} \quad (2)$$

Depending on V_{OUT}, if the output capacitor, C_{OUT}, is dominated by low-ESR (ceramic types) capacitors, a low phase margin could result. To improve the phase boost, an external feed-forward capacitor, C8, can be added in parallel with R2. C8 is chosen such that phase margin is boosted at the crossover frequency.

C8 is calculated in Equation 3:

$$C8 = \frac{1}{2\pi f_o} \times \frac{1}{R_2} \quad (3)$$

For this design, C8 = 75 pF. C8 is not needed when C_{OUT} has high ESR, and C8 calculated from Equation 3 should be reduced with medium ESR. Use Table 1-3 as a starting point.

1.3.3 Adjustable UVLO

The under voltage lock out (UVLO) can be adjusted externally using R4 and R5. The EVM is set for a start voltage of 6.74 V and a stop voltage of 5.83 V using R4 = 510 kΩ and R5 = 105 kΩ. Use Equation 4 and Equation 5 to calculate required resistor values for different start and stop voltages. For higher light-load efficiency, consider choosing a larger R4 and R5. Make adjustments to V_{START} or V_{STOP} for a proper R4.

$$R4 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (4)$$

$$R5 = \frac{R4 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R4\,(I_p + I_h)} \quad (5)$$

I_p = 0.7 µA, I_h = 1.55 µA, $V_{ENFALLING}$ = 1.19 V and $V_{ENRISING}$ = 1.22 V

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54202EVM-716 evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

2.1 Input/Output Connections

The TPS54202EVM-716 is provided with input/output connectors and test points as shown in Table 2-1. A power supply capable of supplying 2 A must be connected to J1 through a pair of 20-AWG wires. The load must be connected to J2 through a pair of 20-AWG wires. The maximum load current capability must be at least 3 A to use the full capability of this EVM. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. TP6 is used to monitor the output voltage with TP7 as the ground reference.

Table 2-1. EVM Connectors and Test Points

Reference Designator	Function
J1	VIN (see Table 1-1 for V_{IN} range)
J2	VOUT, 5 V at 2 A maximum
JP1	2-pin header for enable. Connect EN to ground to disable, open to enable.
TP1	V_{IN} test point at VIN connector
TP2	GND test point at VIN
TP3	GND test point
TP4	SW test point
TP5	Test point between voltage divider network and output. Used for loop response measurements.
TP6	Output voltage test point at OUT connector
TP7	GND test point at VOUT connector

2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 0.5 A – 1 A, and then decreases as the load current increases towards full load. Figure 2-1 shows the efficiency for the TPS54202EVM-716 at an ambient temperature of 25°C.

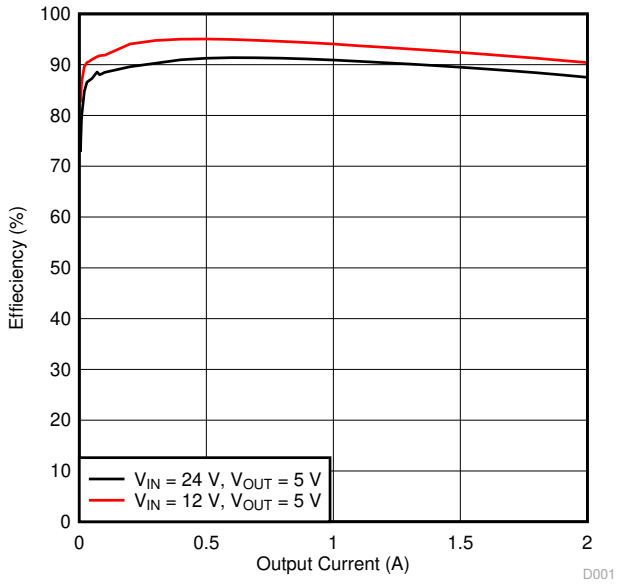

Figure 2-1. TPS54202EVM-716 Efficiency

Figure 2-2 shows the efficiency for the TPS54202EVM-716 on a semi-log scale to better show light load efficiency. The ambient temperature is 25°C.

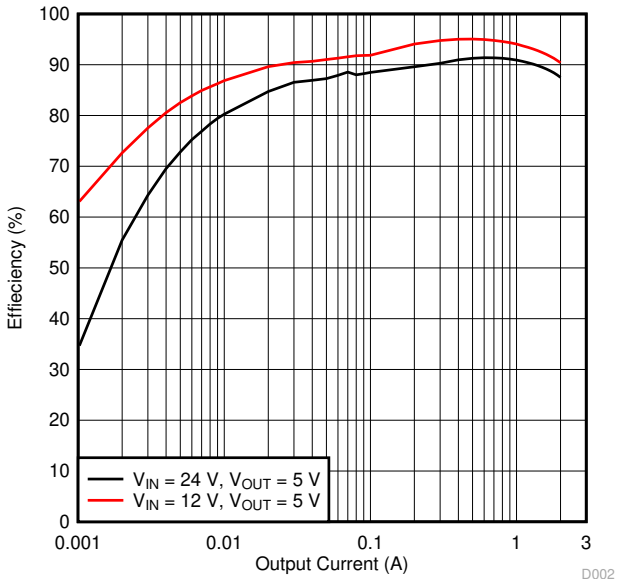

Figure 2-2. TPS54202EVM-716 Low Current Efficiency

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

2.3 Output Voltage Load Regulation

Figure 2-3 shows the load regulation for the TPS54202EVM-716.

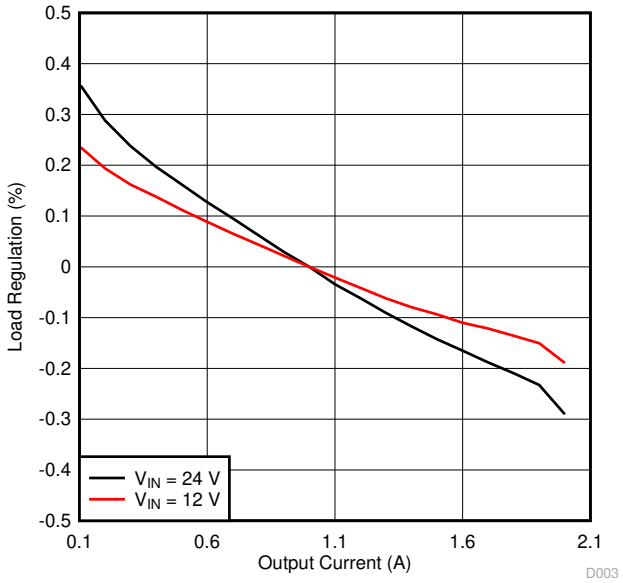

Figure 2-3. TPS54202EVM-716 Load Regulation

Measurements are given for an ambient temperature of 25°C.

2.4 Output Voltage Line Regulation

Figure 2-4 shows the line regulation for the TPS54202EVM-716.

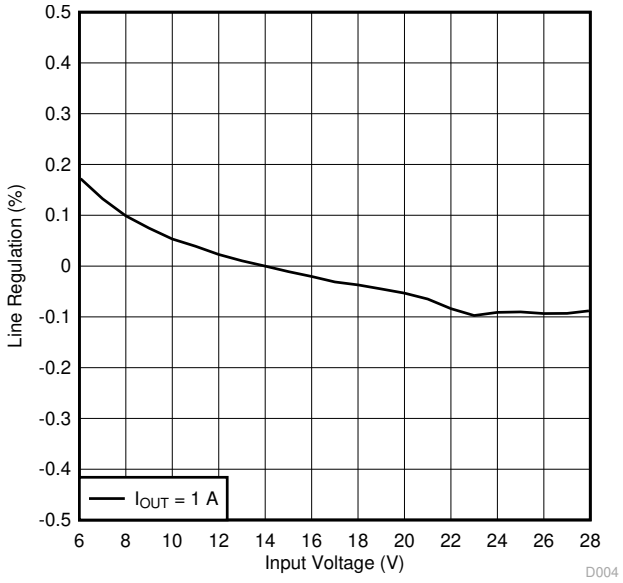

Figure 2-4. TPS54202EVM-716 Line Regulation

2.5 Load Transients

Figure 2-5 shows the TPS54202EVM-716 response to load transients. The current step is from 25% to 75% of maximum rated load at 24-V input. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

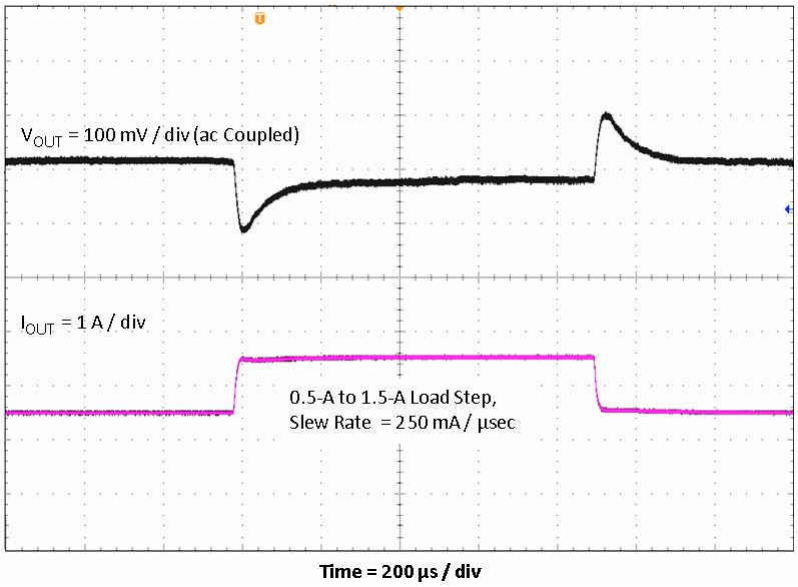

Figure 2-5. TPS54202EVM-716 Transient Response

2.6 Output Voltage Ripple

Figure 2-6, Figure 2-7, Figure 2-8, and Figure 2-9 show the TPS54202EVM-716 output voltage ripple for full-load, skip-mode, light-load and no-load operation. V_{IN} = 24 V. The output The ripple voltage is measured directly across the output capacitors.

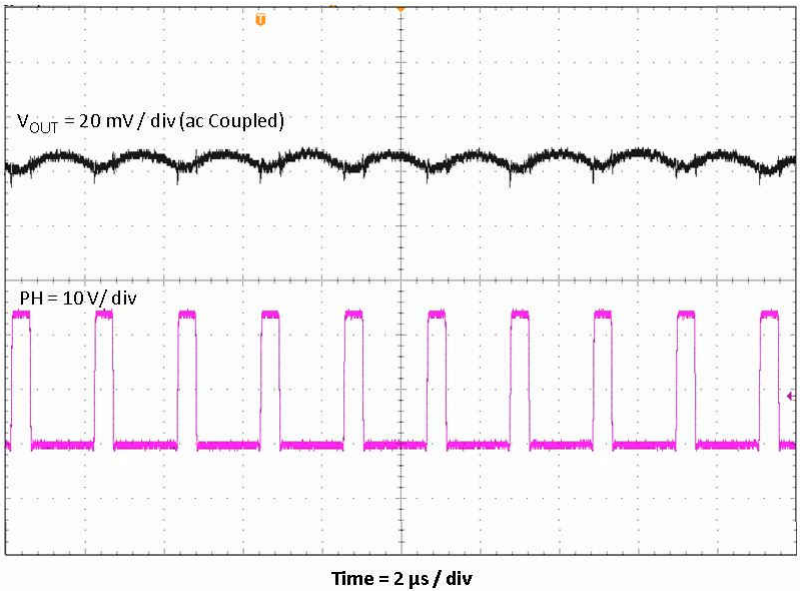

Figure 2-6. TPS54202EVM-716 Output Ripple, I_{OUT} = 2 A

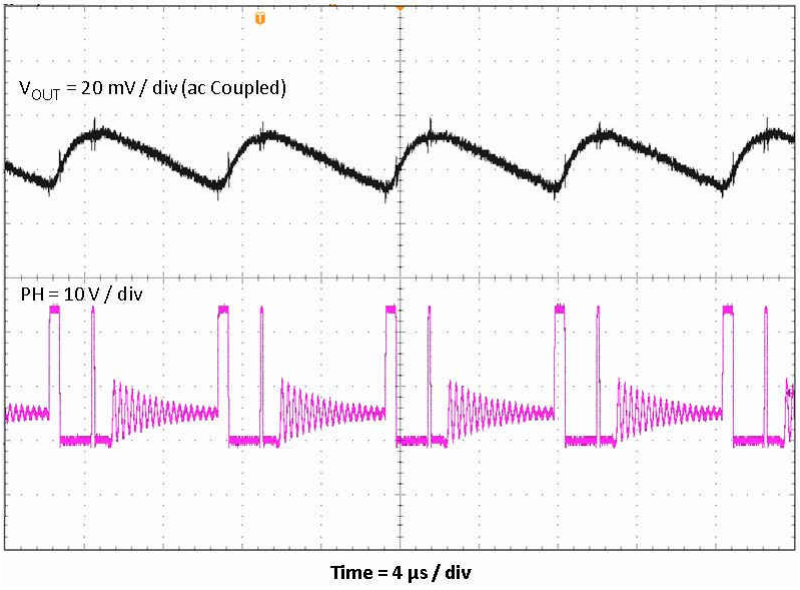

Figure 2-7. TPS54202EVM-716 Output Ripple, I_{OUT} = 100 mA

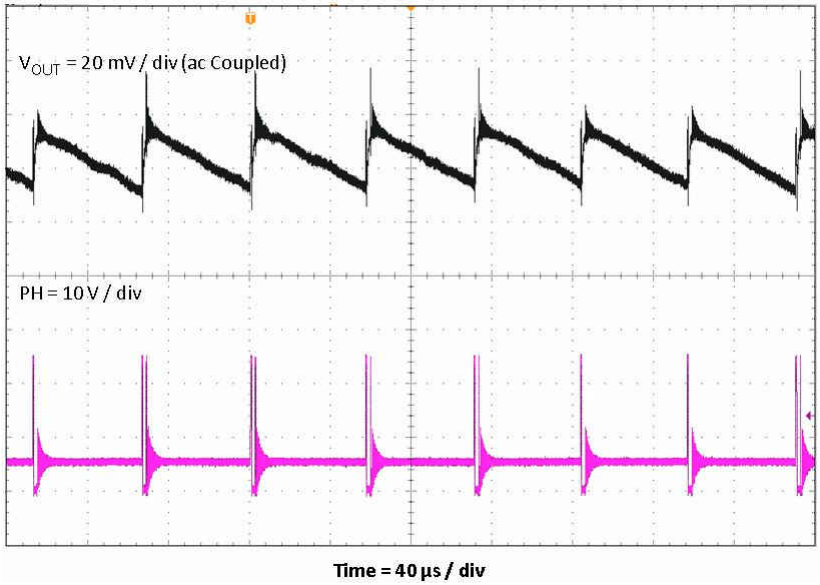

Figure 2-8. TPS54202EVM-716 Output Ripple, I_{OUT} = 10 mA

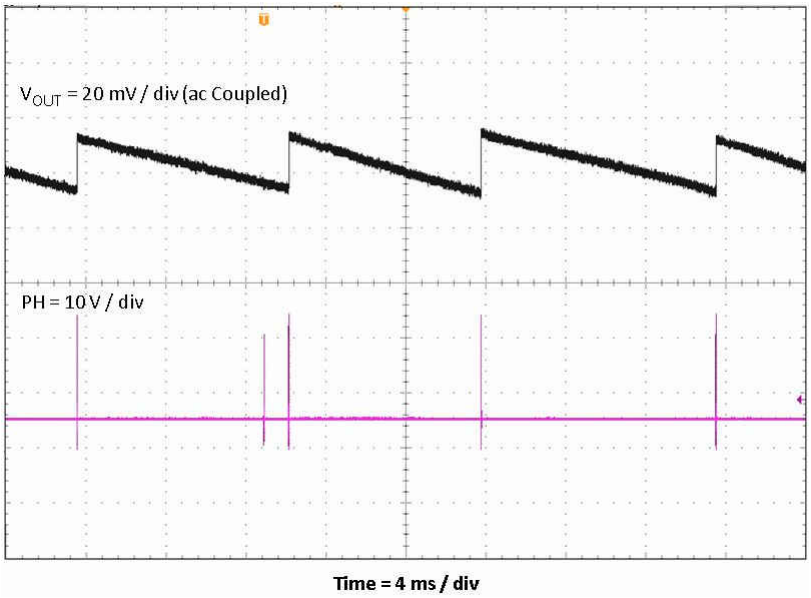

Figure 2-9. TPS54202EVM-716 Output Ripple, I_{OUT} = 0 A

2.7 Input Voltage Ripple

Figure 2-10 shows the TPS54202EVM-716 input voltage ripple. The output current is the rated full load of 2 A and V_{IN} = 24 V. The ripple voltage is measured directly across the input capacitors.

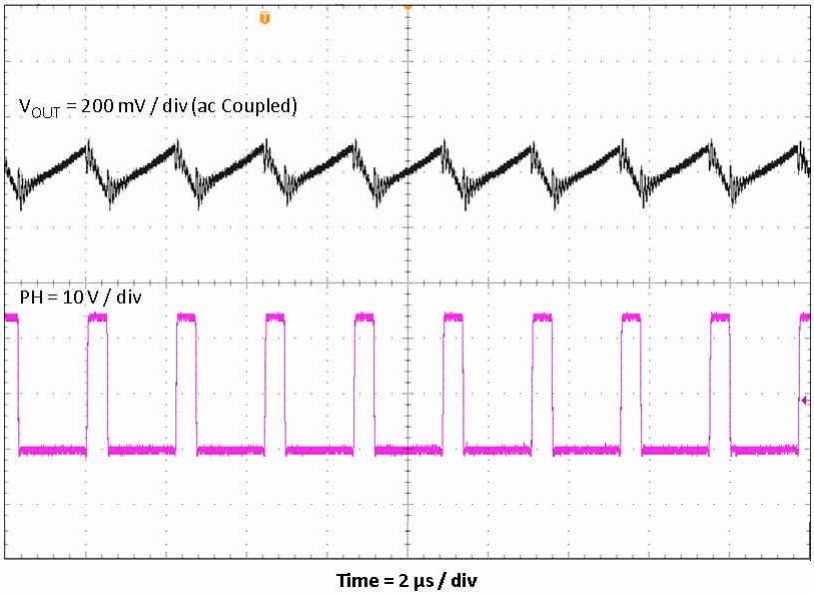

Figure 2-10. TPS54202EVM-716 Input Ripple

2.8 Powering Up

Figure 2-11 and Figure 2-12 show the start-up waveforms for the TPS54202EVM-716. In Figure 2-11, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold as set by the R4 and R5 resistor divider network. In Figure 2-12, the input voltage is initially applied and the output is inhibited by using a 3.3-V logic signal between EN and GND. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 5 V. The input voltage for these plots is 24 V and the load is 5 Ω.

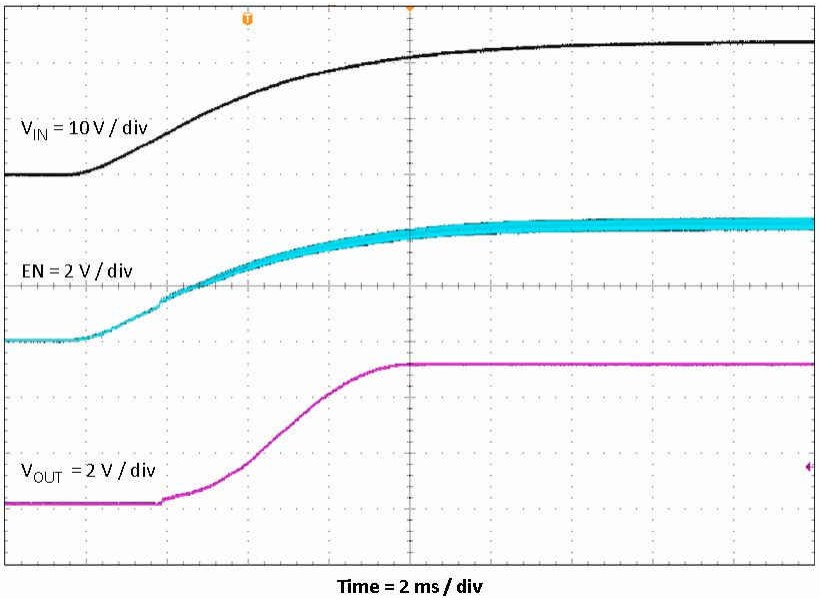

Figure 2-11. TPS54202EVM-716 Startup Relative to V_{IN}

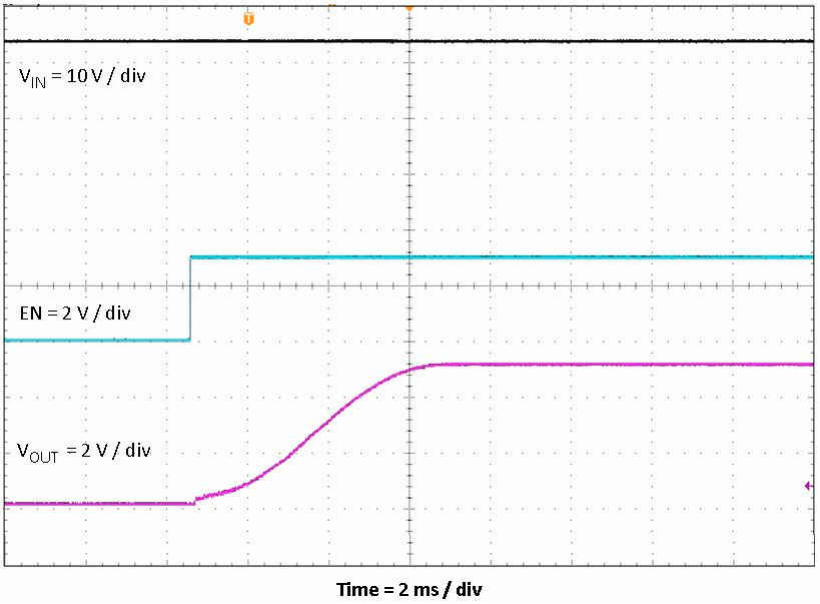

Figure 2-12. TPS54202EVM-716 Startup Relative to Enable

2.9 Powering Down

Figure 2-13 and Figure 2-14 show the start-up waveforms for the TPS54202EVM-716. In Figure 2-13, the output voltage ramps down as soon as the input voltage falls below the UVLO stop threshold as set by the R4 and R5 resistor divider network. In Figure 2-14, the output is inhibited by using a 3.3-V logic signal between EN and GND. The input voltage for these plots is 24 V and the load is 5 Ω.

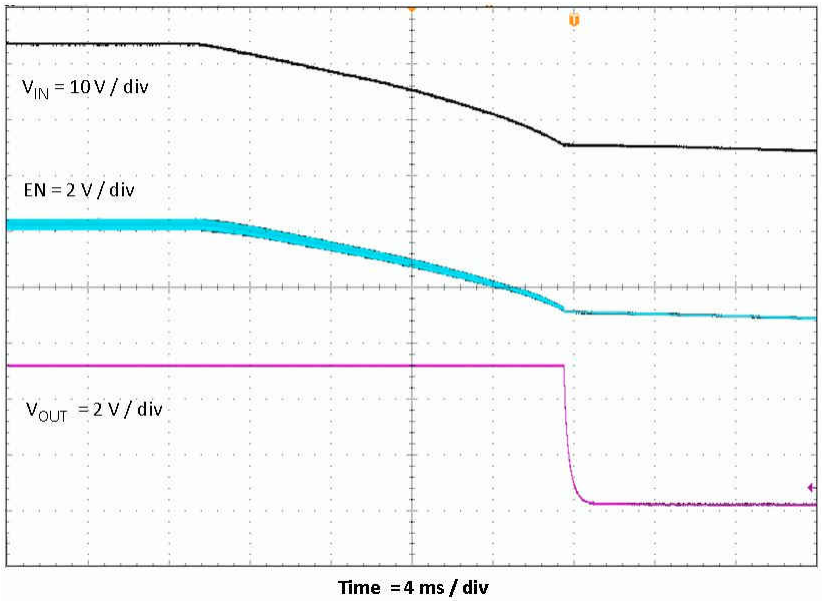

Figure 2-13. TPS54202EVM-716 Shutdown Relative to V_{IN}

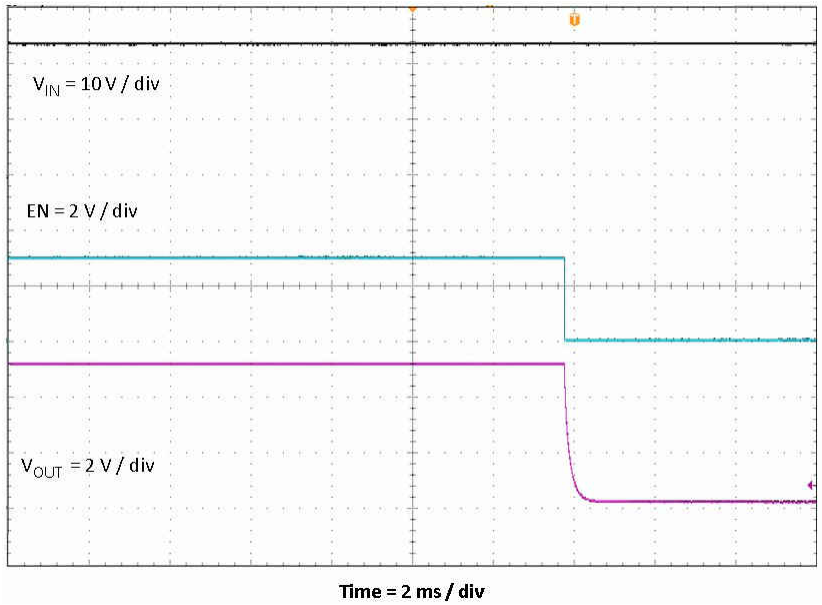

Figure 2-14. TPS54202EVM-716 Shutdown Relative to EN

3 Board Layout

This section provides a description of the TPS54202EVM-716, board layout, and layer illustrations.

3.1 Layout

Figure 3-1 and Figure 3-2 show the board layout for the TPS54202EVM-716. The topside layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz. copper.

The top layer contains the main power traces for V_{IN}, V_{OUT}, and SW. Also on the top layer are connections for the remaining pins of the TPS54202 and a large area filled with ground. To facilitate the placement of the main input bypass capacitor as close to the V_{IN} and GND pins as possible, the trace for SW is routed to the bottom layer immediately at the pin 3 connection. It is routed back to the top layer at the L1 inductor and C4 BOOT capacitor. The bottom layer contains a ground plane plus a copper fill area for SW, an etch run to connect the upper resistor of the voltage set point divider to the regulation point at the J2 output connector, and a trace to connect the upper resistor of the UVLO set point divider network to V_{IN}. The top-side ground areas are connected to the bottom and internal ground planes with multiple vias placed around the board to provide a thermal path from the top-side ground area to the bottom-side and internal ground planes.

The input decoupling capacitors (C2, and C1) and bootstrap capacitor (C4) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. For the TPS54202, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply.

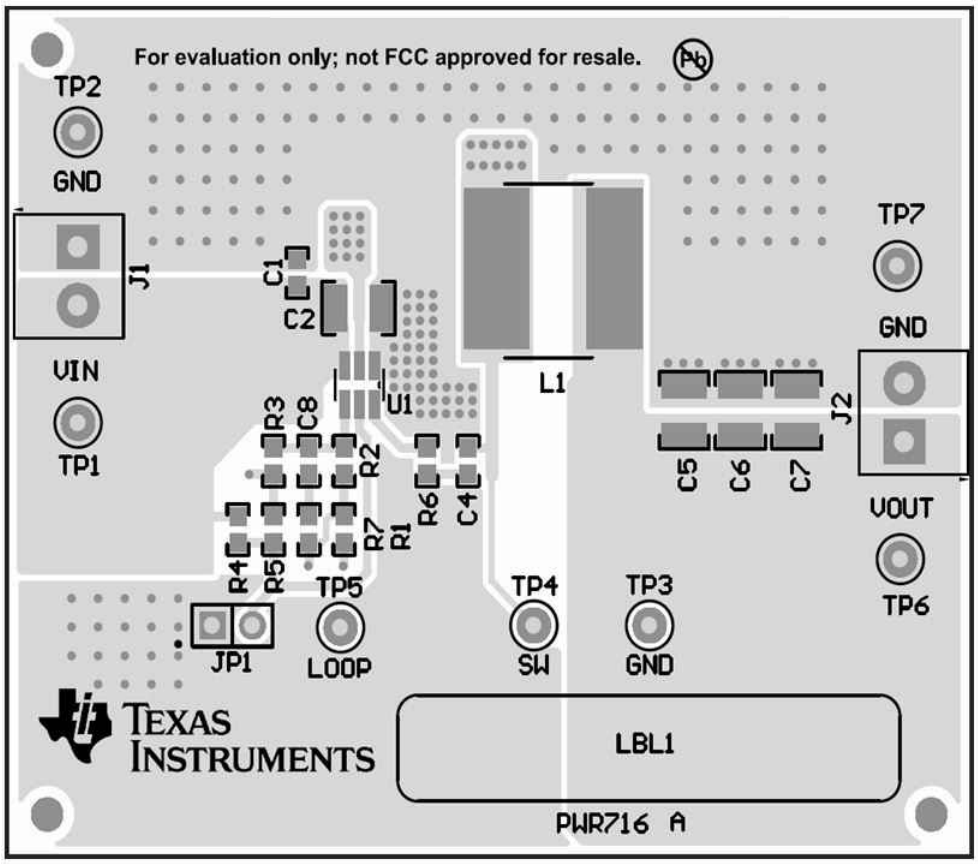

Figure 3-1. TPS54202EVM-716 Top-Side Assembly

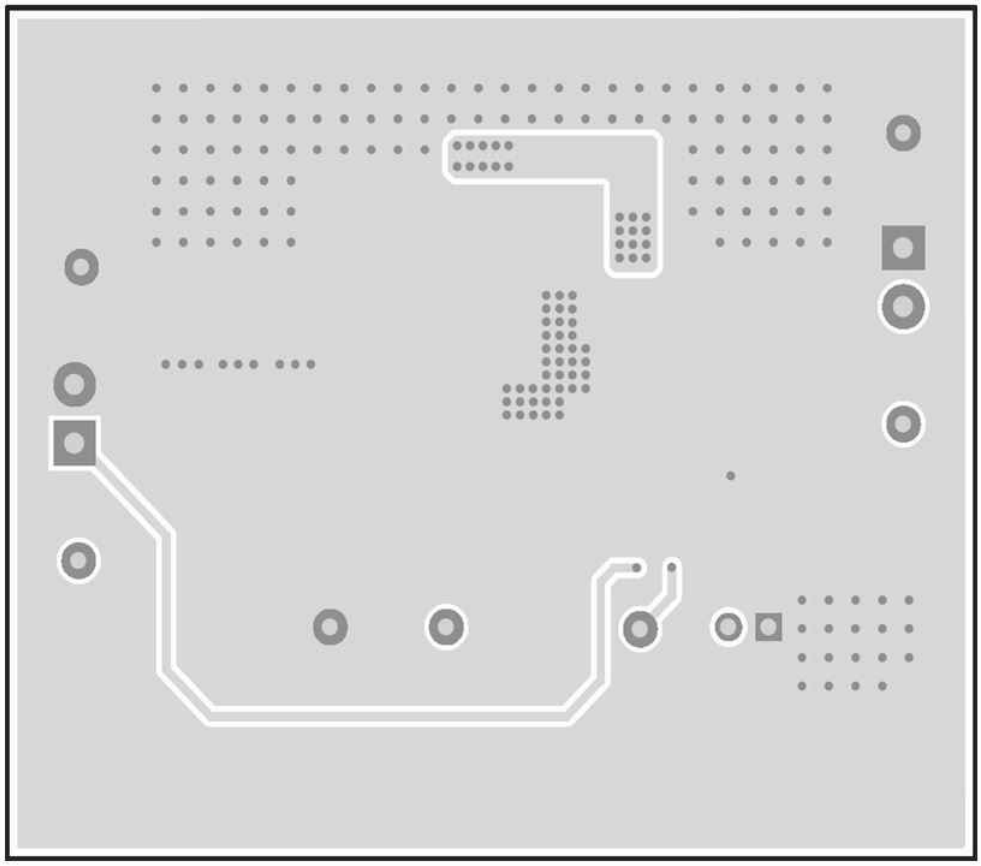

Figure 3-2. TPS54202EVM-716 Bottom-Side Layout

4 Schematic and Bill of Materials

This section presents the TPS54202EVM-716 schematic and bill of materials.

4.1 Schematic

Figure 4-1 is the schematic for the TPS54202EVM-716.

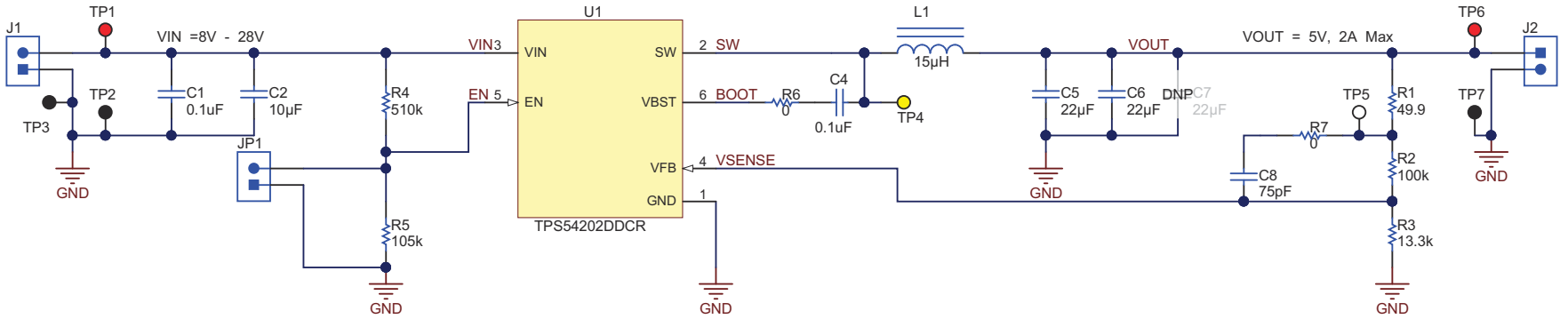

Figure 4-1. TPS54202EVM-716 Schematic

4.2 Bill of Materials

Table 4-1 presents the bill of materials for the TPS54202EVM-716.

Table 4-1. TPS54202EVM-716 Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C1, C4	2	0.1 µF	CAP, CERM, 0.1 µF, 25 V, ±10%, X5R, 0603	0603	GRM188R61E104KA01D	Murata
C2	1	10 µF	CAP, CERM, 10 µF, 35 V, ±10%, X7R, 1210	1210	GRM32ER7YA106KA12L	Murata
C5, C6	2	22 µF	CAP, CERM, 22 µF, 25 V, ±10%, X7R, 1210	1210	GRM32ER71E226KE15L	Murata
C8	1	75 pF	CAP, CERM, 75 pF, 50 V, ±5%, C0G/NP0, 0603	0603	GRM1885C1H750JA01D	Murata
J1, J2	2		Terminal Block, 6 A, 3.5 mm Pitch, 2-Pos, TH	7.0 × 8.2 × 6.5 mm	ED555/2DS	On-Shore Technology
JP1	1		Header, 100 mil, 2 × 1, Gold, TH	2 × 1 Header	TSW-102-07-G-S	Samtec
L1	1	15 µH	Inductor, Shielded Drum Core, Ferrite, 15 µH, 3.5 A, 0.036 Ω, SMD	10 × 5 × 10 mm	7447714150	Wurth Elektronik
R1	1	49.9	RES, 49.9, 1%, 0.1 W, 0603	0603	CRCW060349R9FKEA	Vishay-Dale
R2	1	100 k	RES, 100 k, 1%, 0.1 W, 0603	0603	CRCW0603100KFKEA	Vishay-Dale
R3	1	13.3 k	RES, 13.3 k, 1%, 0.1 W, 0603	0603	CRCW060313K3FKEA	Vishay-Dale
R4	1	510 k	RES, 510 k, 5%, 0.1 W, 0603	0603	CRCW0603510KJNEA	Vishay-Dale
R5	1	105 k	RES, 105 k, 1%, 0.1 W, 0603	0603	CRCW0603105KFKEA	Vishay-Dale
R6, R7	2	0	RES, 0 ohm, 5%, 0.1W, 0603	0603	ERJ-3GEY0R00V	Panasonic
TP1, TP6	2	Red	Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
TP2, TP3, TP7	3	Black	Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone

Table 4-1. TPS54202EVM-716 Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
TP4	1	Yellow	Test Point, Miniature, Yellow, TH	Yellow Miniature Testpoint	5004	Keystone
TP5	1	White	Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone
U1	1		4.5-V TO 28-V INPUT, 2-A OUTPUT, EMI FRIENDLY SYNCHRONUOUS STEP-DOWN CONVERTOR, DDC0006A	DDC0006A	TPS54202DDCR	Texas Instruments
C7	0	22 µF	CAP, CERM, 22 µF, 25 V, ±10%, X7R, 1210	1210	GRM32ER71E226KE15L	Murata

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2016) to Revision A (October 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2
• Updated the user's guide title.	2

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Last updated 10/2025