Design Guide: TIDA-050026-23881

24-Port (4 Pair) Power Sourcing Equipment Reference Design for Multiport Applications

Description

This reference design features an evaluation module for the 24-port PSE system which contains a hardware kit, a system firmware image, and a system firmware GUI. The hardware kit consists of a motherboard (PSEMTHR24EVM-081), MSP430 daughtercard (PSEMCUDAUEVM-082) or MSPM0 daughtercard (PSEM0DAUEVM-018), and a PSE daughtercard (TPS23881EVM-083). To evaluate the system (both hardware and software), USB2ANY and MSP-FET adapters are also needed. This guide has been revised to reflect hardware design using the new MSPM0G1107 MCU for multiport PoE systems.

Resources

TIDA-050026-23881	Design Folder
TPS23881EVM-083, PSEMTHR24EVM-081	Tool Folder
PSEMCUDAUEVM-082, PSEM0DAUEVM-018	Tool Folder
TPS23881, MSP430F5234	Product Folder
MSPM0G1107, CSD19538Q3A	Product Folder

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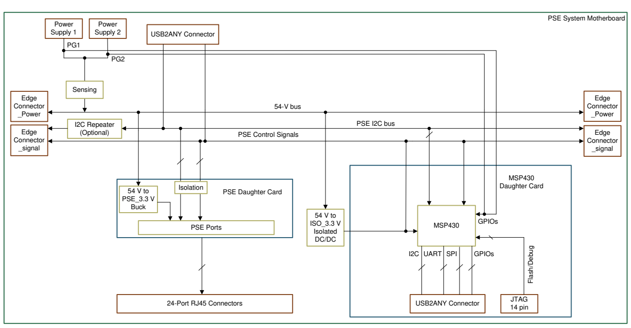


Features

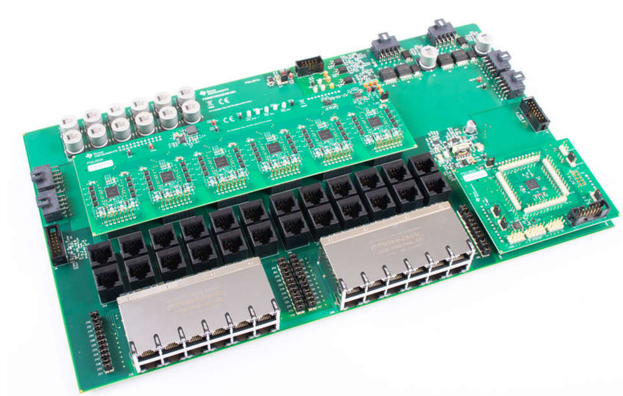
- Onboard power monitoring
- 24 4-pair port system, and expandable to 48 port system
- Highly flexible system with configurable GUI and selectable host interface (I2C or UART)
- Multiport power management
- Multiple power supplies
- Supports legacy powered devices (PDs)

Note

The MSP430F5234 on PSEMCUDAUEVM-082 and the MSPM0G1107 on PSEM0DAUEVM-018 are programmed with pre-production firmware for EVM testing purposes. Follow the instructions in this user's guide to flash the latest firmware from TI.com before evaluation.

Applications

- Campus and branch switches
- Edge router
- Video recorder



1 System Description

This reference design provides a competitive approach to multiport, high-power applications.

In a multiport PSE system, the system-level software is the biggest challenge. The software handles complicated situations and addresses the following challenges:

- The power supply is typically not able to support all ports with a full load due to size and cost constraints. The system software manages the port power with priority to keep the total power consumption below the power budget.
- There are multiple power supplies in the system. These power supplies can be in sharing mode or backup mode. The system software shuts down low-priority ports fast enough to keep the total power consumption below the remaining power budget.
- There are some legacy PD devices that do not present the standard PoE PD signature. The system software finds a way to supply power to these devices.
- System software limits the port power based on the PD class levels or host configuration.
- When there are load-step changes on multiple ports, the system software acts quickly enough to keep the power consumption below the power budget.

1.1 Key System Specifications

Table 1-1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input voltage	44 V–57 V	
Port power limit	2 W–120 W	> 90 W is considered as nonstandard power
Compliance	IEEE 802.3bt Type 3 and Type 4	
PD class level supported	Class 0 to class 8	
Number of power supply supported	1–2	In sharing mode and redundant mode
Max port number supported	48	Referred to RJ45 ports

1.2 Description

This reference design features the TPS23881 daughtercard, the octal channel, the TPS23881 device, and the IEEE802.3bt ready PoE PSE controller. When paired with the PSE motherboard PSEMTHR24-081 (sold separately) and MCU daughtercard PSEMCUDAUEVM-082/PSEM0DAUEVM-018 (sold separately), users can evaluate the TPS23881 device and PSE system firmware solution.

The full PoE evaluation ecosystem includes the following:

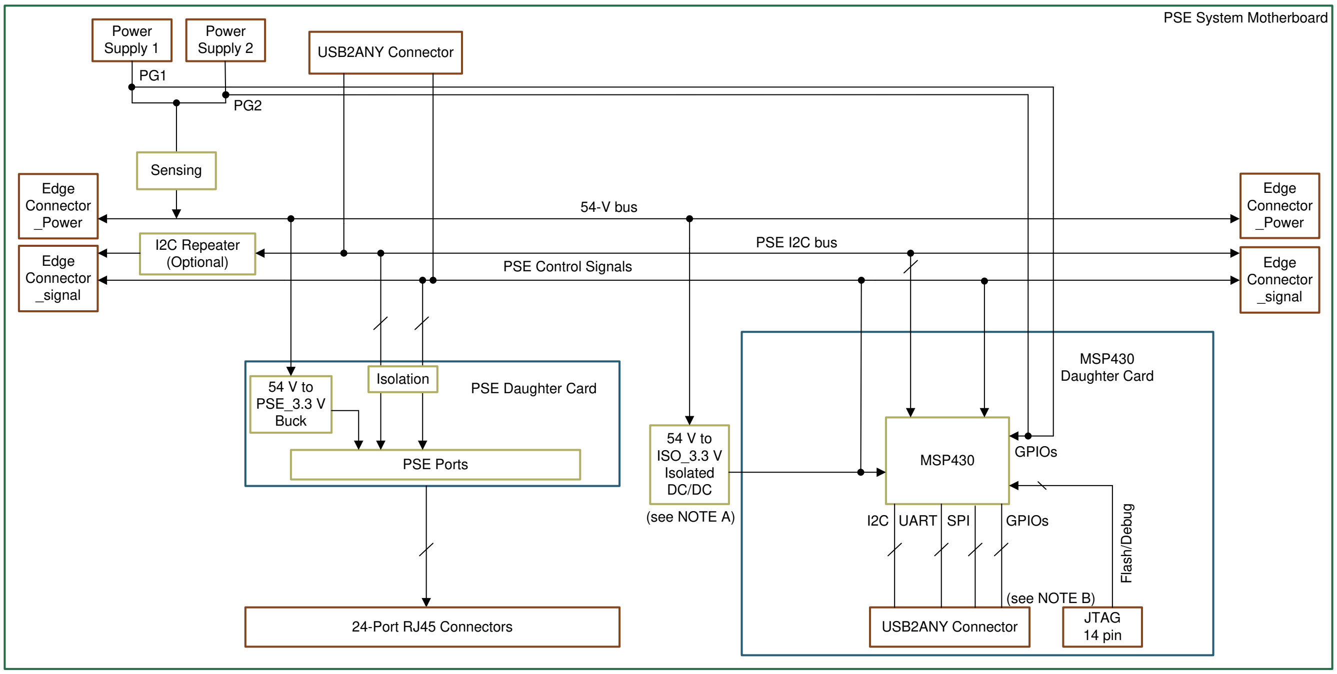
- PSEMTHR24EVM-081: motherboard for 24-port PoE PSE applications (sold separately)
- PSEMCUDAUEVM-082: MSP430 daughtercard for 24-port PoE PSE applications (sold separately)
- PSEM0DAUEVM-018: MSPM0 daughtercard for 24-port PoE PSE applications (sold separately)
- TPS23881EVM-083: TPS23881 daughtercard for 24 port Type 3 and Type 4 PSE applications (sold separately)
- USB2ANY interface adapter: used with the PSE system firmware GUI for I2C/UART interaction with the MCU daughtercard (sold separately)
- MSP-FET programmer: used with UniFlash GUI for programming the MSP430 or MSPM0 device
- PSE system firmware code image (request access through the TIDA-050026-23881 folder or the PSEMCUDAUEVM-082 tool folder)
- PSE system firmware GUI (request access through the TIDA-050026-23881 folder or the PSEMCUDAUEVM-082 tool folder)
- PSE system firmware GUI using MSPM0 access can be requested from the PoE team and accessed here: FirmPSE MSPM0 GUI

Note

The MSP430F5234 on PSEMCUDAUEVM-082 is programmed with pre-production firmware for EVM testing purposes. Follow the instructions in this user's guide to flash the latest firmware from the TIDA-050026-23881 folder or the PSEMCUDAUEVM-082 tool folder before evaluation. Similarly, latest firmware for the MSPM0G1107 on PSEM0DAUEVM-018 can be found from the TIDA-050026-23881 folder.

2 System Overview

2.1 Block Diagram



A. The 54-V to 3.3-V isolated DC/DC is for demonstration purposes only and is not needed in a real system.

B. Only connect a USB2ANY connector or JTAG to avoid GND loops.

Figure 2-1. TIDA-050026-23881 Block Diagram

2.2 Design Considerations

2.2.1 Input Power

2.2.1.1 Vpwr

DC input voltage is provided through J1 and J3. This board supports a dual power source in sharing mode and redundant mode. If the power supplies are in redundant mode, make sure the main power supply is connected to J1 and a backup power supply is connected to the J3 connector.

The minimum PSE port voltage is 44 VDC for Type 1, 50 V for Type 2 and Type 3, and 52 V for Type 4. The maximum DC voltage at VPWR is 57 V for all types. During evaluation, choose the appropriate DC power supply for the different type environment.

2.2.1.2 3.3 V

A local 3.3 V for local devices (labeled as 3.3 V) is provided by the onboard LM5017 buck converter. The LM5017 device provides a basic power-on sequence and provides a well-controlled and consistent start-up to prevent erratic operation. In addition to 44 V to 57 V, the TPS238x requires 3.3 V for the digital circuitry and each TPS2388x device consumes 6-mA typical and 12-mA maximum.

2.2.1.3 3.3 V_ISO

The reference design kit provides galvanic isolation between PoE power side and host side using digital isolators. The host side power is provided by 3.3 V_ISO.

2.2.2 Communication Interface

2.2.2.1 PSE I2C Communication

The motherboard provides two I2C interfaces communicating to PSE:

1. J10 on the motherboard (PSEMTHR24EVM-081) provides I2C access to all PSE devices directly. The TPS2388x GUI can communicate to PSE devices with the USB2ANY interface adapter.
2. J11 and J12 on the motherboard (PSEMTHR24EVM-081) provides I2C access and system control signal to the MCU daughtercard.

2.2.2.2 MCU - Host Communication

The MSP430 daughtercard provides I2C/UART communication port to host through J12 to J14 on MSP430 daughtercard (PSEMCUDAUEVM-082). The MSPM0 daughtercard (PSEM0DAUEVM-018) provides I2C communication to host through J12, J13, and J16. The PSE system GUI provides host configurations to the PSE system

Host interface protocol user's guide can be accessed from the TIDA-050026-23881 folder.

2.2.3 MSP430F523x and MSPM0G1107x Hardware Design

Table 2-1. MSP430 GPIO Pin Assignment

PIN NUMBER MSP430F5234 (48RGZ)	TERMINAL	FUNCTION	COMMENT
COMMUNICATION			
22	P3.0	I2C SDA USCI_B0	I2C to PSEs
23	P3.1	I2C SCL USCI_B0	I2C to PSEs
30	P4.1	I2C SDA USCI_B1	I2C to host
31	P4.2	I2C SCL USCI_B1	I2C to host
33	P4.4	UART TX USCI_A1	UART to host (debug only)
34	P4.5	UART RX USCI_A1	UART to host (debug only)
21	P2.7	SPI CLK USCI_A0	SPI to host (reserved)
24	P3.2	SPI slave TX enable, USCI_A0	SPI to host (reserved)
25	P3.3	UART TX,USCI_A0 or SPI slave in, master out	UART to host TX or SPI to host (reserved)
26	P3.4	UART RX, USCI_A0 or SPI slave out, master in	UART to host RX or SPI to host (reserved)
HARDWARE INTERRUPT			
13	P1.0	PSE INT	Connect to PSE INT pin
16	P1.3	OC Alert	Connect to external current sensing circuit if not used, connect to 3.3 V
18	P1.5	Power supply 1	Connect to power supply 1 power good signal. In RPS mode, P1.5 must be connected to main power supply. **If there is only one power supply, the power good signal must be connected to P1.5.**
19	P1.6	Power supply 2	Connect to power supply 2 power good signal, if not used, connect to GND. In RPS mode, P1.6 must be connected to backup power supply
20	P1.7	Disable all ports	This is for hardware disable ports (reserved)
GENERAL I/O			
4	P5.0	RESET	PSE RESET Connect to PSE RESET pin
17	P1.4	OSS	PSE OSS Connect to PSE OSS pin
46	P6.0	Interrupt pin to host	
35	P4.6	BSL mode indication to host	MCU configures as output. If MCU is in BSL mode, output high. If in normal operation mode, output low.
48	P6.2	Guard-band indication	Need an external LED

Table 2-1. MSP430 GPIO Pin Assignment (continued)

PIN NUMBER MSP430F5234 (48RGZ)	TERMINAL	FUNCTION	COMMENT
47	P6.1	Selection between I2C and SPI, UART	Need to pullup or pulldown
PROGRAM DOWNLOAD AND DEBUG			
44	PJ.3	TCK	JTAG clock input
43	PJ.2	TMS	JTAG state control
42	PJ.1	TDI/TCLK	JTAG data input, TCLK input
41	PJ.0	TDO	JTAG data output
40		TEST/SBWTCK	Enable JTAG pins
45		RSTDVCC/SBWTDIO	External reset
EXTERNAL CRYSTAL			
7	P5.4	XTIN	External low frequency clock (use if needed)
8	P5.5	XTOUT	External low frequency clock (use if needed)

Pre-configure the host interface protocol through hardware as Table 2-2 shows.

Table 2-2. Host Interface Protocol

	P6.1	CS (P3.2)
I2C	high	Don't care
UART	low	low
SPI (CS ActiveLow)	low	high

Table 2-3 shows the MSPM0 GPIO Pin Assignments:

Table 2-3. MSPM0 GPIO Pin Assignments

PIN NUMBER MSPM0G1107 (48RGZ)	TERMINAL	FUNCTION	COMMENT
COMMUNICATION			
31	PA16	I2C SDA Master	I2C1_SDA
30	PA15	I2C SCL Master	I2C1_SCL
1	PA0	I2C SDA Slave	I2C0_SDA
2	PA1	I2C SCL Slave	I2C0_SCL
18	PA10	UART TX (Comm and BSL)	UART0 transmit to host (reserved), Bootstrap loader
19	PA11	UART RX (Comm and BSL)	UART0 receive to host (reserved), Bootstrap loader
29	PA14	UART TX (Debug)	UART3 TX Debug
28	PA13	UART RX (Debug)	UART3 RX Debug
23	PB9	SPI CLK	SPI1 clock signal I/O
20	PB6	SPI slave TX enable	SPI1 chip-select 0
24	PB14	SPI slave in/master out	SPI1 POCI
25	PB15	SPI slave out/master in	SPI1 PICO
HARDWARE INTERRUPT			
13	PA7	PSE INT	Connect to PSE INT pin
16	PA18	OC Alert	Connect to external current sensing circuit if not used, connect to 3.3 V

Table 2-3. MSPM0 GPIO Pin Assignments (continued)

PIN NUMBER MSPM0G1107 (48RGZ)	TERMINAL	FUNCTION	COMMENT
21	PB7	Power supply 1	Connect to power supply 1 power good signal. In RPS mode, PB7 must be connected to main power supply. **If there is only one power supply, the power good signal must be connected to PB7.**
22	PB8	Power supply 2	Connect to power supply 2 power good signal, if not used, connect to GND. In RPS mode, PB8 must be connected to backup power supply
17	PA9	Disable all ports	This is for hardware disable ports (reserved)
32	PA17	I2C Reset	Connect to host GPIO pin to reset I2C module when host I2C fails.
GENERAL I/O			
14	PB2	RESET	PSE RESET Connect to PSE RESET pin
15	PB3	OSS	PSE OSS Connect to PSE OSS pin
46	PA26	Interrupt pin to host	
36	PB17	BSL mode indication to host	MCU configures as output. If MCU is in BSL mode, output high. If in normal operation mode, output low.
33	PA18	BSL Invoke	Input pin used to invoke bootloader
45	P6A25	Guard-band indication	Need an external LED
47	PA27	Selection between I2C and SPI, UART	Need to pullup or pulldown
PROGRAM DOWNLOAD AND DEBUG			
35	PA20	SWCLK	Serial wire debug input clock
34	PA19	SWDIO	Serial wire debug I/O
EXTERNAL CRYSTAL AND POWER			
9	PA3	XTIN	External low frequency clock (use if needed)
10	PA4	XTOUT	External low frequency clock (use if needed)
11	PA5	HFXIN	Extra high frequency clock
12	PA6	HFXOUT	Extra high frequency clock
8		ROSC	Output for high frequency HFXT
7	VSS	M0+ Ground Supply	Refer to MSPM0 datasheet for schematic requirements
6	VDD	M0+ Power Supply	Refer to MSPM0 datasheet for schematic requirements
48	VCORE	M0+ Regulated core power supply output	Refer to MSPM0 datasheet for schematic requirements

2.3 Highlighted Products

2.3.1 TPS23881

The TPS2388x device is the main IC to handle PoE functions to deliver power to PDs through Ethernet cable.

The TPS23881 device is an 8-channel power sourcing equipment (PSE) controller engineered to insert power onto Ethernet cables in accordance with the IEEE 802.3bt (draft) standard. The eight individual power channels can be configured in any combination of 2-pair (1-channel) or 4-pair (2-channels) PoE ports. The PSE controller can detect PDs that have a valid signature, determine the power requirements of the devices according to the classification, and apply power.

Programmable SRAM enables in field firmware upgradability over I2C to provide IEEE compliance and interoperability with the latest PoE enabled devices.

Dedicated per-port ADCs provide continuous port current monitoring and the ability to perform parallel classification measurements for faster port turn on times. A ±2.5%accurate programmable port power limit provides the ability to expand the maximum power sourced to 95 W without exceeding 100 W, and for non-standard applications, the power limit may be set as high as 125 W. The 200-mΩ current sense resistor and external FET architecture allows designs to balance size, efficiency, thermal, and solution cost requirements.

Port remapping and pin-to-pin compatibility with the TPS23880 and TPS2388 devices eases migration from previous generation PSE designs and enables interchangeable 2-layer PCB designs to accommodate different system PoE power configurations.

2.3.2 MSP430F523x and MSPM0G1107x

The TI MSP family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode in 3.5 µs (typical). The MSP430F524x series are microcontroller configurations with four 16-bit timers, a high-performance 10-bit ADC, two USCIs, a hardware multiplier, DMA, a comparator, and an RTC module with alarm capabilities. The MSP430F523x series microcontrollers include all of the peripherals of the MSP430F524x series except for the ADC.

The TI MSPM0G1107 family of ultra-low-power microcontrollers consists of devices featuring a range of peripherals targeted for various applications, including industrial, medical, and consumer electronics. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 32-bit Arm Cortex-M0+ CPU, up to 128KB of flash memory, and up to 32KB of SRAM. The device also includes a range of peripherals, such as two 12-bit ADCs, two I2C interfaces, two SPIs, four UART interfaces, and a real-time clock (RTC) module with alarm capabilities. The MSPM0G1107 family also includes a range of low-power modes, including sleep, stop, and standby modes, which can be used to minimize power consumption. The device is an excellent choice for a range of applications, including industrial control, medical devices, and consumer electronics.

MSP430F523x and MSPM0G1107x are the main controllers to control PSE devices (TPS2388x) through the I2C bus and also communicate to host CPU through I2C or UART to receive configurations and report system status.

2.3.3 ISO1541

The ISO1541 bidirectional isolator is used to isolate I2C signals between PSE devices and the MCU.

The ISO1540 and ISO1541 devices are low-power, bidirectional isolators that are compatible with I2C interfaces. These devices have logic input and output buffers that are separated by TI's *Capacitive Isolation* technology using a silicon dioxide (SiO2) barrier. When used with isolated power supplies, these devices block high voltages, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

2.3.4 ISO7731

The ISO7731 digital isolator is used to isolate control signals (OSS, RESET, INT) between MSP430 and PSE devices.

The ISO773x devices are high-performance, triple channel digital isolators with 5000 V_{RMS} (DW package) and 3000 V_{RMS} (DBQ package) isolation ratings per UL 1577.

This family of devices has reinforced insulation ratings according to VDE, CSA, TUV, and CQC.

The ISO773x family of devices provides high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO2) insulation barrier. This device comes with enable pins which can be used to put the respective outputs in high impedance for multi-master driving applications and to reduce power consumption. The ISO7730 device has all three channels in the same direction and the ISO7731 device has two forward and one reverse-direction channel. If the input power or signal is lost, the default output is high for devices without suffix F and low for devices with suffix F. See the device *Functional Modes* section for further details.

Used in conjunction with isolated power supplies, this device helps prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through remarkable chip design and layout techniques, electromagnetic compatibility of the ISO773x device is significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance.

2.3.5 CSD19538

This 100-V, 49-mΩ, SON 3.3-mm × 3.3-mm NexFET™ power MOSFET is designed to minimize conduction losses and reduce the board footprint in PoE applications.

2.3.6 LM5017

The LM5017 device is used to generate 3.3 V to supply PSE devices.

The LM5017 is a 100-V, 600-mA synchronous step-down regulator with integrated high-side and low-side MOSFETs. The constant on-time (COT) control scheme employed in the LM5017 device requires no loop compensation, provides excellent transient response, and enables very high step-down ratios. The on-time varies inversely with the input voltage resulting in nearly constant frequency over the input voltage range. A high-voltage start-up regulator provides bias power for internal operation of the IC and for integrated gate drivers. A peak current limit circuit protects against overload conditions. The undervoltage lockout (UVLO) circuit allows the input undervoltage threshold and hysteresis to be independently programmed. Other protection features include thermal shutdown and bias supply undervoltage lockout (VCC UVLO).

2.3.7 LM5020

The LM5020 device is used to generate isolated LM5020 to supply MSP430 and isolators.

The LM5020 high-voltage pulse-width modulation (PWM) controller contains all of the features needed to implement single-ended primary power converter topologies. Output voltage regulation is based on current-mode control, which eases the design of loop compensation while providing inherent line feed-forward. The LM5020 device includes a high-voltage start-up regulator that operates over a wide-input range up to 100 V. The PWM controller is designed for high-speed capability including an oscillator frequency range to 1 MHz and total propagation delays less than 100 ns. Additional features include an error amplifier, precision reference, line undervoltage lockout, cycle-by-cycle current limit, slope compensation, soft start, oscillator synchronization capability and thermal shutdown.

2.3.8 LM5050

The LM5050 device is used to support 2 power supplies in the system to work in backup mode.

The LM5050-1 and LM5050-1-Q1 high-side ORing FET controller operates in conjunction with an external MOSFET as an ideal diode rectifier when connected in series with a power source. This ORing controller allows MOSFETs to replace diode rectifiers in power distribution networks thus reducing both power loss and voltage drops.

The LM5050-1 and LM5050-1-Q1 controllers provide charge pump MOSFET gate drive for an external N-channel MOSFET and a fast response comparator to turn off the FET when current flows in the reverse direction. The LM5050-1 and LM5050-1-Q1 devices can connect power supplies ranging from 5 V to 75 V and can withstand transients up to 100 V.

2.3.9 INA240

The INA240 amplifier is used to measure the total current from the input to support fast shutdown in an event of load step change.

The INA240 device is a voltage-output, current-sense amplifier with enhanced PWM rejection that can sense drops across shunt resistors over a wide common-mode voltage range from –4 V to 80 V, independent of the supply voltage. The negative common-mode voltage allows the device to operate below ground, accommodating the flyback period of typical solenoid applications. Enhanced PWM rejection provides high levels of suppression for large common-mode transients ($\Delta V/\Delta t$) in systems that use PWM signals (such as motor drives and solenoid control systems). This feature allows for accurate current measurements without large transients and associated recovery ripple on the output voltage. This device operates from a single 2.7-V to 5.5-V power supply, drawing a maximum of 2.4 mA of supply current. Four fixed gains are available: 20 V/V, 50 V/V, 100 V/V, and 200 V/V. The low offset of the zero-drift architecture enables current sensing with maximum drops across the shunt as low as 10-mV full-scale.

2.3.10 REF3425

The REF3425 device is used to provide a threshold to output the INA240 and generate a signal to MCU for overcurrent alert.

The REF34xx device is a low temperature drift (6 ppm/°C), low-power, high-precision CMOS voltage reference, featuring ±0.05% initial accuracy, low operating current with power consumption less than 95 µA. This device also offers very low output noise of 3.8 µVp-p/V, which enables the ability of the device to maintain high signal integrity with high-resolution data converters in noise critical systems. With a small SOT-23 package, the REF34xx offers enhanced specifications and pin-to-pin replacement for MAX607x and ADR34xx. The REF34xx family is compatible to most of the ADC and DAC such as the ADS1287, ADUCM360, and ADS1112 devices. Stability and system reliability are further improved by the low output-voltage hysteresis of the device and low long-term output voltage drift. Furthermore, the small size and low operating current of the devices (95 µA) can benefit portable and battery-powered applications.

2.3.11 TPS3890

The TPS3890 device is used to monitor the existence of the power supply and generate power good signal to MCU. The MCU can adjust the total power budget of the system.

The TPS3890 device is a precision voltage supervisor with low-quiescent current that monitors system voltages as low as 1.15 V, asserting an open-drain RESET signal when the SENSE voltage drops below a preset threshold or when the manual reset (MR) pin drops to a logic low. The RESET output remains low for the user-adjustable delay time after the SENSE voltage and manual reset (MR) return above the respective thresholds. The TPS3890 family uses a precision reference to achieve 1% threshold accuracy. The reset delay time can be user-adjusted between 40 µs and 30 s by connecting the CT pin to an external capacitor. The TPS3890 device has a very low quiescent current of 2.1 µA and is available in a small 1.5-mm × 1.5-mm package, making the device well-suited for battery-powered and space-constrained applications.

3 Hardware, Software, Testing Requirement and Test Result

3.1 Required Hardware and Software

3.1.1 Hardware

The following hardware is required to get started with the reference design:

- PSEMTHR24EVM-081: motherboard for 24 port PoE PSE applications (sold separately)
- PSEMCUDAUEVM-082: MSP430 daughtercard for 24 Port PoE PSE applications (sold separately)
- PSEM0DAUEVM-018: MSPM0 daughtercard for 24 Port PoE PSE applications (sold separately)
- TPS23881EVM-083: TPS23881 daughtercard for 24-port Type 3 and Type 4 PSE PoE PSE applications (sold separately)
- USB2ANY interface adapter: used with PSE system firmware GUI for I2C/UART interaction with MCU daughtercard (sold separately)
- MSP-FET programmer: used with the UniFlash GUI for programming the MSP430 device

3.1.2 Software

- FirmPSE code image (request access to the code image through the TIDA-050026-23881 folder ,PSEM0DAUEVM-018 tool folder, or PSEMCUDAUEVM-082 tool folder)
- FirmPSE GUI MSP430 (request access to the GUI through the TIDA-050026-23881 folder or the PSEMCUDAUEVM-082 tool folder)
- FirmPSE GUI MSPM0 (reach out to TI PoE team member for access request, and access GUI here)

3.2 Testing and Results

3.2.1 Test Setup

3.2.1.1 Hardware Setup

Figure 3-1 shows the hardware test setup of the ecosystem.

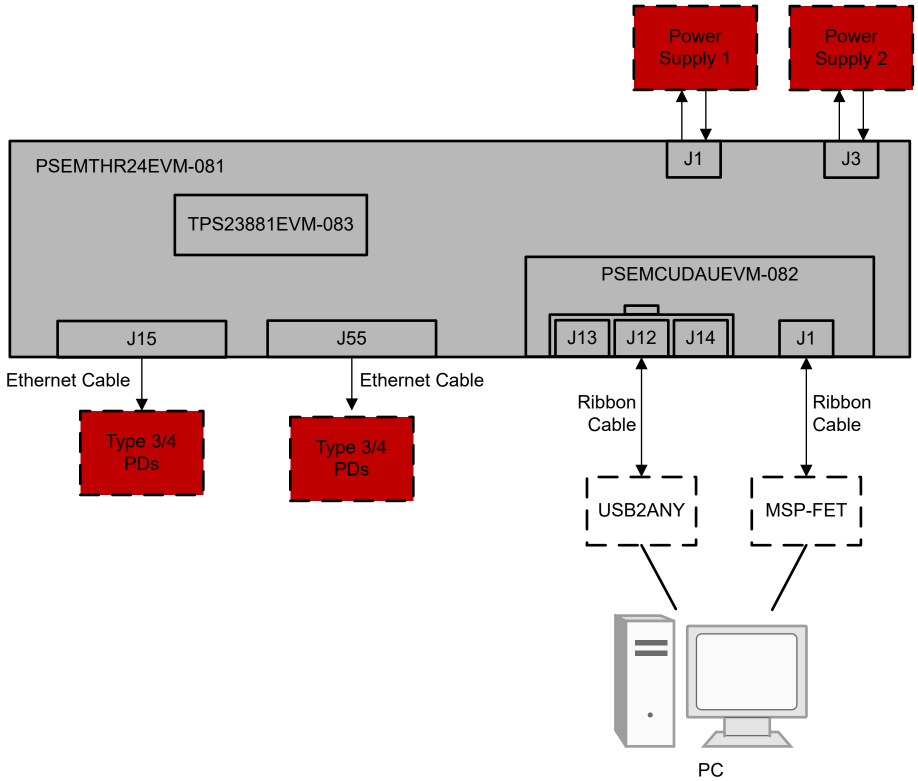


Figure 3-1. Ecosystem Setup

Note

A 30-pin ribbon cable is required to enable the full features of PSE system firmware GUI.

3.2.1.2 LED, Test Point, Jumper and Connector Settings

3.2.1.2.1 EVM LEDs

Table 3-1 lists the EVM LEDs and the LED descriptions.

Table 3-1. EVM LEDs

LED	COLOR	DESCRIPTION
PSEMTHR24EVM-081		
J15, J55	Green, Yellow	There is one green and yellow LED on each RJ45 port
PSEMCUDAUEVM-082		
D1	Green	The total power consumption remains within the pre-configured guardband limits
PSEM0DAUEVM-018		
D1	Green	The total power consumption remains within the pre-configured guardband limits.

3.2.1.2.2 EVM Test Points

Table 3-2 lists the EVM test points.

Table 3-2. EVM Test Points

TP	LABEL	DESCRIPTION
PSEMTHR24EVM-081		
TP1	55VDC	VPWR
TP2	GND	VPWR ground
TP3	OC-ALERT	System over current alert signal
TP4	SDA	I2C data
TP5	SCL	I2C clock
TP6	PG1	Power good signal for power supply #1
TP7	PG2	Power good signal for power supply #2
TP8	PSE_3.3V	3.3 V for PSE devices
TP9	GND	PSE_3.3V ground
TP10	3.3V_ISO	Isolated 3.3 V for MSP430
TP11	3.3V	3.3 V for debug
TPS12 , TP13	GND_ISO	3.3V_ISO ground
TP14	OSS	OSS signal from MCU to PSE
TPS23881EM-083		
TP1	VPWR	VPWR
TP2	PSE_3.3	3.3 V for PSE devices
TP3, TP4, TP14, TP18	GND	VPWR and PSE_3.3V ground
TP5	RESET	Reset signal from MCU
TP6	OSS	OSS signal from MCU
TP7	INT	INT signal to MCU
TP8	SCL	I2C clock from MCU
TP9	SDA	I2C data from and to MCU
TP10	3.3V_ISO	Isolated 3.3 V
TP11	PSE_RST	Reset signal to PSE
TP12	PSE_OSS	OSS signal to PSE
TP13	PSE_INT	INT signal from PSE
TP15	GND_ISO	3.3V_ISO ground
TP16	PSE_SDA	I2C data from or to PSE
TP17	PSE_SCL	I2C clock to PSE

3.2.1.2.3 EVM Jumpers

Table 3-3 lists the EVM test jumpers and descriptions.

Table 3-3. EVM Test Jumpers

JUMPER	DEFAULT PIN POSITION	DESCRIPTION
PSEMTHR24EVM-081		
J13	1-2	3.3 V comes from PSE daughtercard
J14	1-2	Connect 3.3V_ISO to supply the circuit
J17, J22, J38, J43, J19, J23, J32, J28, J52, J47, J31, J26	1-2	Enable port LED
J45, J42, J24, J21, J44, J49, J53, J30, J33, J51, J54	1-2	Enable port LED
J57, J62, J78, J83, J59, J63, J72, J68, J92, J87, J71, J66	1-2	Enable port LED
J85, J82, J64, J61, J84, J80, J89, J93, J70, J91, J94	1-2	Enable port LED

3.2.1.2.4 EVM Input and Output Connectors

Table 3-4 lists the EVM input and output connectors.

Table 3-4. EVM Input and Output Connectors

CONNECTOR	DESCRIPTION
PSEMTHR24EVM-081	
J1, J3	DC power supply input (44–57 V VDC, 41 A)
J2, J4, J6, J7	Edge connector for DC bus when connecting 2 boards together
J5	Power to PSE daughtercard
J8, J9	Edge connector for PSE signals (I2C, OSS, RESET and INT) when connecting 2 boards together
J10	Connector to USB2ANY for direct I2C access to PSE devices (for debug purpose only)
J11	Connectors to PSE daughter for PSE signals (I2C, OSS, RESET and INT)
J12	Connectors to MSP430 daughter for PSE signals (I2C, OSS, RESET and INT), system level signals (OC-ALERT, PG) and isolated 3.3 V
J15, J55	PSE ports magjacks
J34, J35, J36, J74, J75, J76	PSE port connector to PSE daughtercard
J95, J96	For MSP430 daughtercard mechanical mounting purpose
TPS23881EVM-083	
J1	Pair with J5 on motherboard
J4	Pair with J11 on motherboard
J5	Pair with J34, J35, J36, J74, J75, J76 on motherboard
PSEMCUDAUEVM-082	
J1	JTAG connector
J3, J7, J8, J9	Extended GPIO access
J11	Pair with J12 on motherboard
J12, J13, J14	USB2ANY connector (30 pin)
J17, J18	For MSP430 daughtercard mechanical mounting purpose
PSEM0DAUEVM-018	
J3, J4, J6, J10	Extended GPIO access
J9	Pair with J12 on motherboard
J12, J13, J14	USB2ANY connector (30 pin)
J11, J15	For MSP430 daughtercard mechanical mounting purpose

3.2.1.3 System Firmware GUI Setup

3.2.1.3.1 PSE System Firmware GUI Installation

TI's PSE system firmware GUI is used with the PSE system EVM kit (PSEMTHR24EVM-081, PSEMCUDAUEVM-082/PSEM0DAUEVM-018, TPS23881EVM-083) to configure the system, generate the code image and flash to MSPM0/MSP430 device. Download the PSE system firmware GUI from the TIDA-050026-23881 folder or the PSEMCUDAUEVM-082 tool folder.

3.2.1.3.2 PSE System Firmware GUI Operation

Start the PSE system firmware GUI by double clicking the GUI icon and clicking the start button. A window similar to Figure 3-2 comes up. Offline mode is selected by default.

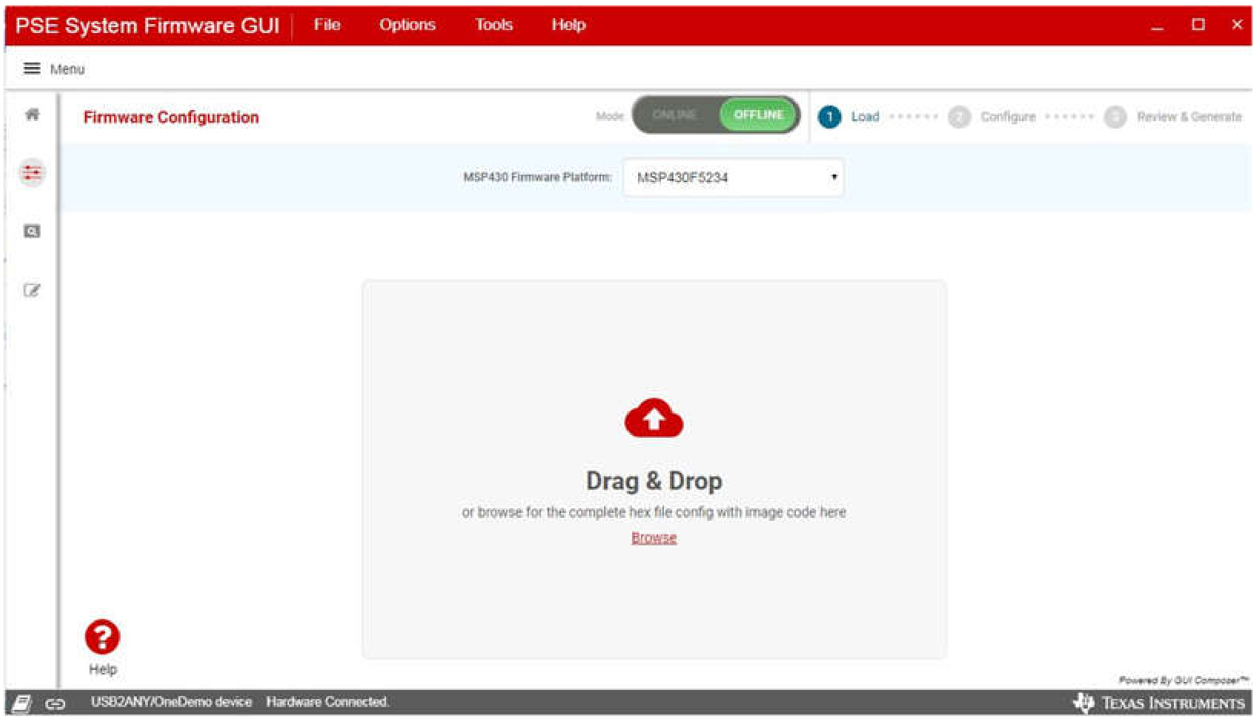


Figure 3-2. GUI Start-Up

Select the MSPM0/MSP430 device you want to start with and then load the PSE system firmware code image (request from the TIDA-050026-23881 folder , PSEM0DAUEVM-018 tool folder, or the PSEMCUDAUEVM-082 tool folder). Once finished, click *Proceed* to go to the configuration page.

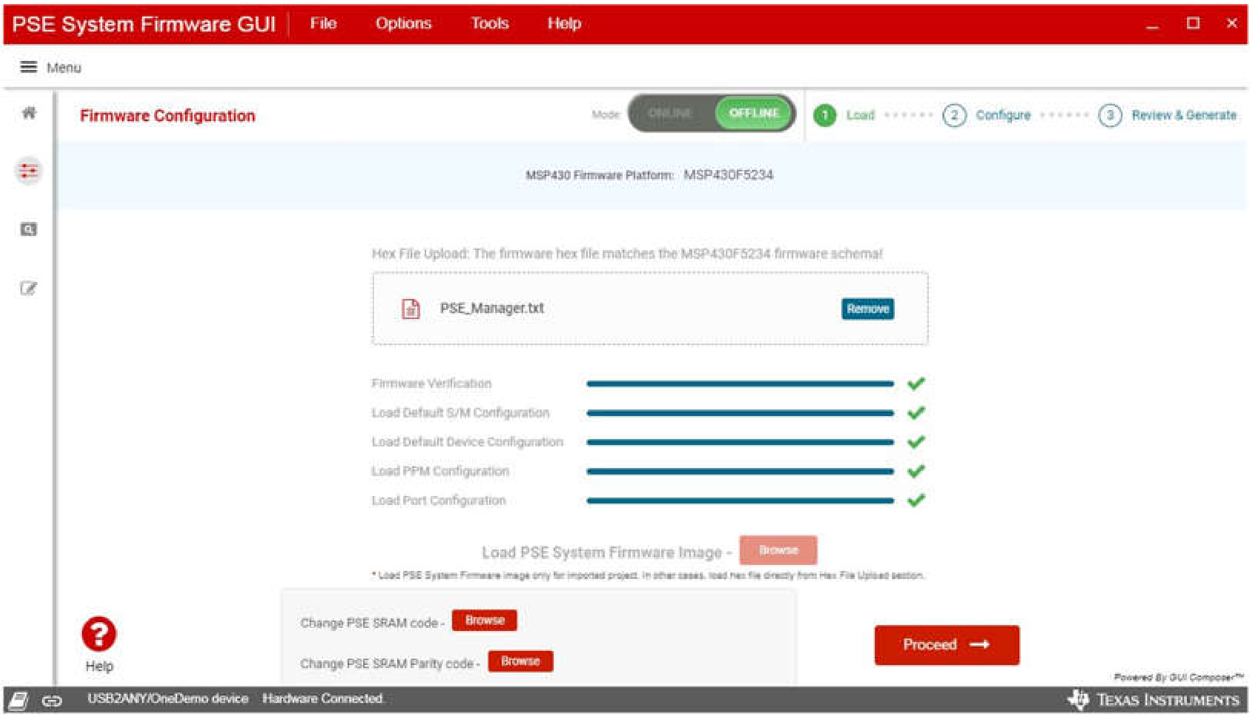


Figure 3-3. GUI Device Selection and Image Load

The configurations are split into 4 sections: system configuration, PPM (Port Power Management) configuration, device configuration, and port configuration.

The system configuration is applied to the whole system. This tab is always available on the right side of the GUI. The following parameters can be configured through the system configuration tab:

- Legacy detection functions

  Legacy devices released prior to the PoE standard can be powered through the Ethernet cable. The PSE system firmware detects these legacy PDs and powers on with protection.
- Use of external sensing circuit

  The external sensing circuit is used to measure the total power consumption of the system. Once the current exceeds the power budget, the MCU shuts down low priority ports. This increases the system response to the load step change.
- System boot-up setting
  1. Turn on the PSE port as soon as the power is up.
  2. Turn on the PSE port after the PoE enable command is sent from the host
- Port overload retry mode
  1. Re-enable immediately: after overload happens, the port is re-enabled immediately. If the overload still presents, re-enable occurs at most 5 times and shuts down the port if the overload is not removed within 5 retries. The port is re-enabled after the PD is removed from the port and reconnects to the port.
  2. Re-enable after PD is disconnected and connected: after overload happens, the port is disabled immediately and is re-enabled after the PD is removed from the port and reconnects to the port.
  3. Timer controlled: the port is re-enabled immediately after overload happens. The port keeps retrying for a period (controller by timer) and is disabled after the timer expires. The port is re-enabled after the PD is removed from the port and reconnects to the port.

- OSS signal source (from MCU or CPLD):In a multipower supply system, when one power supply has faults and the remaining power supply is not able to supply the current power consumption, turn off low priority ports to protect the remaining power supply. The OSS function of the PSE is used to fast shutdown the low priority ports. There are 2 sources to generate the OSS signal:
  1. MSPM0/MSP430 generates the OSS signal
  2. CPLD generates the OSS signal
- Interrupt mask

  The interrupt mask in Figure 3-4 can be configured to enable interrupt events to notify the host through the MSP430 P6.0 or MSPM0 PA26.

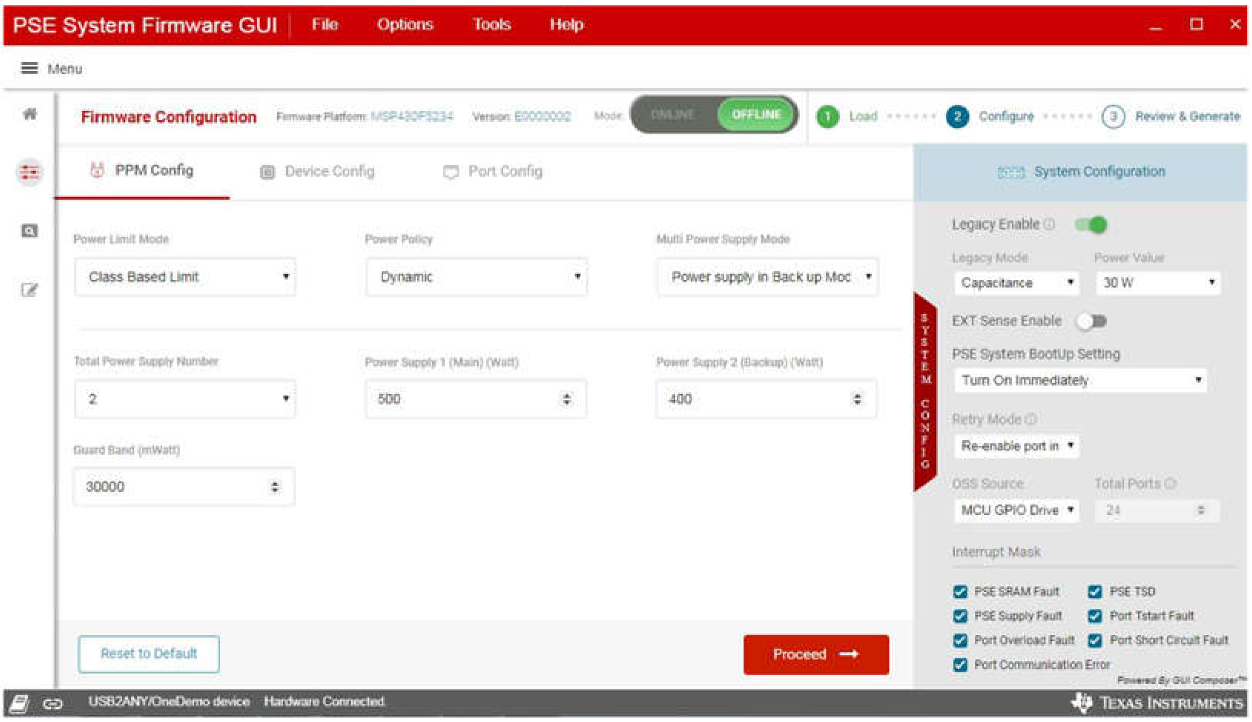


Figure 3-4. GUI System Configuration and PPM Configuration

PPM configuration is applied to the port power management mechanism. The following parameters can be configured through the PPM configuration tab:

- Power limit mode: class limit mode and port limit mode
  - Class limit mode: in class limit mode, the port power is limited by the class level of the PD. For example, if the PD is class 8, the port power limit (PCUT) is set to 90 W.
  - Port limit mode: in port limit mode, the port power is limited by the host. The host must set port power limit before the port is powered on.
- Power policy:static and dynamic mode
  - Static mode: in static mode, the port power allocation is set to port power limit. So in class limit mode, port power allocation is class level power of the PD and in port limit mode, the port power allocation is the port power limit configured from the host.
  - Dynamic mode: in dynamic mode, the port power allocation equals to the actual consumed power of the port. This mode allocates the unused power of the port to other ports.
- Multipower supply mode: RPS and sharing mode:
  - Redundant power supply (RPS) mode: in RPS mode, the total power budget equals to the power budget of the main power supply when both main power supply and backup power supply are connected. The total power budget equals to backup the power budget of the power supply when the main power supply is disconnected.

  - Sharing power supply mode: in sharing mode, the total power budget equals to the sum of the power budget of the two power supplies when both power supplies are connected. The total power budget equals to the remaining power budget of the power supply if one of the power supplies is disconnected.
- Total number of power supplies and the power budget of each power supply. **If there is only one power supply, the power good signal must be connected to P1.5 on MSP430 or PB7 on MSPM0.**
- Power guard band: when the total allocated power < total power budget - guard band, there is no more low priority ports to be turned on and the guard band LED turns on.

Device configuration is mainly used to configure the mapping between the PSE device channels and the logical RJ45 ports. When mapping a 4-pair port, only channels within the same quad (channel 1–4 or channel 5–8) can be mapped to one 4-pair port.

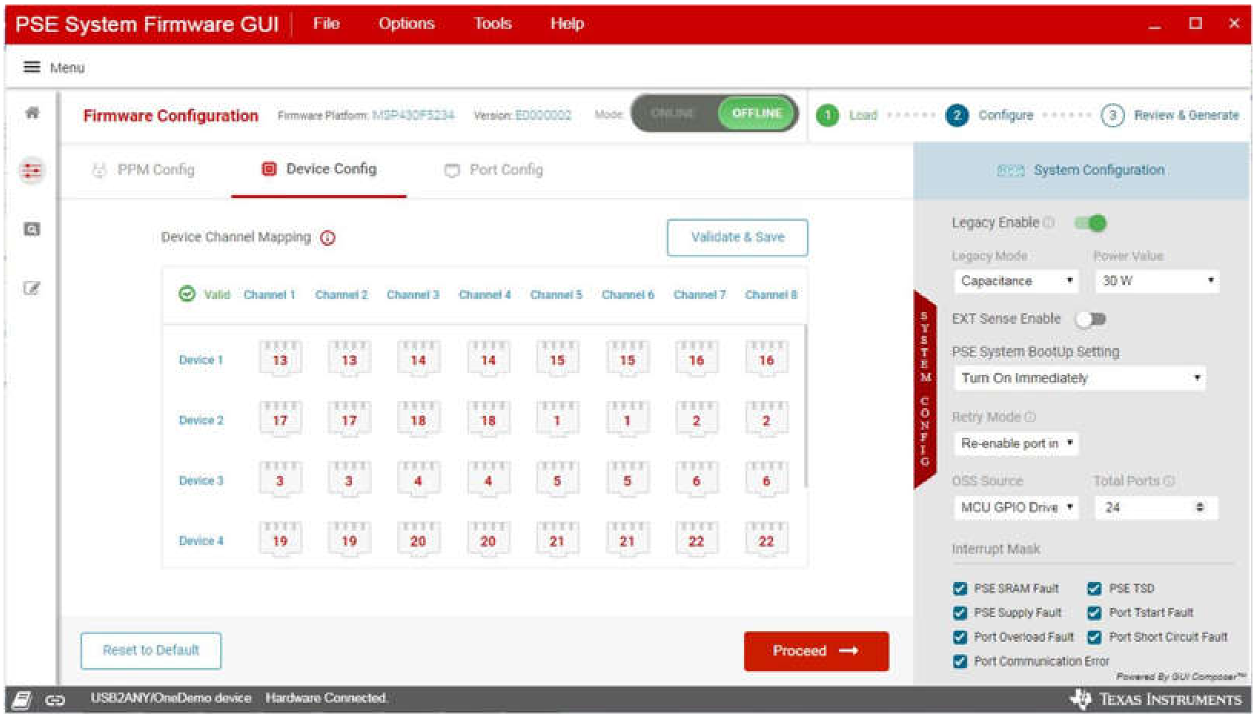


Figure 3-5. GUI Device Configuration

The *Port Configuration* is applied to the port by port settings, such as port PoE enable and disable, port priority, and port power limit (only in port limit mode).

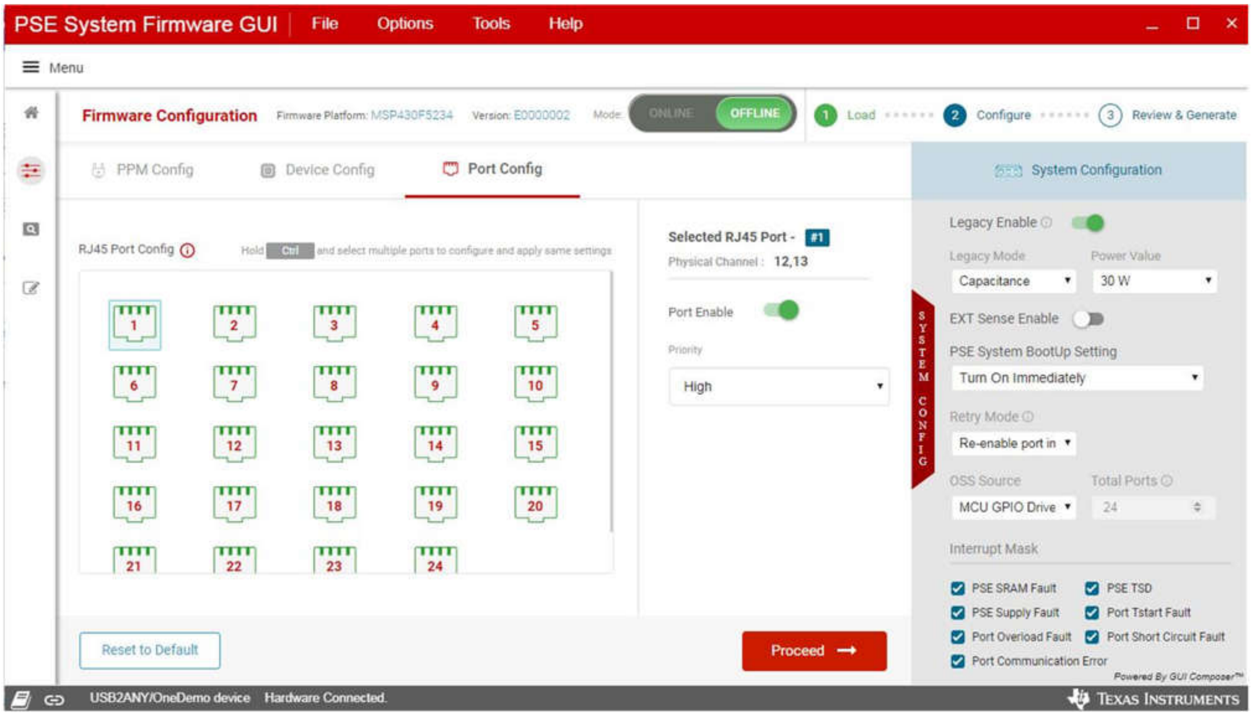


Figure 3-6. GUI Port Configuration

Once everything is configured, click the *Proceed* button. The summary page shows all the configurations being set compared to the factory default configurations. Once everything is verified, you can generate the hex file or flash the code to the MSPM0/MSP430 device directly.

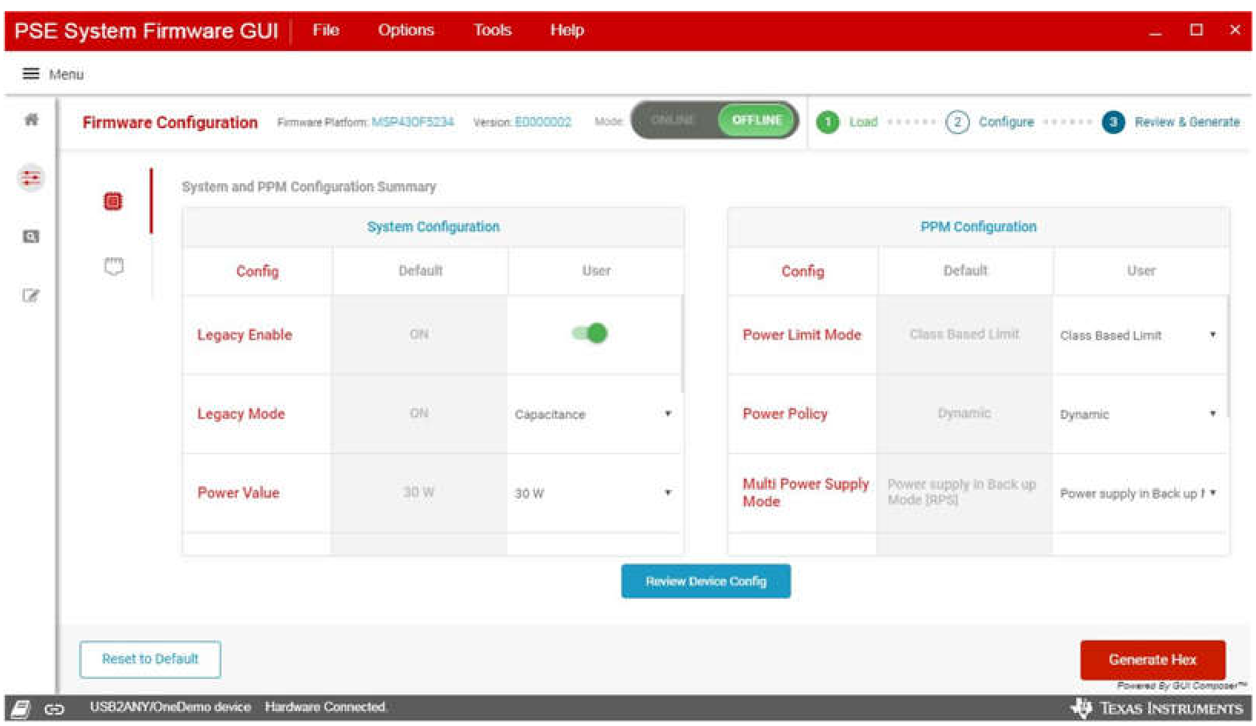


Figure 3-7. GUI Configuration Summary

Once configurations are reviewed, the GUI can generate the default code image and program the device directly through **MSP-FET**.

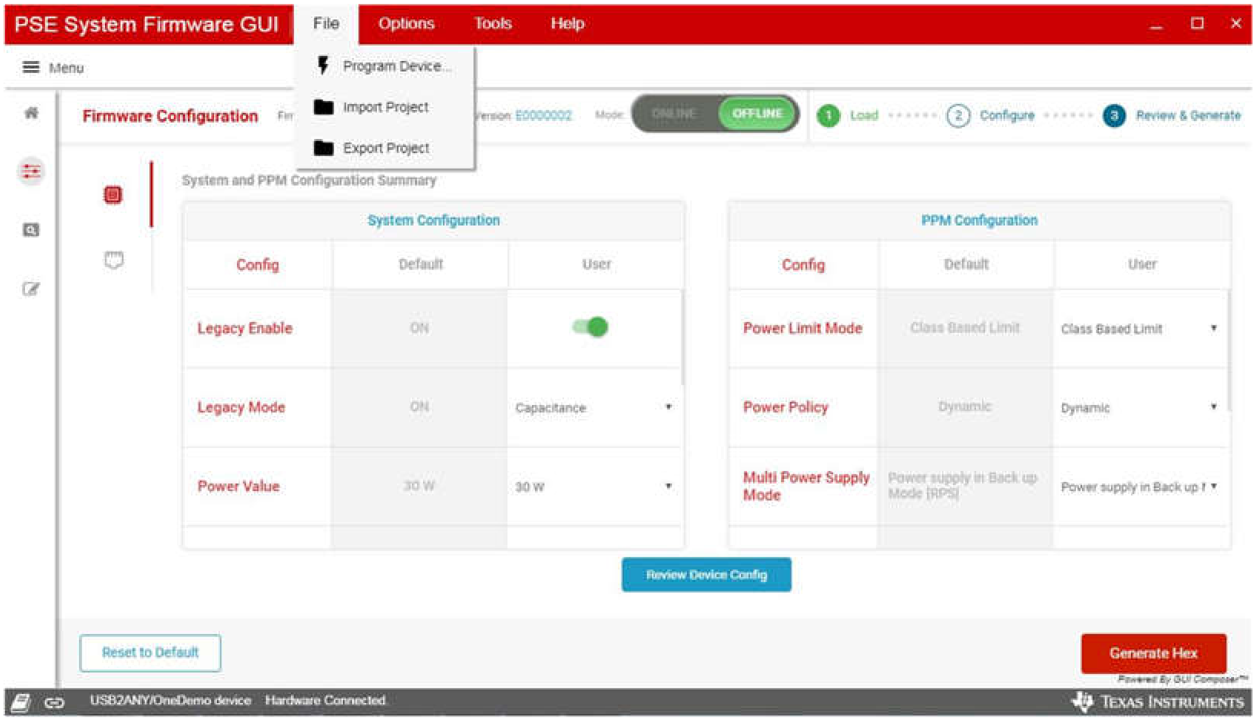


Figure 3-8. GUI Program Device and Generate Hex

Once the code is successfully flashed to the MCU, the system is up and running. The MSP-FET can be disconnected from the laptop or PC. Connect the USB2ANY (with 30-pin ribbon cable) to a laptop or PC and the GUI is in online mode after selecting the host interface protocol.

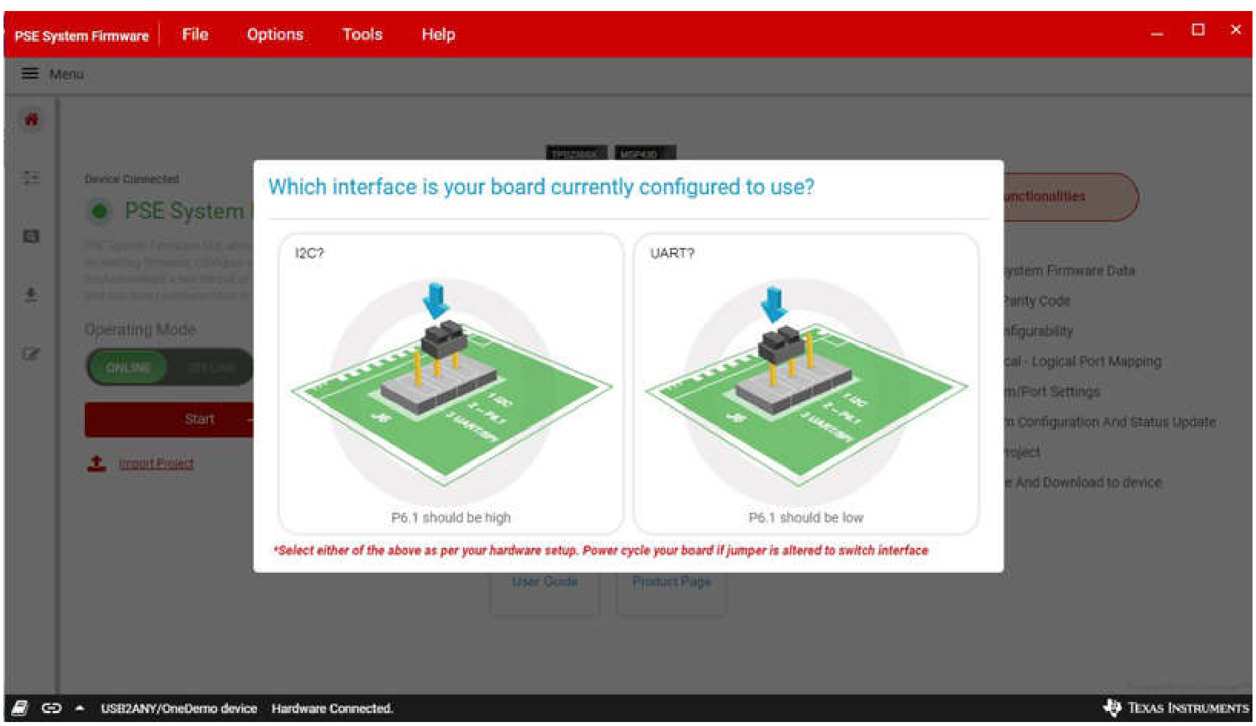


Figure 3-9. Host Interface Protocol Selection in Online Mode

Once the device is connected to the GUI, real time changes can be made on the configuration page and status page shows the real time system status. The status page shows the system, device, and port real-time status. The user can also change the system configuration in the configuration page: each change is converted to a host command to the MCU. The user can also press the *Save Configuration* button to save the current configuration as the default setting.

Note

For the FirmPSE MSPM0 GUI, the Host Interface Protocol selection only shows the I2C choice, as MSPM0 does not support UART at the moment.

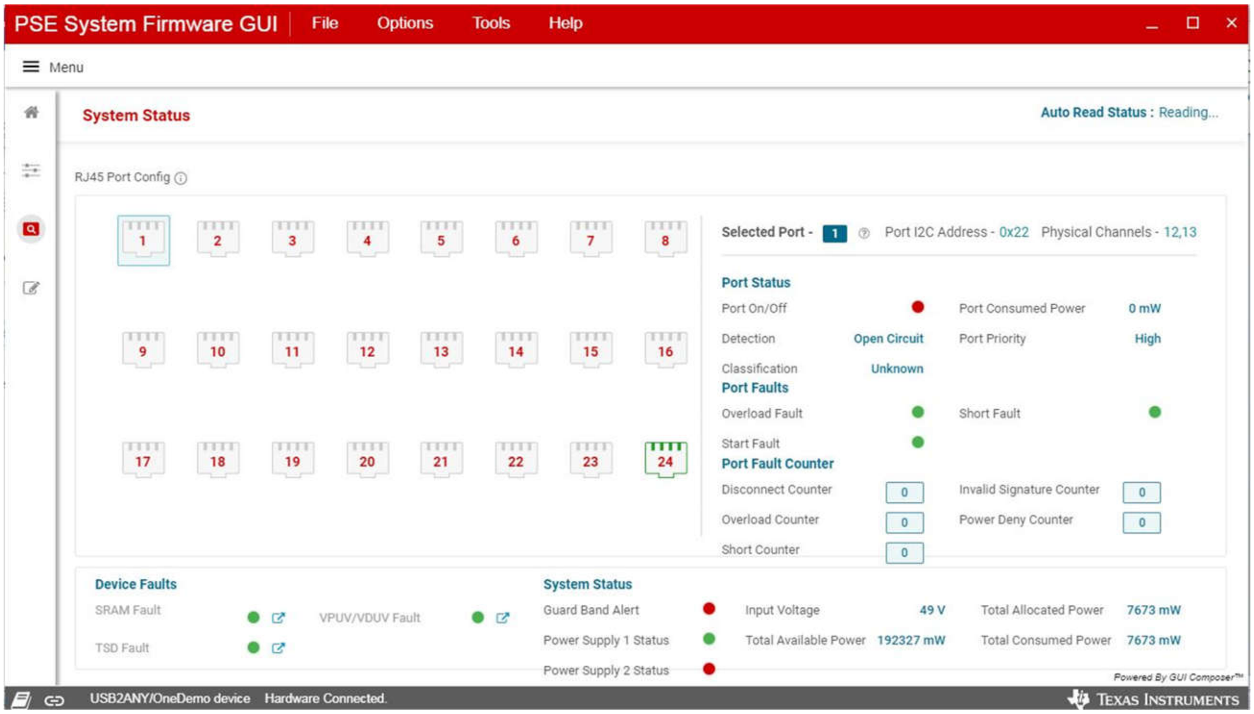


Figure 3-10. GUI Status Page

The BSL firmware update page provides the field firmware upgrade functions where the firmware can be upgraded through the same I2C or UART port as the normal communication. This is beneficial to firmware upgrade after the product is released to customers.

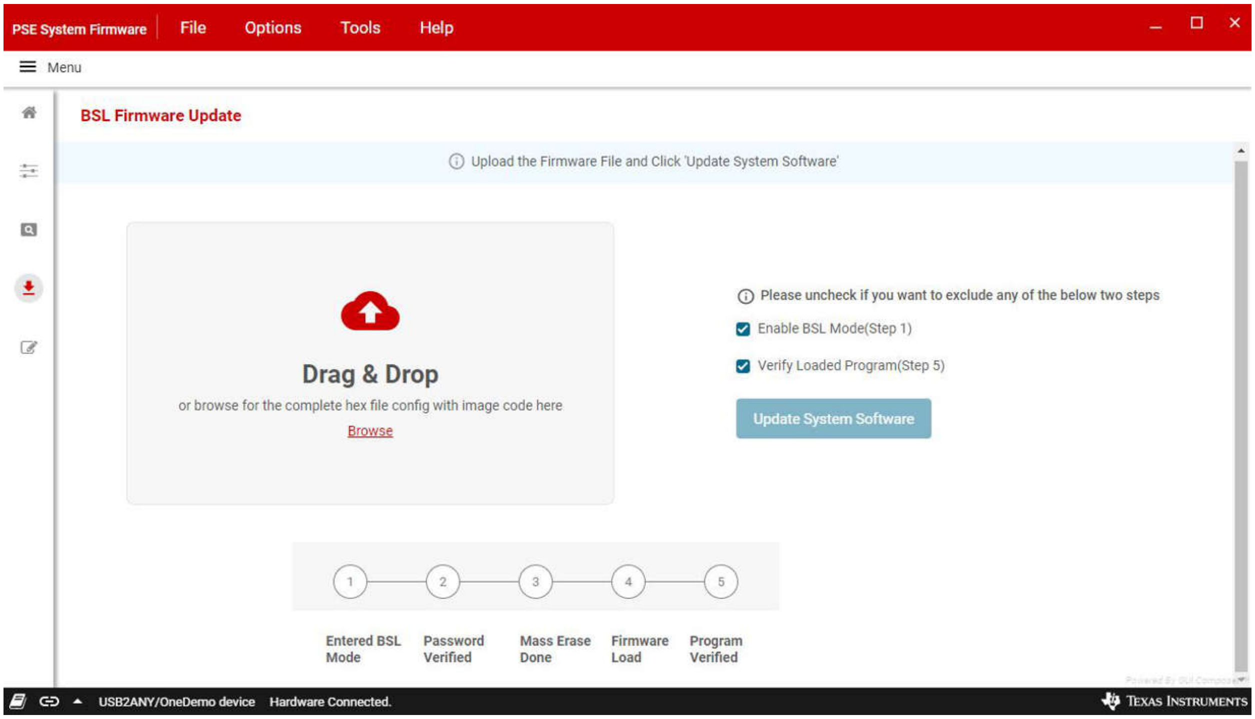


Figure 3-11. BSL Firmware Update Page

Before using the BSL page to update the MCU firmware, BSL code must be flashed to the MCU if it is not flashed. Download UniFlash from ti.com and use it to flash the BSL code with the following steps:

1. Select the MCU device to MSP430F5234/MSPM0G1107

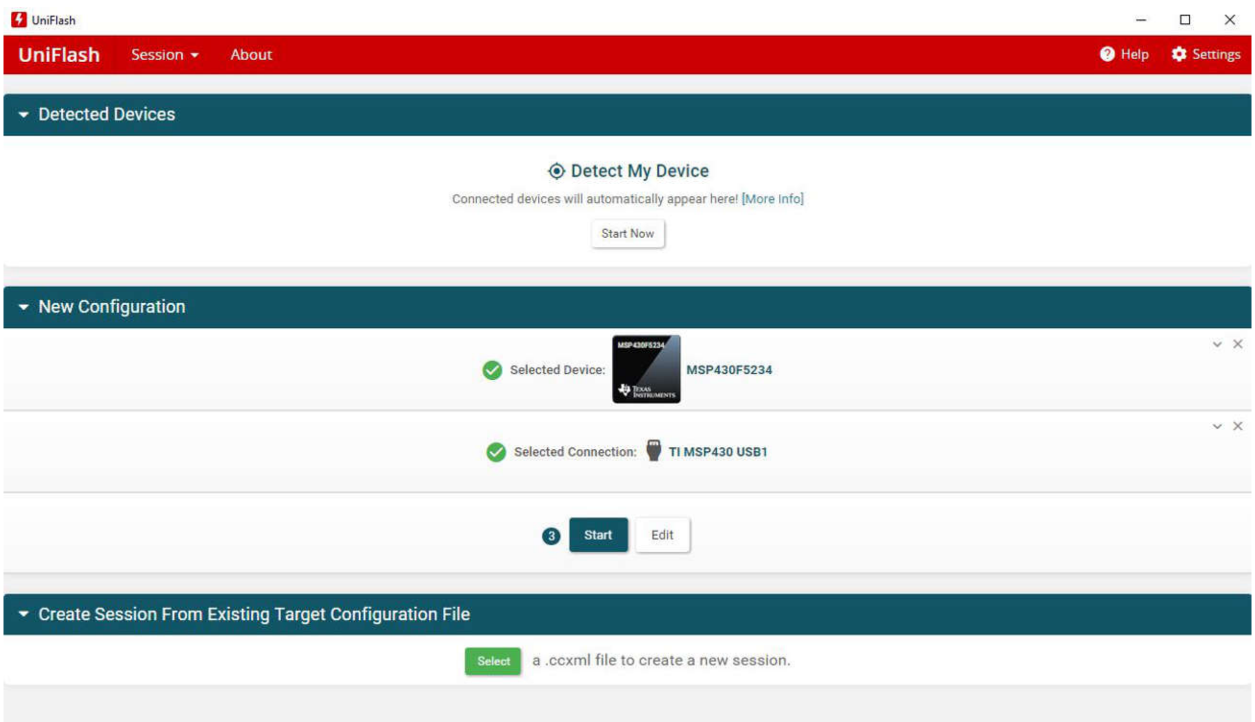


Figure 3-12. MCU Device Selection Page

2. Configure the flash section.

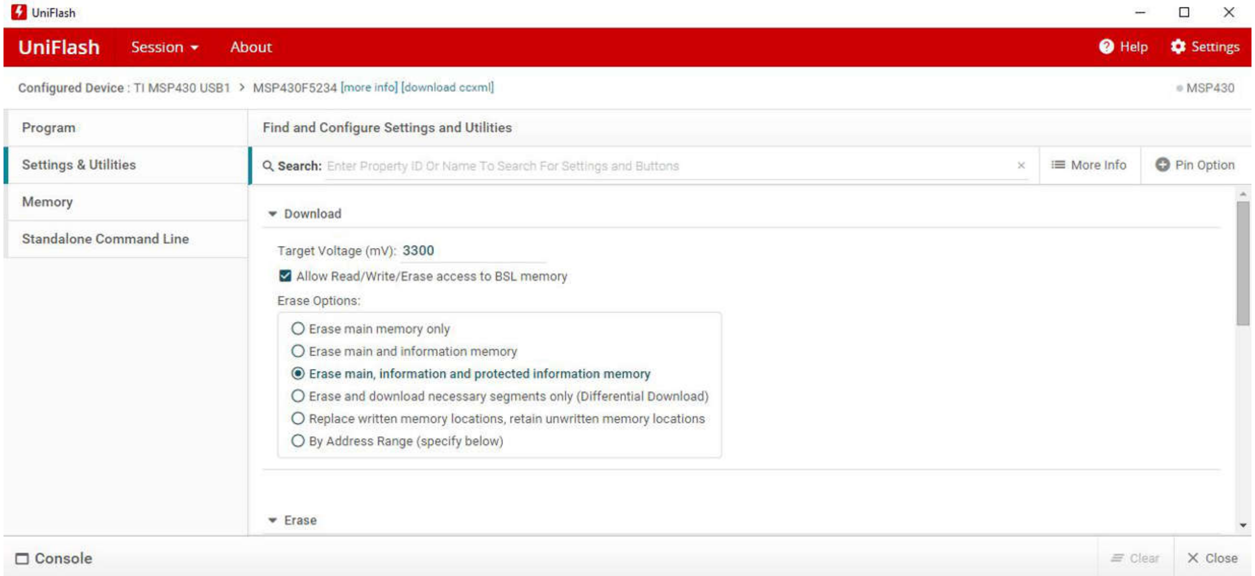


Figure 3-13. Configure Settings and Utilities Page

3. Load BSL code and flash to the MCU.

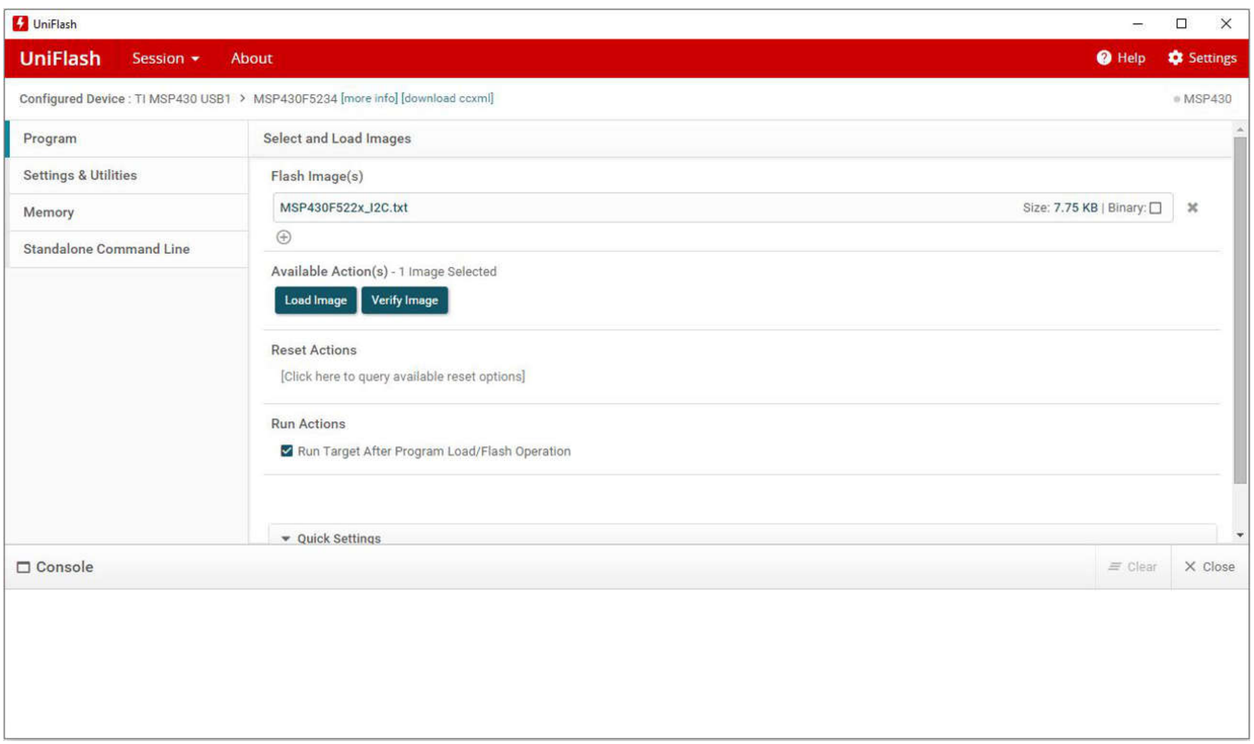


Figure 3-14. Select and Load Images Page

4. In the debug page, user can read and write raw data to the MCU following host interface protocol and to each PSE device's registers by providing I2C address and register number. The password is "C430".

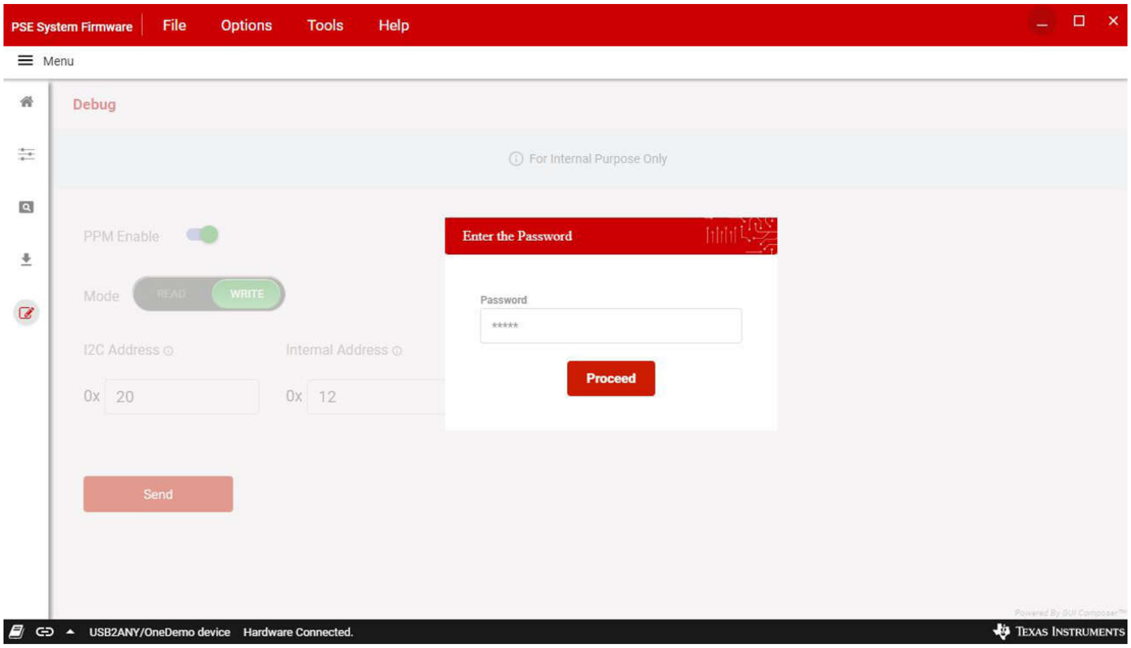


Figure 3-15. Debug Page

3.2.2 Test Results

The IEEE 802.3bt compliance test suite is not available now. The test report will be added once available.

4 Design and Documentation Support

4.1 Design Files

4.1.1 Schematic

To download the schematics, see the design files at TIDA-050026-23881.

4.1.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-050026-23881.

4.1.3 PCB Layout Recommendations

KSENSA is shared between SEN1 and SEN2, KSENSB is shared between SEN3 and SEN4, KSENSEC is shared between SEN5 and SEN6, KSENSED is shared between SEN7 and SEN8. To optimize the accuracy of the measurement, the PCB layout must be done carefully to minimize the impact of PCB trace resistance. For an example, see the *Layout* section of the *TPS23881 Type-4 4-Pair 8-Channel PoE PSE Controller With SRAM and 200 mΩ* R_{SENSE} data sheet.

4.1.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-050026-23881.

4.1.4 Altium Project

To download the Altium project files, see the design files at TIDA-050026-23881.

4.1.5 Gerber Files

To download the Gerber files, see the design files at TIDA-050026-23881.

4.1.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-050026-23881.

4.2 Software Files

To download the software files, see the design files at TIDA-050026-23881.

4.3 Related Documentation

1. Texas Instruments, *TPS23881 High-Power, 8-Channel, Power-Over-Ethernet PSE With 200-mΩ* R_{SENSE} *Data Sheet*
2. Texas Instruments, *TPS23882 Type-3, 30W, 2-pair, PSE daughter card for 24-port PSE systems*

4.4 Trademarks

TI E2E™ and NexFET™ are trademarks of Texas Instruments.
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5 Revision History

Changes from Revision A (October 2019) to Revision B (December 2025) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Added comprehensive MSPM0G1107 part family description throughout the document................................. 1
- Added MSPM0 and MSP430 MCUs in appropriate statements throughout the document............................... 1
- Added LEDs for PSEM0DAUEVM-018 in Table 3-1...12
- Added EVM I/O pins for PSEM0DAUEVM-018 in Table 3-4.. 13