

ABSTRACT

This document is the user's manual for the DRV3946-Q1 evaluation module (EVM) and the GUI to control the EVM. The DRV3946-Q1 allows for easy control and evaluation of the DRV3946-Q1 which is a dual-channel and fully integrated solenoid and contactor driver. This manual provides a detailed overview of the DRV3946-Q1 hardware features and instructions for using the included GUI to control the DRV3946-Q1EVM.

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1 Introduction



WARNING

The evaluation module (EVM) has a fuse that is rated for 20 A. To prevent the fuse from activating, verify that the maximum current draw of the battery voltage supply is always less than 20 A.

The DRV3946-Q1EVM includes two DRV3946-Q1 ICs, each able to drive two contactors in a low-side configuration. The DRV3946-Q1 is able to drive up to 9 A per channel for a total of 18 A if both output channels are driving at maximum capacity. The EVM comes with a 20-A fuse which disconnects the power supply from the rest of the board in the case of large current increase. The fuse protects all of the components on the board. The DRV3946-Q1 has many multiple-protection features such as overcurrent protection, overtemperature shutdown, undervoltage, and more that protect the device and contactor but do not provide system-level protection.



2 Hardware Overview

The following sections provide information on the main components of the EVM. A detailed explanation of each of the main components, such as connectors, configuration headers, and signal-test points, is given. Other information, such as voltage and current ratings, is described so that the user is aware of the limitation of the hardware to prevent potential damage to the board and its components. Figure 2-1 shows the main components of the DRV3946-Q1EVM. Table 2-1 gives a detailed description of each of the marked components. Both Figure 2-1 and Table 2-1 are referenced in the following sections.



Figure 2-1. DRV3946-Q1EVM Hardware Components

| Table 2-1. DRV3946-Q1E | /M Detailed Description of Components | |
|------------------------|---|--|
| Component | Description | |
| ٥ | J16: NAD_nFAULT resitor for Driver A | |
| A | J17: NAD_nFAULT resitor for Driver B | |
| | J11: IPROPI1 resistor for Driver A | |
| 6 | J12: IPROPI2 resistor for Driver A | |
| В | J15: IPROPI1 resistor for Driver B | |
| | J20: IPROPI2 resistor for Driver B | |
| | J1: S1 button function selection header; default position set to RST. | |
| | PUSH function is not supported by firmware. Firmware can be | |
| | modified to perform any desired task when the button is pressed | |
| С | and the shunt is placed in PUSH position. | |
| | S1: MCU Reset/Push function button. Only the MCU Reset function | |

is supported. Press the button to reset the MCU when J1 is in RST position.



| Component | Description | |
|-----------|---|--|
| | J7: Header for serial communication signals (RX, TX) and TDIO/TCK for programming main MCU (U3). Shunts are required for communication between the main MCU (U3) and the ezEET-LITE | |
| D | debugger. J5: EZFET-LITE flashing connector. Leave the header disconnected. | |
| E | STATUS LEDs. Refer to Section 2.3 | |
| F | Main signal header. Refer to Section 2.2 | |
| G | U1: DRV3946-Q1 Driver A J2: Driver A OUT1 and PVDD connector J3: Driver A OUT2 and PVDD connector | |
| н | Reverse battery protection, fuse, and EMI filter circuit | |
| 1 | Main power supply (VBAT) connector | |
| J | U8: DRV3946-Q1 Driver B J8: Driver B OUT1 and PVDD connector J21: Driver BOUT2 and PVDD connector | |

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2.1 Connectors and Configuration Headers

The main power connector J14 (I) is where the VBAT supply is connected. The maximum current the connector can withstand before damage or malfunction occurs is 20 A. To prevent potential damage to the board, ensure that the supply current does not exceed 20 A. If the current does exceed 20 A, the included 20-A fuse should protect the board. Protection should not soley rely on the fuse. TI recommends limiting the supply current to below 20 A to further protect the board.

The output connectors J2, J3, J21, and J8 (L) are the same as the J14 (I) main power connector. The DRV3946-Q1 is able to drive up to 9 A per channel, the maximum current expected for each connector is 9 A.

The IPROPIX_y headers (A) select the IPROPI resistor for each driver output. See the data sheet for the full list of suitable IPROPI resistor values. To minimize the board area, only select resistor values are included in the header. If the user desires to use a resistor value that is not listed in the header, the resistor can be soldered to the DNP footprint. Table 2-2 lists the available IPROPI resistor values in the EVM.

| Header Pins | Resistor Value to GND | | |
|-------------|-----------------------|--|--|
| 1-2 | 4.7 kΩ | | |
| 3-4 | 5.6 kΩ | | |
| 5-6 | 6.8 kΩ | | |
| 7-8 | 8.25 kΩ | | |
| 9-10 | 10 kΩ | | |
| 11-12 | 12 kΩ | | |
| 13-14 | 15 kΩ | | |
| 15-16 | 18 kΩ | | |
| 17-18 | 20 kΩ | | |
| 19-20 | DNP | | |

| Tahle | 2-2 | IPROPI | Resistor | Selector | Headers | Values |
|-------|------|--------|-----------|----------|------------|--------|
| able | Z-Z. | | 116313101 | Delector | i leauei 3 | values |

The NAD FAULT x headers select the NAD FAULT resistor values. By default, 8.7 kΩ is chosen for driver A and 22 kΩ is chosen for driver B. See the data sheet for more information about the NAD FAULT resistors and their functions. Table 2-3 lists the available NAD FAULT resistor values for each header.

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| Header Pins | Resistor value to GND | |
|-------------|--|--|
| 1-2 | DNP. Placeholder resistor. Do not place shunt. | |
| 3-4 | 5.6 kΩ | |
| 5-6 | 12 kΩ | |
| 7-8 | 27 kΩ | |
| 9-10 | 56 kΩ | |

Table 2-3. NAD_FAULT Resistor Selector Headers Values

2.2 Signal Test Points

Table 2-4 provides descriptions for each MCU signal in header J4. There are two rows of resistors on each side of the header that are labeled "A" and "B" in Figure 2-2. Removing resistors in row "A" disconnects the signal from the MCU and allows an external controller to control the drivers. Conversely, removing the resistors on row "B" disconnects the signals from the driver. Removing the resistors allows for the on-board MCU and GUI application to control an external DRV3946-Q1 driver.



Figure 2-2. J4 MCU Signal Header

| Signal | Description | |
|--------------|---|--|
| GND | Common board GND | |
| 3.3 V | 3.3 V output from on-board LDO | |
| IPROPI1_A | OUT1 IPROPI output for Diver A | |
| IPROPI2_A | OUT2 IPROPI output for Diver A | |
| ENABLE1_A | OUT1 enable for Driver A | |
| | (EN/EN1 in production IC) | |
| ENABLE2_A | OUT2 enable for Driver A (DIS/EN2 in production IC) | |
| SW_EN2_CTL | High-side switch 2 control signal | |
| SW_EN1_CTL | High-side switch 1 control signal | |
| NAD_nFAULT_A | FAULT signal for Driver A | |
| SDO | SDO signal | |
| SDI | SDI signal | |
| SCLK | SCLK signal | |
| nSCS_A | nSCS signal for Driver A | |
| nSCS_B | nSCS signal for Driver B | |
| IPROPI1_B | OUT1 IPROPI output for Diver B | |
| IPROPI2_B | OUT2 IPROPI output for Diver B | |



Table 2-4. MCU Signal Header (continued)

| Signal | Description | | |
|--------------|---|--|--|
| ENABLE1_B | OUT1 enable for Driver B (EN/EN1 in production IC) | | |
| ENABLE2_B | OUT2 enable for Driver B (DIS/EN2 in production IC) | | |
| NAD_nFAULT_B | FAULT signal for Driver B | | |

2.3 LED Indicators

There are LEDs on the EVM that are used for various visual indicators. Figure 2-3 highlights all of the LEDs in the DRV3946-Q1EVM and Table 2-5 provides a brief description of each LED.



Figure 2-3. EVM Indicator LEDs

Table 2-5. Description of LEDs

| LED | Description |
|-----|---|
| D3 | PVDD supply indicator |
| D5 | EZFET-LITE flashing indicator. Will flash when the EVM is being programmed. |
| D6 | When EVM USB connects successfully to the computer |
| D7 | Blinks ON/OFF at a rate of approximately 1 second when the MCU is active and indicates that the EVM is programmed |
| D1 | Will blink rapidly ON/OFF when the the EVM has successfully connected to the GUI |
| D11 | Driver B fault indicator. Will turn ON when a fault is detected. |
| D9 | Driver A fault indicator. Will turn ON when a fault is detected. |
| D2 | Driver A fault indicator. Will turn ON when a fault is detected. |
| D13 | Turn ON when Driver B is active |



Table 2-5. Description of LEDs (continued)

| LED | Description | |
|-----|---------------------------------|--|
| D12 | Turn ON when Driver A is active | |

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3 EVM GUI Control Application

The GUI application is written with Texas Instruments' GUI Composer, and can be run directly from a Chromebased web browser, or installed onto your computer. Because GUI Composer apps are written with a NodeJS back end, the GUI application is cross-platform compatible by design. This document only covers installation on a PC for sake of brevity, but Mac[®] and Linux[®] users can find installers in the GUI Composer Gallery.

3.1 MSP430 FET Drivers

The MSP430 FET Drivers are required for the operating system to properly enumerate the JTAG and UART ports created by the EZFET_LITE. The latest drivers can be found here: MSP430 FET Drivers

Download the driver package corresponding to your operating system, extract the archive, and run the installer.

In Windows®, two new ports must be enumerated when the EVM is connected Figure 3-1:

Ports (COM & LPT)
 MSP Application UART1 (COM18)
 MSP Debug Interface (COM19)

Figure 3-1. MSP430 EZFET_LITE Enumerated USB Ports

Successful installation also shows Texas Instruments as the driver publisher (Figure 3-2):

| General | Port Settings | Driver | Details | Event | s | |
|---------|----------------|----------|---------------------------|------------------------|------------------------------|--------------------|
| | MSP Applicat | tion UAF | T1 (COM | 18) | | |
| | Driver Provide | ər: T | exas Instr | uments | | |
| | Driver Date: | 1 | 0/27/2016 | 5 | | |
| | Driver Version | n: 1 | .6.0.0 | | | |
| | Digital Signer | : т | exas Instr | uments | Incorporated | |
| Dr | iver Details | Viev | v details a ate the dr | bout the | installed drive | r files. |
| Roll | Back Driver | If the | e device fa | ails after eviously | updating the installed drive | driver, roll r. |
| Dis | able Device | Disa | ble the de | evice. | | |
| Uni | nstall Device | Unir | nstall the d | levice fro | om the system | (Advanced). |

Figure 3-2. MSP Application UART Driver Properties

3.2 Cloud-based GUI

To launch the GUI application from your Chrome-based browser:

- 1. Navigate to the DRV3946-Q1EVM-GUI.
- 2. When presented with the list of available GUIs, launch the latest version by clicking on the title. Only click areas that are not related to the icons for downloading the installer or GUI Composer. Refer to Figure 3-3.



We've found 2 result(s) for "DRV3946



Figure 3-3. TI GUI Composer Gallery Results for Launching or Downloading Local Installer

The setup and operation of the GUI hardware is the same as the desktop version. The setup is consolidated in the following EVM GUI Operation section.

3.3 Local Installation

Follow these instructions for downloading and installing the latest version of the EVM GUI application:

- The EVM GUI application installer can also be downloaded from the TI GUI Composer Gallery, DRV3946-Q1EVM-GUI.
- 2. From the gallery, click the ¹/₂ icon for the latest version and select the installer for your operating system (Windows, Linux or Mac). Refer back to the previous section for a visual depiction of the Gallery page.
- 3. Decompress the .zip file.
- 4. From the decompressed archive, run the installer DRV3946-Q1EVM-GUI-x.y.z.setup-win.exe, refer to the GUI Application Archive Contents. The installer will install the GUI Composer Runtime, if it is has not been previously installed. The installer contents is self-explanitory and will look slightly different for each OS.

DRV3946-Q1EVM-GUI_2.0.0.20220922135922.log

🐝 DRV3946-Q1EVM-GUI-2.0.0.setup-win.exe

Figure 3-4. GUI Application Archive Contents

5. After completing the hardware setup in the next section, the GUI application is prepared to run on your local machine.

4 EVM GUI Operation

4.1 Hardware Setup

Follow these steps to setup the EVM before launching the GUI:

- 1. It is advised to make any jumper configuration changes before powering the EVM. Before powering up the board, selected the IPROPIx_A, IPROPIx_B, and NAD_nFAULT_x headers.
- Connect the micro-USB cable to J6 (Figure 2-1). For proper GUI application operation, it is important to connect the EVM USB cable to a computer before applying +VBAT power to the EVM. For standalone EVM testing a USB connection is not necessary.
- 3. With the +VBAT external supply outputs disabled, connect +BAT supply to the screw terminals on the EVM (J14), while observing polarity (Figure 2-1).
- 4. Energize the +VBAT supply. PVDD LED D3 and 3.3V_MCU LED D7 will illuminate. If VM LED does not illuminate, verify polarity and confirm that fuses are installed and maintain continuity.
- 5. After applying the +VBAT supply, LED D6 will illuminate to indicate that there is a successful USB connection with the computer. If the LED is *not on*, disconnect the USB cable from the computer, turn off the power supply, reconnect the USB to the computer, and turn on the supply.
- 6. The EVM is ready for use with the GUI application (Section 4.2). In certain situations, a proper firmware restart may not happen. One example of an instace where a proper firmware restart does not occur is when disconnecting and reconnecting VM power before the power supply capacitors are fully discharged. If the Status LED (D1) is not blinking as expected, install the jumper J1 in the RST position and press the reset push button once. Do not unplug the USB cable while the VM power is active. If the USB cable is unplugged while the VM power is active, switch off the VM power, wait until it is fully discharged and proceed to step 2.
- 7. The latest version of the GUI application is bundled with the latest version of the EVM firmware. When using the GUI application, it is recommended to do a firmware update before selecting and connecting to an EVM variant. The firmware update procedure is described in the Section 5.1 section of this user's guide.

4.2 Launching the DRV3946-Q1EVM GUI Application

The user experience and steps described below are the same regardless of using the desktop or web version of the GUI. In order to complete the next steps, it is assumed that the hardware setup steps in the previous section have already been completed.

- 1. Launch the GUI application.
- 2. From the screen referenced in Figure 4-1, click on the icon to the right labeled "DRV3946-Q1EVM."

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Figure 4-1. DRV3946-Q1EVM GUI Main Start-up Page

 After clicking the icon, the GUI application initiates communications with the EVM. Connection confirmation is displayed as shown below in Figure 4-2. The EVM should now be connected. The GUI_STATUS LED (D11) blinks to confirm that there is a successfull GUI connection. Do not proceed to use the GUI app if the D11 is not blinking.

Note

If the EVM GUI does not register a successful connection after multiple attempts, update the firmware and use the GUI application to select a connecting EVM variant.

| DRV3946-Q1EVM-GUI File Options Tools Help | |
|---|-------------------------------|
| The connected EVM is DRV3946-Q1EVM | |
| Automotive Contactor Driver With Integrated Current Sense and Diagnostics | What would you like to drive? |
| 5 | Features |
| * | Register Map > |
| | Contactor Control > |
| | |
| | |
| | |
| | |
| | |
| | |
| / COM1589600 Hardware Connected: DRV3946-Q1EVM | Powerd By GU Composer ** |

Figure 4-2. Successful EVM Connection



- 4. Set up the EVM for device evaluation. These are the pages for set up:
 - · Register Map page for reading and writeing access of the register bit fields
 - Contactor control page with configuration and diagnostic options
 - GUI Home page

| DRV3 | 8946-Q1EVM-GUI File | Options Tools Help | | | _ 0 × |
|------------|---|--|---|---|---|
| | DRIVER CONFIGURATION | PWM SETTINGS PWM Frequency ① 10 KHz Y Pseudo Random | Dthering Spread ① No dther v | Device Firmware Version | DRV3946-Q1 0.27 |
| | | CONTROL CONFIGURATION | | Fault | Clear |
| × 5 * | Exactions 97 Addressafe 97 0 Exactle 1 0 0 0 Exactle 2 0 0 0 0 Max 20 0 0 0 0 0 MAD Setting 0 0 | IDAR2 Peado Relicent CONTROL CONFIGURATION RIPROPI 1 DUTFUT 1 Peak Current Hold Current 1.757 A Hold Current 1.757 A Peak Time 0 80 mise Peak Time | 0 10 k2 0 4.61 1.727 0 00maec | Fault FAULT DRIVER A FAULT DRIVER B DEVICE ERROR WARNINGS PVDD_UV_W PVDD_OV_W OT_W SR_VDO_W CH_JRIPROPLW CH_JRIPROPLW CH_JRIPROPLW CA_RIPROPLW CA_RIPROPLW CA_RIPROPLW CA_RIPROPLW | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |
| <i>8</i> G | COM158:9600 Hardware Connected | 1: DRV3946-Q1EVM | | | Forward By GU Composer*** |



| Register Map | | | | | | | | | | | | | Ū | Auto Read | Ever | y i sec | * | | Immediate V |
|--|---------|--------|----|----|----|----|----|----|---|----|---------|---|---|-----------|--------|-----------|-----|----------|---|
| Q Search Registers by name or address (0x) | | | | | | | | | | | | | | | Search | Bitfields | ✓ S | how Bits | |
| Register Name | Address | Value | 15 | 14 | 12 | 12 | 11 | 10 | 0 | Bi | ts 7 | 6 | 5 | 4 | 2 | 2 | 1 | 0 | STATUSO |
| * STATUS REGISTERS | | | | | | | | | | | | | | | | | | | STATUS DEGISTERS / STATUSS / MADINE 14] |
| STATUS0 | @ 0x01 | 0x0008 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | |
| STATUS1 | 0x02 | 0x0400 | 0 | 0 | 0 | 0 | 0 | 1 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| STATUS2 | 0x03 | 0x0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | STATUS REGISTERS / STATUS0 / POR[13] |
| STATUS3 | 0x04 | 0x0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | POR |
| STATUS4 | 0x0A | 0x0000 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - Ton |
| STATUS5 | 0x0B | 0x0000 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STATUS REGISTERS / STATUS0 / ENABLE_PIN_STAT |
| MEASUREMENT REGISTERS | | | | | | | | | | | | | | | | | | | B ENABLE_PIN_STAT |
| MEAS0 | 0x05 | 0x0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ENABLE_PIN_STAT |
| MEAS1 | 0x06 | 0x0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Pin Low 🗸 |
| MEAS2 | 0x07 | 0x0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| MEAS3 | 0x08 | 0x0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STATUS REGISTERS / STATUSO / DISABLE_PIN_STAT |
| MEAS4 | 0x09 | 0x0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DISABLE_PIN_STAT |
| CONFIG A REGISTERS | | | | | | | | | | | | | | | | | | | Pin Low |
| CONFIG_A0 | 0x10 | 0xC040 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | |
| CONFIG_A1 | 0x11 | 0xC040 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | STATUS REGISTERS / STATUS0 / nFAULT_PIN_STAT[|
| CONFIG_A2 | 0x12 | 0x2424 | | | 1 | 0 | | 1 | 0 | 0 | 0 | | 1 | 0 | 0 | 1 | 0 | 0 | nFAULT_PIN_STAT |
| CONFIG_A3 | 0x13 | 0x0088 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | nFAULT_PIN_STAT |
| CONFIG_A4 | 0x14 | 0x130C | | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | Pin Low 🗸 |
| CONFIG_A5 | 0x15 | 0x8000 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | STATUS REGISTERS / STATUSD / DEVICE ERR[9] |
| CONFIG_A6 | 0x16 | 0x0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| V CONFIG B REGISTERS | | | | | | | | | | | | | | | | | | | - DEVICE_ERR |
| CONFIG_B0 | 0x17 | 0x2623 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | | 0 | 1 | 0 | 0 | 0 | 1 | 1 | STATUS REGISTERS / STATUS0 / WARNINGS[8] |
| CONFIG_B1 | 0x18 | 0x0040 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | WARNINGS |
| CONFIG_B2 | 0x1B | 0x0B00 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| COMMAND REGISTERS | | | | | | | | | | | | | | | | | | | STATUS REGISTERS / STATUS0 / CH1_OFF_DIAG_ST |
| CMD0 | 0x1C | 0x8000 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CH1 OFF DIAG STAT |
| CMD1 | 0x1D | 0x0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - |
| CMD2 | 0x1E | 0x0064 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | STATUS REGISTERS / STATUS0 / CH1_STAT[6:4] |
| | | | | | | | | | | | | | | | | | | | A CHI STAT |





5 GUI Overview

Figure 5-1 shows the motor control page of the GUI application. The main sections of the control page are labeled A through S. Table 5-1 describes each labeled section. Before trying to use the GUI, read the data sheet to learn more about the register map and the different configuration parameters for this driver.

Note

The "FAULT DRIVER A" and "FAULT DRIVER B" fault indicators and the corresponding fault LEDs in the EVM are red during the initial power up and GUI connection. The red fault LEDs are due to the DRV3946-Q1 detecting an open load warning (OLD) which is enabled by default. To clear the fault, write 4'b0000 to nFAULT_CONFIG bit field in the register CONFIG_A5 (address 0x15). Read the data sheet to learn about fault reporting the DRV3946-Q1.



Figure 5-1. GUI Contactor Control Page Overview



| 🖊 Register Map 🛛 🕬 🗠 | **E) () | 0 | | | | | | | | | | | q | C | Auto Res | d Ever | y1 sec | - | | And a second second | Immediate Write 🗸 |
|--|----------|---------|-----------------|------|-----|----|----|---|----|---|----|----|----|-----|----------|--------|-----------|------|----------|------------------------------------|--------------------|
| Q Search Registers by name or address (0x) | | 3. | P | | | | | | | | | | | 100 | | Search | Bitfields | V s | how Bits | | |
| Register Name | | Address | Value | 1 | | 12 | - | | | | B | ts | | | | | | | | CONFIG A5 | S |
| * STATUS REGISTERS | | | | 10 | 14 | 13 | 14 | | 10 | 4 | 0 | 1 | 0 | 9 | | 0 | - | 1 | 0 | | |
| STATUSO | | 0x01 | 0x0408 | ö | 0 | 0 | 0 | 0 | Ť | 0 | 0 | Ű. | 0 | 0 | 0 | -1 | 0 | 0 | 0 | CONFIG A REGISTERS / CONFIG_A5 / n | FAULT_CONFIG[15:12 |
| STATUSI | | 0x02 | 0x0400 | 0 | 0 | 0 | 0 | 0 | Ť | | 0 | 0 | 0 | 0 | 8 | 0 | 0 | 0 | 0 | nFAULT_CONFIG | |
| STATUS2 | | 0x03 | 0x0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | 00000 | • |
| STATUS3 | | 0x04 | 0x0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | CONFIG & REGISTERS / CONFIG_A5 / | |
| STATUSA | | 0x0A | 0x0000 | 1.2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | a | 0 | 0 | 0 | 0 | a | CH1_PIN_TURNON_DLY[11.9] | |
| STATUSS | | 0x0B | 0x0000 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CH1_PIN_TURNON_DLY | |
| | | | | | | | | | | | | | | | | | | | | NU delay | * |
| T MEASUREMENT REUISTERS | | 0x05 | 0x0000 | 0 | D. | 0 | 0 | 0 | 0 | 0 | .0 | 0 | 0 | 0 | .0 | 0 | 0 | 1.01 | .0 | CONFIG A REGISTERS / CONFIG_A5 / | |
| MEASI | | 0x06 | 0x0000 | | 0 | | 0 | | 0 | 0 | 0 | | | 0 | 0 | | 1 | 0 | 0 | CH1_PIN_TURNOFF_DLV[8:6] | |
| MEASS | | 0x07 | 0×0000 | | | | | | | | | | ÷. | | | 1 | 2 | | | CH1_PIN_TURNOFF_DLY | |
| MEACO | | 0,00 | 0×0000 | - C | | | | 1 | | | | 3 | 1 | | | 1 | | | 0 | NO delay | ~ |
| MEAGE | | 0x00 | 0x0000 | | | | 0 | | | | | | | | | ő | | | | CONFIG & REGISTERS / CONFIG_A5 / | |
| MEA34 | | 0104 | 0.0000 | 1.00 | . 9 | | .0 | | | | .0 | | | 1.1 | | | | | | CH2,PIN_TURNON_DLY[5:3] | |
| V CONFIG A REGISTERS | | 0410 | 0+0040 | | | | 0 | | 0 | | 0 | 0 | | | | | | 0 | | CH2_PIN_TURNON_DLY | |
| CONFIGAC | | 0410 | 0x0040 | | | 0 | 0 | | 0 | 0 | 0 | .0 | | 0 | 0 | | 0 | 0 | 0 | NO delay | * |
| CONFIG_AT | | UXII | 0x0040 | | 1 | | 0 | 0 | | 0 | 0 | 0 | 1 | | | 0 | | 0 | | CONFIG & REDISTERS / CONFIG: 45 / | |
| CONFIG_AZ | | 0x12 | 082424 | - | - | | 0 | | 1 | | U | | - | 1 | 0 | 0 | 1 | 0 | U | CH2_PIN_TURNOFF_DLY[2:0] | |
| CONFIG_A3 | | 0x13 | 0×0088 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 2 | 0 | 0 | 0 | CH2_PIN_TURNOFF_DLY | |
| CONFIG_A4 | 1721 | 0x14 | 0x130C | 1 | 0 | 0 | 1 | 0 | 0 | 1 | | 0 | 0 | 0 | 0 | | 1 | 0 | 0 | NO delay | × |
| CONFIG_A5 | Θ | 0x15 | 0x0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 56 | |
| CONFIG_A6 | | 0x16 | 0x00C8 | 0 | 0 | e | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | ۵ | 0 | | |
| * CONFIG B REGISTERS | | | | | | | | | | | | | | | | | | | | | |
| CONFIG_B0 | | 0x17 | 0x2623 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | | 0 | 1 | 0 | 0 | 0 | 1 | 1 | | |
| CONFIG_B1 | | 0x18 | 0x0040 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| CONFIG_B2 | | 0x1B | 0x0B00 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| * COMMAND REGISTERS | | | 100 C 100 C 100 | | | | | | | | | | | | | | | | | | |
| CMD0 | | 0x1C | 0x8000 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4 | 0 | | |
| CMD1 | | 0x1D | 0x0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Ω | 0 | | |
| CMD2 | | Ox1E | 0x0064 | .0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | | |

Figure 5-2. GUI Contactor Control Page Overview

Table 5-1. DRV3946-Q1EVM GUI Description

| Section | Description |
|---------|--|
| A | Main GUI start-up page. |
| В | Register map page. Device registers can be read/written to configure device. All of the configurations can be done in the register map if desired. |
| С | Contactor/solenoid control page. Most of the basic configurations can be done in this page. Use the register map for more advanced configurations. |
| D | Home page. |
| E | Select between individual driver control or simultaneous control of both drivers with NAD (Non-addressable) SPI. Jumper setting must be modified in the hardware to support Addressable SPI. Refer to Section 6. |
| F | Select between controlling driver A or B. In Standalone SPI, only the selected driver is active. In Addressable SPI, both drivers are active and only the selected driver can be configured. Refer to Section 6. |
| G | Enable 1 and Enable 2 (EN/EN1 and DIS/EN2 for production IC) control widgets. |
| н | NAD resistor settings. Click the NAD Setting button to switch between Driver A and Driver B and select the NAD resistor from the nFAULT/NAD resistor drop-down menu. The resistor for each Driver must match the selected resistor in J16 and J17 (Figure 2-1). |
| I | PWM settings. |
| J | Control configurations. The RIPROPI 1 and RIPROPI 2 must match the selected IPROPI resistor in J11 and J12 or J15 and J20 depending on the driver selected (Figure 2-1). |
| К | Driver A peak current, hold current, and peak time settings. |
| L | Driver B peak current, hold current, and peak time settings. |
| М | Connected device name and Firmware version. |

| Table 5-1. DRV3946-Q1EVM GUI Description (continued) | | | | | | | |
|--|---|--|--|--|--|--|--|
| Section | Description | | | | | | |
| Ν | Fault summary table. FAULT DRIVER A and FAULT DRIVER B mirror the NAD/nFAULT pins of each driver respectively. When NAD/ nFAULT is LOW, indicating a fault, the corresponding status indicator turns RED. The remaining fault indicators are for common warnings. Click the "CLEAR" button to clear a fault. Refer to the register map to view all the faults and warnings in the STATUS registers. | | | | | | |
| 0 | Device Selector widget. Same as widget F. Register values shown in the register map correspond to the selected driver. Please note that if the drivers are reset from a power cycle, the register values returns to their default values. | | | | | | |
| Р | Register value column. Write desired value to write to the registers. | | | | | | |
| Q | Frequency at which GUI reads all of the registers and display updated values in the register map. Default value is 1 second. If Auto Read function is not desired, the function can be set to "NONE". Doing so activates the "READ REGISTER" and "READ ALL REGISTER" buttons. "READ REGISTER" will only read the selected register. "READ ALL REGISTERS" will read all registers. | | | | | | |
| R | "Immediate Write" writes to the register as soon as the value is entered. "Deferred Write" only writes the to register after value has been entered and the "WRITE REGSITER" button is clicked. | | | | | | |
| S | Bit field view of selected register. | | | | | | |

5.1 Programming the EVM

Complete a firmware update if the EVM is not connecting to the GUI app after multiple attempts. A pop-up message appears when the hardware firmware is out of date. The following steps describe how to update the firmware of the EVM using the GUI:

- 1. Connect the EVM to the GUI following the instructions in Section 4.1.
- Open the GUI and click on the "DRV3946-Q1EVM" icon on the right side of the main start-up page. There is a chance for failure when the GUI attempts to connect to the EVM. Wait until the GUI says the EVM is either successfully or unsuccessfully connected.
- Click on File -> Program Device to program the EVM (see Figure 5-3). A small pop-up small window shows the firmware flashing progress. A message is displayed if errors occur. If there are no errors, the display will indicate that the flashing was successful.
- 4. The GUI will attemp to connect to the EVM. After successfully connecting, the page resembles Figure 4-2. If connection is not successful, follow instructions in Section 4.1 and Section 4.2.



Figure 5-3. GUI Program Device Tab



5.2 Saving and Loading Register Configurations

The DRV3946-Q1EVM GUI has a built-in feature to save the current register configurations as a .json file which loads to the GUI. The following steps outline the procedure for saving and loading register configurations.

- 1. After writing the desired register values, click on the "File" tab and click "Save Registers." A save file pop-up window will appear to name and save the .json file.
- 2. To recall the register configurations, click on the "File" tab and then the click "Load Registers." Select the saved .json file to load the register values.



Figure 5-4. Save and Load Registers Menu



6 Contactor Driver SPI Modes

The EVM and GUI support standalone and addressable SPI which are selectable from the driver configuration widget. Refer to the Figure 5-1 for the widget location. In the standalone SPI, only the selected driver is active and each device has a dedicated nSCS signal. In the addressable SPI, the SPI bus is shared between both of the drivers which allows for both drivers to have simultaenous SPI communication.

6.1 Standalone SPI

Standalone SPI is the default serial communication mode. The Standalone SPI mode is selected when only one driver is controlled while the other driver is inactive. In the standalone SPI mode, each driver has its own nSCS signal and only the nSCS of selected driver functions. Therefore, SPI communication is only possible with a selected driver. The Figure 6-1 shows the SPI connections for a standalone SPI.



Figure 6-1. Standalone SPI Diagram

6.2 Addressable SPI

Addressable SPI allows for SPI communication with both drivers to occur simultaneously. In this mode, one nSCS signal is connected to both drivers. Figure 6-2 shows the SPI connections for an addressable SPI. The register map displays the register values of the selected driver. To write to a specific driver, select the specific driver in the GUI.



Figure 6-2. Addressable SPI Diagram



For both drivers to have successful communication, do the following:

 Verify that the NAD/nFAULT resistor of each driver is different. The NAD resistors for each driver are selected in headers J16 and J17 (Figure 2-1). The resistor value must match the resistor selected in the GUI (Figure 2-1 or communication fails.

Note

While powering-up the DRV3946-Q1, the NAD/nFAULT resistors are latched. Before powering-up the board, verify that the desired resistors for each driver are selected in the EVM.

• The nSCS_A and nSCS_B signals must be shorted in the EVM. Place a shunt across the nSCS_A and nSCS_B test points in J4 as shown in Figure 6-3.



Figure 6-3. Shunt Placement Location for Addressable SPI



7 Revision History NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|--------------|----------|-----------------|
| October 2021 | * | Initial Release |

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