Technical Reference Manual

TPS6503200J Technical Reference Manual

ABSTRACT

This Technical Reference Manual (TRM) can be used as a reference for the default register bits after the NVM download. The device is designed for Automotive Camera applications. This TRM does not provide information about the electrical characteristics, external components, package, or the functionality of the device. For this information and the full register map, refer to the device datasheet.

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Trademarks

1 EEPROM Device Settings

1.1 Device ID

This section lists all of the device settings that are downloaded from NVM for the Device ID.

Table 1-1. Device ID

	Description	Bit Name	TPS6503200J	
Product ID	Device specific ID code	PID	11001	
NVM Revision	Identification code for the NVM version	NVM_Version	0000b	A

1.2 Regulator Voltage Settings

Table 1-2. Regulator Voltage Settings

	Description	Bit Name	TPS6503200J Bit Settings	TPS6503200J
BUCK1	Output voltage	BUCK1_VOUT	0000b	3.3V
BUCK2	Output voltage	BUCK2_VOUT	11101b	1.800V
BUCK3	Output voltage	BUCK3_VOUT	00110b	1.100V
LDO	Output voltage	LDO_VOUT	11110b	2.800V

1.3 Power Sequence Settings

This section breaks out the power sequence settings for the device.

1.3.1 BUCK1 Power Sequence Settings

Table 1-3 lists the power sequence settings for BUCK1.

Table 1-3. Power Sequence Settings - BUCK1

	Description	Bit Name	TPS6503200J Bit Settings	TPS6503200J
Sequence Trigger	Sequence trigger dependency	PWR_ON_bit_BUCK1	0b	Included as part of the power ON/OFF sequence logic
Sequence Trigger	Sequence trigger dependency	BUCK2_PG_BUCK1	1b	Not included as part of the power ON/OFF sequence logic
Sequence Trigger	Sequence trigger dependency	BUCK3_PG_BUCK1	1b	Not included as part of the power ON/OFF sequence logic
Sequence Trigger	Sequence trigger dependency	LDO_PG_BUCK1	1b	Not included as part of the power ON/OFF sequence logic
Sequence Trigger	Sequence trigger dependency	SEQ_PIN_BUCK1	1b	Not included as part of the power ON/OFF sequence logic
Sequence On Delay	Power on sequence delay	BUCK1_SEQ_DLY_ON	0001b	0.5ms
Sequence Off Delay	Power off sequence delay	BUCK1_SEQ_DLY_OFF	0101b	4ms

1.3.2 BUCK2 Power Sequence Settings

Table 1-4 lists the power sequence settings for BUCK2.

Table 1-4. Power Sequence Settings - BUCK2

	Description	Bit Name	TPS6503200J Bit Settings	TPS6503200J
Sequence Trigger	Sequence trigger dependency	PWR_ON_bit_BUCK2	0b	Included as part of the power ON/OFF sequence logic
Sequence Trigger	Sequence trigger dependency	BUCK1_PG_BUCK2	0b	Included as part of the power ON/OFF sequence logic

Table 1-4. Power Sequence Settings - BUCK2 (continued)

	Description	Bit Name	TPS6503200J Bit Settings	TPS6503200J
Sequence Trigger	Sequence trigger dependency	BUCK3_PG_BUCK2	1b	Not included as part of the power ON/OFF sequence logic
Sequence Trigger	Sequence trigger dependency	LDO_PG_BUCK2	0b	Included as part of the power ON/OFF sequence logic
Sequence Trigger	Sequence trigger dependency	SEQ_PIN_BUCK2	1b	Not included as part of the power ON/OFF sequence logic
Sequence On Delay	Power on sequence delay	BUCK2_SEQ_DLY_ON	0001b	0.5ms
Sequence Off Delay	Power off sequence delay	BUCK2_SEQ_DLY_OFF	0011b	2ms

1.3.3 BUCK3 Power Sequence Settings

Table 1-5. Power Sequence Settings - BUCK3

	Description	Bit Name	TPS6503200J Bit Settings	TPS6503200J
Sequence Trigger	Sequence trigger dependency	PWR_ON_bit_BUCK3	0b	Included as part of the power ON/OFF sequence logic
Sequence Trigger	Sequence trigger dependency	BUCK1_PG_BUCK3	0b	Included as part of the power ON/OFF sequence logic
Sequence Trigger	Sequence trigger dependency	BUCK2_PG_BUCK3	0b	Included as part of the power ON/OFF sequence logic
Sequence Trigger	Sequence trigger dependency	LDO_PG_BUCK3	0b	Included as part of the power ON/OFF sequence logic
Sequence Trigger	Sequence trigger dependency	SEQ_PIN_BUCK3	1b	Not included as part of the power ON/OFF sequence logic
Sequence On Delay	Power on sequence delay	BUCK3_SEQ_DLY_ON	0001b	0.5ms
Sequence Off Delay	Power off sequence delay	BUCK3_SEQ_DLY_OFF	0010b	1ms

1.3.4 LDO Power Sequence Settings

Table 1-6. Power Sequence Settings - LDO

	Description	Bit Name	TPS6503200J Bit Settings	TPS6503200J
Sequence Trigger	Sequence trigger dependency	PWR_ON_bit_LDO	0b	Included as part of the power ON/OFF sequence logic
Sequence Trigger	Sequence trigger dependency	BUCK1_PG_LDO	0b	Included as part of the power ON/OFF sequence logic
Sequence Trigger	Sequence trigger dependency	BUCK2_PG_LDO	1b	Not included as part of the power ON/OFF sequence logic
Sequence Trigger	Sequence trigger dependency	BUCK3_PG_LDO	1b	Not included as part of the power ON/OFF sequence logic
Sequence Trigger	Sequence trigger dependency	SEQ_PIN_LDO	1b	Not included as part of the power ON/OFF sequence logic
Sequence On Delay	Power on sequence delay	LDO_SEQ_DLY_ON	0001b	0.5ms
Sequence Off Delay	Power off sequence delay	LDO_SEQ_DLY_OFF	0100b	3ms

1.3.5 nRSTOUT Power Sequence Settings

Table 1-7. Power Sequence Settings - nRSTOUT

	Description	Bit Name	TPS6503200J Bit Settings	TPS6503200J
Sequence Trigger	Sequence trigger dependency	PWR_ON_bit_nRSTOUT	0b	Included as part of the power ON/OFF sequence logic
Sequence Trigger	Sequence trigger dependency	BUCK1_PG_nRSTOUT	0b	Included as part of the power ON/OFF sequence logic
Sequence Trigger	Sequence trigger dependency	BUCK2_PG_nRSTOUT	0b	Included as part of the power ON/OFF sequence logic
Sequence Trigger	Sequence trigger dependency	BUCK3_PG_nRSTOUT	0b	Included as part of the power ON/OFF sequence logic
Sequence Trigger	Sequence trigger dependency	LDO_PG_nRSTOUT	0b	Is part of power ON/OFF sequence
Sequence Trigger	Sequence trigger dependency	SEQ_PIN_nRSTOUT	1b	Not included as part of the power ON/OFF sequence logic
Sequence On Delay	Power on sequence delay	nRSTOUT_SEQ_DLY_ON	0011b	2ms
Sequence Off Delay	Power off sequence delay	nRSTOUT_SEQ_DLY_OFF	0001b	0.5ms

1.4 IO Pin Configurations

Table 1-8. IO Pin Configurations

	Description	Bit Name	TPS6503200J Bit Settings	TPS6503200J
nRSTOUT	Push-pull or Open Drain Configuration	nRSTOUT_PIN_CONFIG	0b	Open Drain

1.5 Configuration Bit Settings

Table 1-9. Configuration Bit Settings

	Description	Bit Name	TPS6503200J Bit Settings	TPS6503200J
Fault Handling	Handling of Priority 2 Faults	STATE_TRANSITION	0b	Priority 2 Faults transition to the RESET state
Die Temperature Warning	120°C or 130°C warning level	TWARN_LEVEL	0b	Temperature Warning Level is set to 120 deg Celcius
LDO Mode	LDO or Load Switch	LDO_BYP_EN	0b	LDO operation
LDO Current Limit	200mA or 400mA	LDO_IOUT	1b	400mA
BUCK1 Undervoltage Fault Configuration	State Machine Transition due to an Undervoltage condition	BUCK1_UV_RST_EN	1b	Fault causes a Transition to the RESET state
BUCK2 Undervoltage Fault Configuration	State Machine Transition due to an Undervoltage condition	BUCK2_UV_RST_EN	1b	Fault causes a Transition to the RESET state
BUCK3 Undervoltage Fault Configuration	State Machine Transition due to an Undervoltage condition	BUCK3_UV_RST_EN	1b	Fault causes a Transition to the RESET state
LDO Undervoltage Fault Configuration	State Machine Transition due to an Undervoltage condition	LDO_UV_RST_EN	1b	Fault causes a Transition to the RESET state

Table 1-9. Configuration Bit Settings (continued)

	Description	Bit Name	TPS6503200J Bit Settings	TPS6503200J
BUCK1 Undervoltage Monitor Setting	UV detection threshold with respect to the target setting	BUCK1_UV_SET	00b	96%
BUCK2 Undervoltage Monitor Setting	UV detection threshold with respect to the target setting	BUCK2_UV_SET	00b	96%
BUCK3 Undervoltage Monitor Setting	UV detection threshold with respect to the target setting	BUCK3_UV_SET	00b	96%
LDO Undervoltage Monitor Setting	UV detection threshold with respect to the target setting	LDO_UV_SET	00b	96.5%

1.6 Control Bit Settings

Table 1-10. Control Bit Settings

	Description	Bit Name	TPS6503200J Bit Settings	TPS6503200J
Spread Spectrum	Controls whether Spread Spectrum is enabled or disabled	ENABLE_SPREAD_SPECTRUM	1b	Enabled
LDO Pre-bias	Controls the action taken based on a pre-bias on the LDO output	LDO_PREBIAS_CTRL	1b	The device remains in the RESET state until the voltage on all outputs are below the Short Circuit to Ground threshold.
Warm Threshold	Controls the action taken if the Warm Threshold setting is exceeded	WARM_THR_STARTUP_CTRL	1b	Device does not power up until the temperature is below the Warm Threshold setting

1.7 PVIN_B1 UVLO Settings

Table 1-11. PVIN_B1 UVLO Settings

	Description	Bit Name	TPS6503200J Bit Settings	TPS6503200J
PVIN_B1 pin UVLO	Sets the rising voltage level on the PVIN_B1 pin which must be exceeded before the voltage regulators will become active.	BUCK1_UVLO_Rising	0010b	4.68V
PVIN_B1 pin UVLO	Sets the falling voltage level on the PVIN_B1 pin which determines when the voltage regulators will become inactive.	BUCK1_UVLO_Falling	0001b	4.0V

1.8 Voltage Regulator Discharge Settings

Table 1-12. Voltage Regulator Discharge Settings

	Description	Bit Name	TPS6503200J Bit Settings	TPS6503200J
BUCK3	Output discharge when converter is disabled.	BUCK3_DISCHARGE_CONTROL	01b	125 ohm
BUCK2	Output discharge when converter is disabled.	BUCK2_DISCHARGE_CONTROL	01b	125 ohm
BUCK1	Output discharge when converter is disabled.	BUCK1_DISCHARGE_CONTROL	01b	125 ohm
LDO	Output discharge when LDO is disabled.	LDO_DISCHARGE_CONTROL	01b	125 ohm

2 Sequence Drawing

2.1 Power On/Off Sequence Drawing

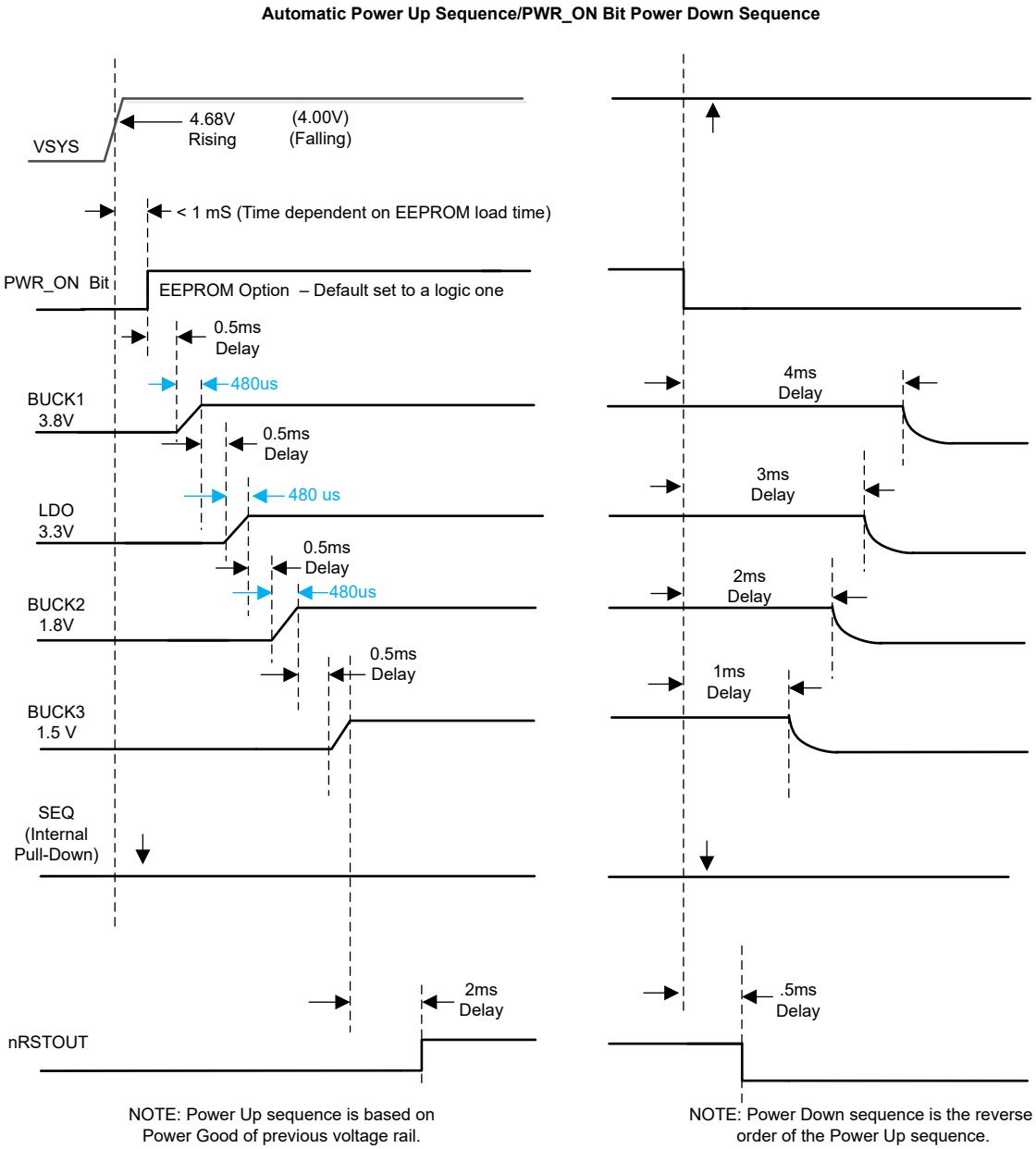

Figure 2-1. TPS6503200J Power On/Off Sequence Diagram

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