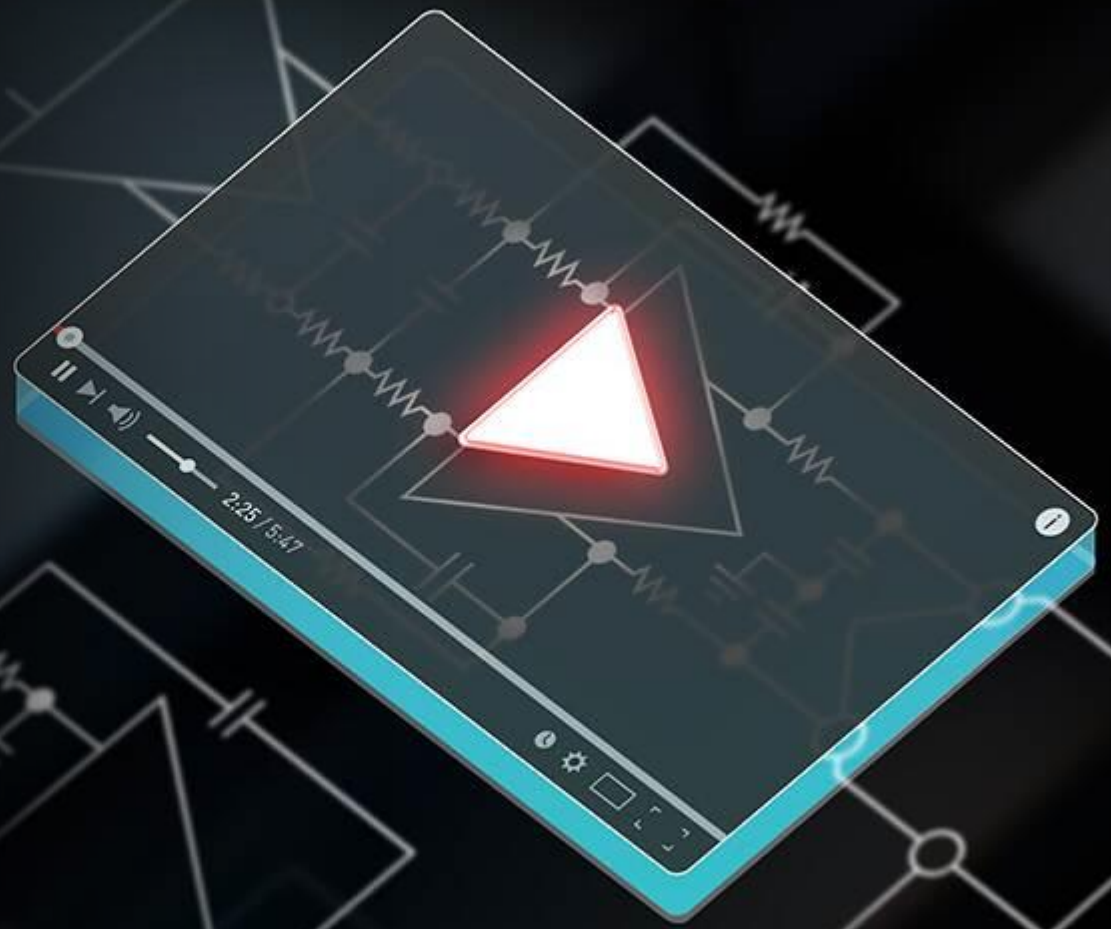
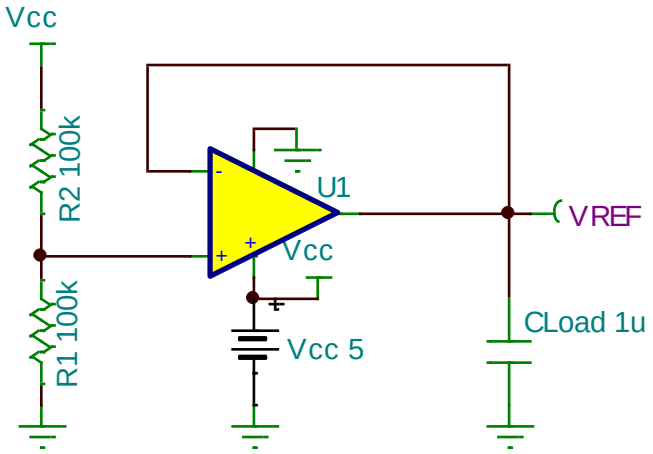
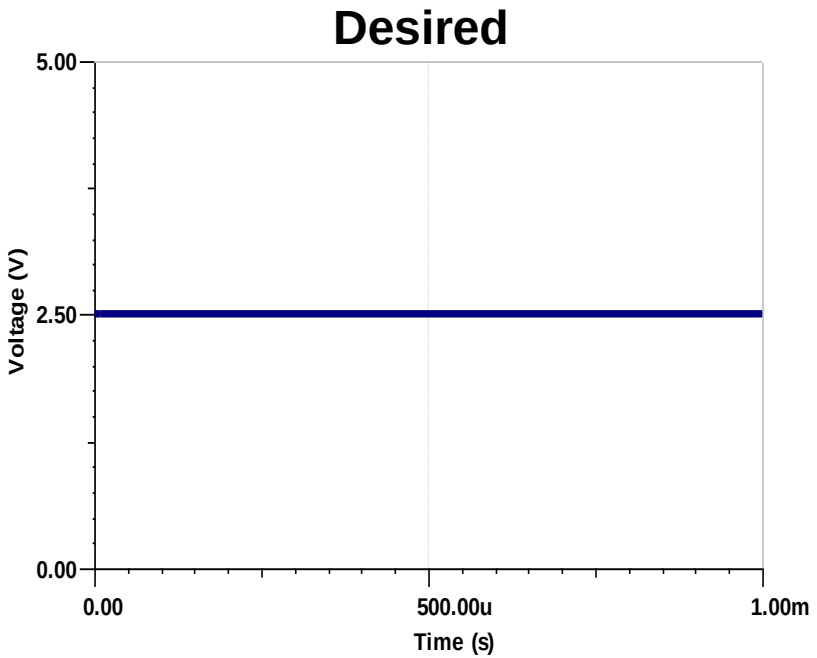
TI Precision Labs Seminar

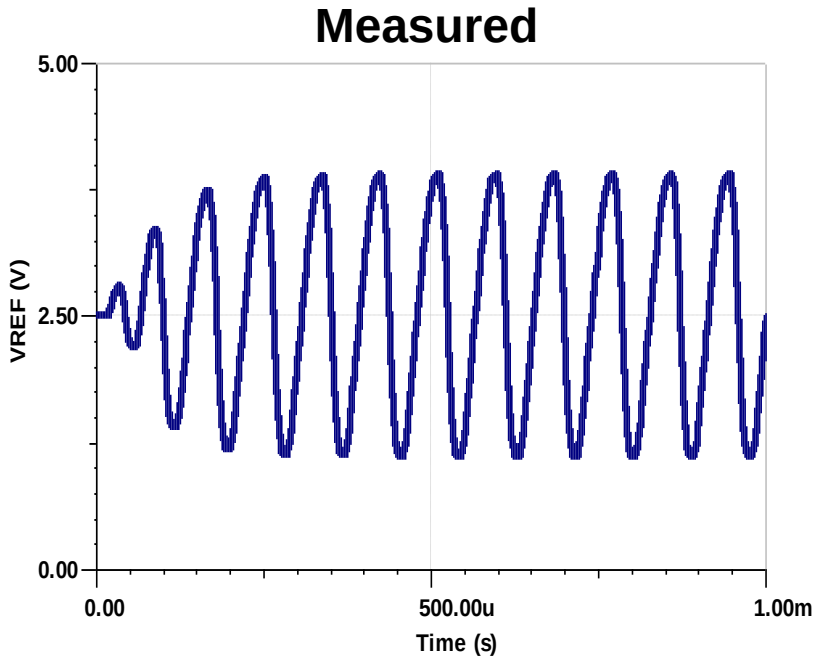
Circuit stability analysis and compensation schemes



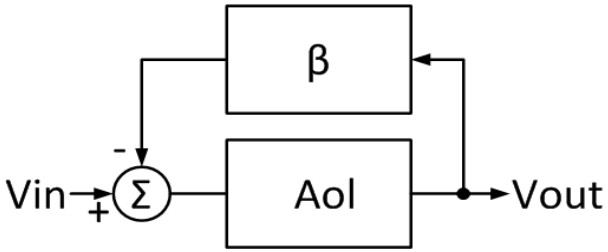
Op amp stability issue



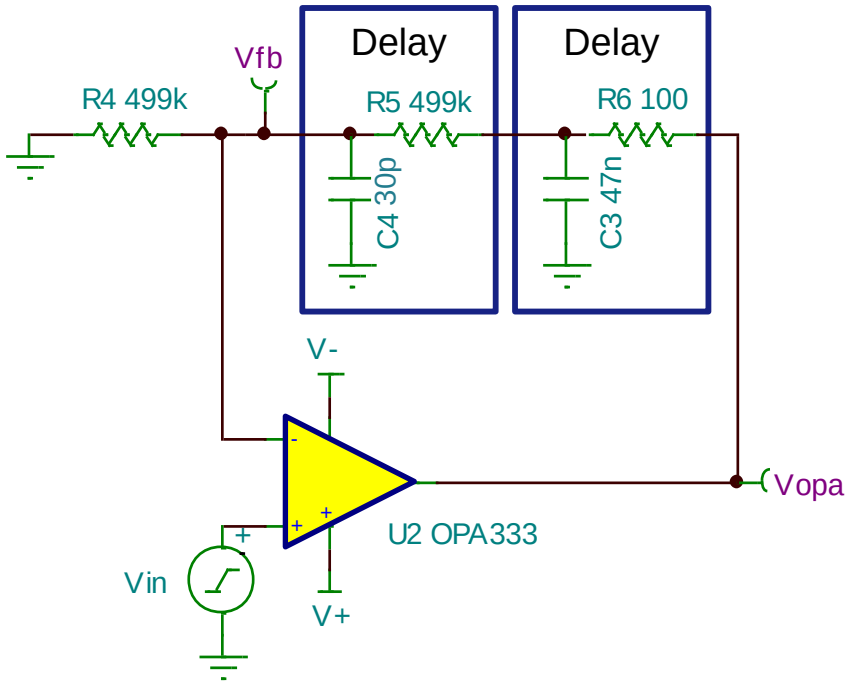


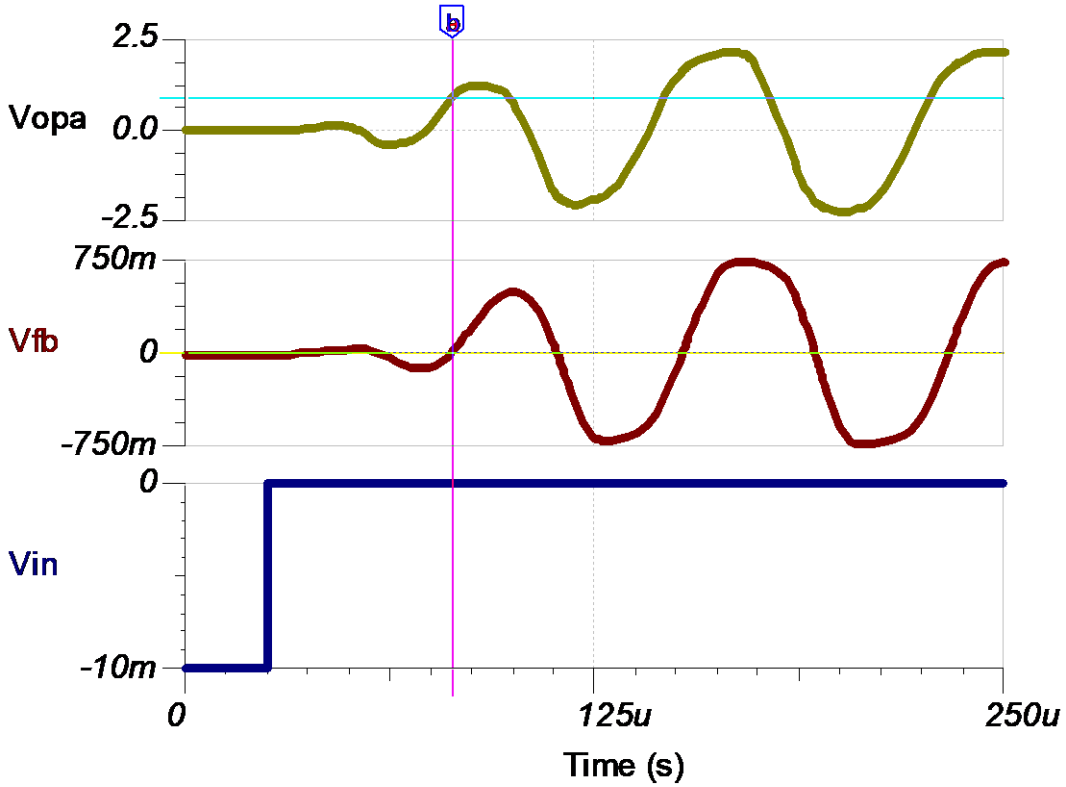


Simplified cause of op amp stability issues

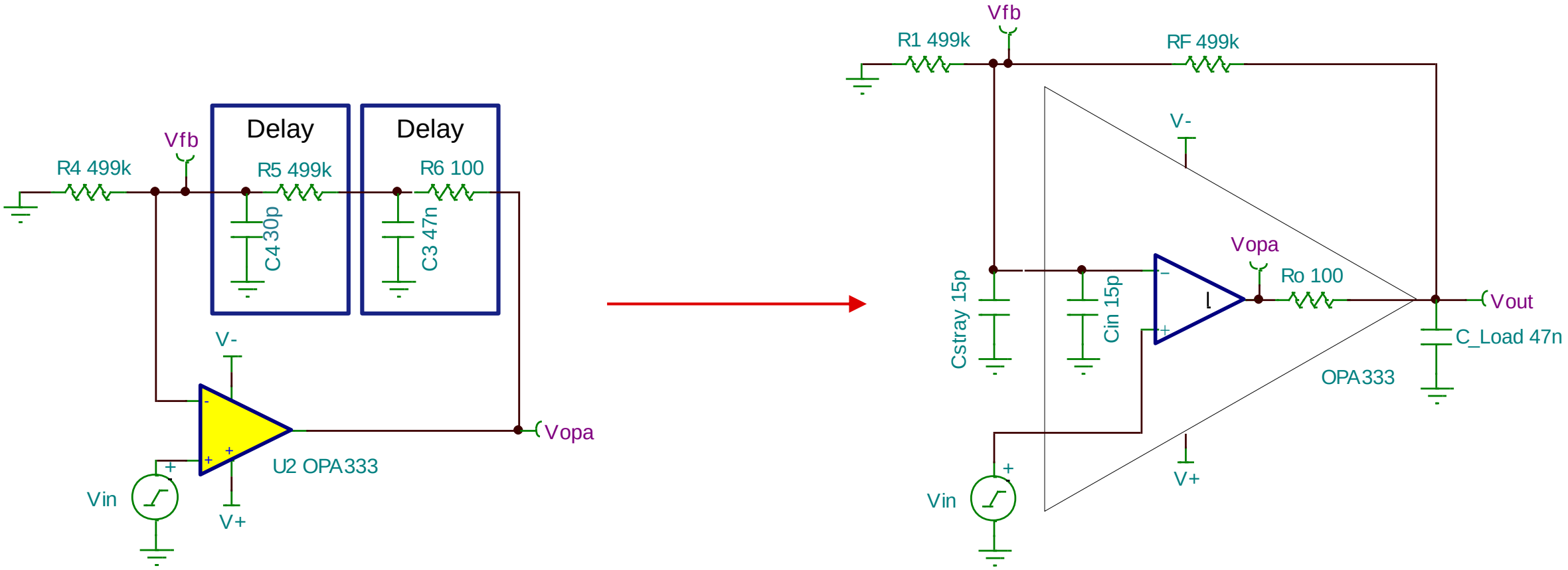


Issues happen because of too much delay from output to feedback!





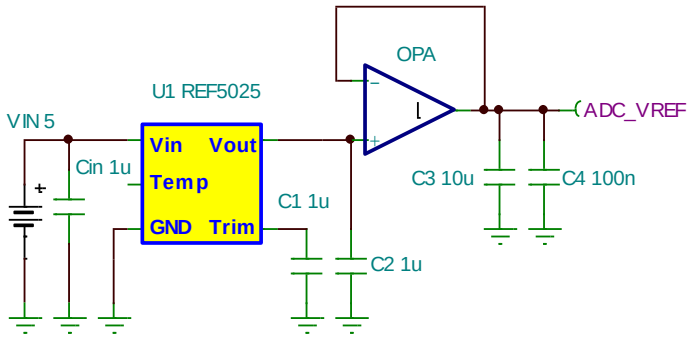
Delay happens in many circuits



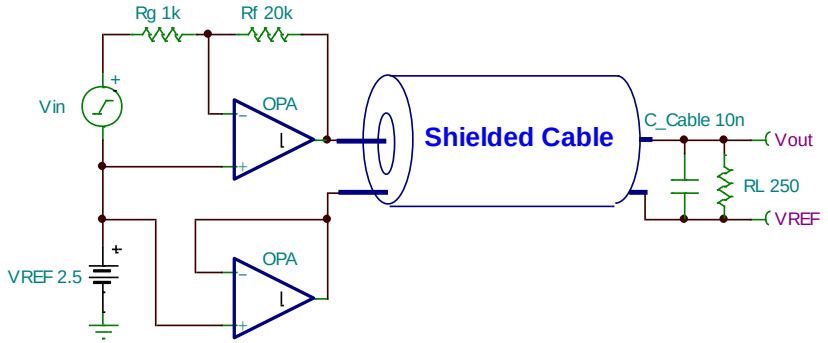
Circuits with possible stability issues

Output Capacitive Loads

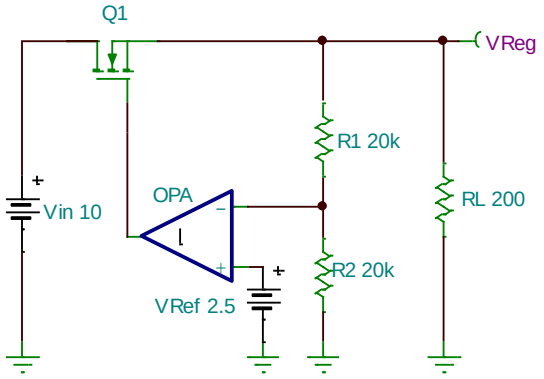
Reference Buffers



Cable/Shield Drive

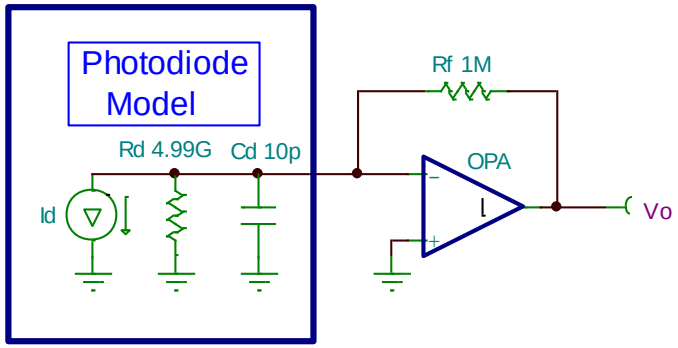


MOSFET Gate Drive

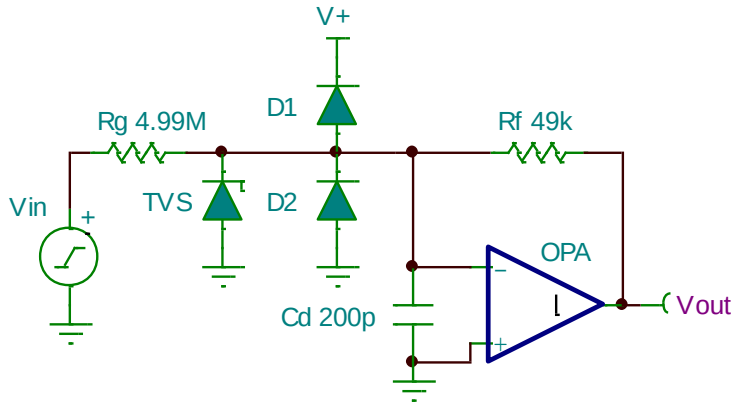


Input Capacitance and Large Value Resistors

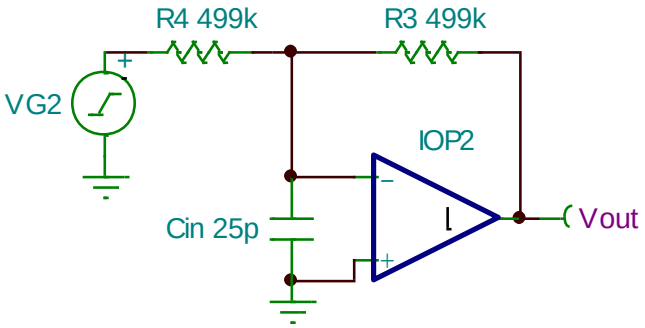
Transimpedance Amplifiers



Transient Suppression



Large Value Resistors for Low-Power Circuits



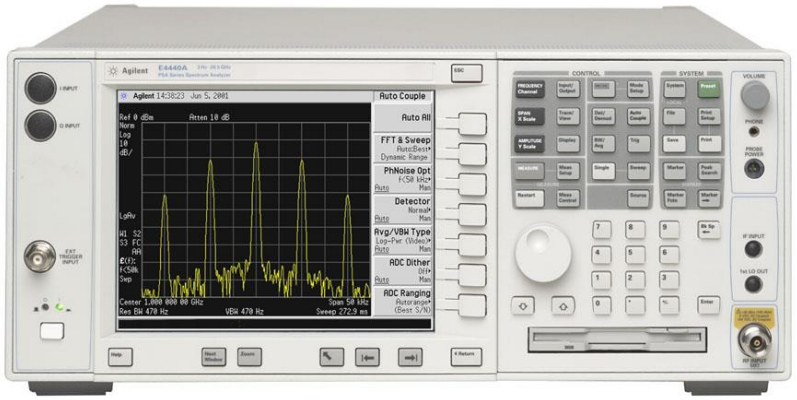
Identify stability issues in the lab

Suggested Tools:

- Oscilloscope
- Signal Generator

Other Useful Tools:

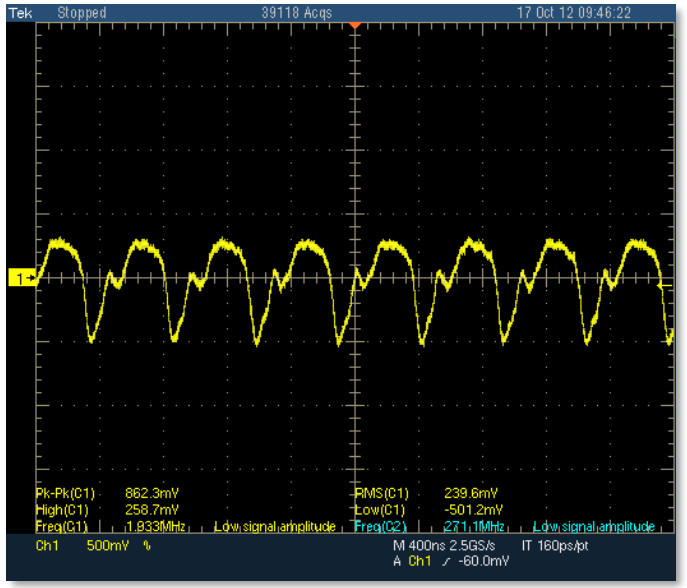
- Gain / Phase Analyzer
- Network / Spectrum Analyzer

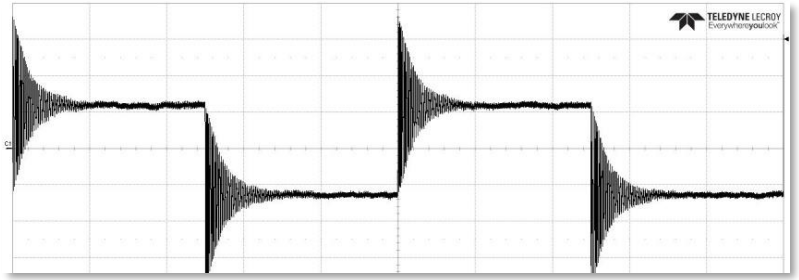


Identify stability issues in the lab

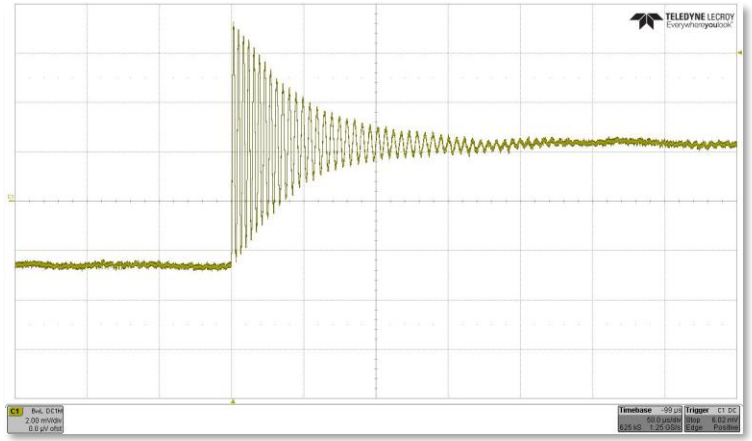
Oscilloscope – Time Domain Analysis:

- Oscillations
- Overshoot and Ringing
- Unstable DC Voltages
- High Distortion

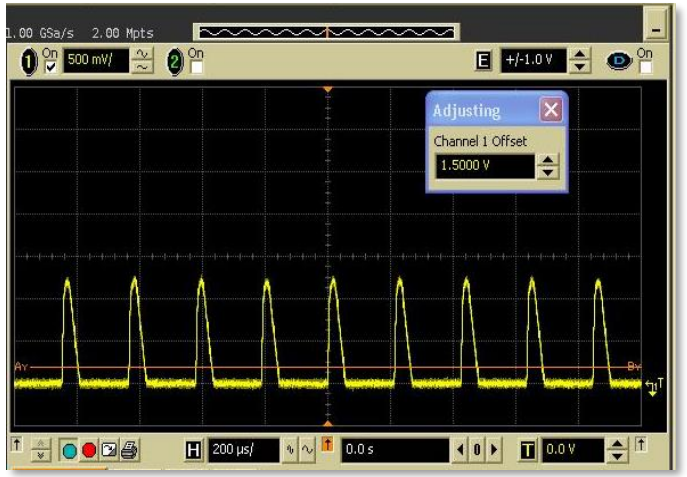




Output Response to Square Wave Input



Output Response to Step Input



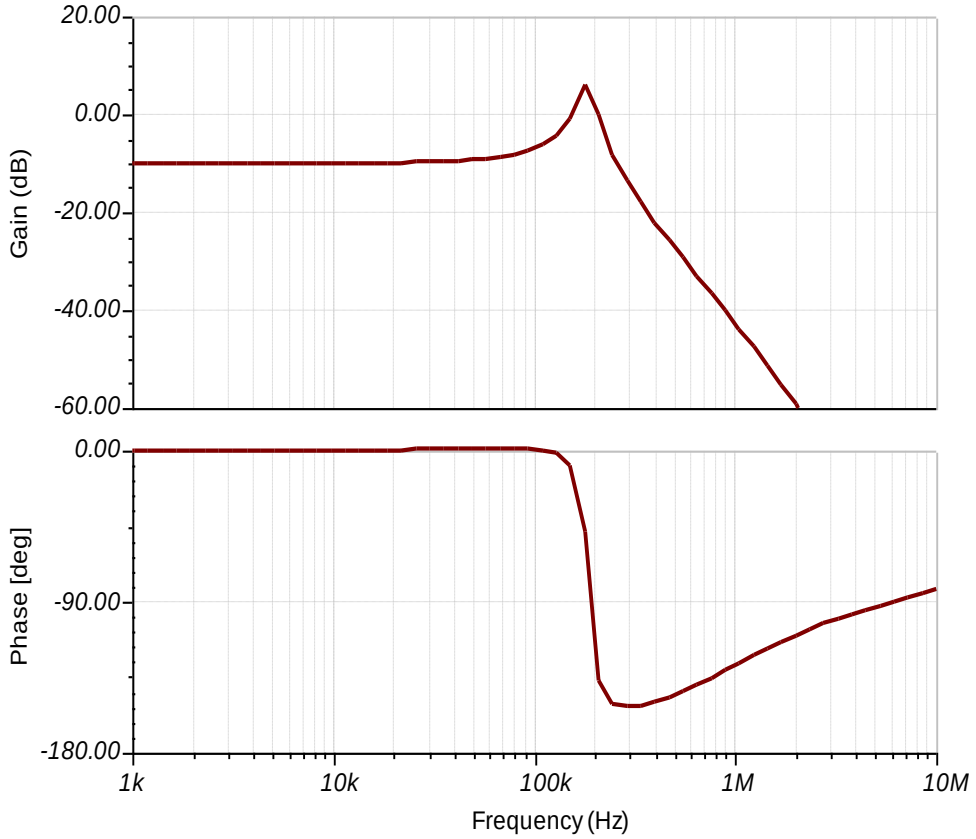
Sustained Output Oscillation with DC Input

Identify stability issues in the lab

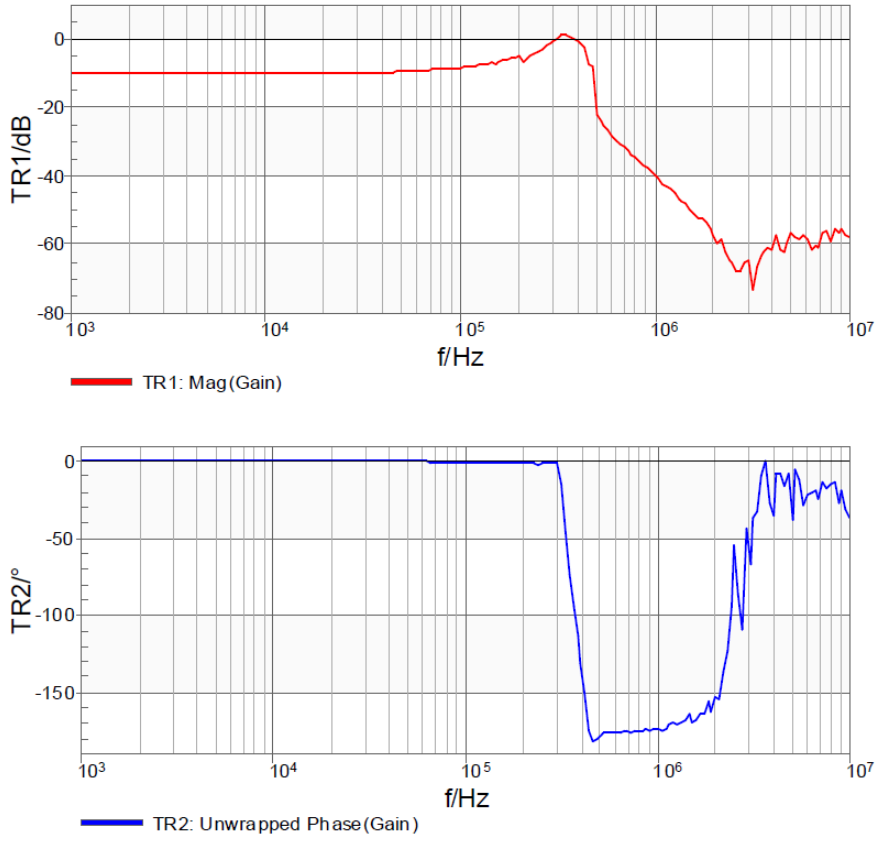
Gain / Phase Analyzer - Frequency Domain:

- Peaking, Unexpected Gains, Rapid Phase Shifts

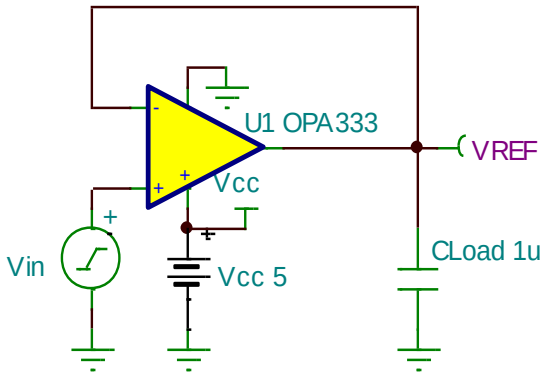
Simulated

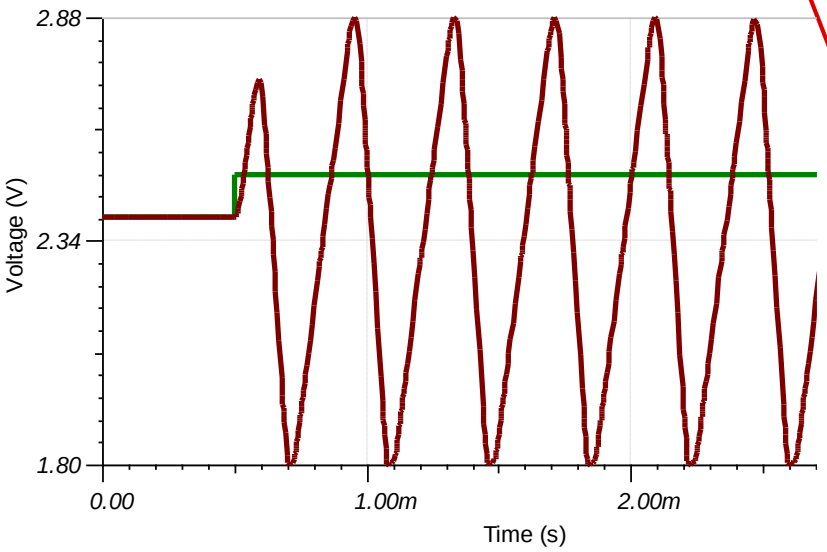


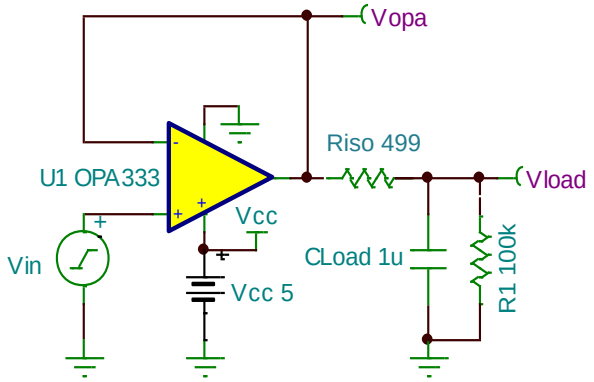
Measured

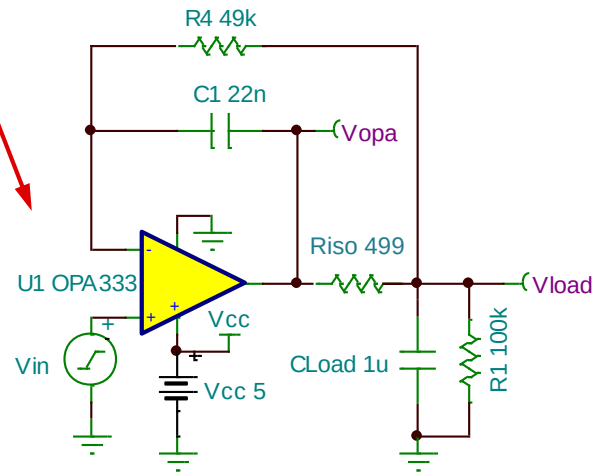


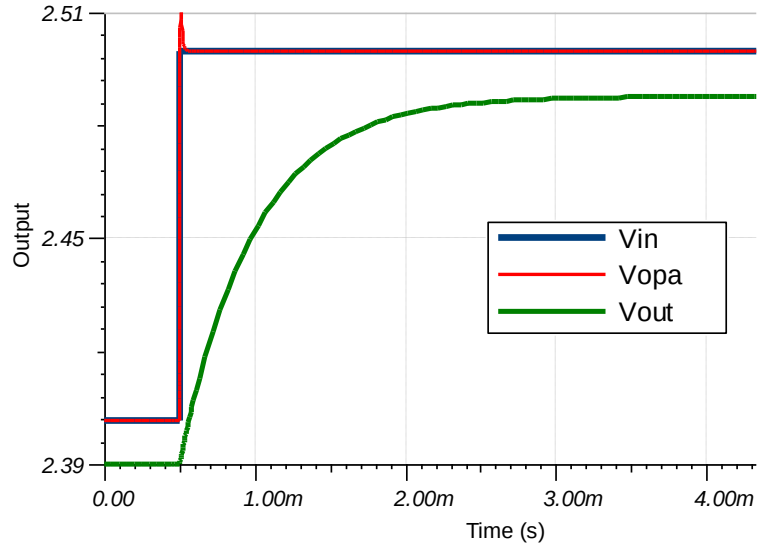
Solving op amp stability issues

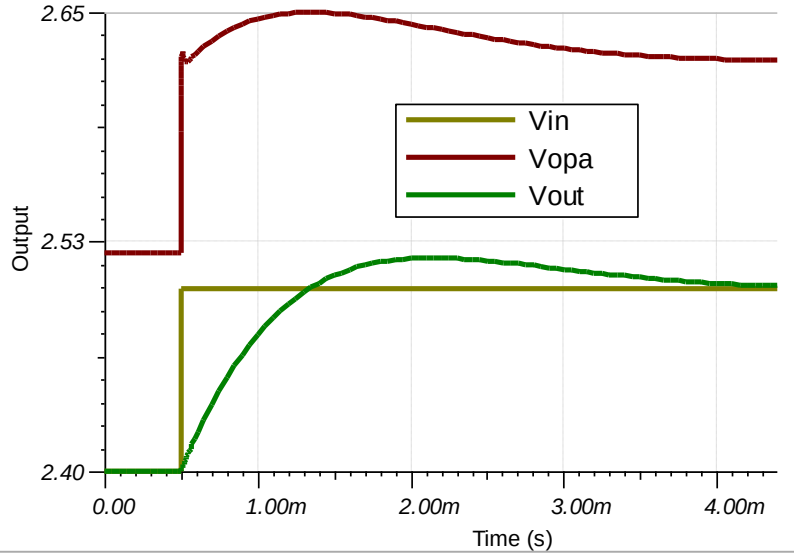




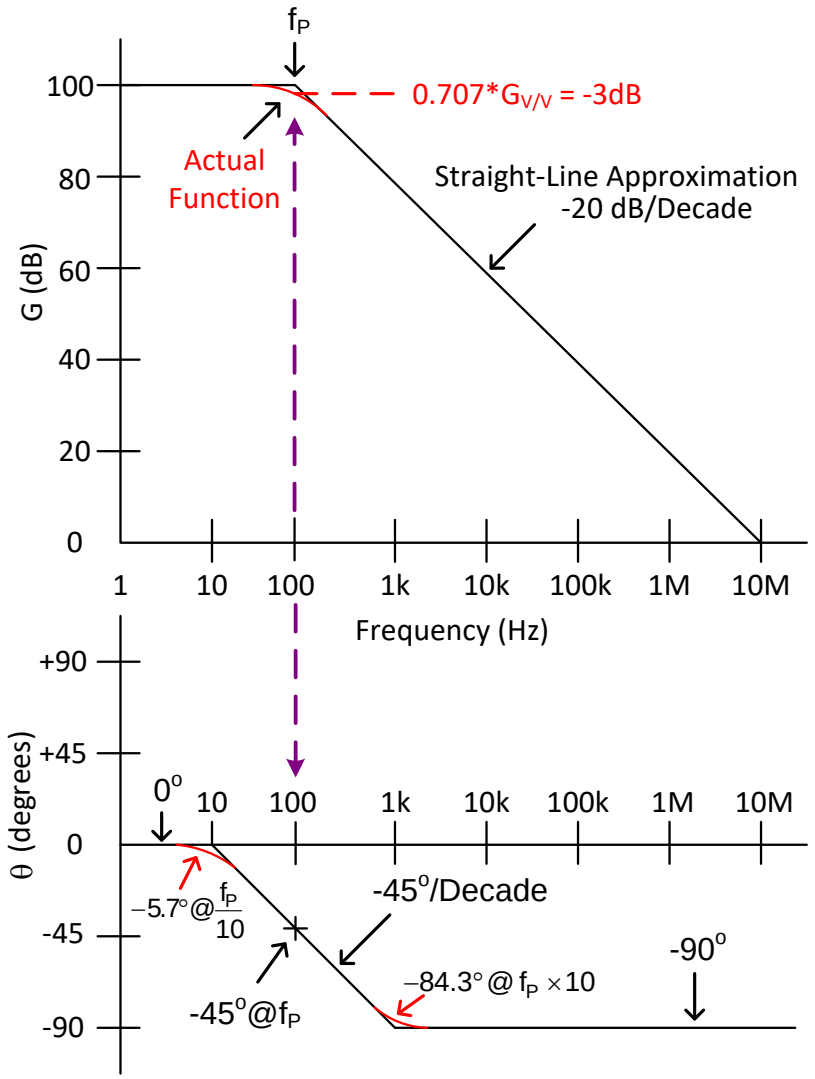








Bode plots – pole



$$G_{V/V} = \frac{Vout}{V_{in}} = \frac{G_{DC}}{\mathrm{j}\left(\frac{f}{f_p}\right) + 1}$$ As a complex number

$$G_{V/V} = \frac{V_{out}}{V_{in}} = \frac{G_{DC}}{\sqrt{\left(\frac{f}{f_p}\right)^2 + 1}}$$ Magnitude

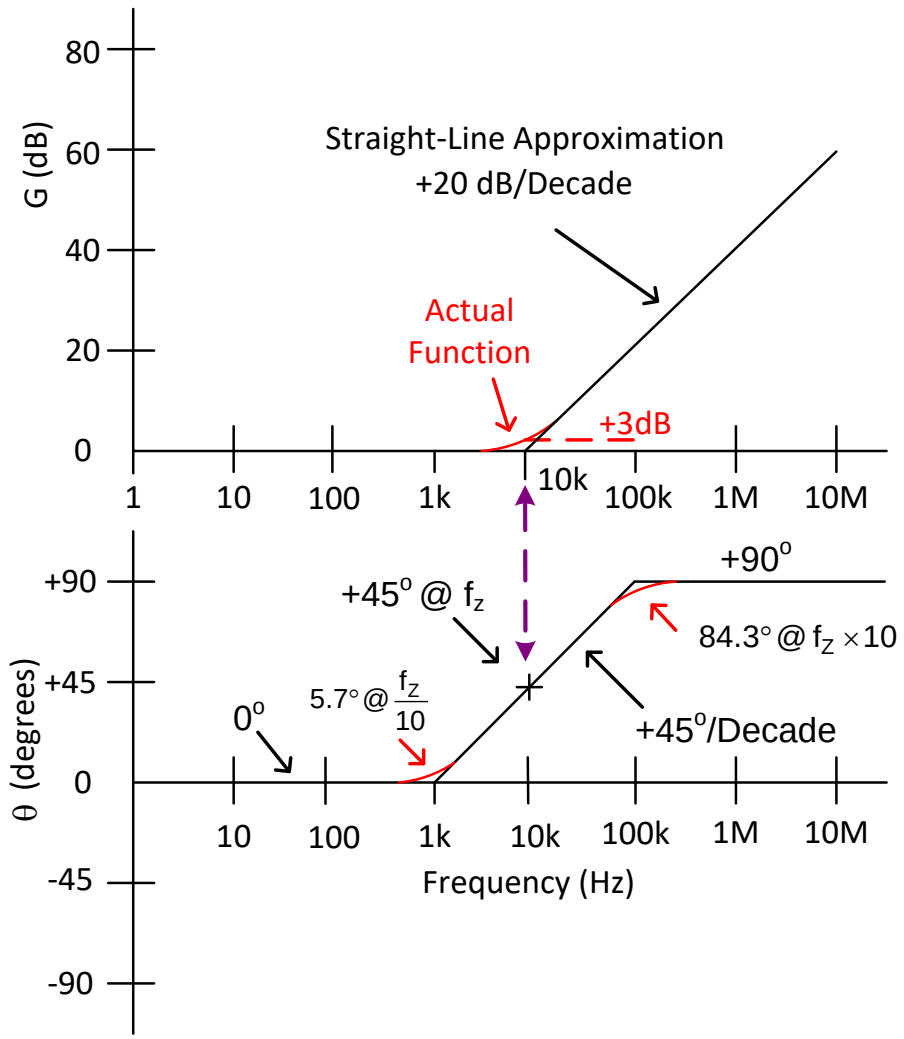
$$\Theta = -\tan^{-1}\left(\frac{f}{f_p}\right)$$ Phase

$$G_{dB} = 20 \times \log_{10}(G_{V/V})$$ Magnitude in dB

Pole location = f_p (cutoff frequency)

	$f << f_p$	$f < 0.1f_p$	$f = f_p$	$f > 10f_p$	$f >> f_p$
Magnitude	G_{DC}	G_{DC}	-3dB	-20dB/dec	-20dB/dec
Phase	0°	-45°/dec	-45°	-45°/dec	-90°

Bode plots – zero



$$G_{V/V} = \frac{Vout}{V_{in}} = G_{DC}\left(\mathrm{i}\left(\frac{f}{f_Z}\right) + 1\right)$$ As a complex number

$$G_{V/V} = \frac{V_{out}}{V_{in}} = G_{DC}\sqrt{\left(\frac{f}{f_p}\right)^2 + 1}$$ Magnitude

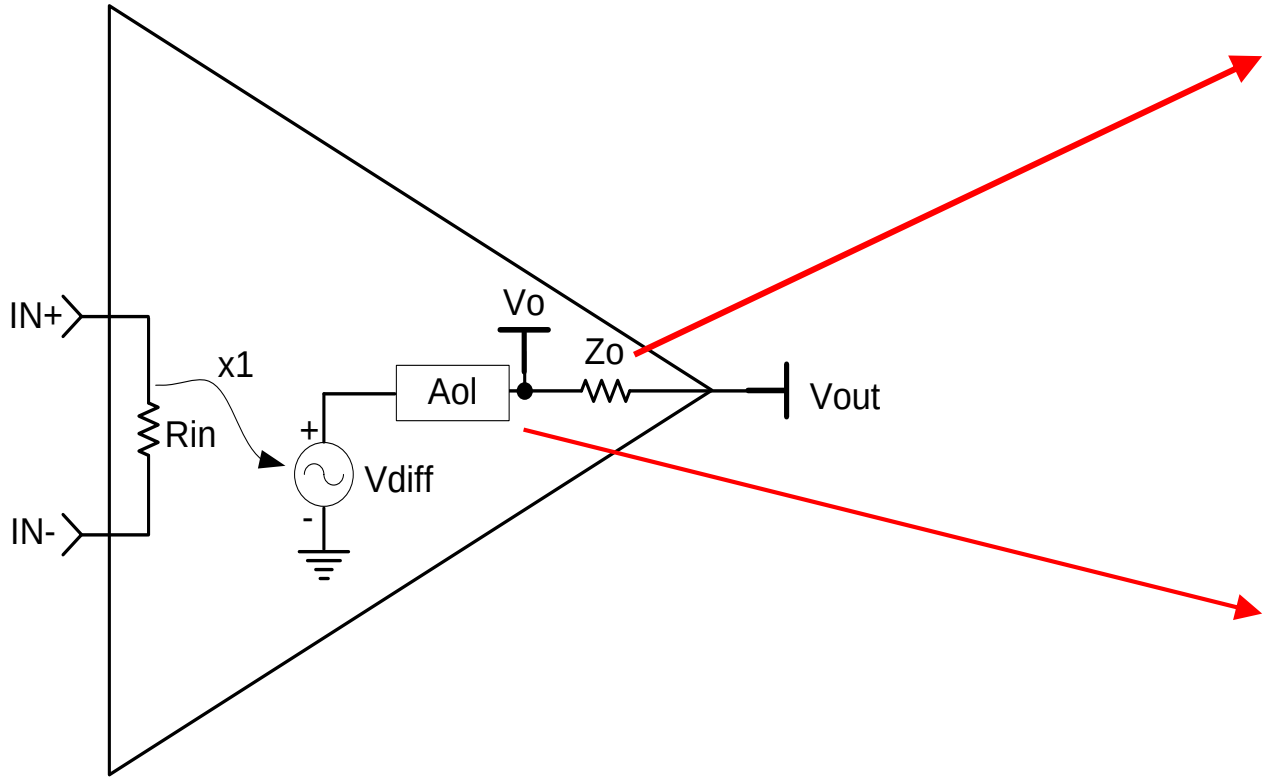
$$\Theta = -\tan^{-1}\left(\frac{f}{f_Z}\right)$$ Phase

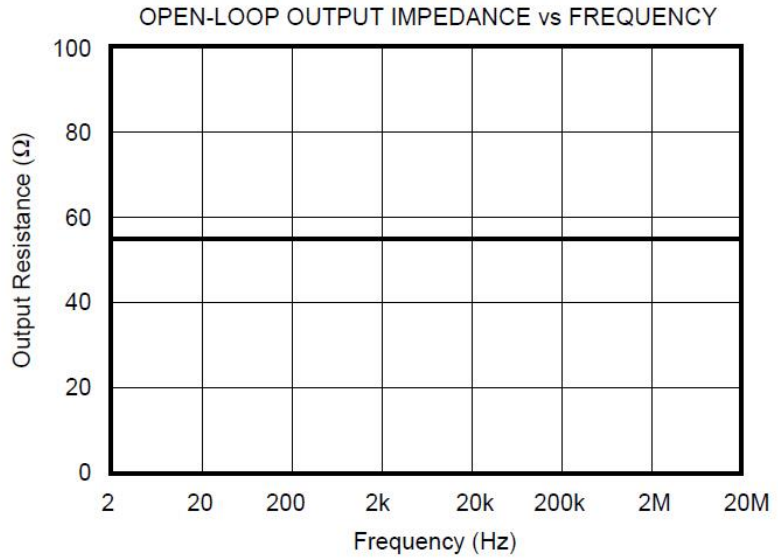
$$G_{dB} = 20 \times \log_{10}(G_{V/V})$$ Magnitude in dB

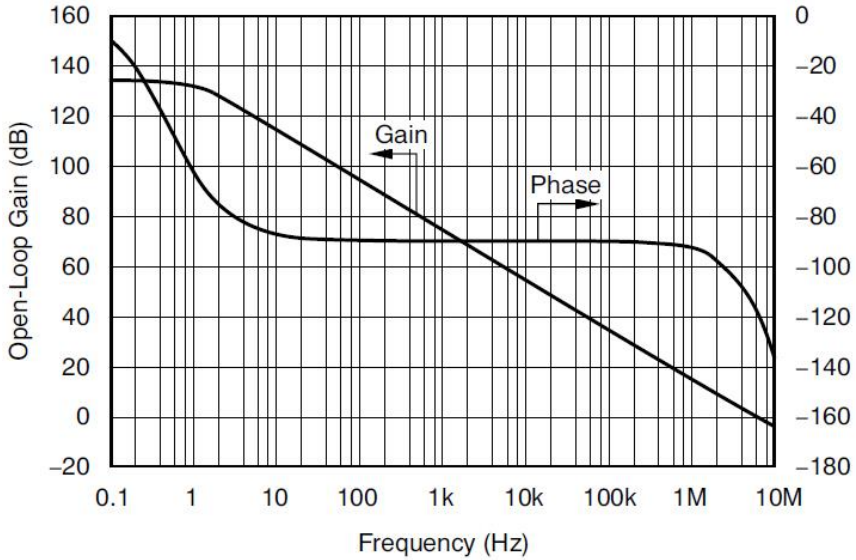
Zero location = f_Z

	$f << f_Z$	$f < 0.1f_p$	$f = f_p$	$f > 10f_p$	$f >> f_p$
Magnitude	0dB	0dB	3dB	+20dB/dec	+20dB/dec
Phase	0°	+45°/dec	45°	+45°/dec	90°

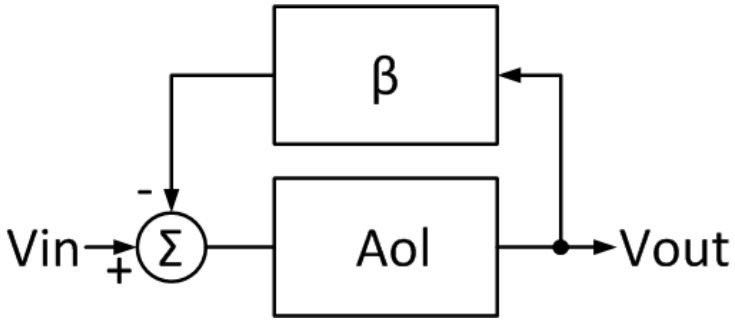
Op amp open loop model

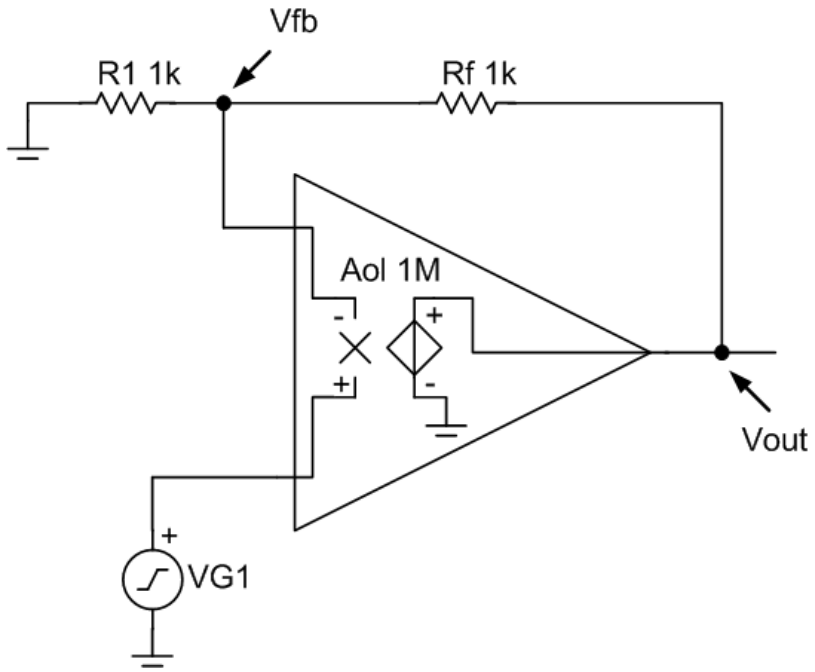






Op amp closed loop model





$A_{OL} = Open\ Loop\ Gain$

$\beta = Feedback\ Factor = \frac{V_{FB}}{V_{OUT}} = \frac{R_1}{R_1 + R_F}$

$A_{CL} = Closed\ Loop\ Gain = \frac{A_{OL}}{1 + A_{OL}\beta}$

$A_{OL}\beta = Loop\ Gain$

$A_{CL} = \lim_{A_{OL}\beta \to \infty} \left(\frac{A_{OL}}{1 + A_{OL}\beta} \right) = \frac{1}{\beta} = 1 + \frac{R_F}{R_1}$

When is an amplifier unstable?

$$\mathbf{A_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta}}$$

$$\beta = Feedback\ Factor = \frac{V_{FB}}{V_{OUT}} = \frac{R_1}{R_1 + R_F}$$

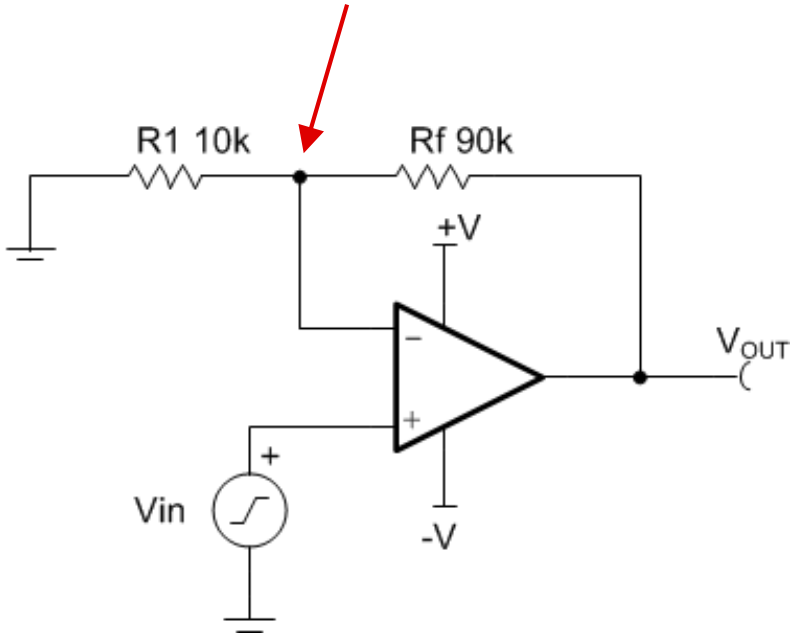
$$A_{CL} = Closed\ Loop\ Gain = \frac{A_{OL}}{1 + A_{OL}\beta}$$

$$A_{OL}\beta = Loop\ Gain$$

$$A_{CL} = \lim_{A_{OL}\beta \to \infty} \left(\frac{A_{OL}}{1 + A_{OL}\beta} \right) = \frac{1}{\beta} = 1 + \frac{R_F}{R_1}$$

- A circuit is unstable when $A_{OL}\beta = -1$
- $A_{OL}\beta = -1$ sets the denominator of $A_{CL} = 0$
- $A_{OL}\beta = -1$ when $A_{OL}\beta(dB) = 0dB$ and phase shift($A_{OL}\beta$) = 180°
  - Phase shift is relative to the DC phase

$A_{OL}\beta = -1$ when the phase at V_{FB} has shifted 180º relative to Vin



Phase Margin (PM):

How close the system is to a 180° phase shift in $A_{OL}\beta$

- PM = Phase($A_{OL}\beta$) when Gain($A_{OL}\beta$) = 0dB
- Ex: 10° phase margin = 170° phase shift in $A_{OL}\beta$

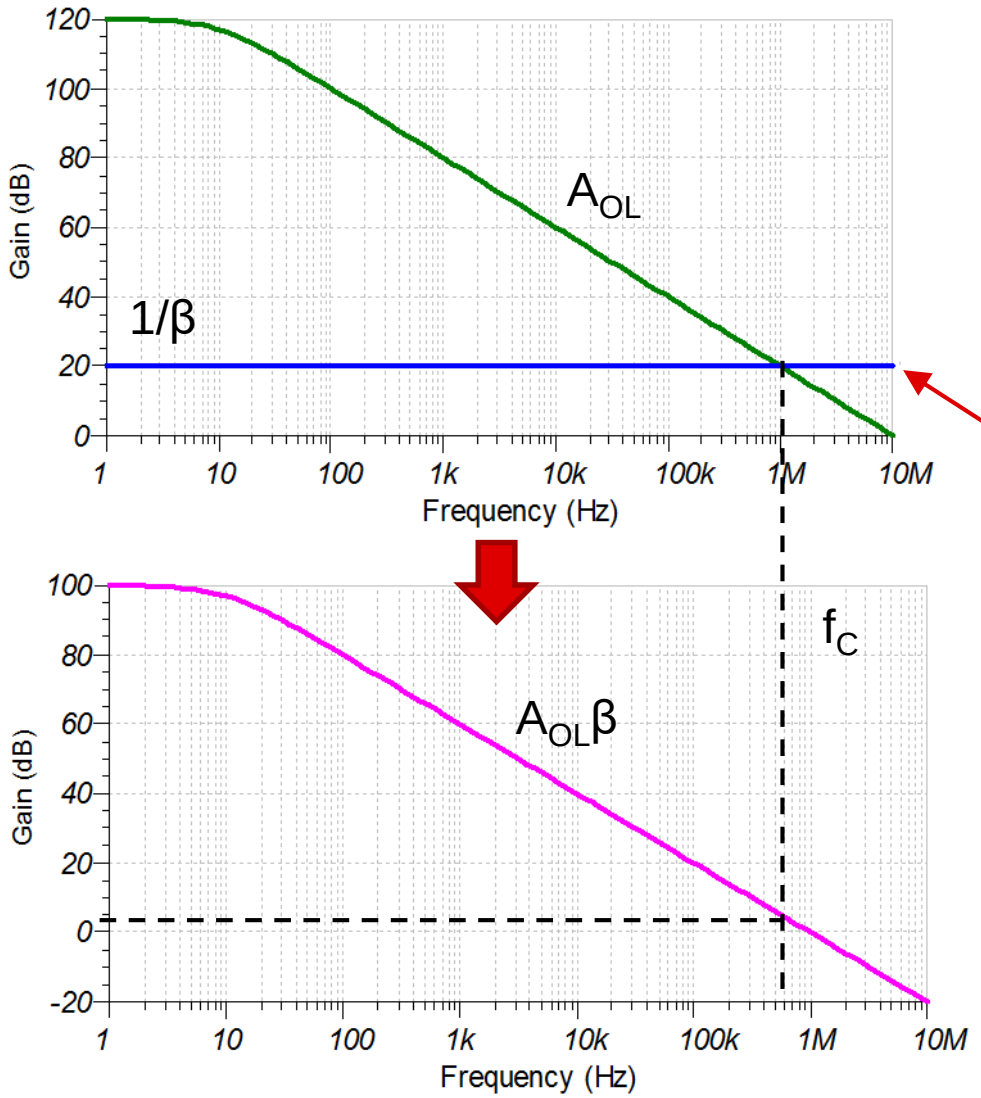
Loop gain magnitude – $A_{OL}\beta$

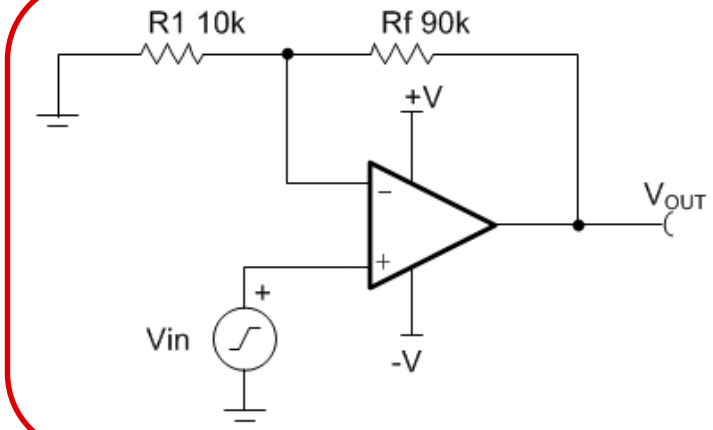
$$\beta = Feedback\ Factor = \frac{V_{FB}}{V_{OUT}} = \frac{R_1}{R_1 + R_F}$$

$$A_{CL} = Closed\ Loop\ Gain = \frac{A_{OL}}{1 + A_{OL}\beta}$$

$$A_{OL}\beta = Loop\ Gain$$

$$A_{CL} = \lim_{A_{OL}\beta \to \infty} \left(\frac{A_{OL}}{1 + A_{OL}\beta} \right) = \frac{1}{\beta} = 1 + \frac{R_F}{R_1}$$





$$\frac{1}{\beta} = \frac{V_{OUT}}{V_{FB}} = \frac{R_F}{R_1} + 1 = 10\,V/V$$

$$\frac{1}{\beta}(dB) = 20log(10) = 20dB$$

Loop gain in dB:

$$20\log(A_{OL}\beta) = 20\log(A_{OL}) - 20\log\left(\frac{1}{\beta}\right)$$

$$A_{OL}\beta(dB) = A_{OL}(dB) - \frac{1}{\beta}(dB)$$

Note: $A_{OL}\beta(dB) = 0dB$ when A_{OL} and $\frac{1}{\beta}$ intersect

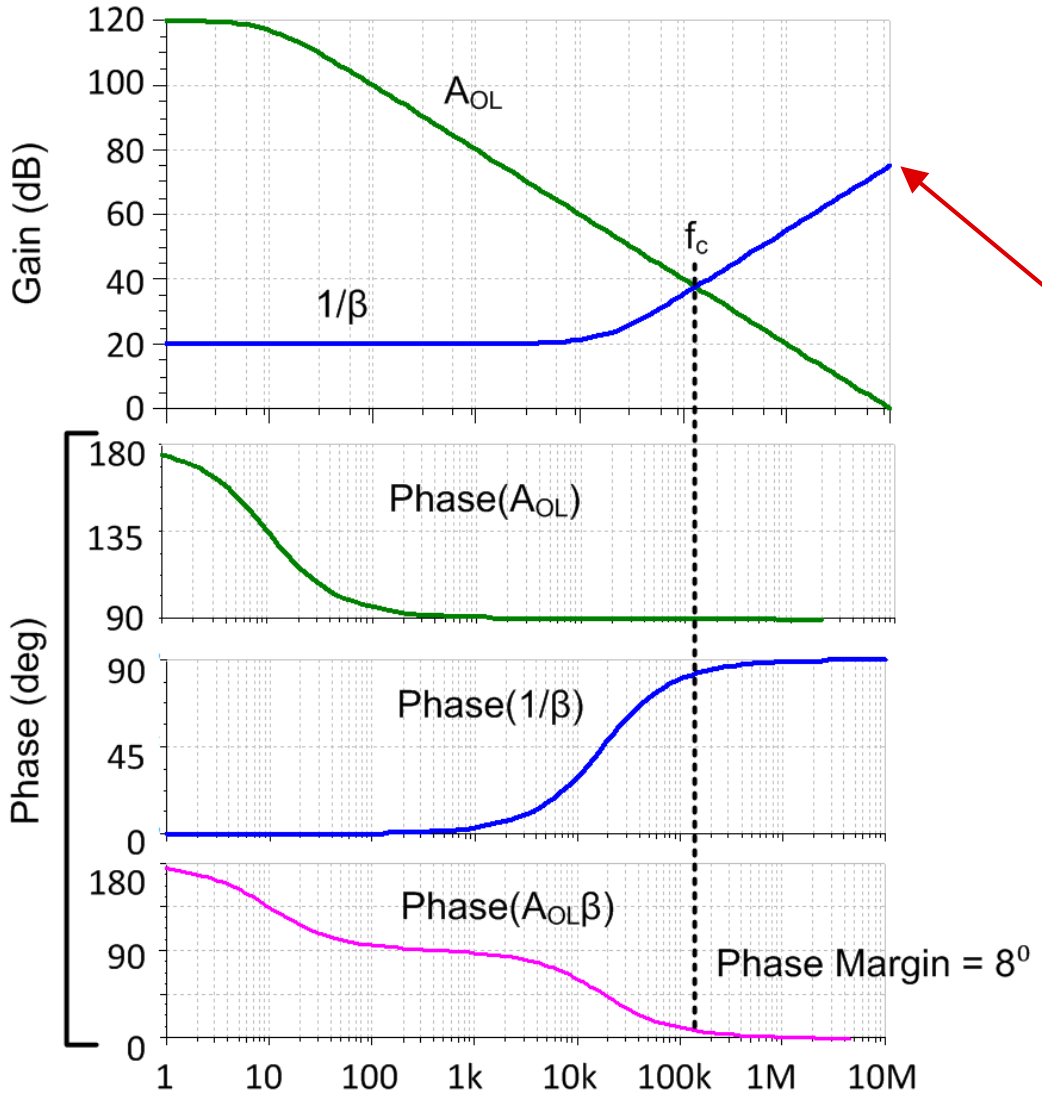
Loop gain phase – phase($A_{OL}\beta$)

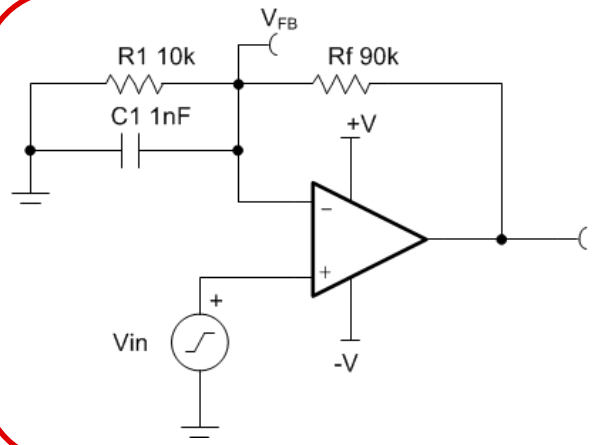
$$\beta = Feedback\ Factor = \frac{V_{FB}}{V_{OUT}} = \frac{R_1}{R_1 + R_F}$$

$$A_{CL} = Closed\ Loop\ Gain = \frac{A_{OL}}{1 + A_{OL}\beta}$$

$$A_{OL}\beta = Loop\ Gain$$

$$A_{CL} = \lim_{A_{OL}\beta \to \infty} \left(\frac{A_{OL}}{1 + A_{OL}\beta} \right) = \frac{1}{\beta} = 1 + \frac{R_F}{R_1}$$





C1 introduces a zero in $\frac{1}{\beta}$

$$\frac{1}{\beta} = \frac{Z_f}{Z_1} + 1$$

Frequency (f)	Capacitor	Gain
At DC	C_1 is open	10V/V
As f increases	C_1 causes Z_1 to decrease	+20dB/decade

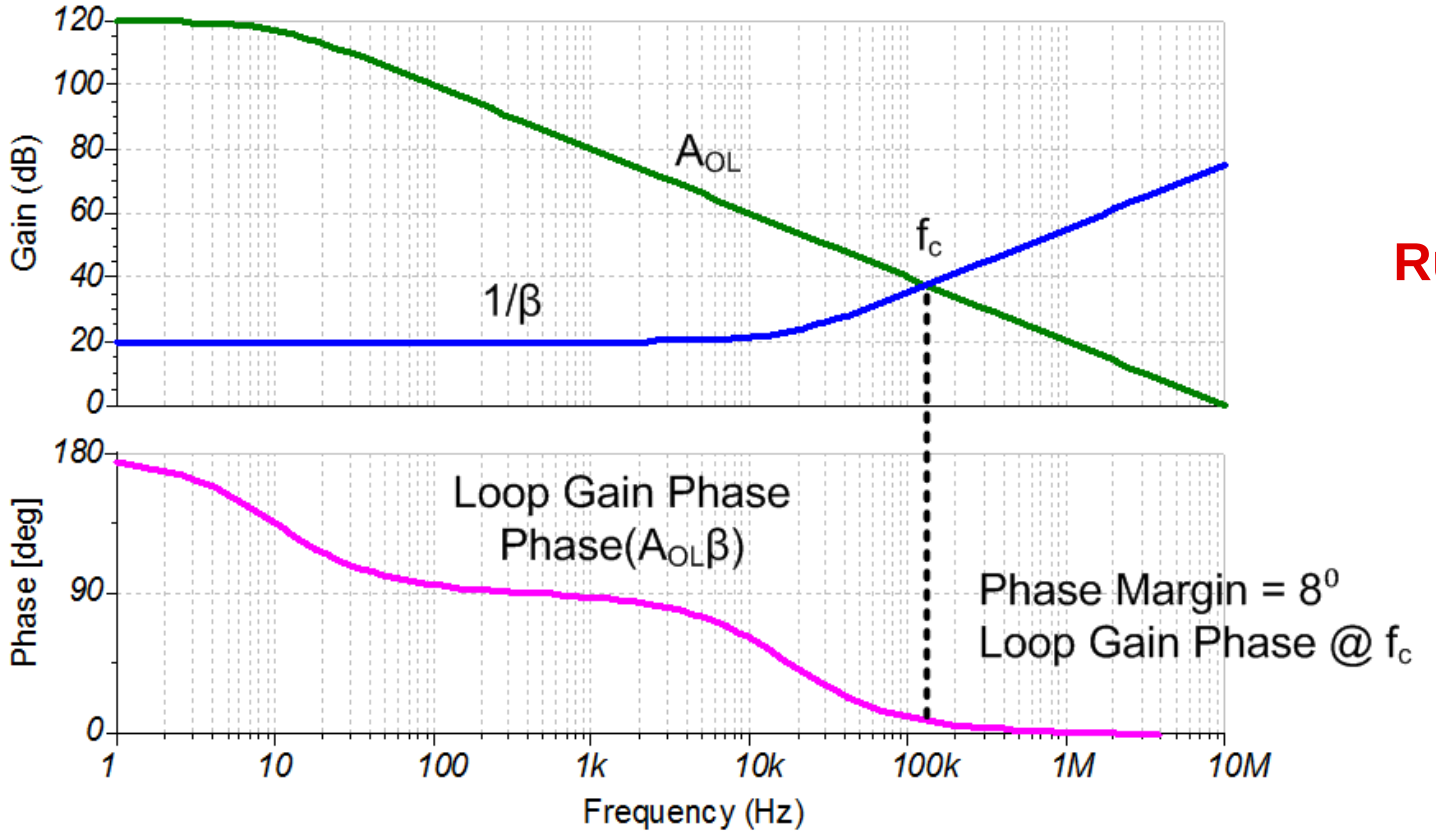
Phase margin

$$\beta = Feedback\ Factor = \frac{V_{FB}}{V_{OUT}} = \frac{R_1}{R_1 + R_F}$$

$$A_{CL} = Closed\ Loop\ Gain = \frac{A_{OL}}{1 + A_{OL}\beta}$$

$$A_{OL}\beta = Loop\ Gain$$

$$A_{CL} = \lim_{A_{OL}\beta \to \infty} \left(\frac{A_{OL}}{1 + A_{OL}\beta} \right) = \frac{1}{\beta} = 1 + \frac{R_F}{R_1}$$



Rule of thumb: Phase margin > 45° is required for optimal stability!

- Phase margin < 45° is considered "marginally stable"
- This does not ensure a robust design over process variation

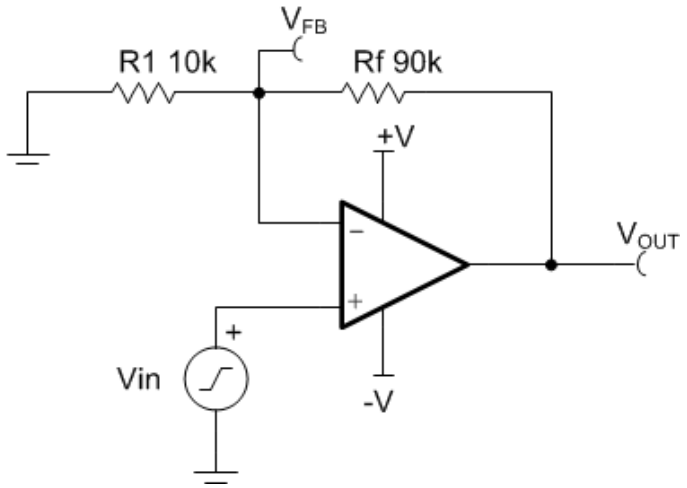
Rate of closure – unstable example

$$\beta = Feedback\ Factor = \frac{V_{FB}}{V_{OUT}} = \frac{R_1}{R_1 + R_F}$$

$$A_{CL} = Closed\ Loop\ Gain = \frac{A_{OL}}{1 + A_{OL}\beta}$$

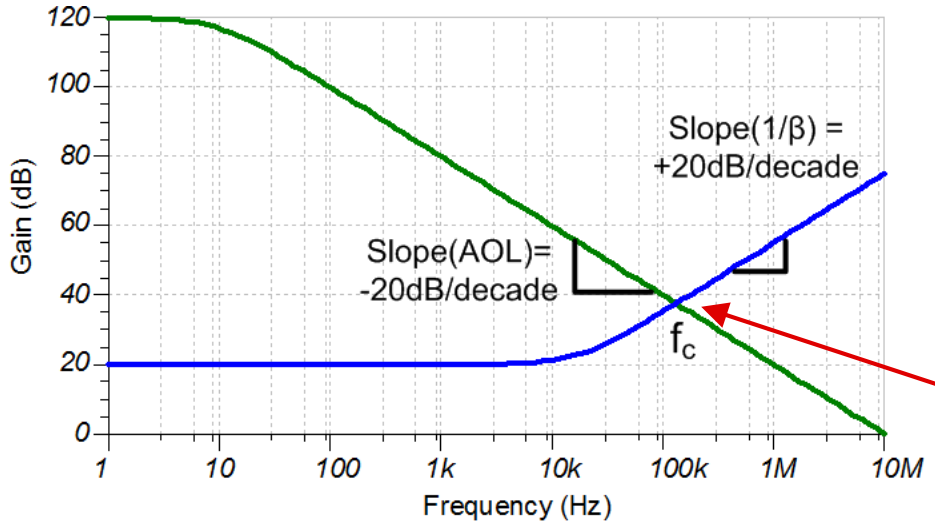
$$A_{OL}\beta = Loop\ Gain$$

$$A_{CL} = \lim_{A_{OL}\beta \to \infty} \left(\frac{A_{OL}}{1 + A_{OL}\beta} \right) = \frac{1}{\beta} = 1 + \frac{R_F}{R_1}$$



$$\frac{1}{\beta} = \frac{V_{OUT}}{V_{FB}} = 10\left(\frac{f}{f_C} + 1\right)$$

1/β(dB) = 20dB at DC, then increases by +20dB/decade after the zero frequency



Rule of thumb: Rate of closure = 20dB is required for optimal stability!

$$Rate\ of\ Closure = \left| Slope(A_{OL}) - Slope\left(\frac{1}{\beta}\right) \right|$$

$$Rate\ of\ Closure = |-20dB - (+20dB)| = 40dB$$

Unstable because rate of closure > 20dB!

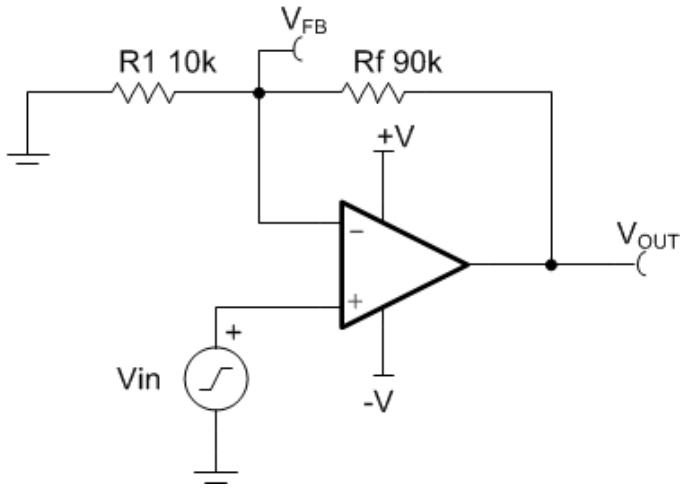
Rate of closure – stable example

$$\beta = Feedback\ Factor = \frac{V_{FB}}{V_{OUT}} = \frac{R_1}{R_1 + R_F}$$

$$A_{CL} = Closed\ Loop\ Gain = \frac{A_{OL}}{1 + A_{OL}\beta}$$

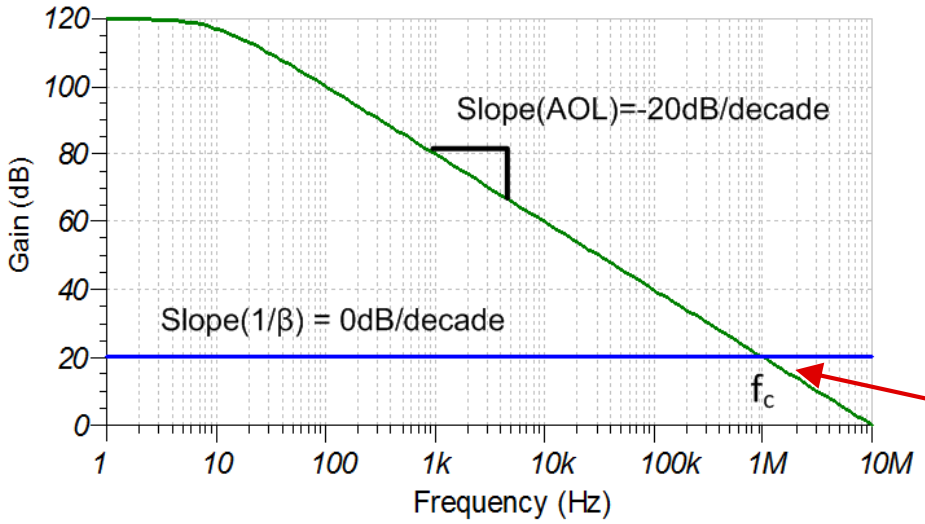
$$A_{OL}\beta = Loop\ Gain$$

$$A_{CL} = \lim_{A_{OL}\beta \to \infty} \left(\frac{A_{OL}}{1 + A_{OL}\beta} \right) = \frac{1}{\beta} = 1 + \frac{R_F}{R_1}$$



$$\frac{1}{\beta} = \frac{V_{OUT}}{V_{FB}} = \frac{R_F}{R_1} + 1 = 10\,V/V$$

$$\frac{1}{\beta}(dB) = 20log(10) = 20dB$$



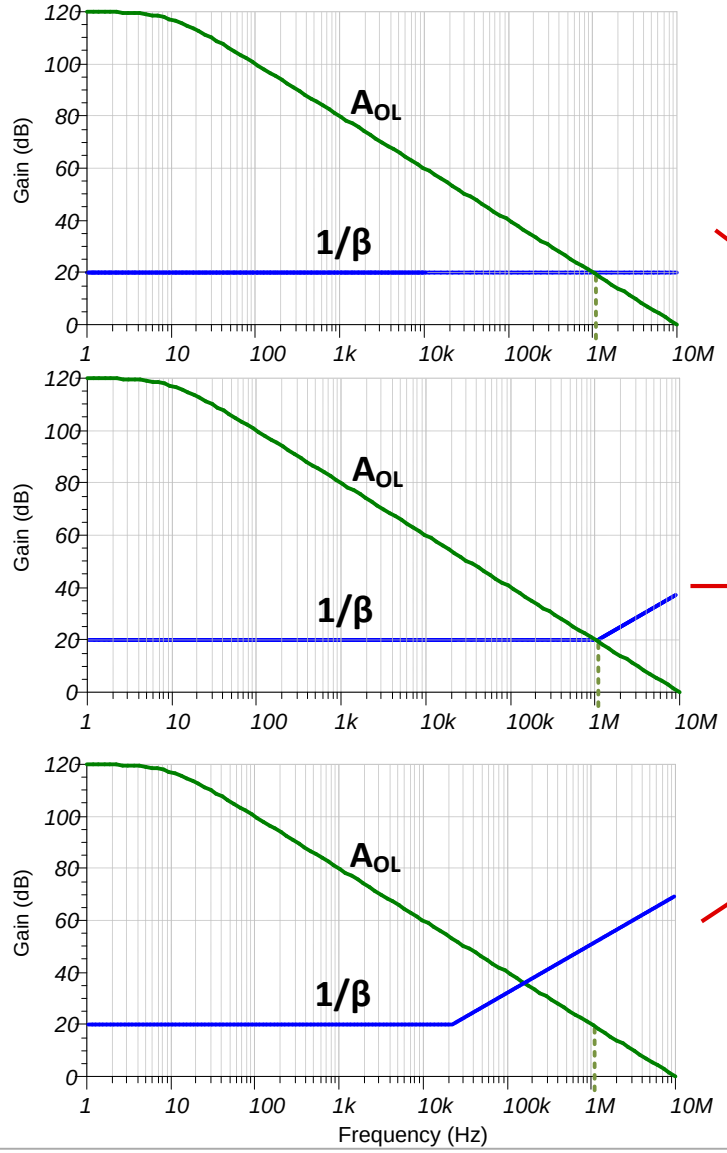
Rule of thumb: Rate of closure = 20dB is required for optimal stability!

$$Rate\ of\ Closure = \left| Slope(A_{OL}) - Slope\left(\frac{1}{\beta}\right) \right|$$

$$Rate\ of\ Closure = |-20dB - 0dB| = 20dB$$

Stable because rate of closure = 20dB!

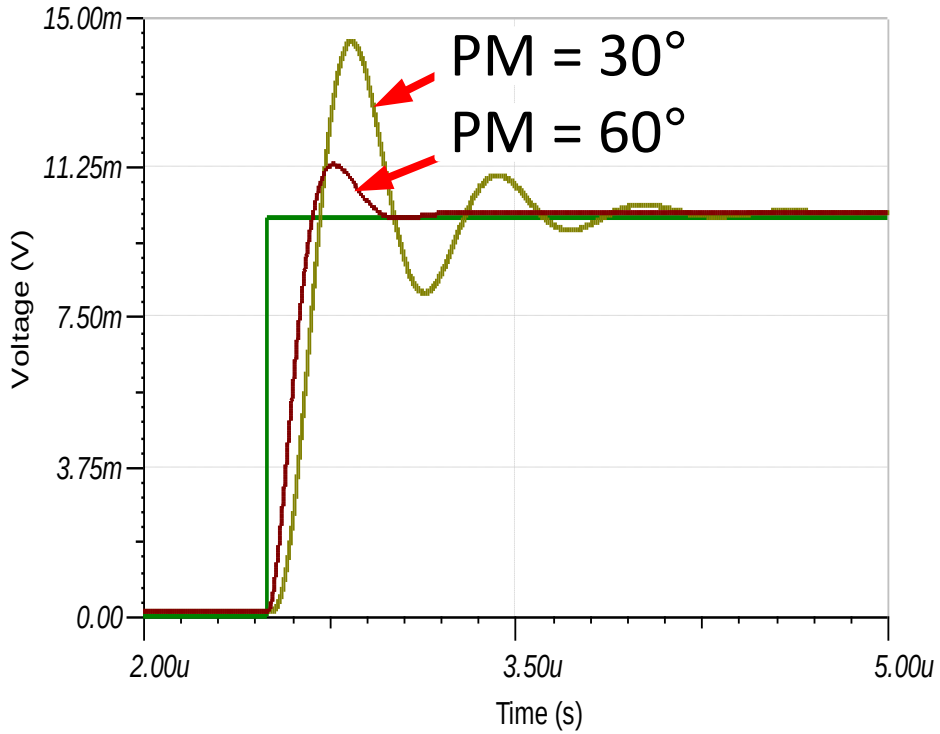
Rate of closure (ROC) and phase margin



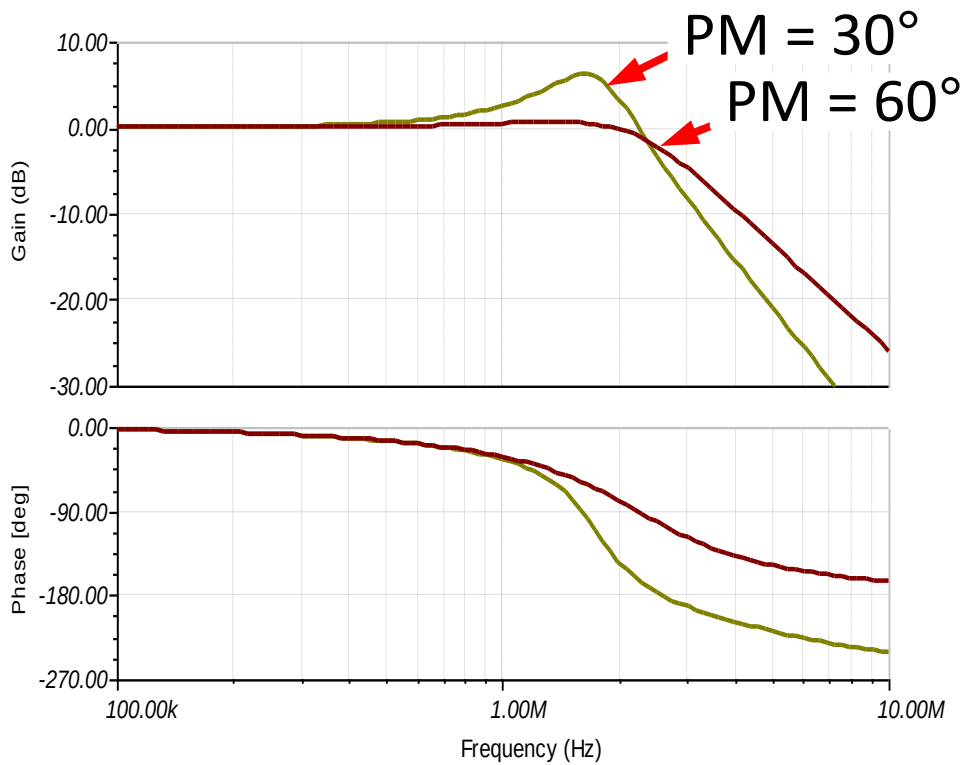
ROC (dB/decade)	Phase Margin (°)
20	45 < PM < 90
20 < ROC < 40	45
40	0 < PM < 45

Indirect phase margin measurements

Phase Margin can be measured indirectly on closed-loop circuits!

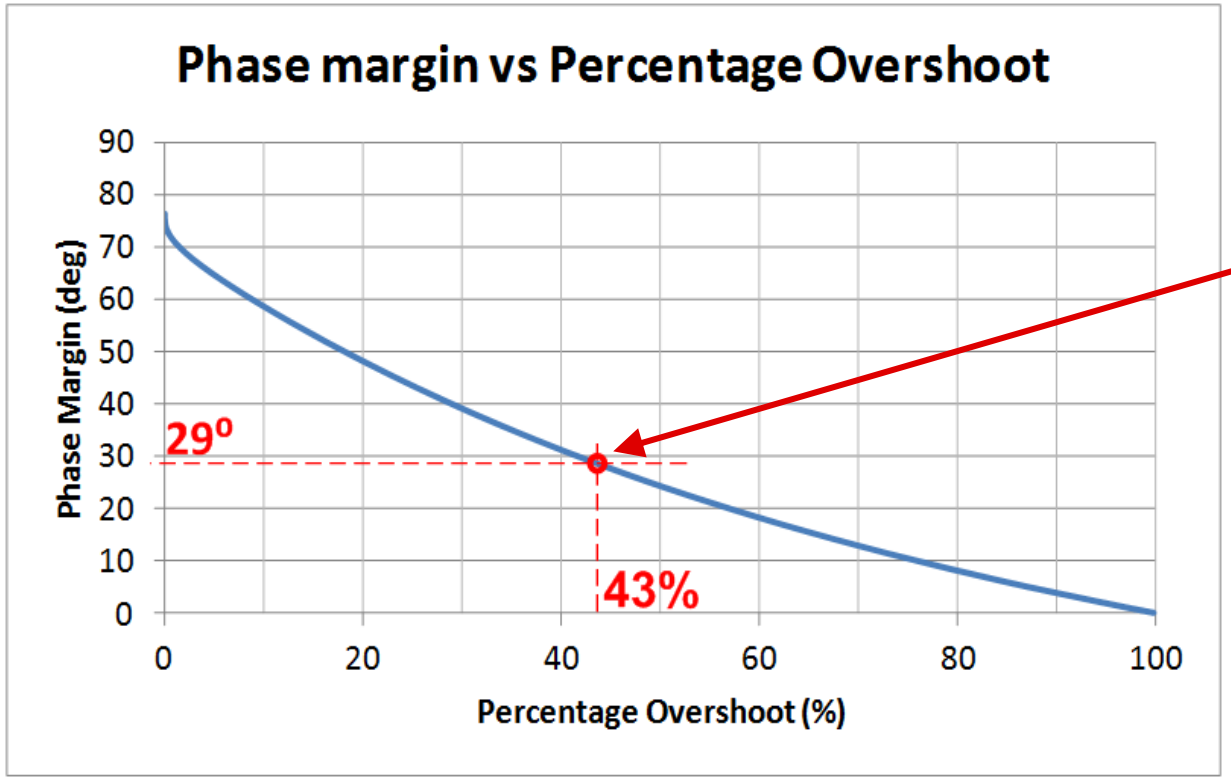


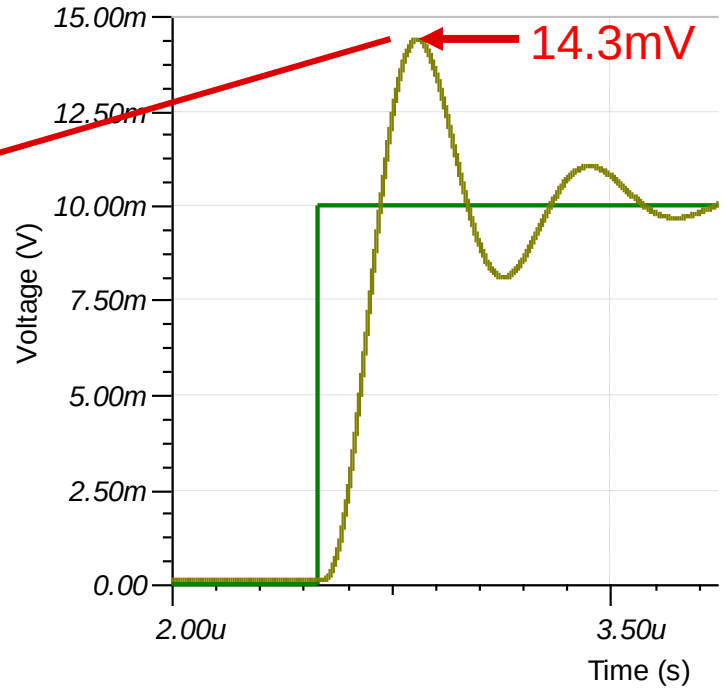
Time Domain → Percent Overshoot



AC Gain/Phase → AC Peaking

Indirect phase margin measurements

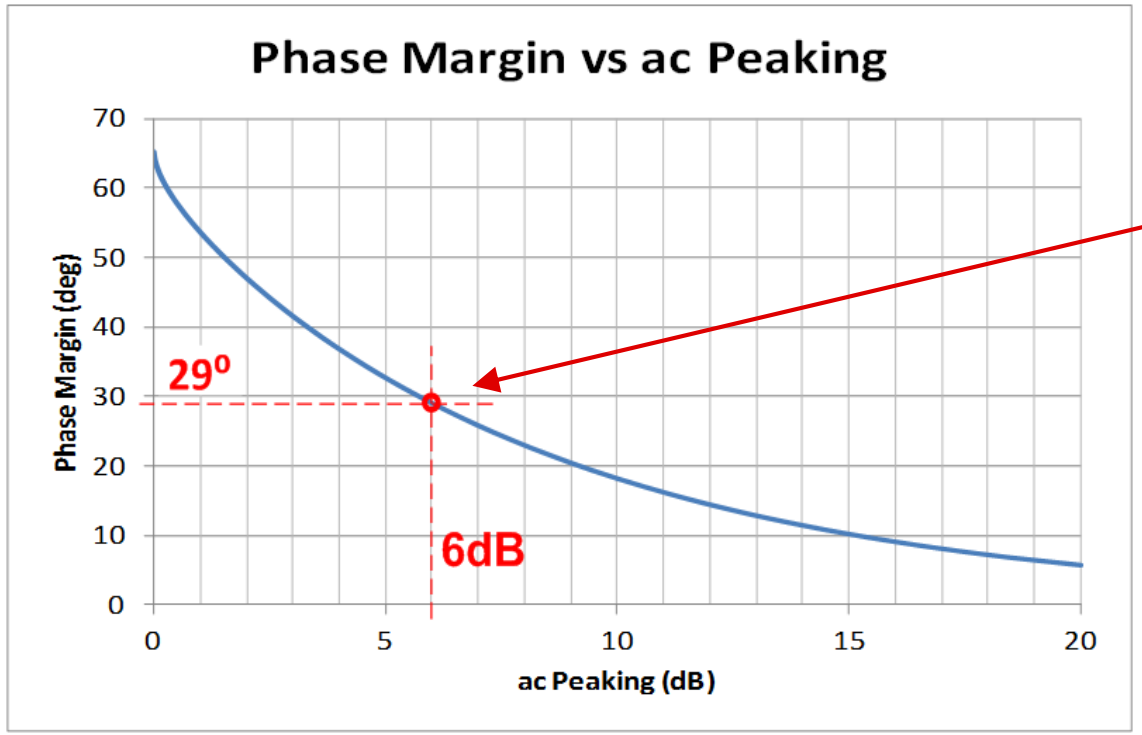


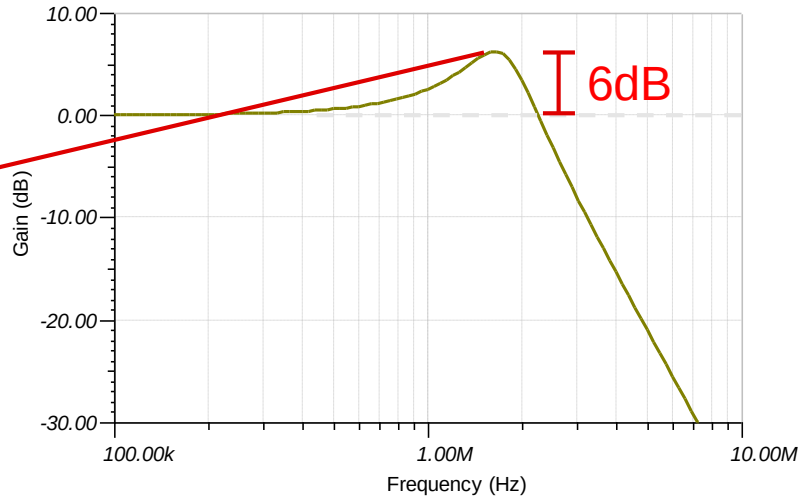


$$\%\ \text{Overshoot} = \left(\frac{14.3\text{mV} - 10\text{mV}}{10\text{mV}}\right) * 100\% = \mathbf{43\%}$$

43% overshoot → **29° phase margin**

Indirect phase margin measurements

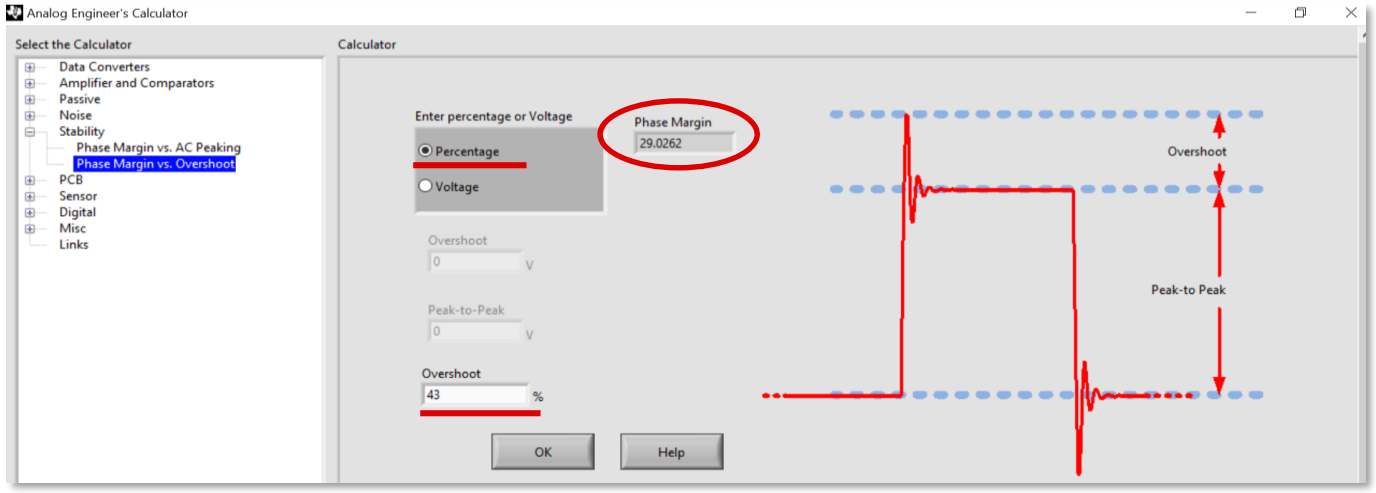


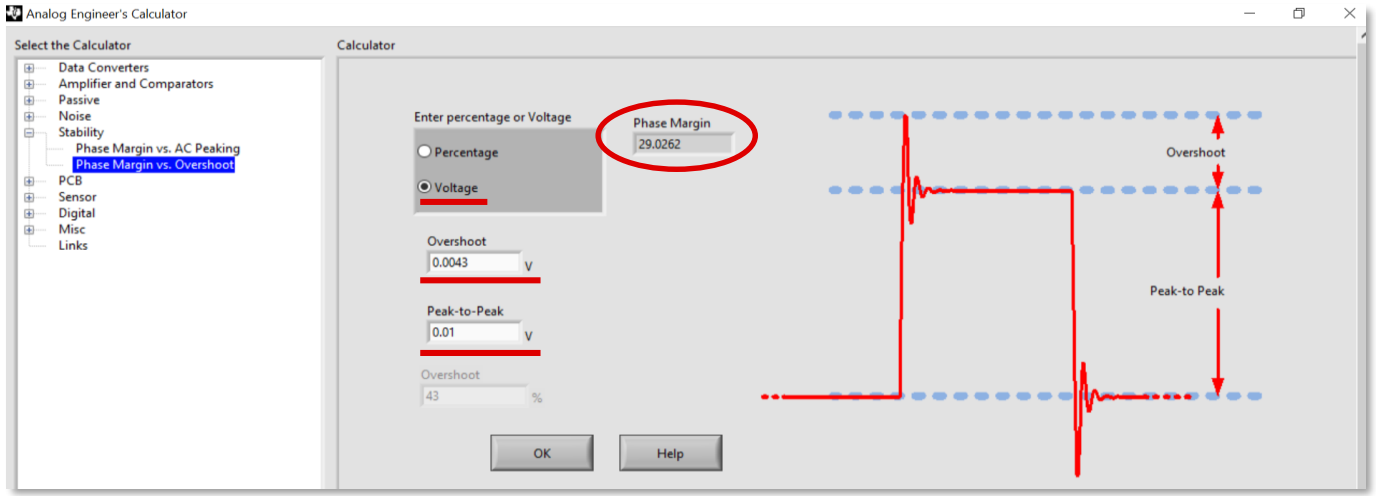


$$\text{AC peaking} = 6\text{dB} - 0\text{dB} = \mathbf{6dB}$$

6dB AC peaking → **29° phase margin**

Analog Engineer’s Calculator – overshoot





Analog engineers calculator

- Free software for download from TI.com
- Determine phase margin given overshoot
- Enter as percentage or voltage
- Download at: ti.com/tool/ANALOG-ENGINEER-CALC

Multiple choice quiz

1. Which of these is **not** a cause of amplifier instability?

   a) Capacitance on the amplifier's output to GND
   b) Capacitance on the amplifier's inverting input
   c) Large value feedback resistors
   d) Low valued resistors on the amplifier's output to GND

2. Amplifiers with stability problems are _____?

   a) Only sensitive to transients on the input
   b) Sensitive to transients on the input, output and power supplies

Multiple choice quiz

3. Amplifiers with DC inputs (eg. Reference buffer) will **not** have stability issues?

a) True
b) False

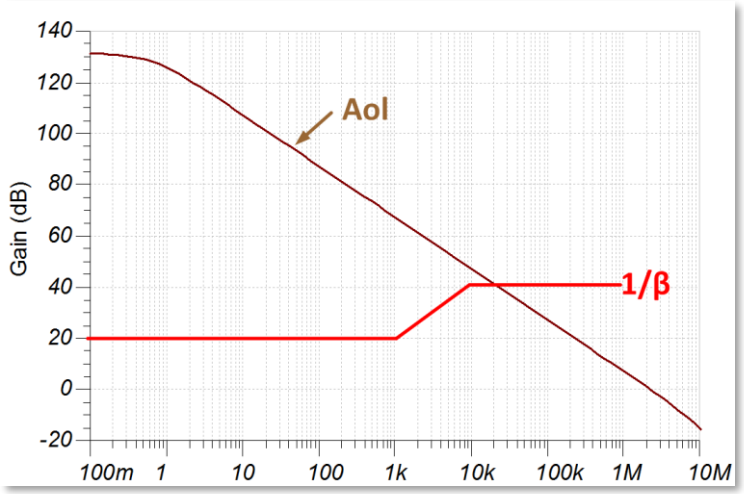
4. Which of the following is a common method for stability testing?

a) Apply a sinusoidal signal, monitor the amplifier output with an oscilloscope
b) Apply a small signal square wave input signal, monitor the amplifier output with an oscilloscope
c) Apply a triangle wave input signal, monitor the amplifier output with an oscilloscope

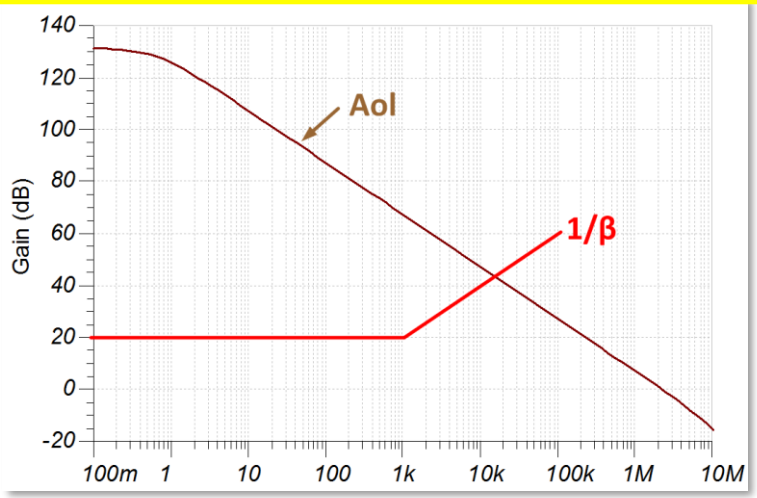
Multiple choice quiz

5. Which **one** of these A_{OL} and 1/β curves is **un**stable

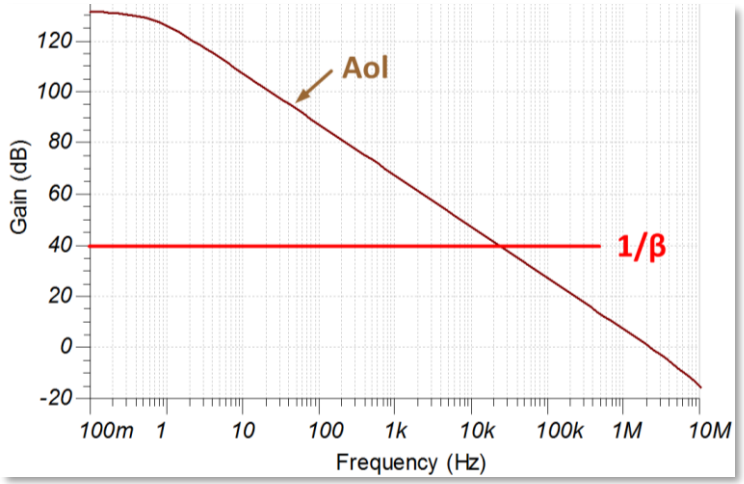
a)



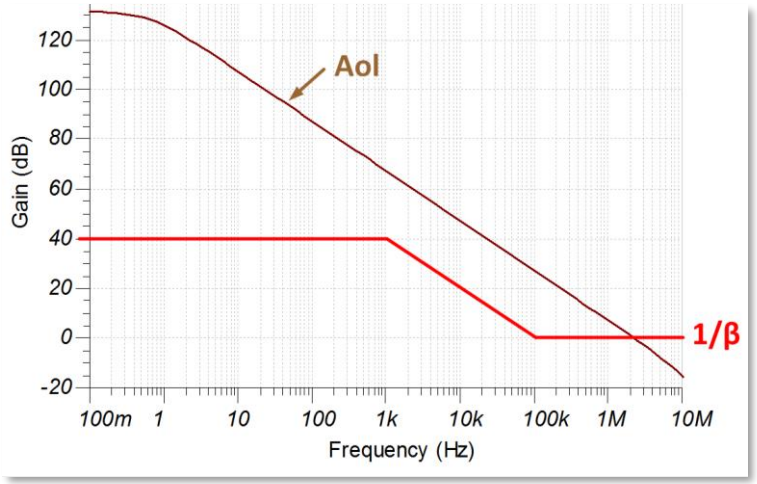
b)



c)



d)

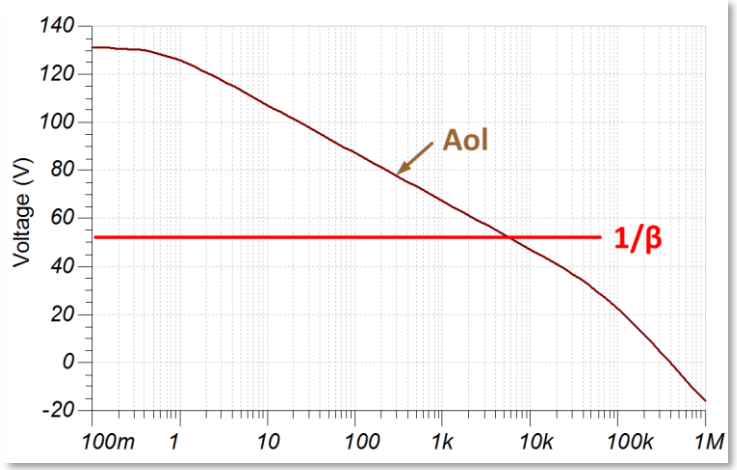


Multiple choice quiz

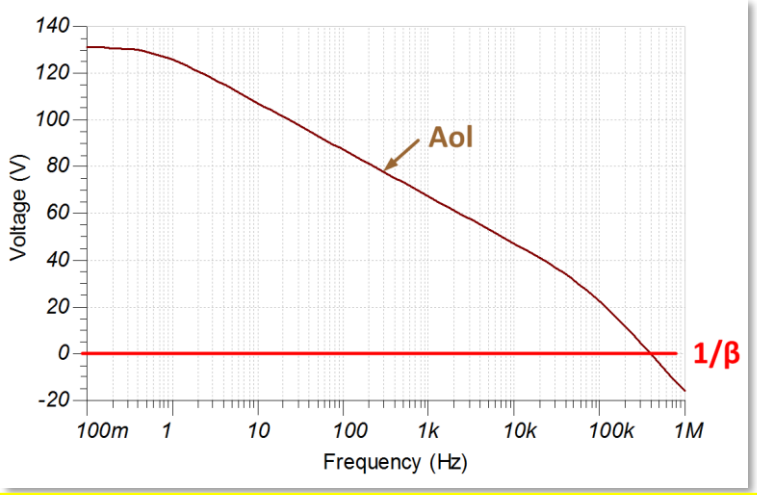
6. Which **one** of these A_{OL} and 1/β curves is **un**stable

a)

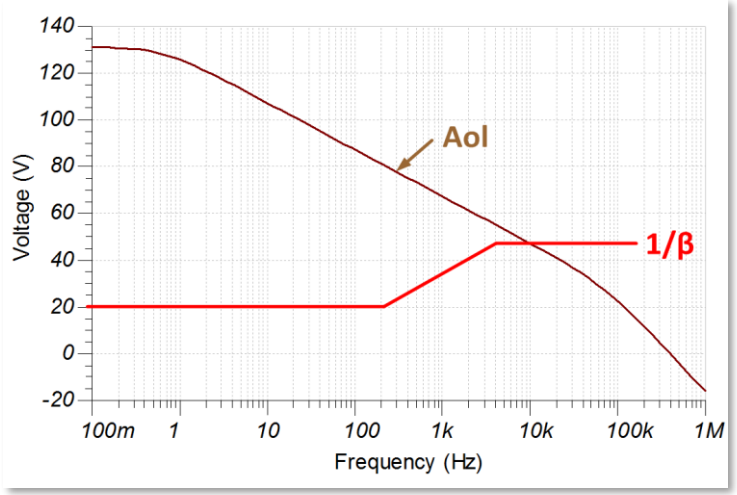
b)



c)

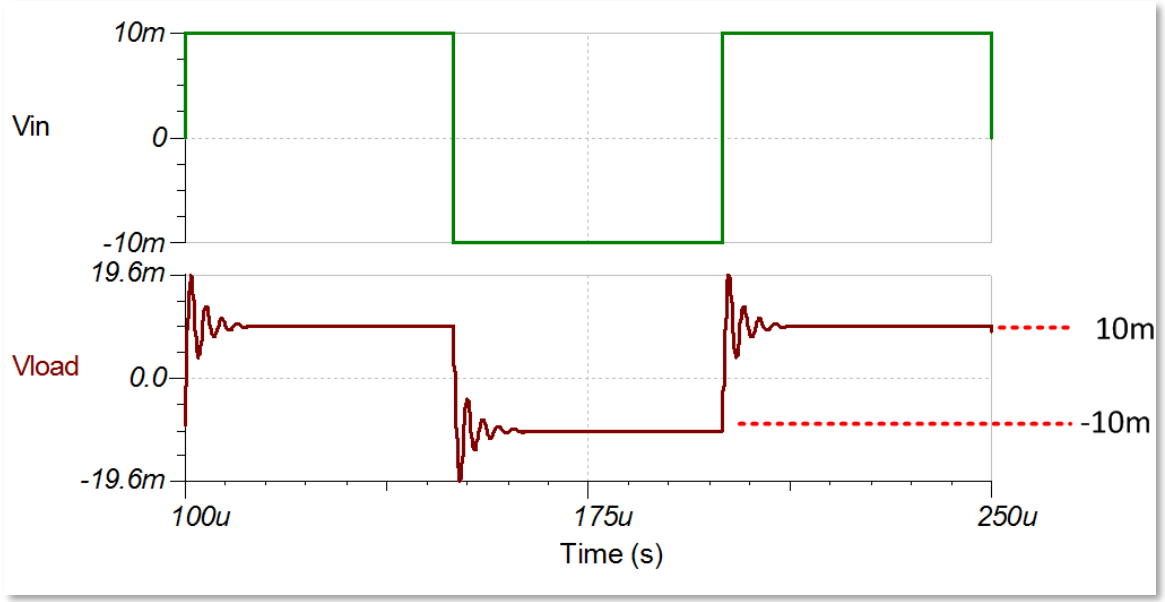


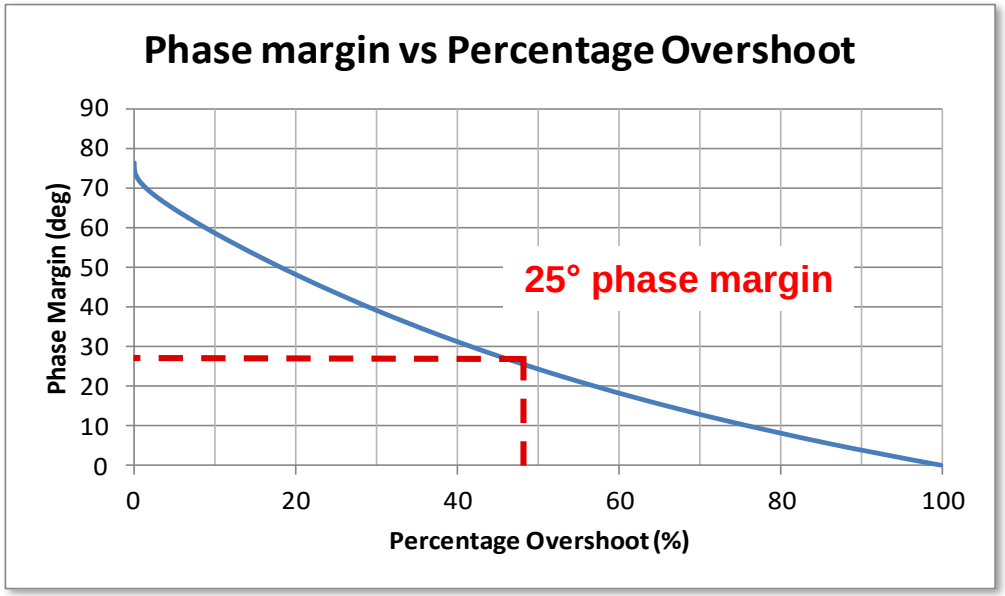
d)



Quiz

7. Find the phase margin of the system according to the % overshoot

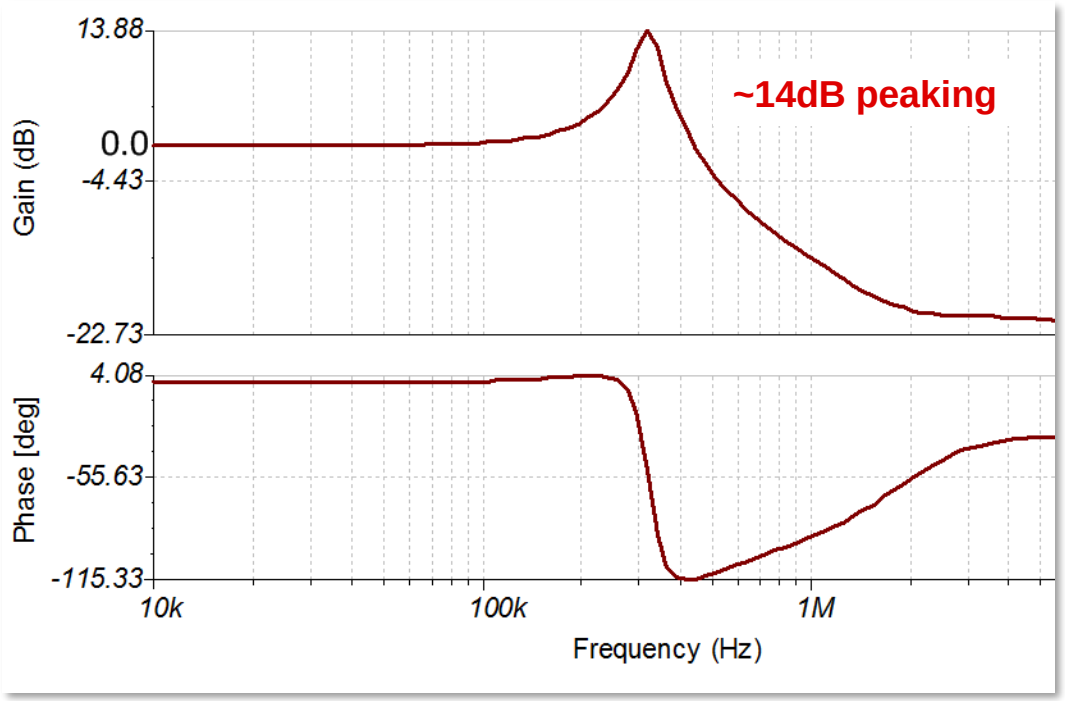


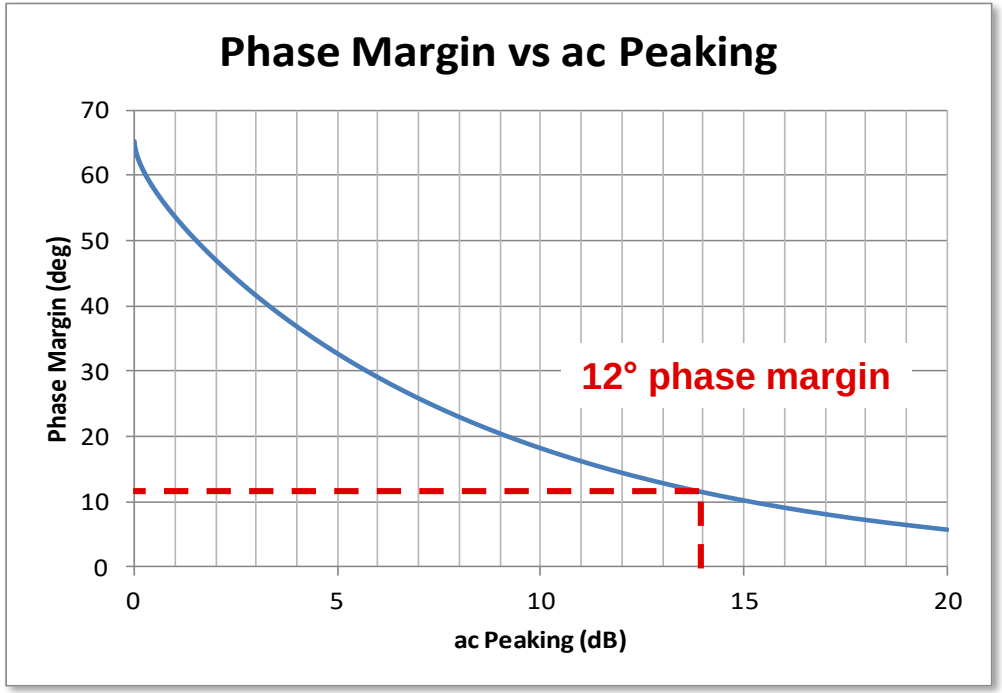


$$\%\ \text{Overshoot} = \left(\frac{19.6\text{mV} - 10\text{mV}}{20\text{mV}}\right) * 100\% = \mathbf{48\%}$$

Quiz

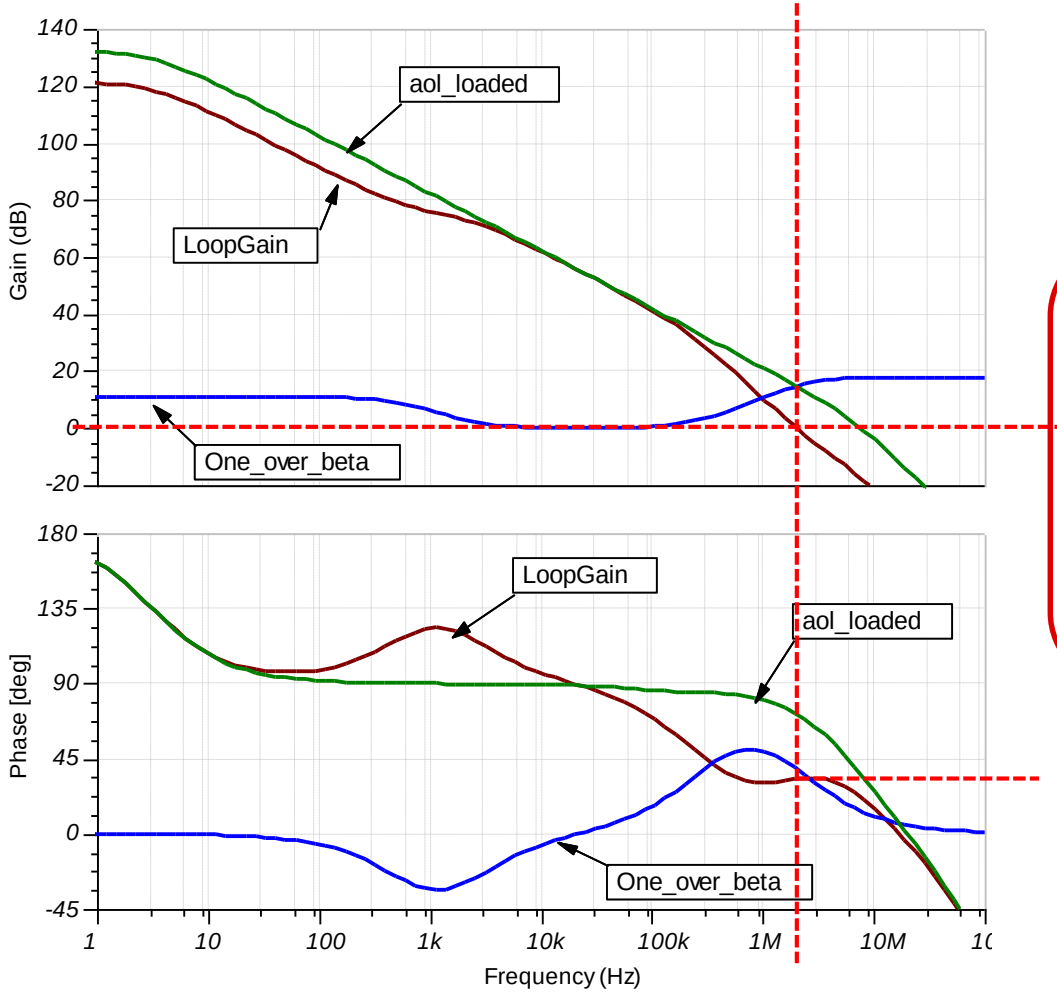
8. Find the phase margin of the system according to the AC peaking





Quiz

9. Find the phase margin of each system according to the Bode plot



- Phase margin is measured where Aol intersects 1/Beta (or where LoopGain = 0dB)
- Look at the LoopGain Phase for phase margin
- Phase margin ≈ 33º

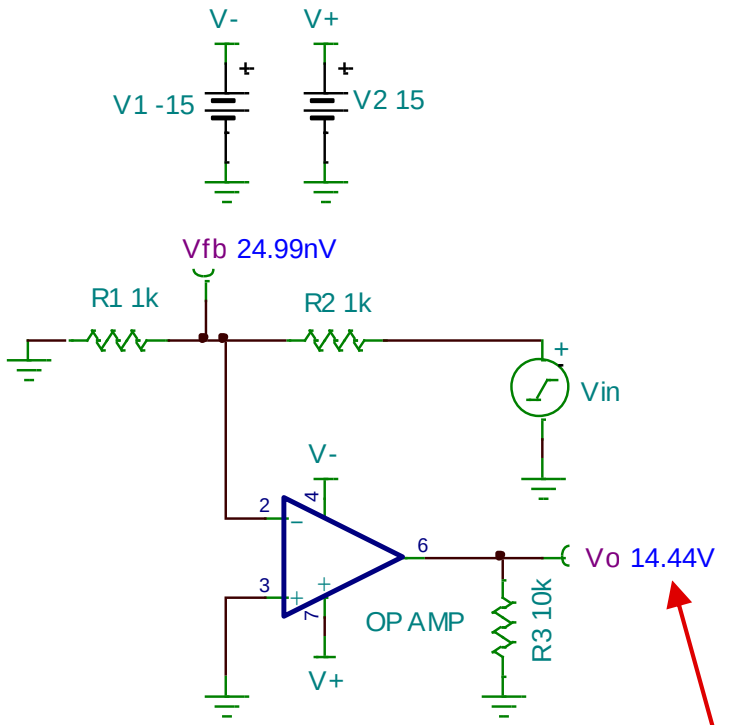
33º LoopGain Curve

Stability – Part 2

TI Precision Labs – Op Amps

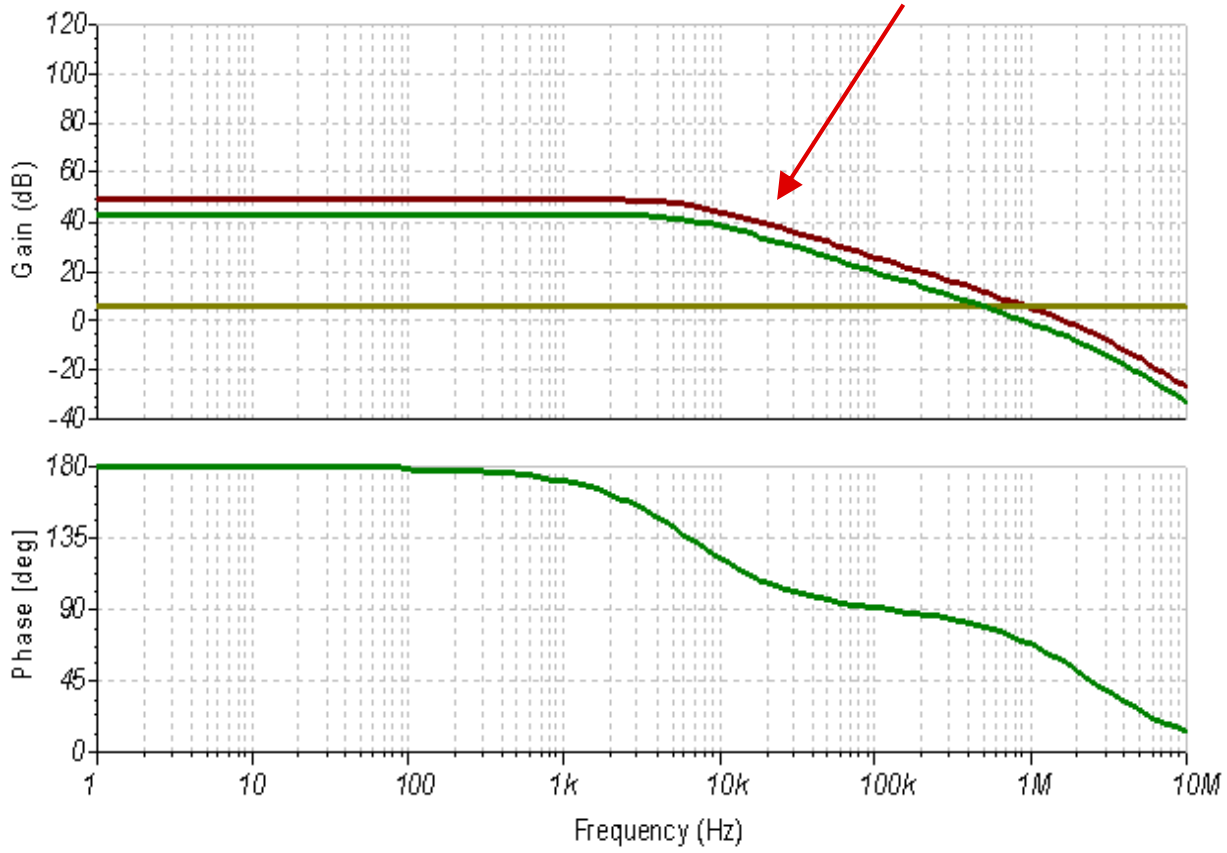
Simulating open-loop circuits

No DC biasing produces erroneous results!



Output saturated

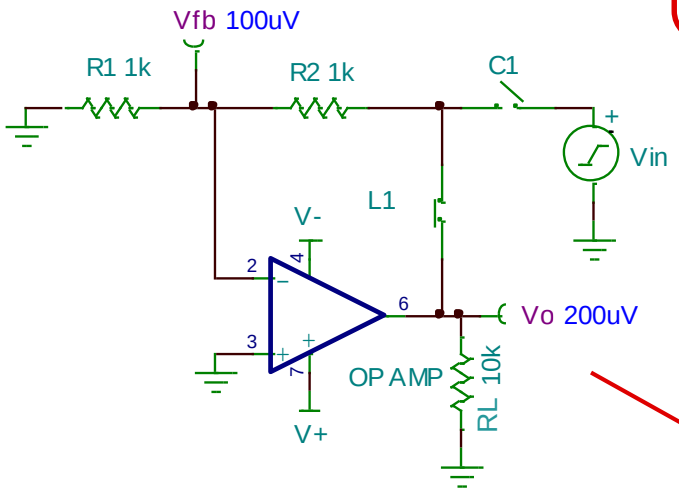
Wrong open loop response



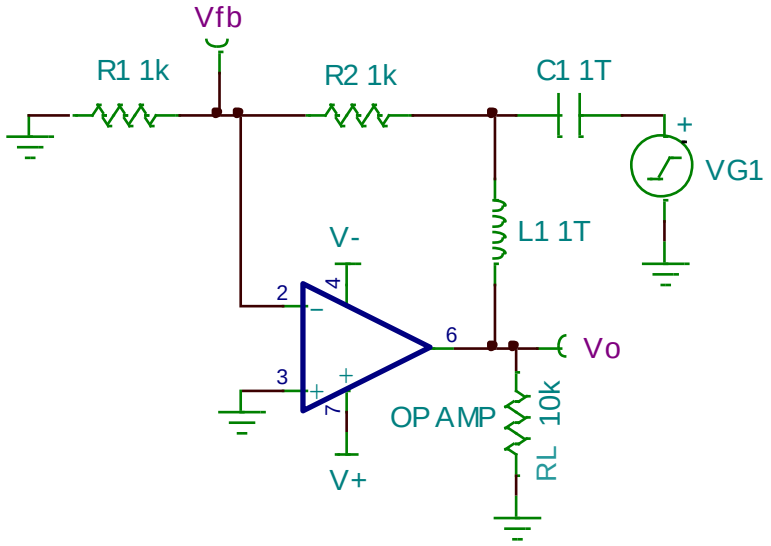
Simulating open-loop circuits

DC: closed loop needed for SPICE operation
AC: open loop needed for stability analysis

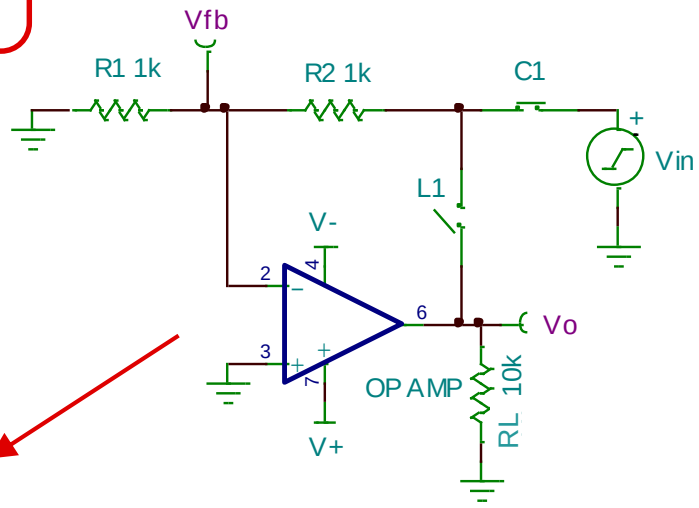
DC



DC+AC

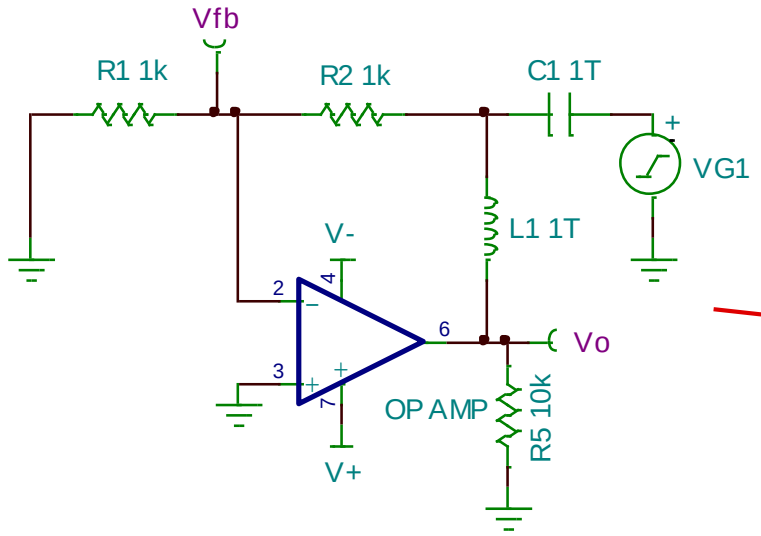


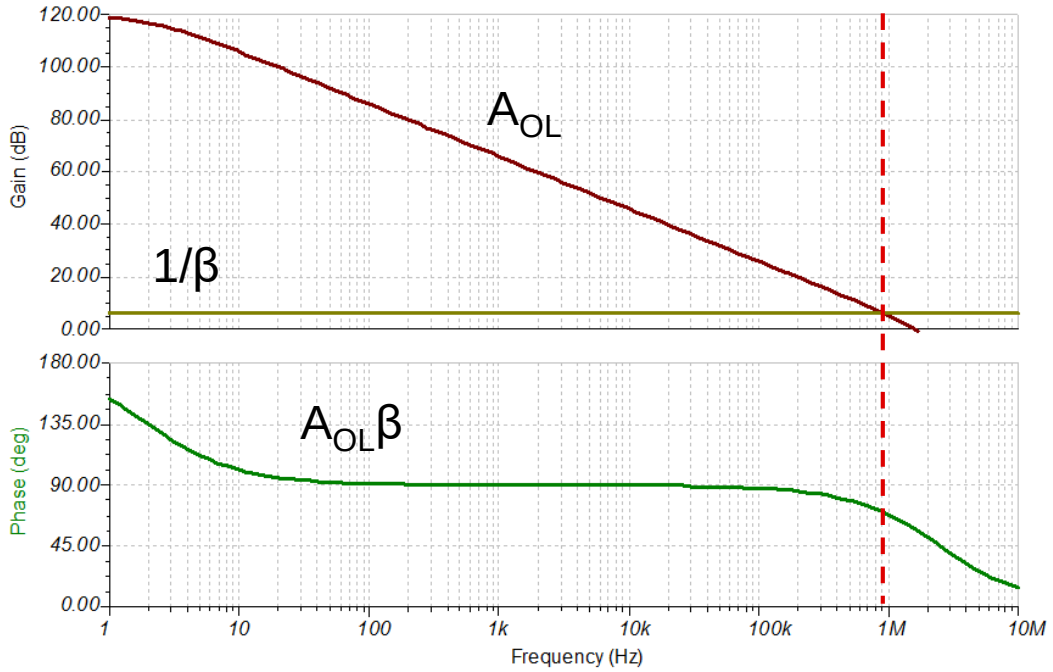
AC



Standard open-loop SPICE configuration

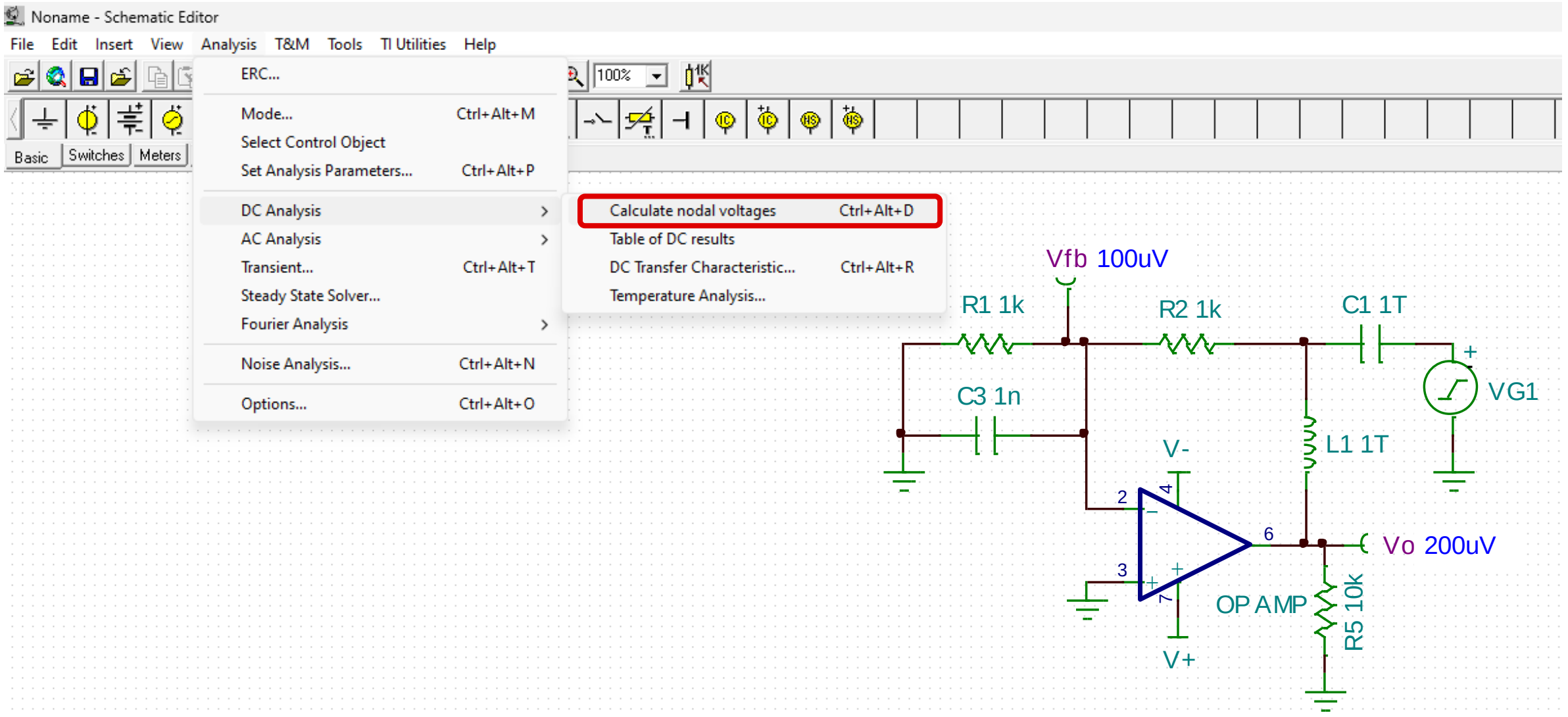
We need an open-loop circuit (no feedback) to generate open-loop gain ($\mathbf{A_{OL}}$), **1/β**, and loop gain ($\mathbf{A_{OL}\beta}$) curves





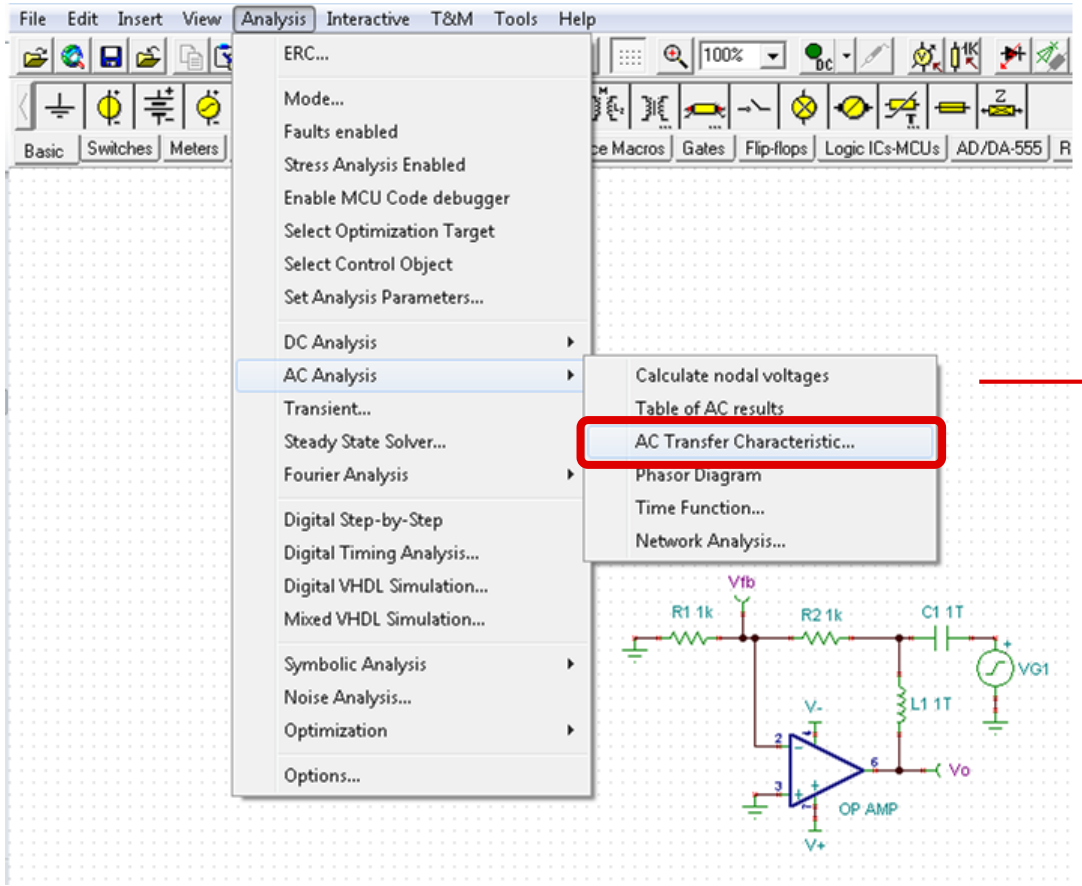
$$\mathbf{A_{OL\_LOADED} = Vo / Vfb}$$
$$\mathbf{1/\beta = 1 / Vfb}$$
$$\mathbf{A_{OL}\beta = Vo}$$

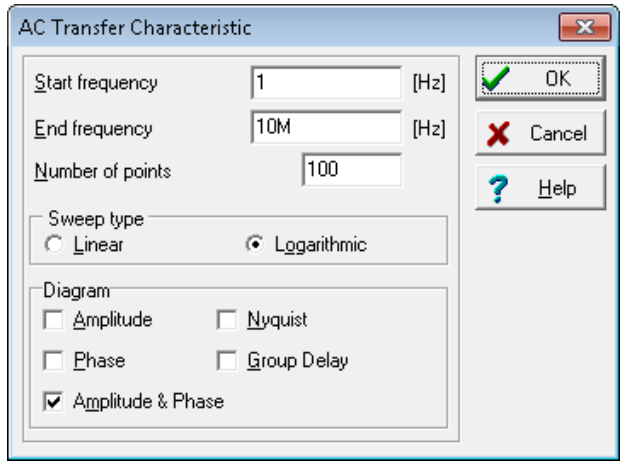
Check DC operating point



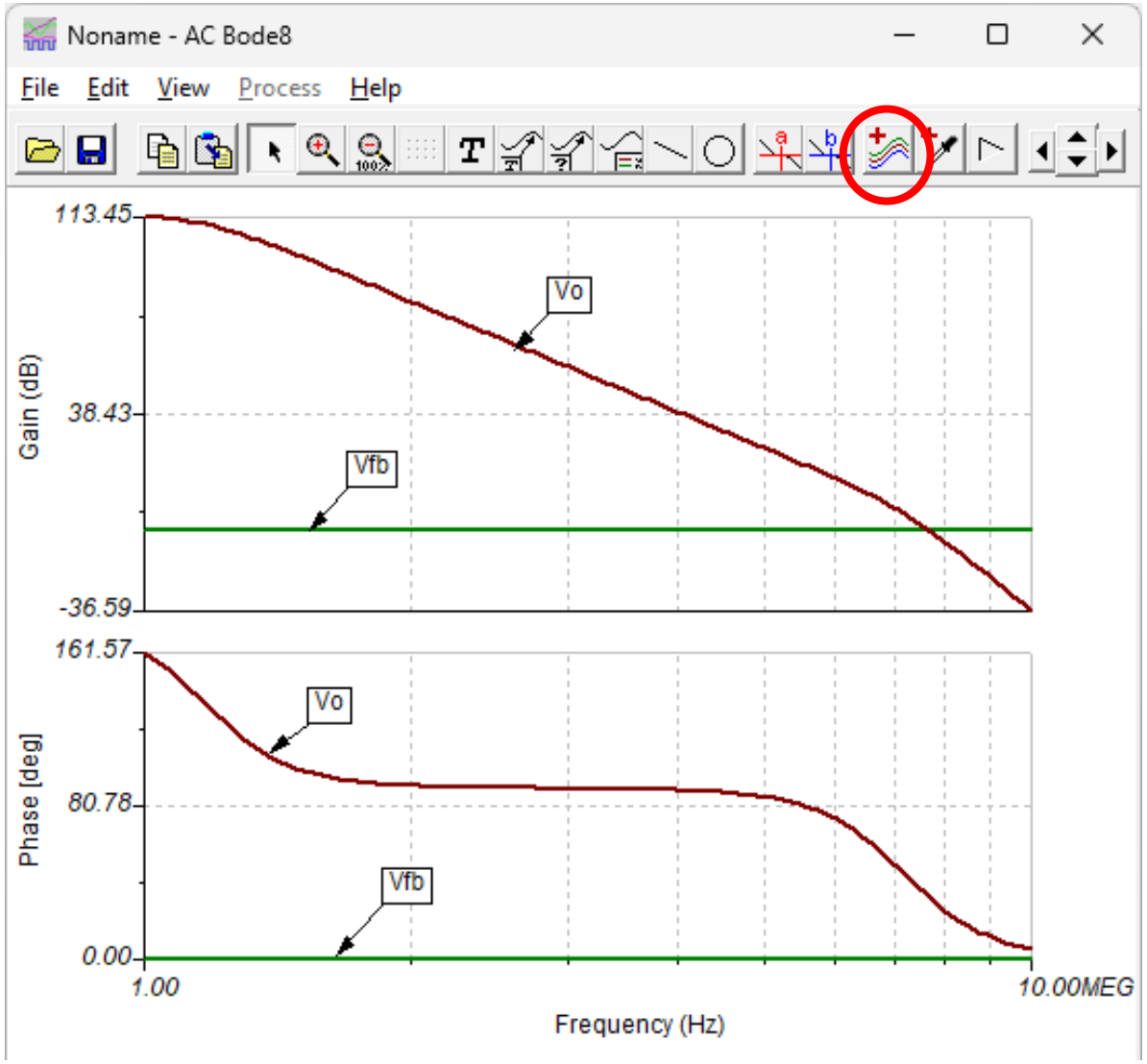
Generating open-loop curves

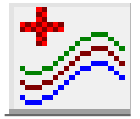
Run an AC transfer characteristic analysis over the appropriate frequency range:
Click **Analysis → AC Analysis → AC Transfer Characteristic**



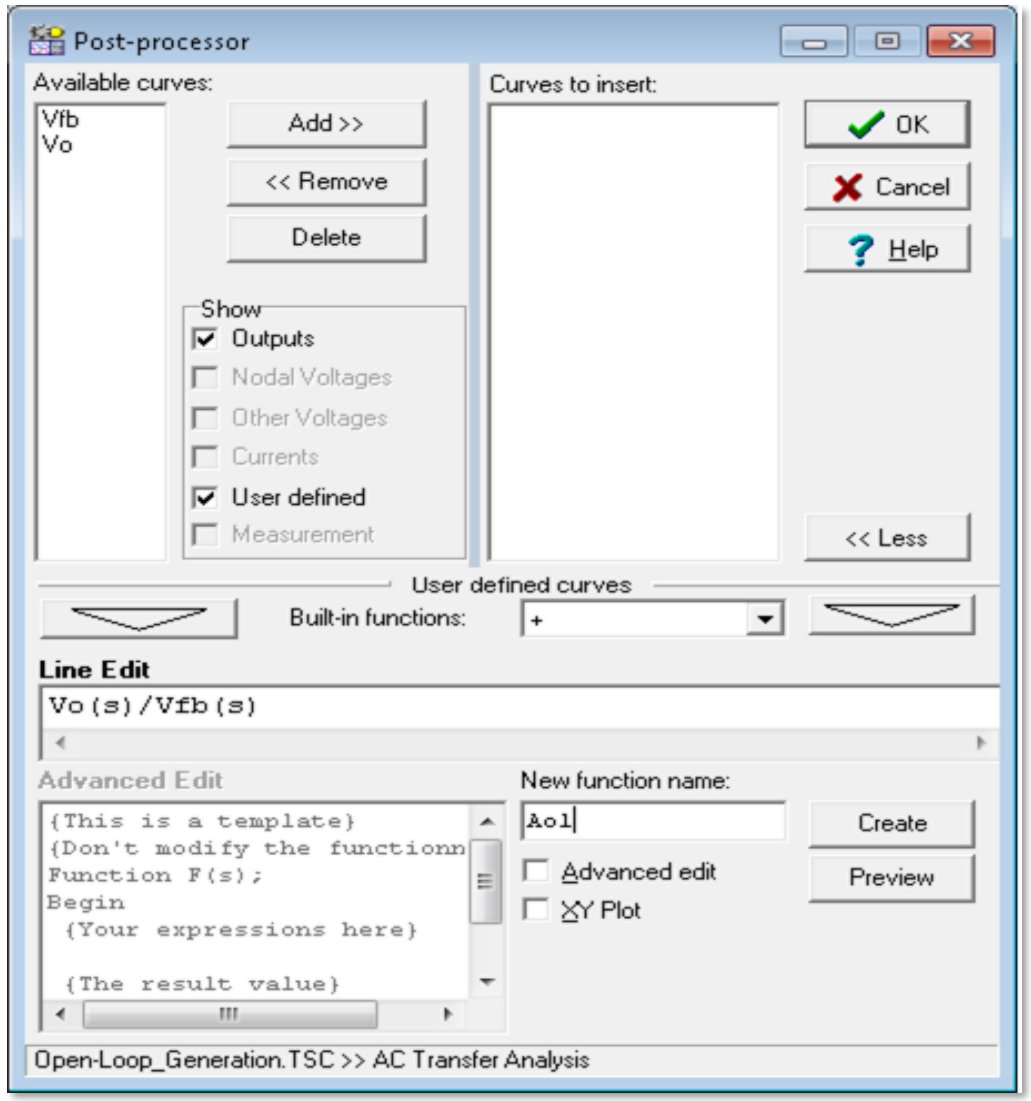


Generating open-loop curves



- The graph does not show 1/Beta, or loop gain
- Press  to use the post processor to generate the missing curves

Generating open-loop curves



- Perform math on the existing curves to create the new curves:

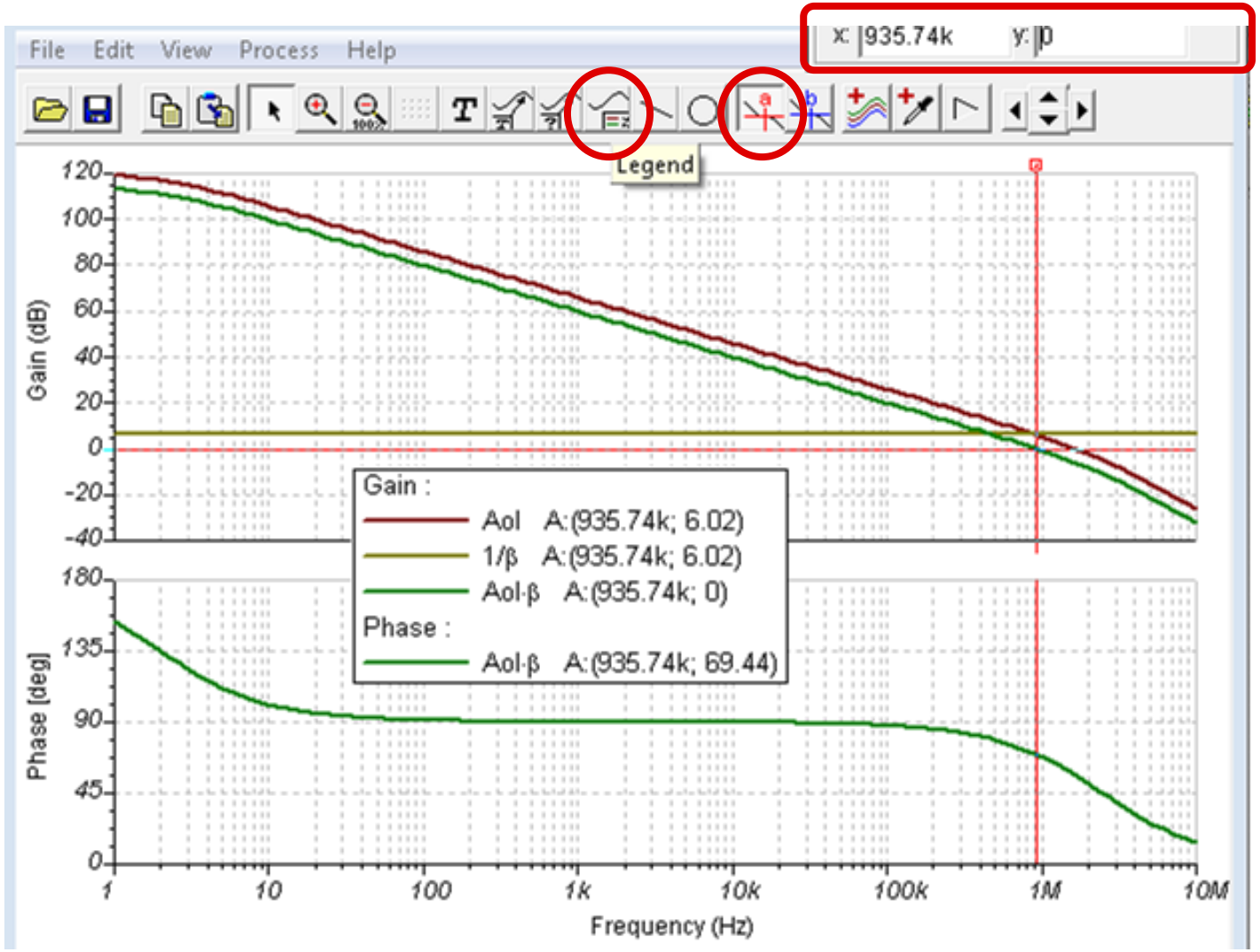
  AOL = Vo / Vfb
  One_Over_Beta = 1 / Vfb
  Loop_Gain = Vo

- Note: Math symbols cannot be used in the function name

Generating open-loop curves

1. In the gain magnitude keep: AOL, Loop_Gain, and One_Over_Beta. Delete other curves.
2. In the phase section, delete all curves except for Loop_Gain.
3. Click on X and Y axis and re-scale as desired.

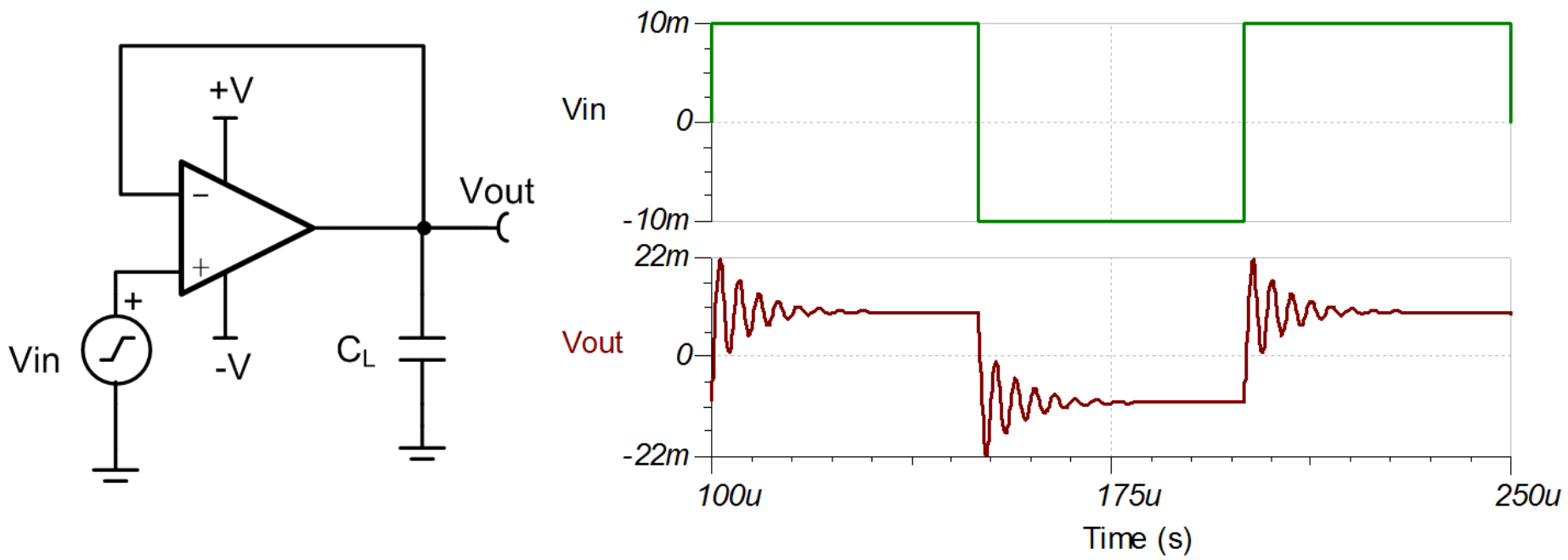
Generating open-loop curves



1. Use  to activate cursor.
2. Place the cursor on Loop_Gain
3. Type in Loop_Gain = 0 dB and press enter. The cursor will jump to appropriate frequency.
4. Use  to generate a legend.
5. The legend will show phase margin

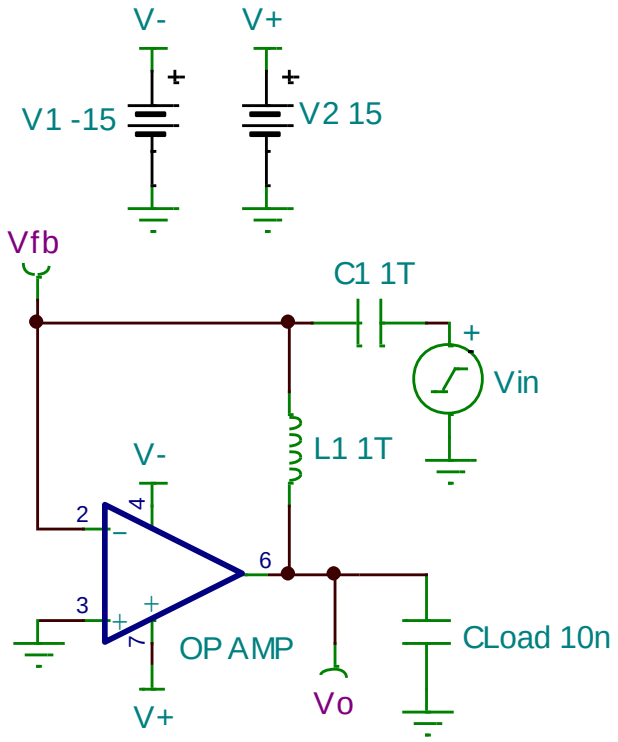
Phase Margin = Aol*β
Phase @ f_c

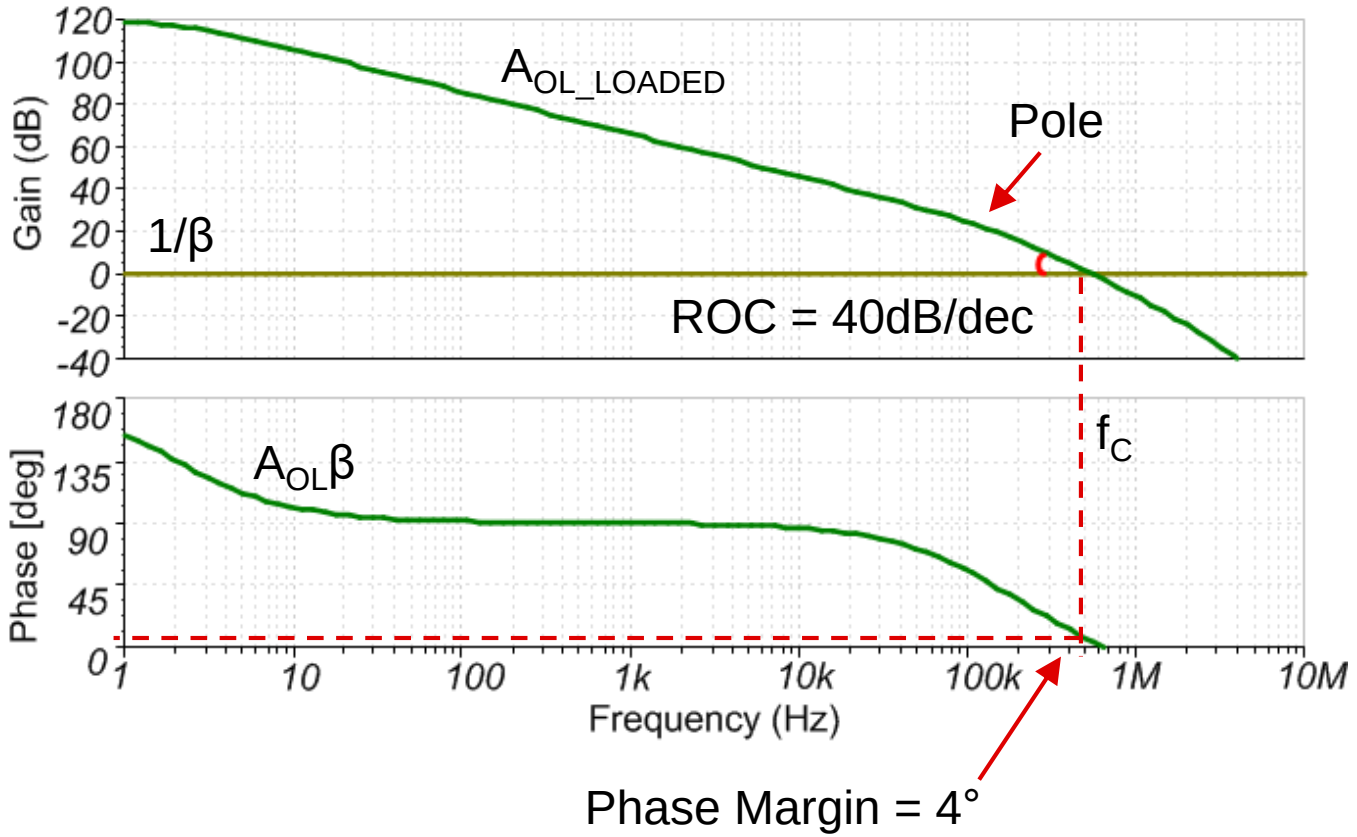
Why do capacitive loads cause instability?



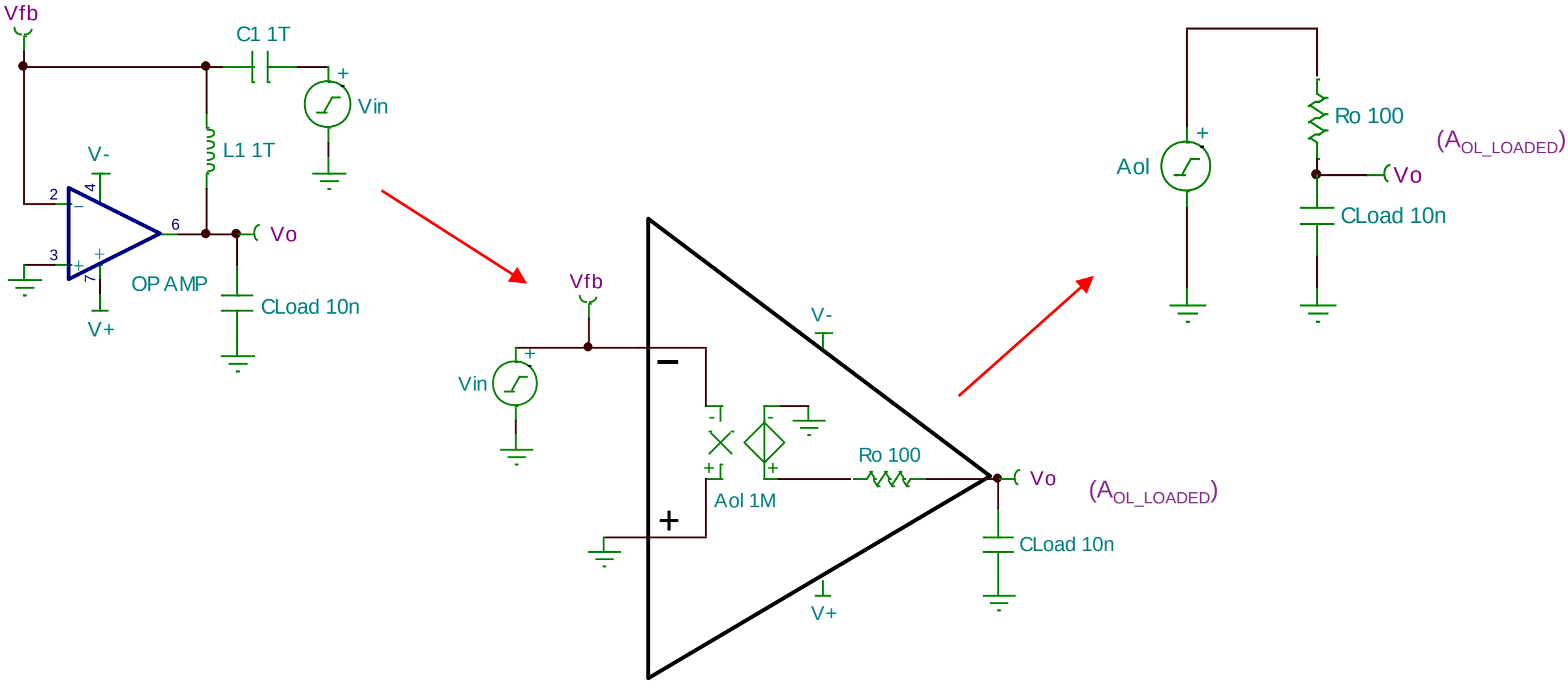
Simulate the effects of output capacitance

Run open-loop analysis on buffer circuit with capacitive load

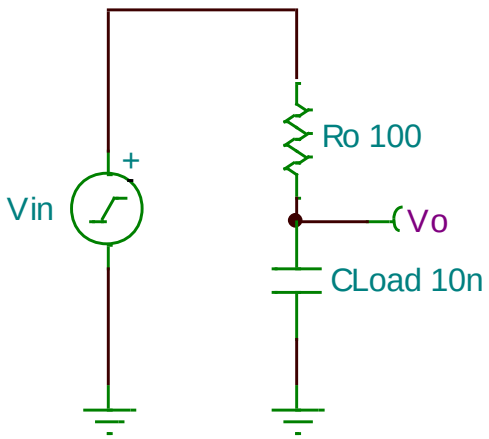


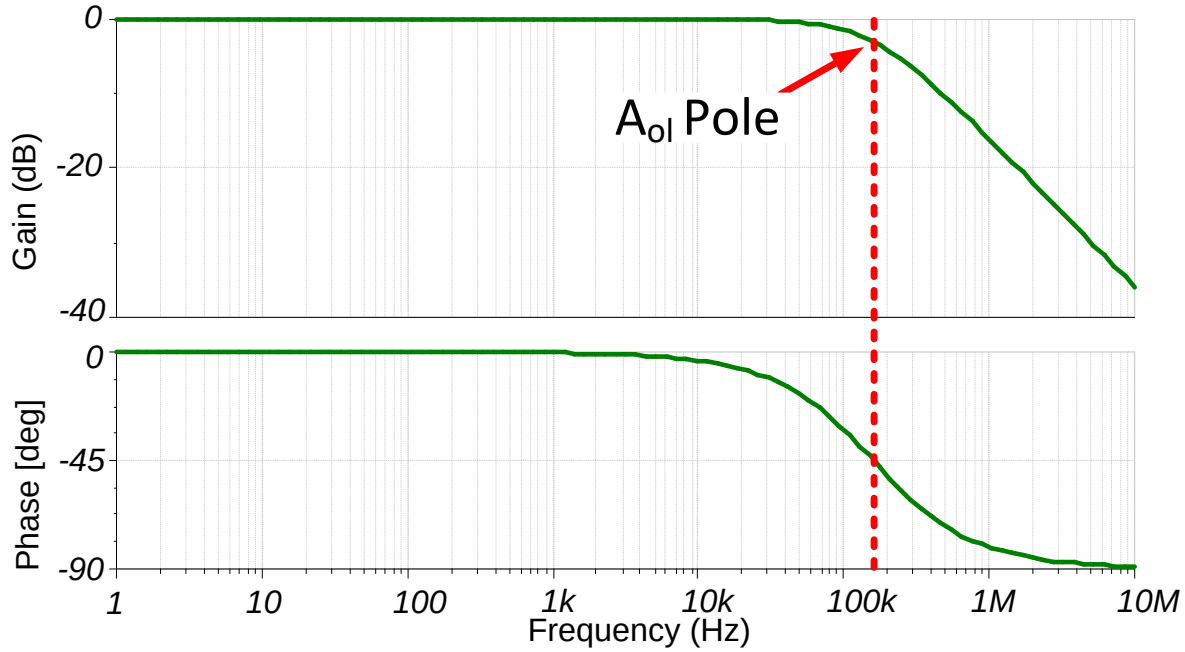


Capacitive loads – stability theory



Capacitive loads – stability theory



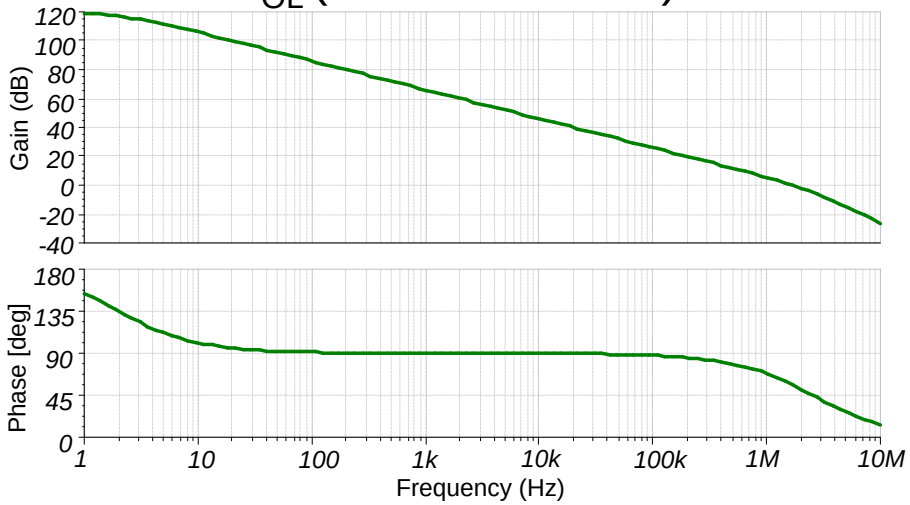


Transfer Function: $\frac{V_o}{V_{in}}(s) = \frac{1}{1 + s * Ro * C_{LOAD}}$

Pole Equation: $f_{POLE} = \frac{1}{2 * \pi * Ro * C_{LOAD}}$

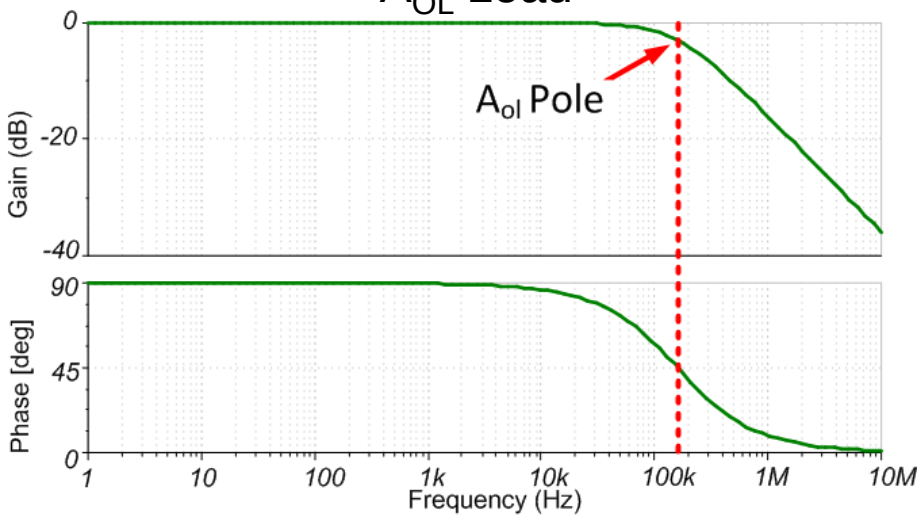
Capacitive loads – stability theory

A_{OL} (from data sheet)

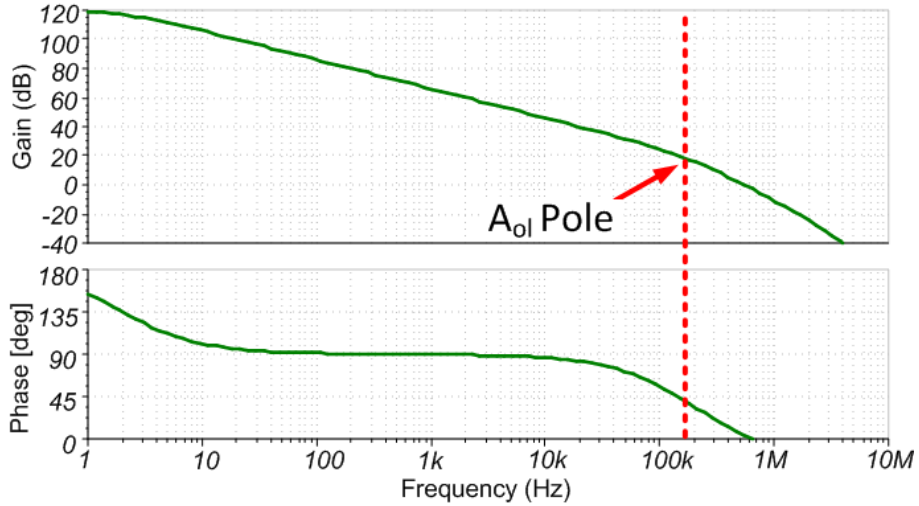


X

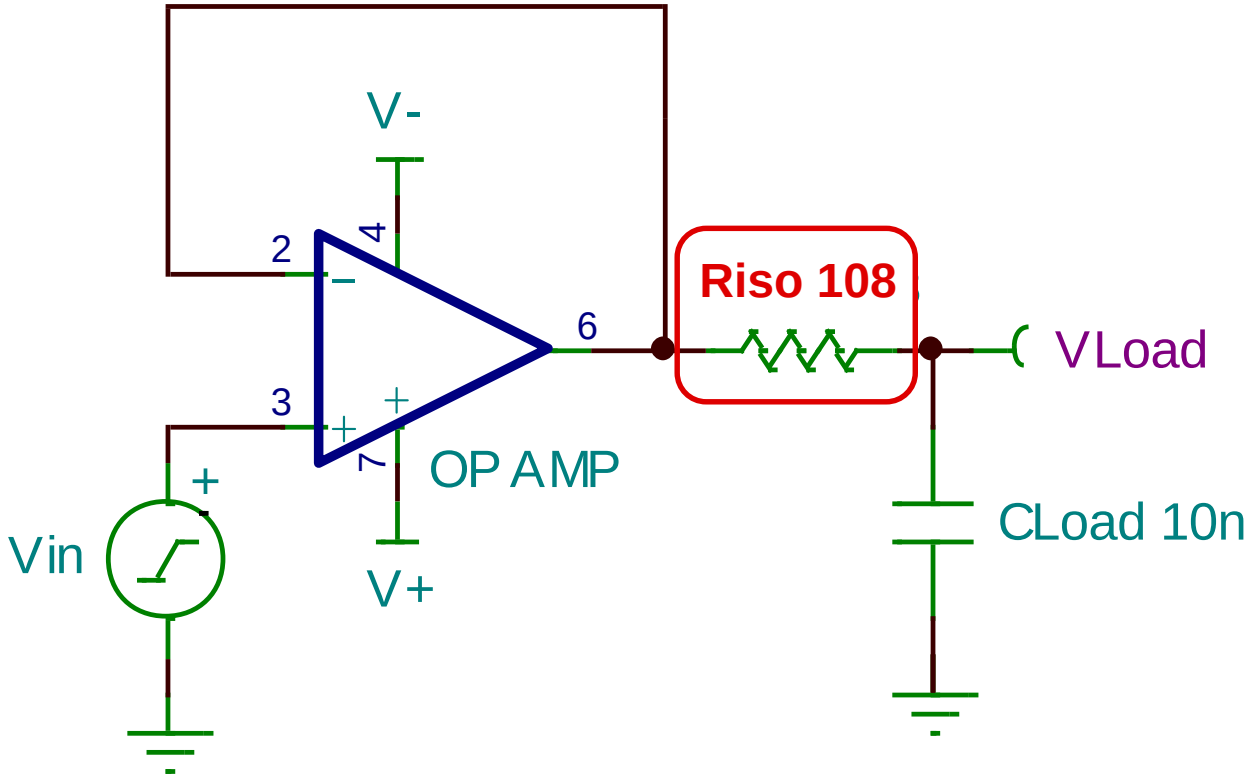
A_{OL} Load



Loaded A_{OL} =



Method 1: R_{ISO}

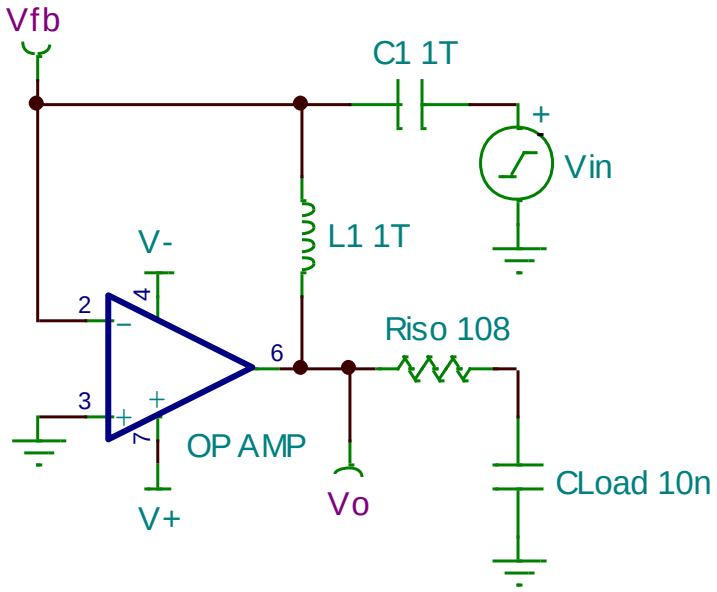


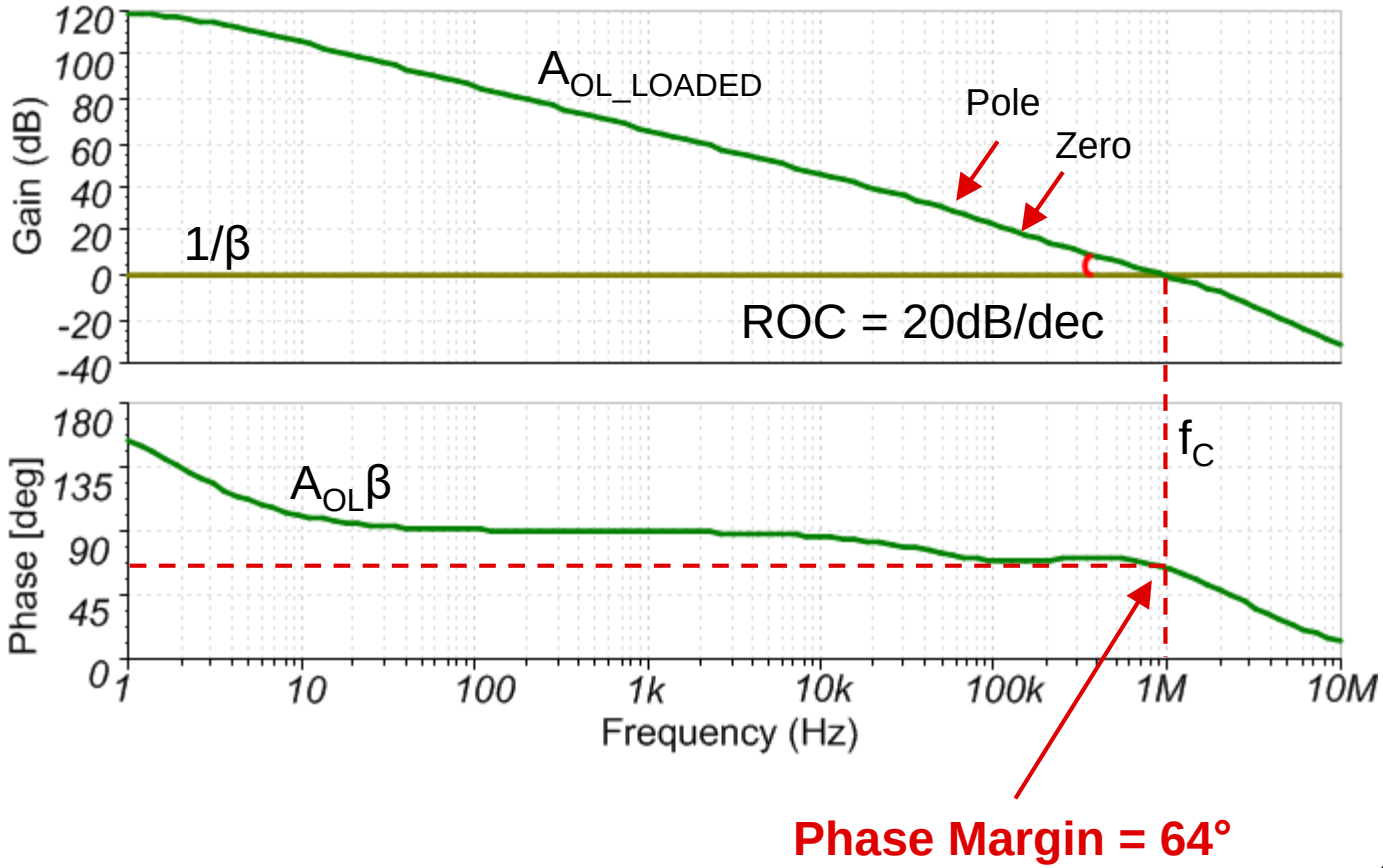
Adding Riso can stabilize the circuit. We will discuss:

- How it stabilizes the circuit (zero cancels pole)
- What value is required?

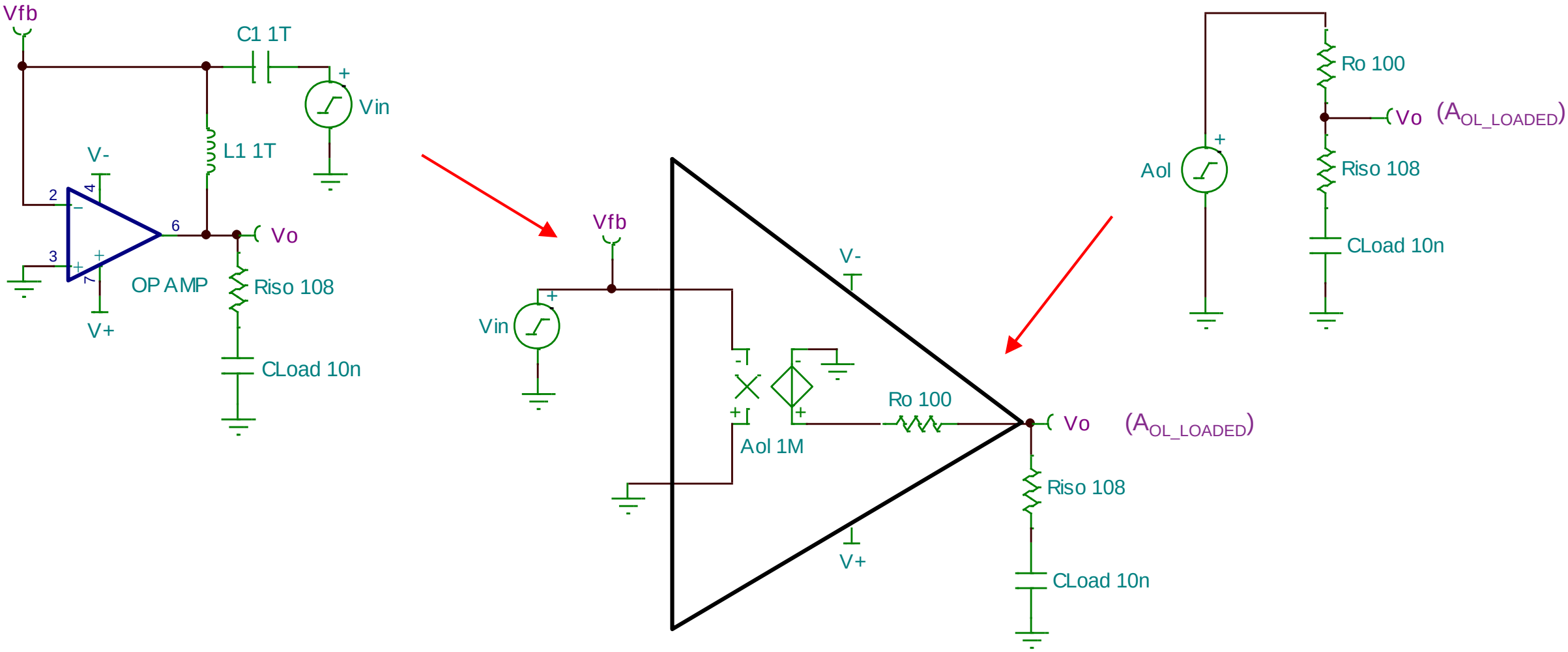
Method 1: R_{ISO} – results

Theory: Adds a zero to cancel the pole in loaded A_{OL}

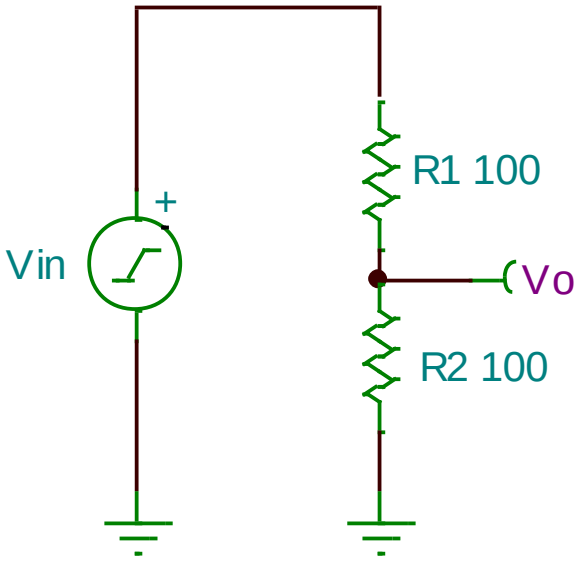




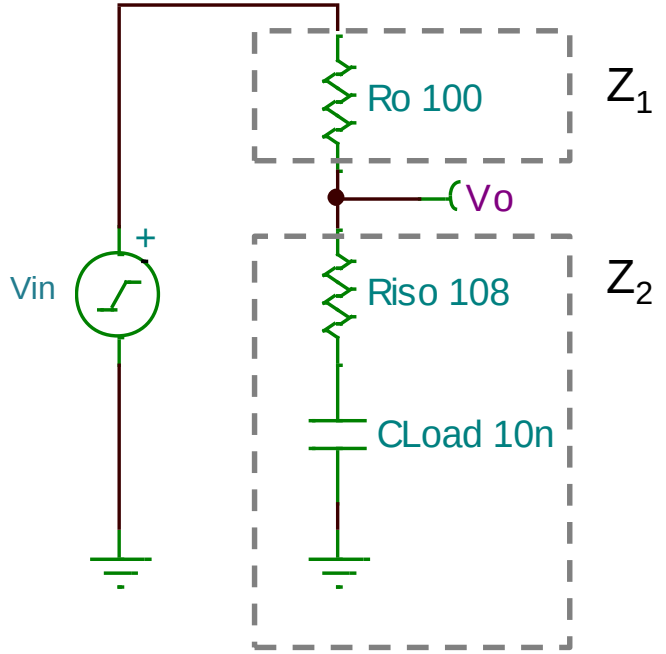
Method 1: R_{ISO} – theory



Resistor divider analogy



$$\frac{V_O}{V_{IN}} = \frac{R_2}{R_2 + R_1}$$



$$\frac{V_O}{V_{IN}} = \frac{Z_2}{Z_2 + Z_1}$$

$$\frac{V_O}{V_{IN}} = \frac{R_{ISO} + \frac{1}{s * C_{LOAD}}}{\left(R_{ISO} + \frac{1}{s * C_{LOAD}}\right) + R_O}$$

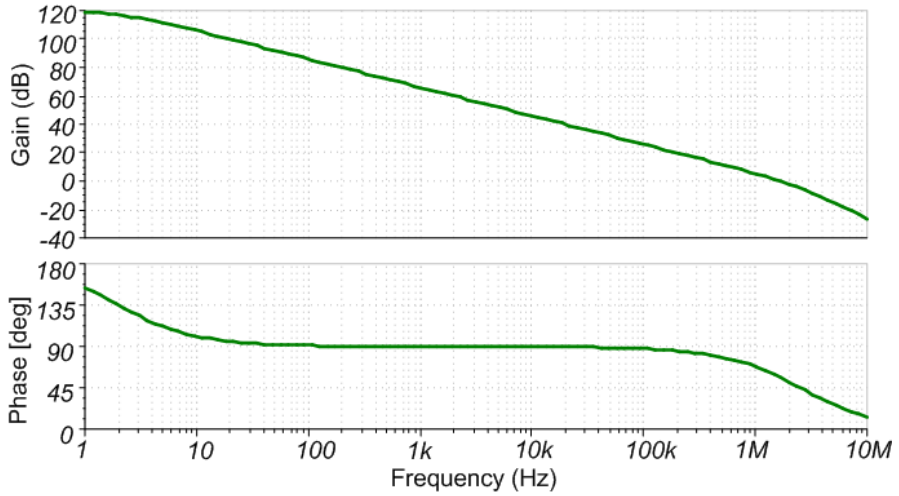
$$\frac{V_O}{V_{IN}} = \frac{1 + s * R_{ISO} * C_{LOAD}}{1 + s * (R_{ISO} + R_O) * C_{LOAD}}$$

Zero: R_{ISO} & C_{LOAD}

Pole: R_O, R_{ISO}, and C_{LOAD}

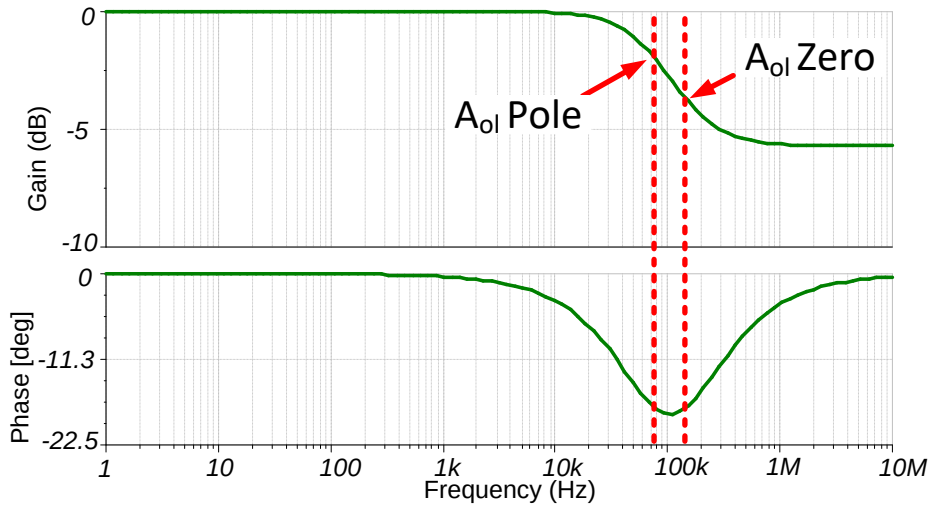
Method 1: R_{ISO} – theory

A_{OL} (from data sheet)

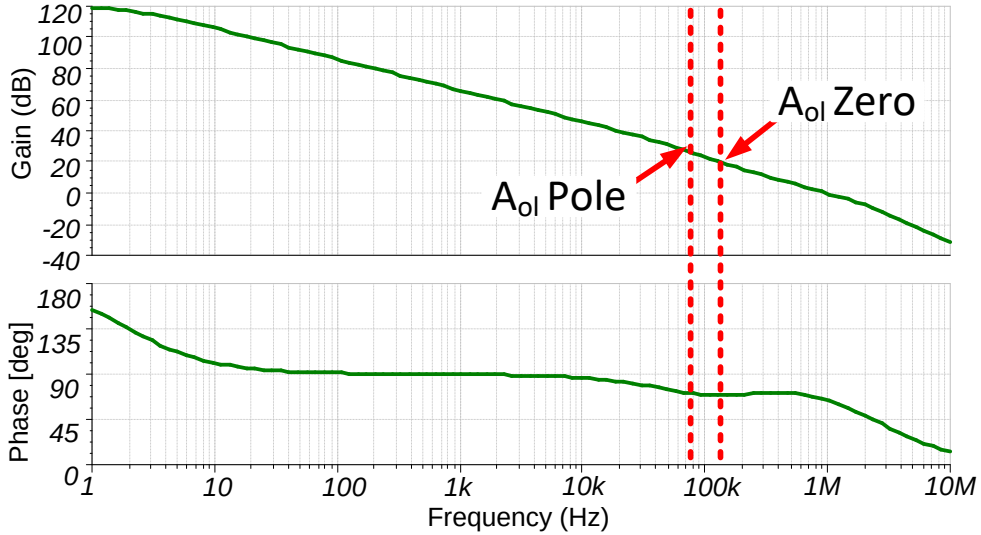


X

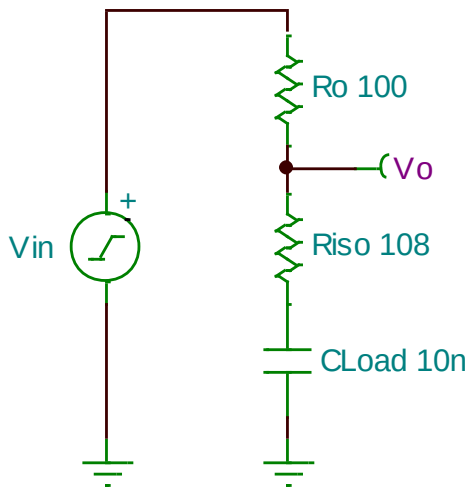
A_{OL} Load

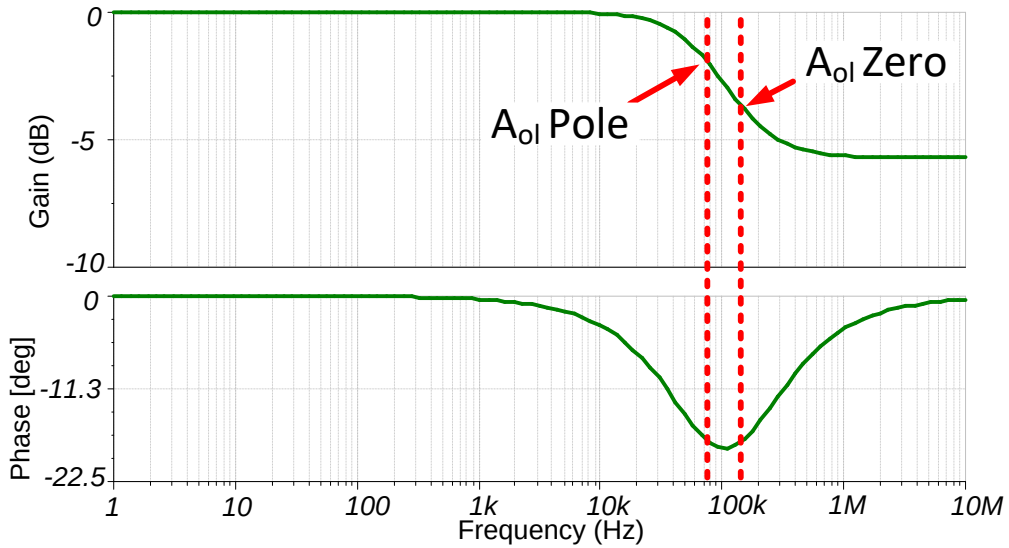


Loaded A_{OL} =



Method 1: R_{ISO} – theory





Transfer Function: $$\frac{V_o}{V_{in}}(s) = \frac{1 + s * R_{ISO} * C_{LOAD}}{1 + s * (R_O + R_{ISO}) * C_{LOAD}}$$

Zero Equation: $$f_{ZERO} = \frac{1}{2 * \pi * R_{ISO} * C_{LOAD}}$$

Pole Equation: $$f_{POLE} = \frac{1}{2 * \pi * (R_O + R_{ISO}) * C_{LOAD}}$$

Method 1: R_{ISO} – design

Design Steps:

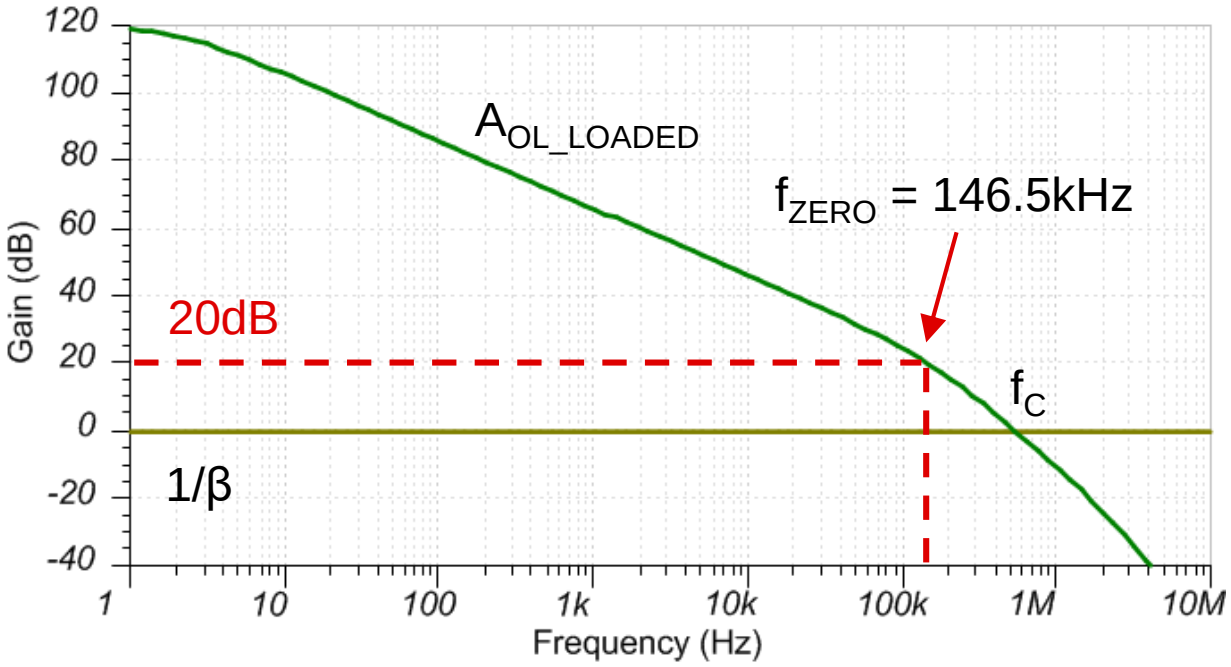
1) Find the zero frequency, f_{ZERO}, where A_{OL_Loaded} = 20 dB
2) Calculate Riso to set the zero at f_{ZERO}
   This will yield between 60° and 90° degrees of phase margin

R_{ISO} Equation:

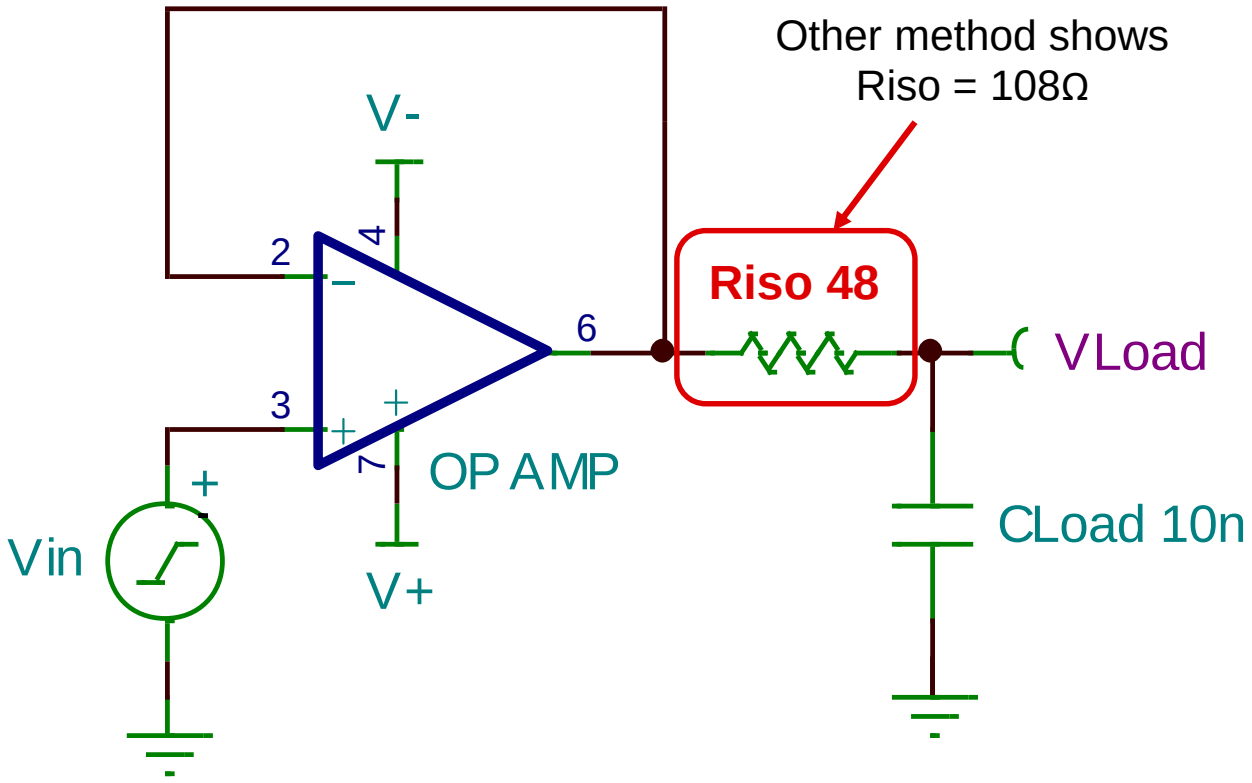
$$R_{iso} = \frac{1}{2 * \pi * f_{ZERO} * C_{LOAD}}$$

$$R_{iso} = \frac{1}{2 * \pi * 146.5kHz * 10nF}$$

$$R_{iso} = \mathbf{108\Omega}$$



Alternative method



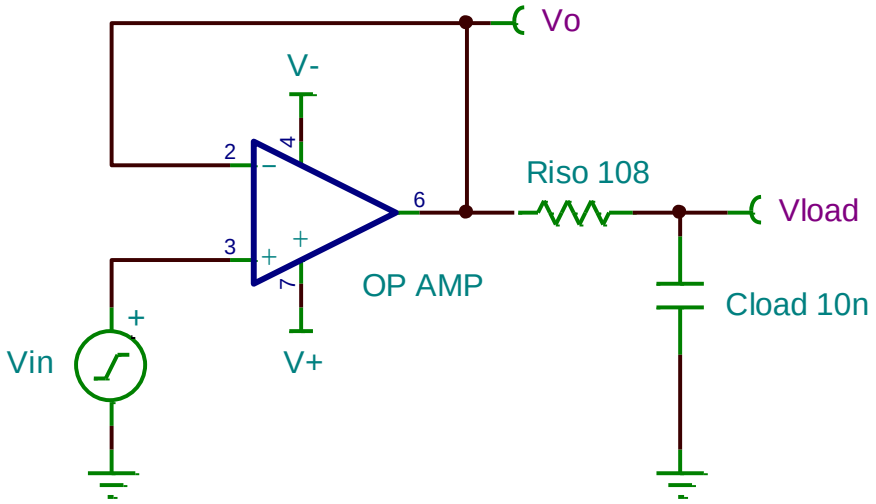
Minimum value for Riso for stability:

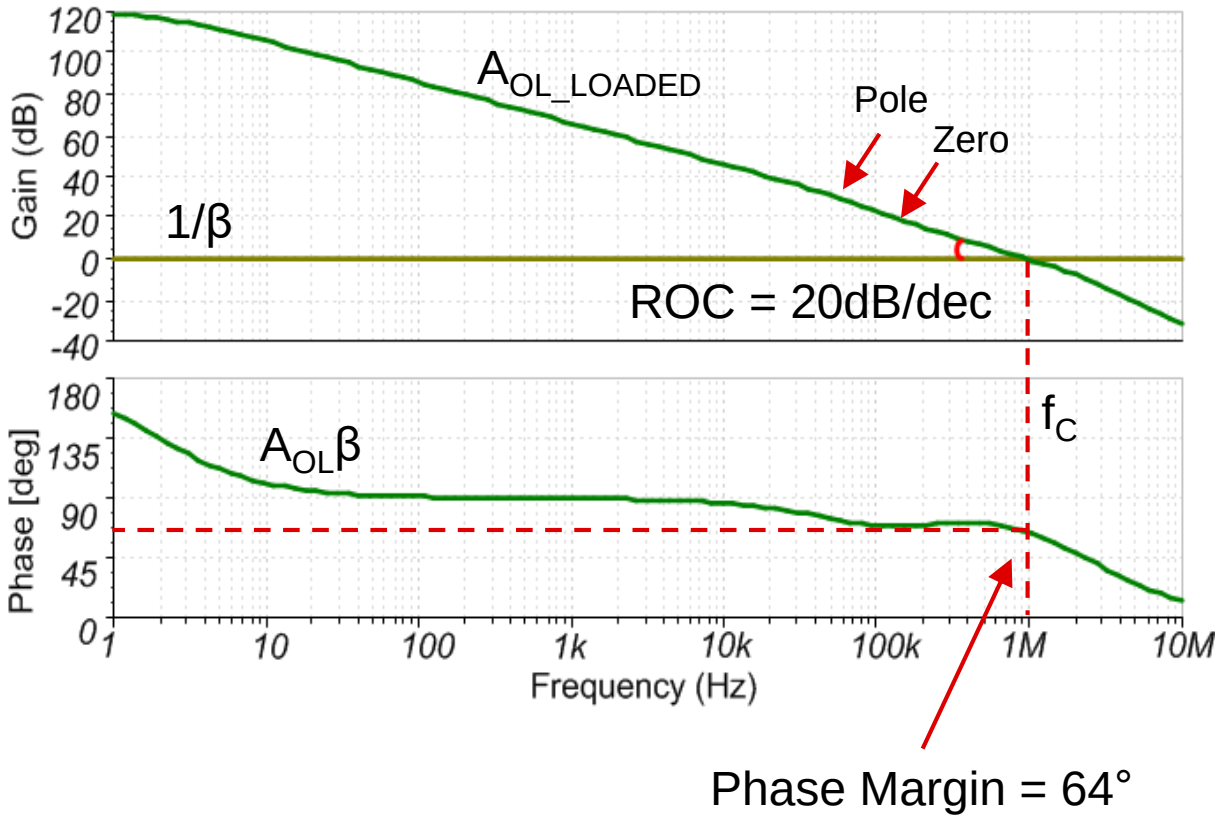
$$R_{ISO} = \frac{1 + \sqrt{1 + (8\pi \cdot R_O \cdot C_{LOAD} \cdot f_{gbw})}}{4\pi \cdot C_{LOAD} \cdot f_{gbw}}$$

- This will provide 45º of phase margin
- Decreasing R_{ISO} further will reduce stability below 45º and is not recommended
- Going forward the presentation will use value from first method 108Ω

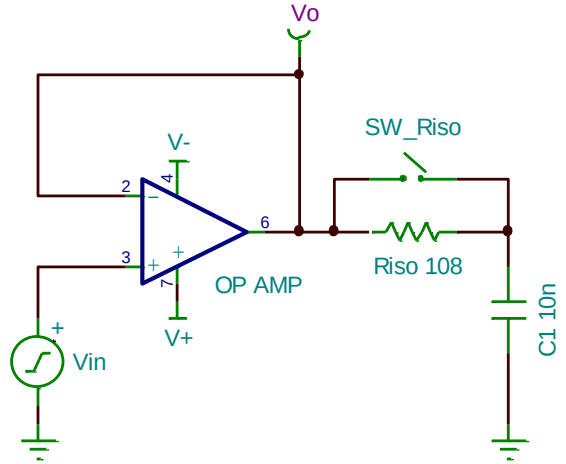
Check out the app note for more detail: http://www.ti.com/lit/pdf/sboa418

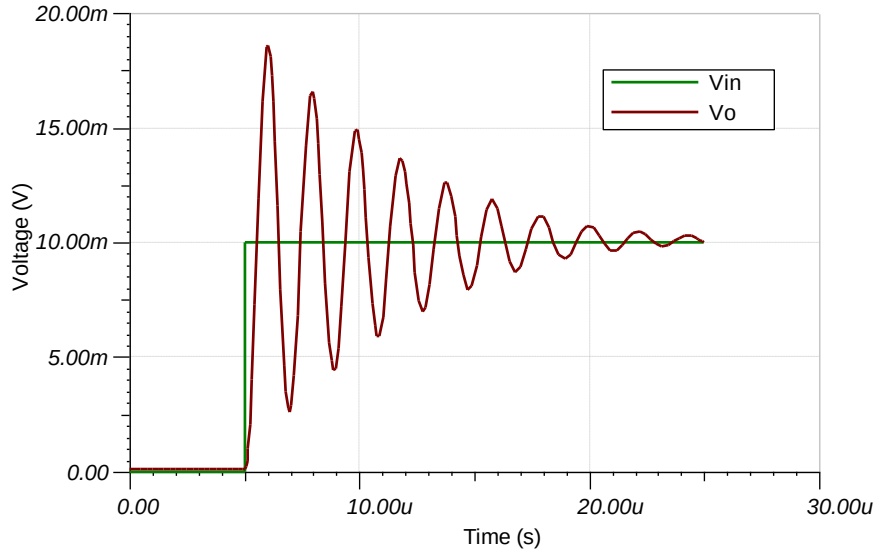
Method 1: R_{ISO} – design summary



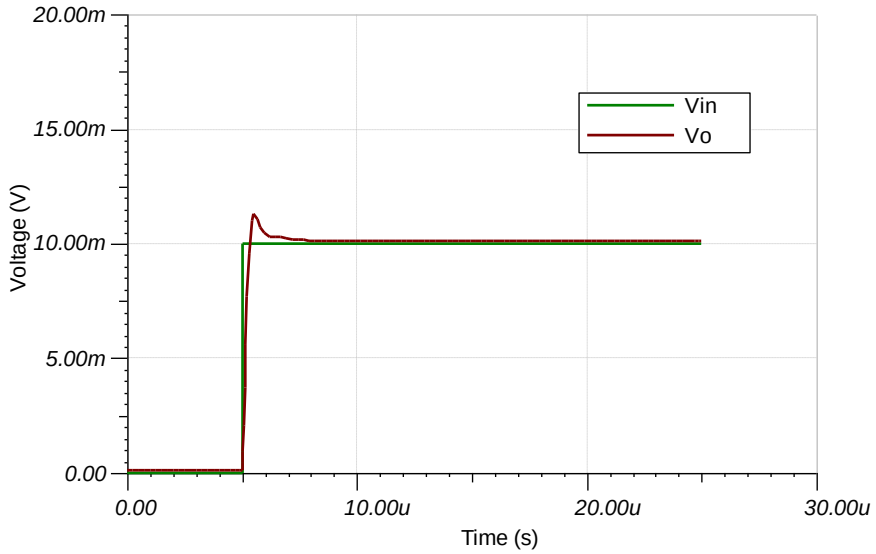


Unstable vs. stable transient results





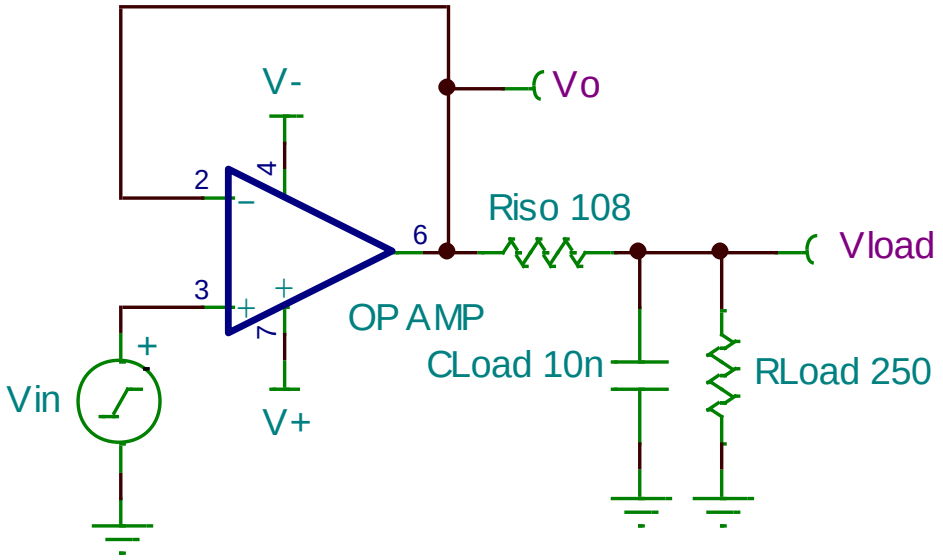
No compensation - Unstable

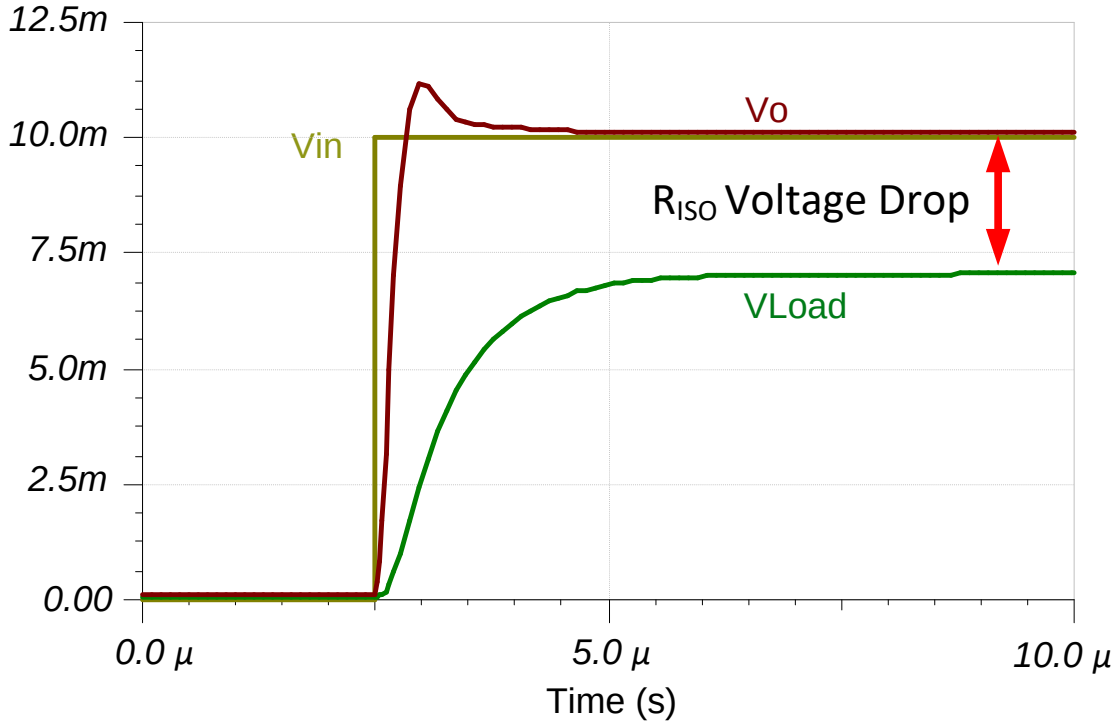


Riso compensation - Stable

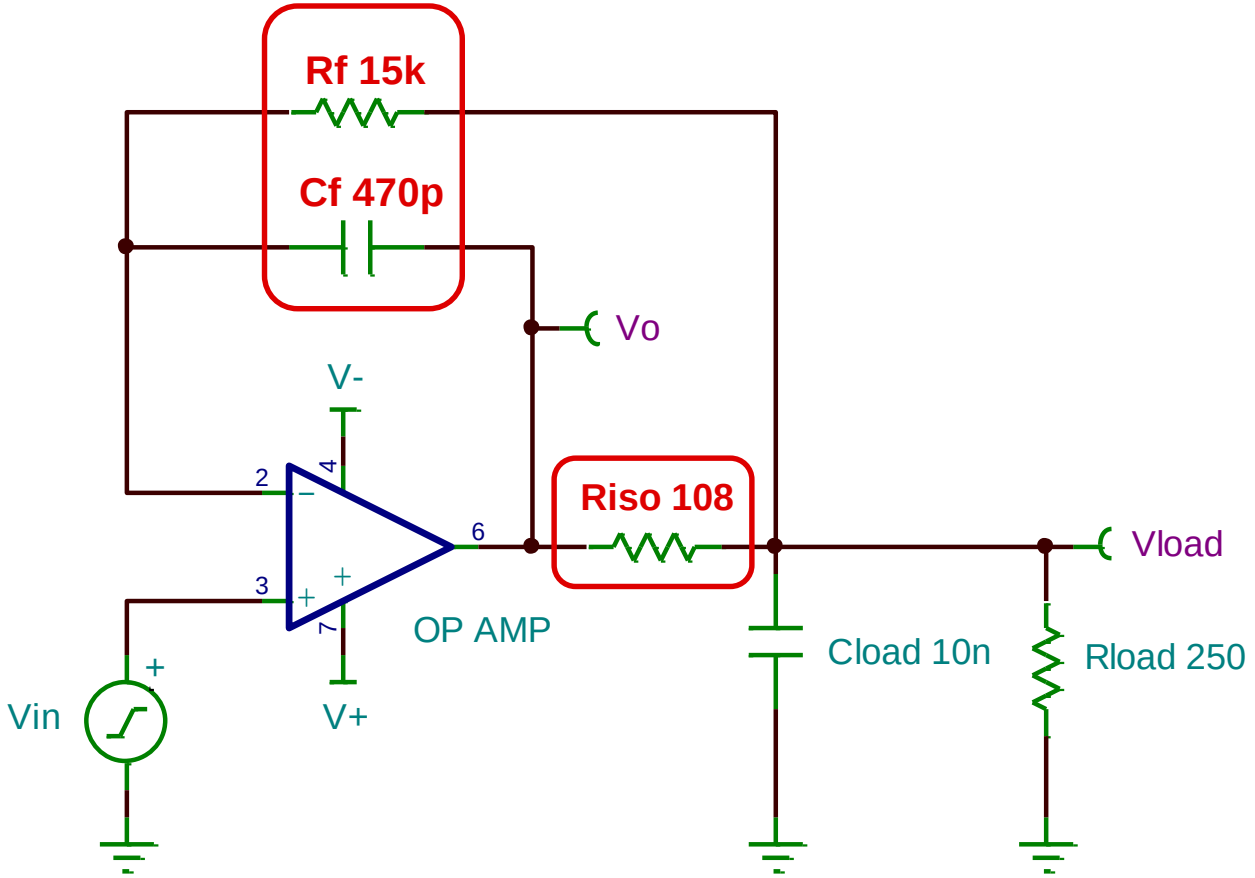
Method 1: R_{ISO} – disadvantage

Disadvantage: Voltage drop across R_{ISO} may not be acceptable for certain applications!





Method 2: R_{ISO} + dual feedback



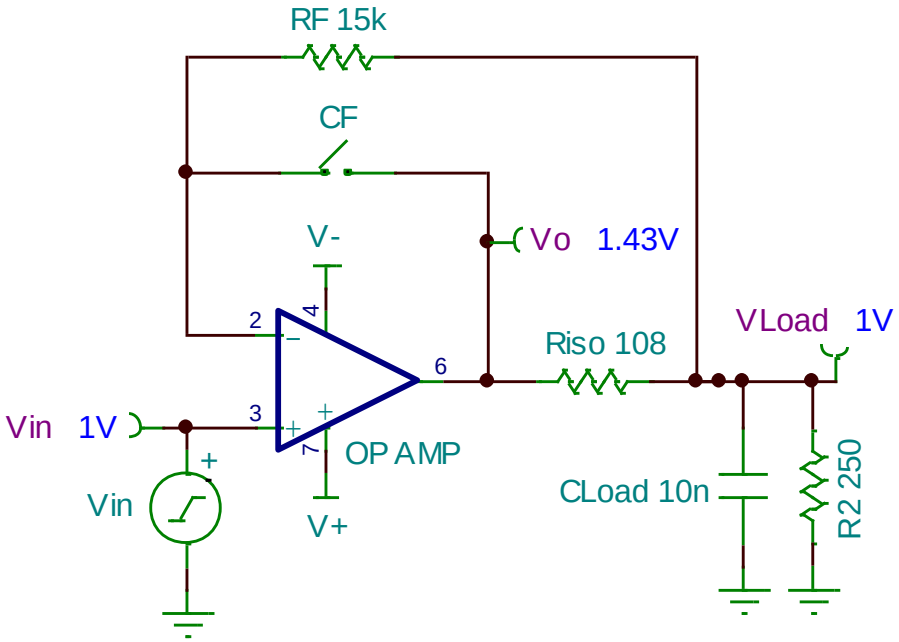
Dual feedback approach:

- Doesn't have voltage divider issue that simple R_{ISO} has
- More components
- Longer settling

Method 2: R_{ISO} + dual feedback – theory

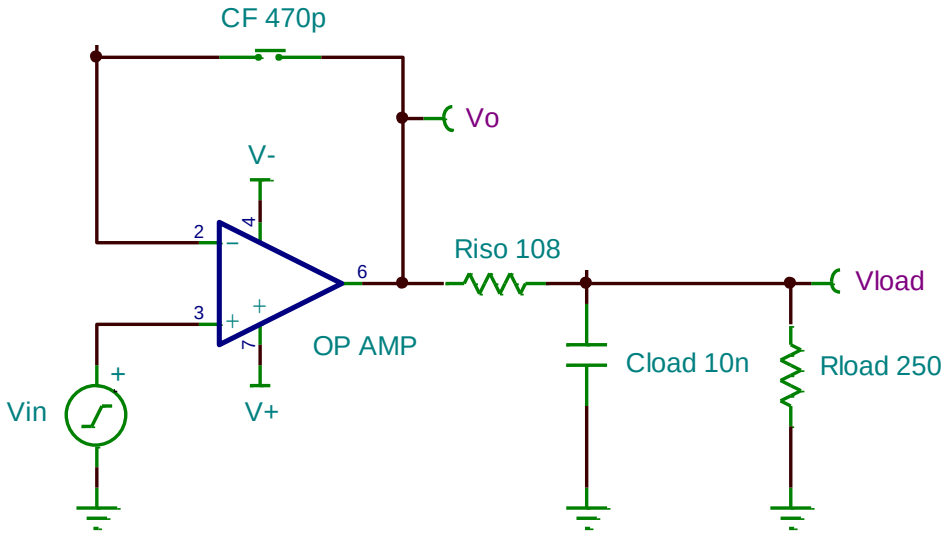
DC Circuit

C_F: Open
R_F: Closes the feedback around R_{ISO}
$V_{LOAD} = V_{IN}$



AC Circuit

C_F: Short
$R_F >> Z_{CF}$, therefore R_F is effectively open
Behaves like R_{ISO} circuit



Method 2: R_{ISO} + dual feedback - design

Design steps:

1. Set R_{ISO} using method 1: R_{ISO} techniques

   $\mathbf{R_{ISO} = 108\Omega}$

2. Set R_F: $R_F \geq (R_{ISO} * 100)$

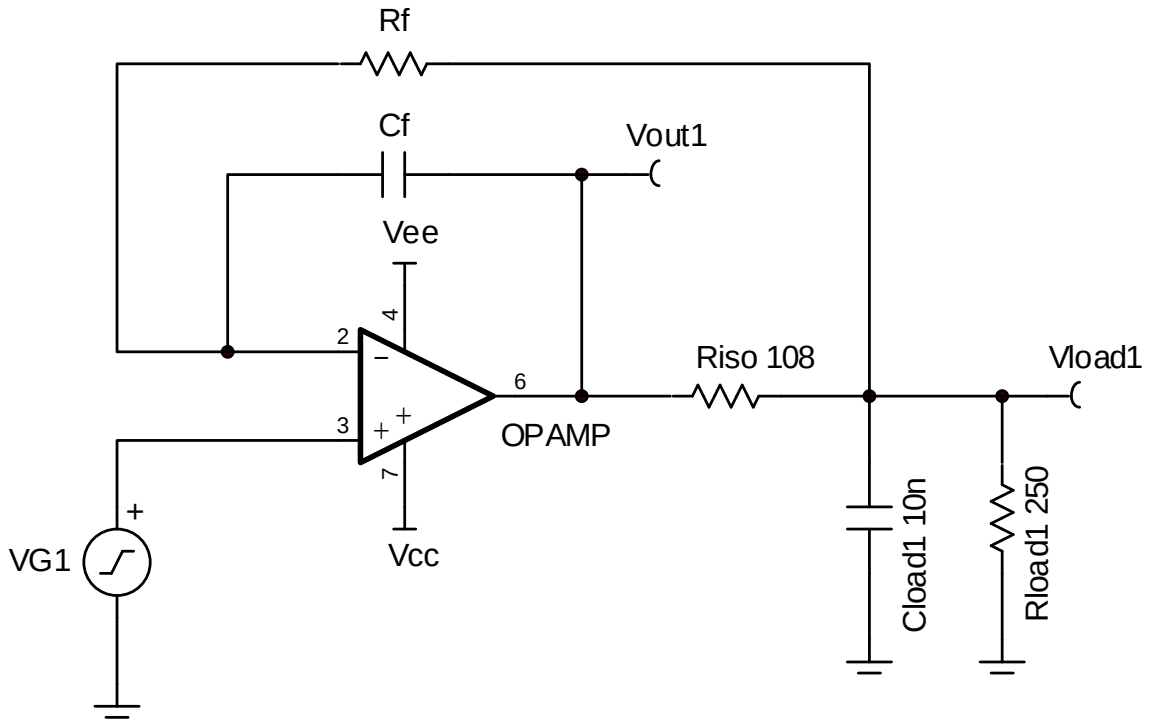
   $R_F \geq R_{ISO} * 100$

   $\mathbf{R_F \geq 10.8k\Omega}$

3. Set C_F:

$$\frac{5 \times R_{iso} \times C_L}{R_F} \leq C_F \leq \frac{10 \times R_{iso} \times C_L}{R_F}$$

$\mathbf{420pF \leq C_F \leq 720pF}$

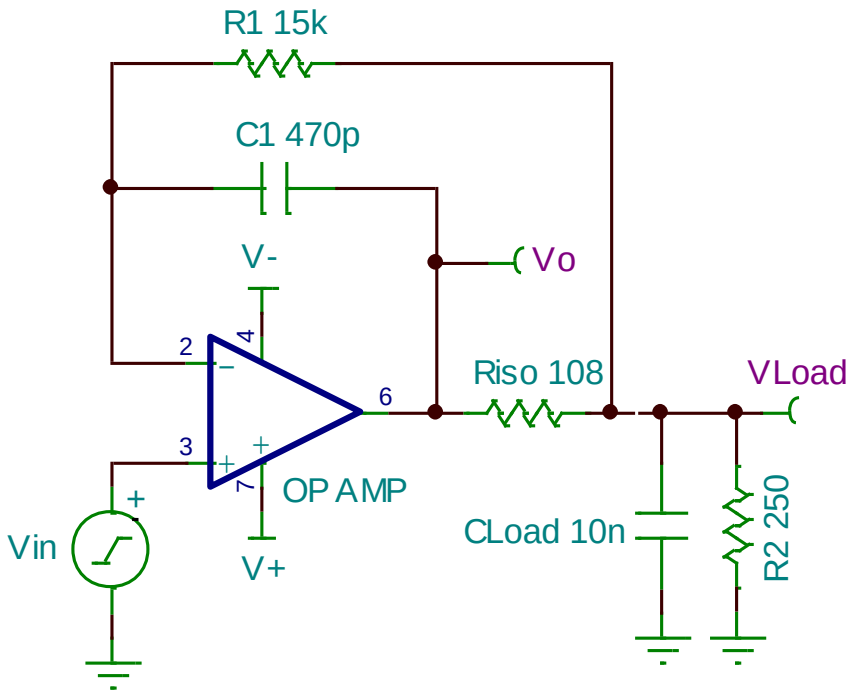


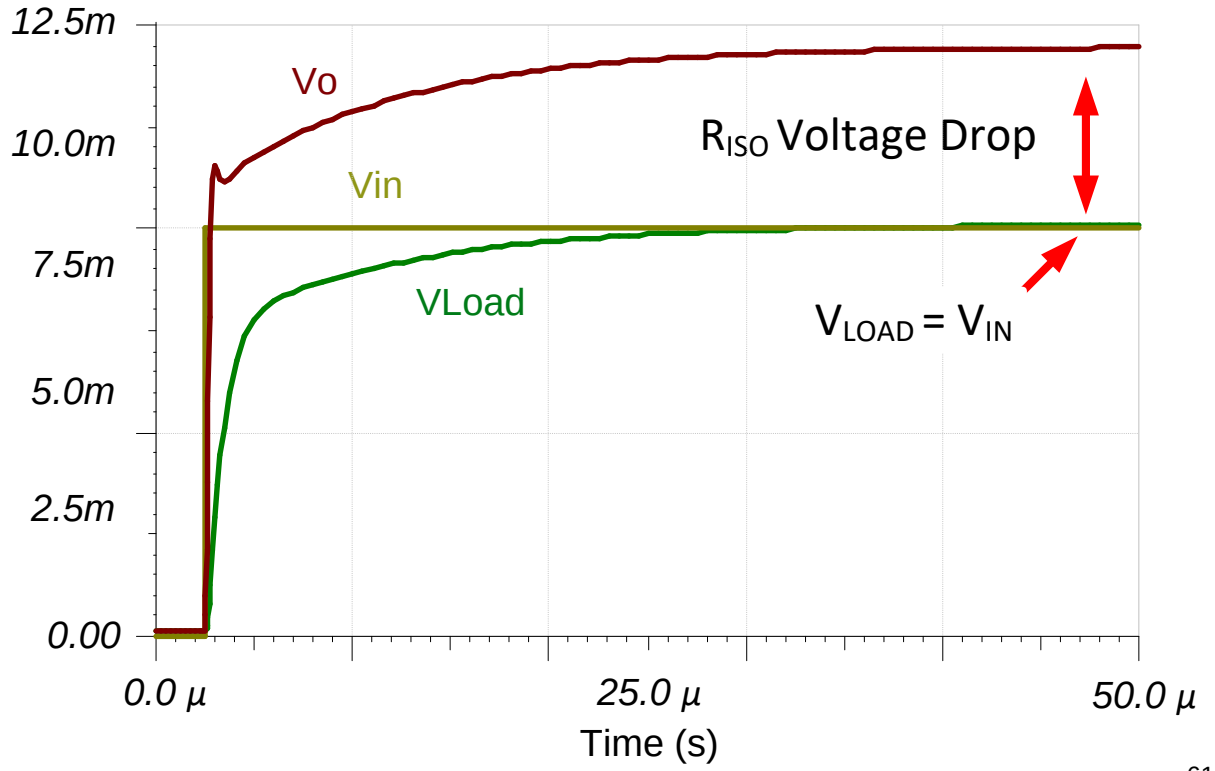
Notes:

- Rule 3 ensures that the two feedback paths will never create a resonance that would cause instability
- Lower values of C_F = faster settling, higher overshoot

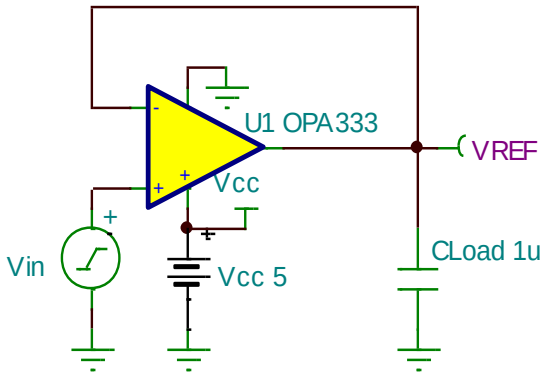
Method 2: R_{ISO} + dual feedback – results

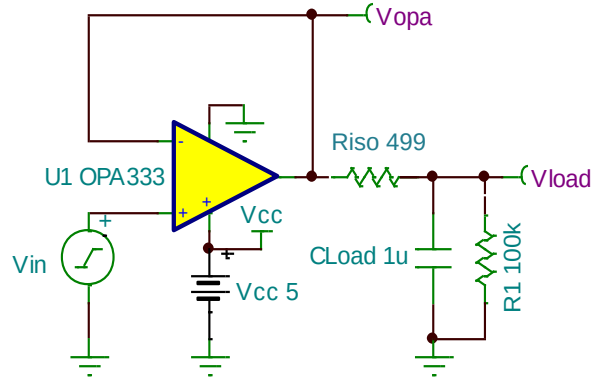
- V_{LOAD} matches V_{IN} – no voltage divider error!
- This topology has some limitations on settling time and capacitive load range

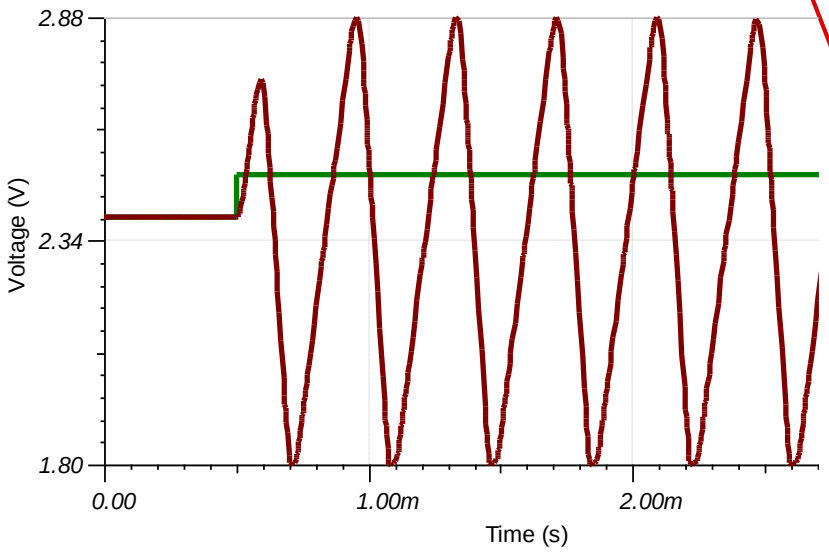


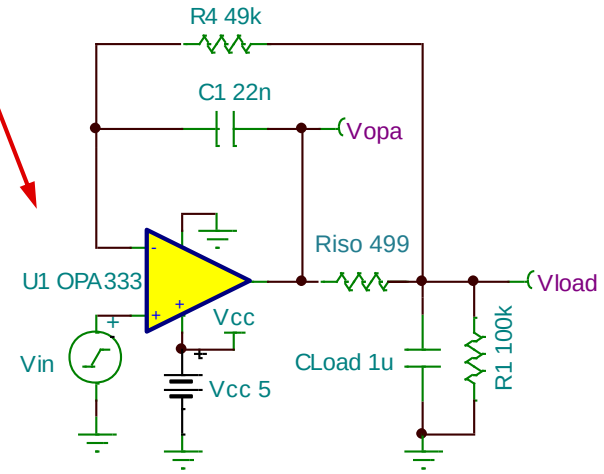


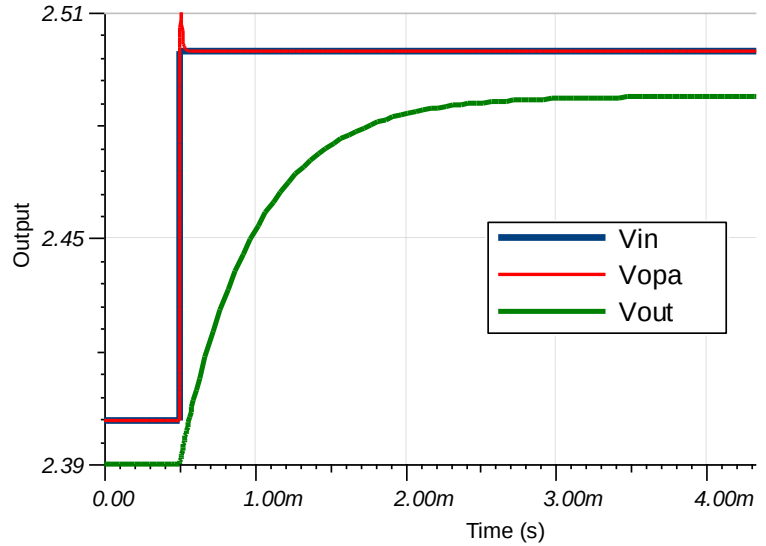
Solving op amp stability issues

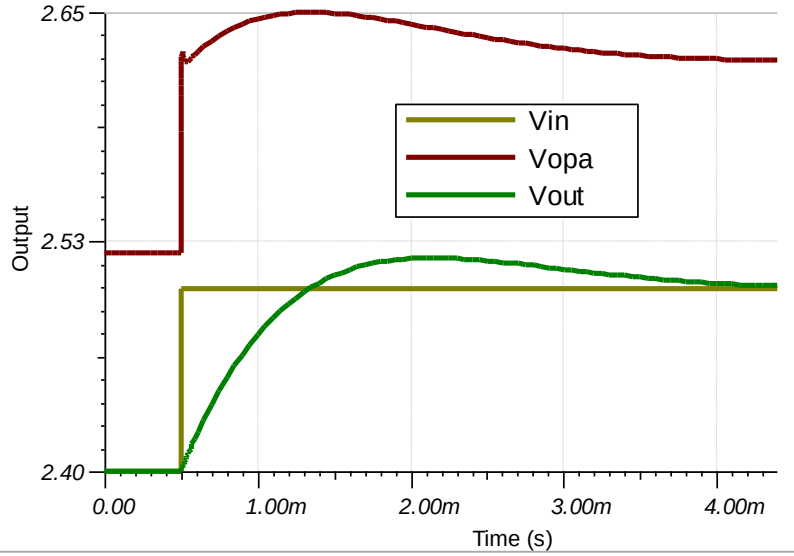






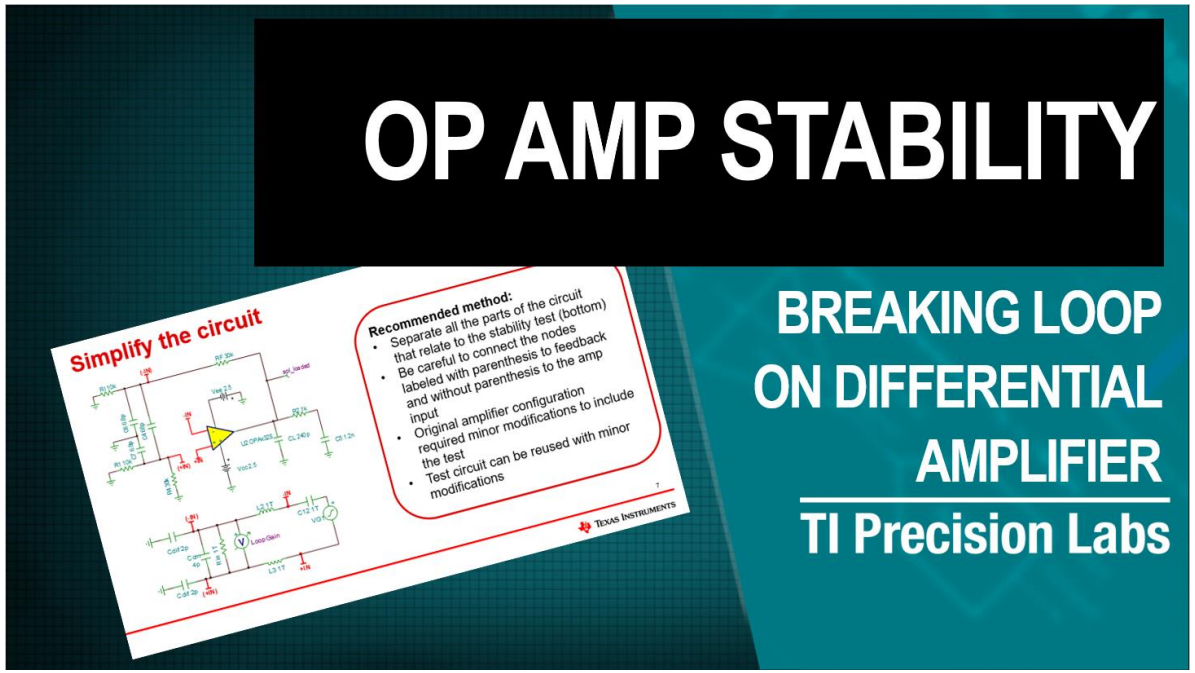




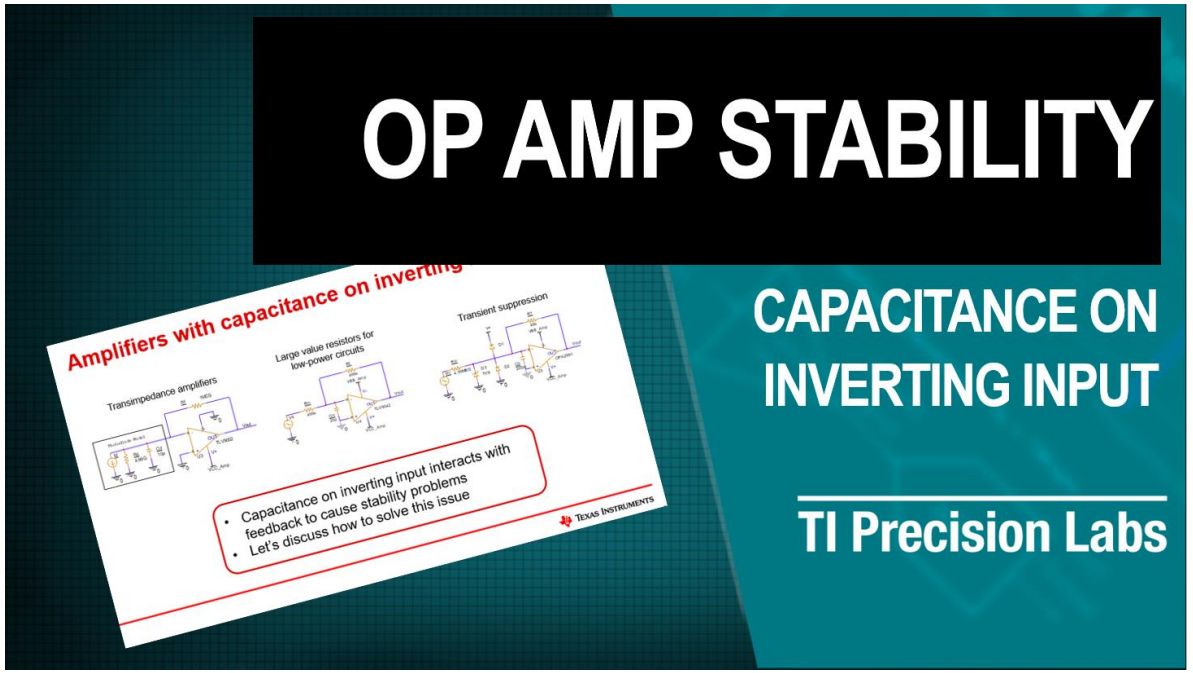


Other stability topics and methods

Breaking the loop on a differential amp



Capacitance on the inverting input



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Questions?

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