User's Guide

LMK05318B Register Maps

1 Device Registers

Table 1-1 lists the Device registers. All register offset addresses not listed in Table 1-1 should be considered as reserved locations and the register contents should not be modified.

Table 1-1. Device Registers

Address	Acronym	Register Name	Section
0x0	R0	VNDRID_BY1	Go
0x1	R1	VNDRID_BY0	Go
0x2	R2	PRODID	Go
0x3	R3	REVID	Go
0x4	R4	PARTID_BY3	Go
0x5	R5	PARTID_BY2	Go
0x6	R6	PARTID_BY1	Go
0x7	R7	PARTID_BY0	Go
0x8	R8	PINMODE_SW	Go
0xA	R10	SLAVEADR	Go
0xB	R11	EEREV	Go
0xC	R12	DEV_CTL	Go
0xD	R13	INT_LIVE0	Go
0xE	R14	INT_LIVE1	Go
0xF	R15	INT_MASK0	Go
0x10	R16	INT_MASK1	Go
0x11	R17	INT_FLAG_POL0	Go
0x12	R18	INT_FLAG_POL1	Go
0x13	R19	INT_FLAG0	Go
0x14	R20	INT_FLAG1	Go
0x15	R21	INTCTL	Go
0x16	R22	STAT_POL	Go
0x17	R23	MUTELVL1	Go
0x18	R24	MUTELVL2	Go
0x19	R25	OUT_MUTE	Go
0x1D	R29	DPLL_MUTE	Go
0x24	R36	GPIO_OUT	Go
0x27	R39	SPARE_NVMBASE2_BY2	Go
0x28	R40	SPARE_NVMBASE2_BY1	Go
0x2A	R42	XO_CLKCTL1	Go
0x2B	R43	XO_CLKCTL2	Go
0x2C	R44	XO_CONFIG	Go
0x2D	R45	REF_CLKCTL1	Go
0x2E	R46	REF_CLKCTL2	Go
0x2F	R47	PLL_CLK_CFG	Go
0x30	R48	STAT0_SEL	Go

Table 1-1. Device Registers (continued)

Address	Acronym	Register Name	Section
0x31	R49	STAT1_SEL	Go
0x32	R50	PWDN	Go
0x33	R51	OUTCTL_0	Go
0x34	R52	OUTCTL_1	Go
0x35	R53	OUTDIV_0_1	Go
0x36	R54	OUTCTL_2	Go
0x37	R55	OUTCTL_3	Go
0x38	R56	OUTDIV_2_3	Go
0x39	R57	OUTCTL_4	Go
0x3A	R58	OUTDIV_4	Go
0x3B	R59	OUTCTL_5	Go
0x3C	R60	OUTDIV_5	Go
0x3D	R61	OUTCTL_6	Go
0x3E	R62	OUTDIV_6	Go
0x3F	R63	OUTCTL_7	Go
0x40	R64	OUTDIV_7_STG2_BY2	Go
0x41	R65	OUTDIV_7_STG2_BY1	Go
0x42	R66	OUTDIV_7_STG2_BY0	Go
0x43	R67	OUTDIV_7	Go
0x44	R68	PREDRIVER	Go
0x46	R70	OUTSYNCCTL	Go
0x47	R71	OUTSYNCEN	Go
0x4A	R74	PLL1_CTRL0	Go
0x4F	R79	PLL1_CALCTRL0	Go
0x50	R80	BAW_LOCKDET_PPM_MAX_BY1	Go
0x51	R81	BAW_LOCKDET_PPM_MAX_BY0	Go
0x52	R82	BAW_LOCKDET_CNTSTRT_BY3	Go
0x53	R83	BAW_LOCKDET_CNTSTRT_BY2	Go
0x54	R84	BAW_LOCKDET_CNTSTRT_BY1	Go
0x55	R85	BAW_LOCKDET_CNTSTRT_BY0	Go
0x56	R86	BAW_LOCKDET_VCO_CNTSTRT_BY3	Go
0x57	R87	BAW_LOCKDET_VCO_CNTSTRT_BY2	Go
0x58	R88	BAW_LOCKDET_VCO_CNTSTRT_BY1	Go
0x59	R89	BAW_LOCKDET_VCO_CNTSTRT_BY0	Go
0x5A	R90	BAW_UNLOCKDET_PPM_MAX_BY1	Go
0x5B	R91	BAW_UNLOCKDET_PPM_MAX_BY0	Go
0x5C	R92	BAW_UNLOCKDET_CNTSTRT_BY3	Go
0x5D	R93	BAW_UNLOCKDET_CNTSTRT_BY2	Go
0x5E	R94	BAW_UNLOCKDET_CNTSTRT_BY1	Go
0x5F	R95	BAW_UNLOCKDET_CNTSTRT_BY0	Go
0x60	R96	BAW_UNLOCKDET_VCO_CNTSTRT_BY3	Go
0x61	R97	BAW_UNLOCKDET_VCO_CNTSTRT_BY2	Go
0x62	R98	BAW_UNLOCKDET_VCO_CNTSTRT_BY1	Go
0x63	R99	BAW_UNLOCKDET_VCO_CNTSTRT_BY0	Go
0x64	R100	PLL2_CTRL0	Go
0x65	R101	PLL2_CTRL1	Go
0x66	R102	PLL2_CTRL2	Go

Table 1-1. Device Registers (continued)

Address	Acronym	Register Name	Section
0x68	R104	PLL2_CTRL4	Go
0x69	R105	PLL2_CALCTRL0	Go
0x6C	R108	PLL1_NDIV_BY1	Go
0x6D	R109	PLL1_NDIV_BY0	Go
0x6E	R110	PLL1_NUM_BY4	Go
0x6F	R111	PLL1_NUM_BY3	Go
0x70	R112	PLL1_NUM_BY2	Go
0x71	R113	PLL1_NUM_BY1	Go
0x72	R114	PLL1_NUM_BY0	Go
0x73	R115	PLL1_MASHCTRL	Go
0x74	R116	PLL1_MODE	Go
0x7B	R123	PLL1_NUM_STAT_BY4	Go
0x7C	R124	PLL1_NUM_STAT_BY3	Go
0x7D	R125	PLL1_NUM_STAT_BY2	Go
0x7E	R126	PLL1_NUM_STAT_BY1	Go
0x7F	R127	PLL1_NUM_STAT_BY0	Go
0x81	R129	PLL1_LF_R2	Go
0x83	R131	PLL1_LF_R3	Go
0x84	R132	PLL1_LF_R4	Go
0x86	R134	PLL2_NDIV_BY1	Go
0x87	R135	PLL2_NDIV_BY0	Go
0x88	R136	PLL2_NUM_BY2	Go
0x89	R137	PLL2_NUM_BY1	Go
0x8A	R138	PLL2_NUM_BY0	Go
0x8B	R139	PLL2_MASHCTRL	Go
0x8C	R140	PLL2_LF_R2	Go
0x8E	R142	PLL2_LF_R3	Go
0x8F	R143	PLL2_LF_R4	Go
0x90	R144	PLL2_LF_C3C4	Go
0x91	R145	XO_OFFSET_SW_TIMER	Go
0x9C	R156	NVMCNT	Go
0x9D	R157	NVMCTL	Go
0x9F	R159	MEMADR_BY1	Go
0xA0	R160	MEMADR_BY0	Go
0xA1	R161	NVMDAT	Go
0xA2	R162	RAMDAT	Go
0xA4	R164	NVMUNLK	Go
0xB4	R180	DPLL_TUNING_FREE_RUN_BY4	Go
0xB5	R181	DPLL_TUNING_FREE_RUN_BY3	Go
0xB6	R182	DPLL_TUNING_FREE_RUN_BY2	Go
0xB7	R183	DPLL_TUNING_FREE_RUN_BY1	Go
0xB8	R184	DPLL_TUNING_FREE_RUN_BY0	Go
0xB9	R185	DPLL_REF_HISTCTL	Go
0xBA	R186	DPLL_REF_HISTCNT	Go
0xBB	R187	DPLL_REF_HISTDLY_BY3	Go
0xBC	R188	DPLL_REF_HISTDLY_BY2	Go
0xBD	R189	DPLL_REF_HISTDLY_BY1	Go

Table 1-1. Device Registers (continued)

Address	Acronym	Register Name	Section
0xBE	R190	DPLL_REF_HISTDLY_BY0	Go
0xC0	R192	REF01_DETAMP	Go
0xC1	R193	REF0_DETEN	Go
0xC2	R194	REF1_DETEN	Go
0xC3	R195	REF0_MISSCLK_DIV_BY2	Go
0xC4	R196	REF0_MISSCLK_DIV_BY1	Go
0xC5	R197	REF0_MISSCLK_DIV_BY0	Go
0xC6	R198	REF1_MISSCLK_DIV_BY2	Go
0xC7	R199	REF1_MISSCLK_DIV_BY1	Go
0xC8	R200	REF1_MISSCLK_DIV_BY0	Go
0xC9	R201	REF_MISSCLK_CTL	Go
0xCA	R202	REF0_EARLY_CLK_DIV_BY2	Go
0xCB	R203	REF0_EARLY_CLK_DIV_BY1	Go
0xCC	R204	REF0_EARLY_CLK_DIV_BY0	Go
0xCD	R205	REF1_EARLY_CLK_DIV_BY2	Go
0xCE	R206	REF1_EARLY_CLK_DIV_BY1	Go
0xCF	R207	REF1_EARLY_CLK_DIV_BY0	Go
0xD0	R208	REF0_PPM_MIN_BY1	Go
0xD1	R209	REF0_PPM_MIN_BY0	Go
0xD2	R210	REF0_PPM_MAX_BY1	Go
0xD3	R211	REF0_PPM_MAX_BY0	Go
0xD4	R212	REF1_PPM_MIN_BY1	Go
0xD5	R213	REF1_PPM_MIN_BY0	Go
0xD6	R214	REF1_PPM_MAX_BY1	Go
0xD7	R215	REF1_PPM_MAX_BY0	Go
0xD9	R217	REF0_CNTSTRT_BY3	Go
0xDA	R218	REF0_CNTSTRT_BY2	Go
0xDB	R219	REF0_CNTSTRT_BY1	Go
0xDC	R220	REF0_CNTSTRT_BY0	Go
0xDD	R221	REF0_HOLD_CNTSTRT_BY3	Go
0xDE	R222	REF0_HOLD_CNTSTRT_BY2	Go
0xDF	R223	REF0_HOLD_CNTSTRT_BY1	Go
0xE0	R224	REF0_HOLD_CNTSTRT_BY0	Go
0xE1	R225	REF1_CNTSTRT_BY3	Go
0xE2	R226	REF1_CNTSTRT_BY2	Go
0xE3	R227	REF1_CNTSTRT_BY1	Go
0xE4	R228	REF1_CNTSTRT_BY0	Go
0xE5	R229	REF1_HOLD_CNTSTRT_BY3	Go
0xE6	R230	REF1_HOLD_CNTSTRT_BY2	Go
0xE7	R231	REF1_HOLD_CNTSTRT_BY1	Go
0xE8	R232	REF1_HOLD_CNTSTRT_BY0	Go
0xE9	R233	REF0_VLDTMR	Go
0xEA	R234	REF1_VLDTMR	Go
0xEB	R235	REF0_PH_VALID_CNT_BY3	Go
0xEC	R236	REF0_PH_VALID_CNT_BY2	Go
0xED	R237	REF0_PH_VALID_CNT_BY1	Go
0xEE	R238	REF0_PH_VALID_CNT_BY0	Go

Table 1-1. Device Registers (continued)

Address	Acronym	Register Name	Section
0xEF	R239	REF1_PH_VALID_CNT_BY3	Go
0xF0	R240	REF1_PH_VALID_CNT_BY2	Go
0xF1	R241	REF1_PH_VALID_CNT_BY1	Go
0xF2	R242	REF1_PH_VALID_CNT_BY0	Go
0xF3	R243	REF0_PH_VALID_THR	Go
0xF4	R244	REF1_PH_VALID_THR	Go
0xF9	R249	DPLL_REF01_PRTY	Go
0xFB	R251	DPLL_REF_SWMODE	Go
0xFC	R252	DPLL_GEN_CTL	Go
0xFD	R253	DPLL_SWITCHOVER_TMR_EXP	Go
0xFE	R254	DPLL_SWITCHOVER_TMR_MANT_BY1	Go
0xFF	R255	DPLL_SWITCHOVER_TMR_MANT_BY0	Go
0x100	R256	DPLL_REF0_RDIV_BY1	Go
0x101	R257	DPLL_REF0_RDIV_BY0	Go
0x102	R258	DPLL_REF1_RDIV_BY1	Go
0x103	R259	DPLL_REF1_RDIV_BY0	Go
0x104	R260	DPLL_REF_TDC_CTL	Go
0x105	R261	DPLL_REF_DLY_GEN	Go
0x106	R262	DPLL_REF_CYCSLIP_OFFSET_BY4	Go
0x107	R263	DPLL_REF_CYCSLIP_OFFSET_BY3	Go
0x108	R264	DPLL_REF_CYCSLIP_OFFSET_BY2	Go
0x109	R265	DPLL_REF_CYCSLIP_OFFSET_BY1	Go
0x10A	R266	DPLL_REF_CYCSLIP_OFFSET_BY0	Go
0x10B	R267	DPLL_REF_LOOPCTL	Go
0x10C	R268	DPLL_REF_LOOPCTL_CHG	Go
0x10D	R269	DPLL_REF_DECIMATION	Go
0x10E	R270	DPLL_REF_FILTSCALAR_BY1	Go
0x10F	R271	DPLL_REF_FILTSCALAR_BY0	Go
0x110	R272	DPLL_REF_FILTGAIN	Go
0x111	R273	DPLL_REF_FILTGAIN_FL1	Go
0x112	R274	DPLL_REF_FILTGAIN_FL2	Go
0x113	R275	DPLL_REF_LOOPGAIN	Go
0x114	R276	DPLL_REF_LOOPGAIN_FL1	Go
0x115	R277	DPLL_REF_LOOPGAIN_FL2	Go
0x116	R278	DPLL_REF_LPF0GAIN	Go
0x117	R279	DPLL_REF_LPF0GAIN_FL1	Go
0x118	R280	DPLL_REF_LPF0GAIN_FL2	Go
0x119	R281	DPLL_REF_LPF1GAIN	Go
0x11A	R282	DPLL_REF_LPF1GAIN_FL1	Go
0x11B	R283	DPLL_REF_LPF1GAIN_FL2	Go
0x11C	R284	DPLL_REF_LPF0GAIN2_FL	Go
0x11D	R285	DPLL_REF_LPF1GAIN2_FL	Go
0x11E	R286	DPLL_REF_TMR_FL1_BY1	Go
0x11F	R287	DPLL_REF_TMR_FL1_BY0	Go
0x120	R288	DPLL_REF_TMR_FL2_BY1	Go
0x121	R289	DPLL_REF_TMR_FL2_BY0	Go
0x122	R290	DPLL_REF_TMR_LCK_BY1	Go

Table 1-1. Device Registers (continued)

Address	Acronym	Register Name	Section
0x123	R291	DPLL_REF_TMR_LCK_BY0	Go
0x124	R292	DPLL_REF_PHC_LPF	Go
0x125	R293	DPLL_REF_PHC_CTRL	Go
0x126	R294	DPLL_REF_PHC_TIMER_BY1	Go
0x127	R295	DPLL_REF_PHC_TIMER_BY0	Go
0x128	R296	DPLL_REF_QUANT	Go
0x129	R297	DPLL_REF_QUANT_FL1	Go
0x12A	R298	DPLL_REF_QUANT_FL2	Go
0x12C	R300	DPLL_PL_LPF_GAIN	Go
0x12D	R301	DPLL_PL_THRESH	Go
0x12E	R302	DPLL_PL_UNLK_THRESH	Go
0x130	R304	DPLL_REF_FB_PREDIV	Go
0x131	R305	DPLL_REF_FB_DIV_BY3	Go
0x132	R306	DPLL_REF_FB_DIV_BY2	Go
0x133	R307	DPLL_REF_FB_DIV_BY1	Go
0x134	R308	DPLL_REF_FB_DIV_BY0	Go
0x135	R309	DPLL_REF_NUM_BY4	Go
0x136	R310	DPLL_REF_NUM_BY3	Go
0x137	R311	DPLL_REF_NUM_BY2	Go
0x138	R312	DPLL_REF_NUM_BY1	Go
0x139	R313	DPLL_REF_NUM_BY0	Go
0x13A	R314	DPLL_REF_DEN_BY4	Go
0x13B	R315	DPLL_REF_DEN_BY3	Go
0x13C	R316	DPLL_REF_DEN_BY2	Go
0x13D	R317	DPLL_REF_DEN_BY1	Go
0x13E	R318	DPLL_REF_DEN_BY0	Go
0x13F	R319	DPLL_REF_MASHCTL	Go
0x140	R320	DPLL_REF_LOCKDET_PPM_MAX_BY1	Go
0x141	R321	DPLL_REF_LOCKDET_PPM_MAX_BY0	Go
0x142	R322	DPLL_REF_LOCKDET_CNTSTRT_BY3	Go
0x143	R323	DPLL_REF_LOCKDET_CNTSTRT_BY2	Go
0x144	R324	DPLL_REF_LOCKDET_CNTSTRT_BY1	Go
0x145	R325	DPLL_REF_LOCKDET_CNTSTRT_BY0	Go
0x146	R326	DPLL_REF_LOCKDET_VCO_CNTSTRT_BY3	Go
0x147	R327	DPLL_REF_LOCKDET_VCO_CNTSTRT_BY2	Go
0x148	R328	DPLL_REF_LOCKDET_VCO_CNTSTRT_BY1	Go
0x149	R329	DPLL_REF_LOCKDET_VCO_CNTSTRT_BY0	Go
0x14A	R330	DPLL_REF_UNLOCKDET_PPM_MAX_BY1	Go
0x14B	R331	DPLL_REF_UNLOCKDET_PPM_MAX_BY0	Go
0x14C	R332	DPLL_REF_UNLOCKDET_CNTSTRT_BY3	Go
0x14D	R333	PLL2_DEN_BY2	Go
0x14E	R334	PLL2_DEN_BY1	Go
0x14F	R335	PLL2_DEN_BY0	Go
0x150	R336	DPLL_REF_UNLOCKDET_VCO_CNTSTRT_BY3	Go
0x151	R337	DPLL_REF_UNLOCKDET_VCO_CNTSTRT_BY2	Go
0x152	R338	DPLL_REF_UNLOCKDET_VCO_CNTSTRT_BY1	Go
0x153	R339	PLL1_24B_NUM_MSB	Go

Table 1-1. Device Registers (continued)

Address	Acronym	Register Name	Section
0x154	R340	DPLL_REF_SYNC_PH_OFFSET_BY5	Go
0x155	R341	DPLL_REF_SYNC_PH_OFFSET_BY4	Go
0x156	R342	DPLL_REF_SYNC_PH_OFFSET_BY3	Go
0x157	R343	DPLL_REF_SYNC_PH_OFFSET_BY2	Go
0x158	R344	DPLL_REF_SYNC_PH_OFFSET_BY1	Go
0x159	R345	DPLL_REF_SYNC_PH_OFFSET_BY0	Go
0x15A	R346	DPLL_FDEV_CTL	Go
0x15B	R347	DPLL_FDEV_BY4	Go
0x15C	R348	DPLL_FDEV_BY3	Go
0x15D	R349	DPLL_FDEV_BY2	Go
0x15E	R350	DPLL_FDEV_BY1	Go
0x15F	R351	DPLL_FDEV_BY0	Go
0x160	R352	DPLL_FDEV_REG_CTL	Go
0x165	R357	PLL1_CALSTAT1	Go
0x16F	R367	PLL2_CALSTAT1	Go
0x19B	R411	REFVALSTAT	Go

Complex bit access types are encoded to fit into small table cells. Table 1-2 shows the codes that are used for access types in this section.

Table 1-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W0C	W 0C	Write 0 to clear
W1S	W 1S	Write 1 to set
Reset or Default Value		
- *n*		Value after reset or the default value

1.1 R0 Register (Address = 0x0) [Reset = 0x10]

R0 is shown in Table 1-3.

Return to the Summary Table.

Table 1-3. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VNDRID_15:8	R	0x10	Bits 15:8 of VNDRID

1.2 R1 Register (Address = 0x1) [Reset = 0xB]

R1 is shown in Table 1-4.

Return to the Summary Table.

Table 1-4. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	VNDRID	R	0xB	Vendor Identification Number Unique 16-bit number assigned to chip vendors.

1.3 R2 Register (Address = 0x2) [Reset = 0x35]

R2 is shown in Table 1-5.

Return to the Summary Table.

Table 1-5. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRODID	R	0x35	Product Identification Number Unique 8-bit number used to identify the LMK05318.

1.4 R3 Register (Address = 0x3) [Reset = 0x0]

R3 is shown in Table 1-6.

Return to the Summary Table.

Table 1-6. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REVID	R	0x0	Device Revision Number Used to identify the mask-set revision.

1.5 R4 Register (Address = 0x4) [Reset = 0x0]

R4 is shown in Table 1-7.

Return to the Summary Table.

Table 1-7. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRTID_31:24	R	0x0	Bits 31:24 of PRTID

1.6 R5 Register (Address = 0x5) [Reset = 0x0]

R5 is shown in Table 1-8.

Return to the Summary Table.

Table 1-8. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRTID_23:16	R	0x0	Bits 23:16 of PRTID

1.7 R6 Register (Address = 0x6) [Reset = 0x0]

R6 is shown in Table 1-9.

Return to the Summary Table.

Table 1-9. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRTID_15:8	R	0x0	Bits 15:8 of PRTID

1.8 R7 Register (Address = 0x7) [Reset = 0x0]

R7 is shown in Table 1-10.

Return to the Summary Table.

Table 1-10. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRTID	R	0x0	Part Identification Number 32-bit number used to serialize individual LMK05318 devices. Factory programmed. Cannot be modified by the user.

1.9 R8 Register (Address = 0x8) [Reset = 0x0]

R8 is shown in Table 1-11.

Return to the Summary Table.

Table 1-11. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	HW_SW_CTRL_MODE	R	0x0	HW_SW_CTRL Pin Configuration Reflects the values sampled on the HW_SW_CTRL pin during device power-on reset (POR). 0x0 = EEPROM/Soft Pin Mode 0x1 = ROM/Hard Pin Mode
5:3	RESERVED	R	0x0	Reserved
2:0	OP_MODE	R	0x0	Operating Mode The OP_MODE fields reflects the device operating mode as determined by the input levels on the HW_SW_CTRL, STATUS0, and STATUS1 pins respectively during POR. 0x0 = Reserved 0x1 = Reserved 0x2 = EEPROM + I2C, Soft pin mode 0x3 = ROM + I2C, Hard pin mode 0x4 = EEPROM + SPI, Soft pin mode 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved

1.10 R10 Register (Address = 0xA) [Reset = 0xC8]

R10 is shown in Table 1-12.

Return to the Summary Table.

Table 1-12. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	SLAVEADR_GPIO1_SW	R	0x64	7-bit I2C Slave Address The five MSBs (base address bits) are programmable in EEPROM, which is 11001b for generic factory devices. The two LSBs are determined by control input pin levels. When the HW_SW_CTRL pin is 1, the two LSBs are fixed to 00b. When the HW_SW_CTRL pin is 0, the 2 LSBs are determined by the GPIO1 input state (3-level) during POR.
0	RESERVED	R	0x0	Reserved

1.11 R11 Register (Address = 0xB) [Reset = 0x0]

R11 is shown in Table 1-13.

Return to the Summary Table.

Table 1-13. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	EEREV	R	0x0	EEPROM Image Revision ID EEPROM Image Revision ID is automatically retrieved from EEPROM and reflected in the EEREV register after a reset or after a NVM commit operation. This register is user programmable. EEPROM register 11 can be written through the SRAM.

1.12 R12 Register (Address = 0xC) [Reset = 0x39]

R12 is shown in Table 1-14.

Return to the Summary Table.

Table 1-14. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET_SW	R/W	0x0	Software Reset ALL functions Writing a 1 will cause the device to return to its power-up state apart from the registers and the configuration controller. The configuration controller is excluded to prevent a re-transfer of EEPROM data to on-chip registers.
6	SYNC_SW	R/W	0x0	Output Synchronization (SYNC) Assert bit
5	SYNC_AUTO_DPLL	R/W	0x1	Enable Automatic Output SYNC after DPLL lock
4	SYNC_AUTO_APLL	R/W	0x1	Enable Automatic Output SYNC after PLL lock
3	SYNC_MUTE	R/W	0x1	Determines if the output drivers are muted during a SYNC event 0x0 = Do not mute any outputs during SYNC 0x1 = Mute all outputs during SYNC
2	RESERVED	R	0x0	Reserved
1:0	RESERVED	R/W	0x1	Reserved

1.13 R13 Register (Address = 0xD) [Reset = 0x0]

R13 is shown in Table 1-15.

Return to the Summary Table.

Table 1-15. R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	LOS_FDET_XO	R	0x0	Loss of source freq detection XO
3	LOL_PLL2	R	0x0	Loss of Lock APLL2
2	LOL_PLL1	R	0x0	Loss of Lock APLL1
1	RESERVED	R	0x0	Reserved
0	LOS_XO	R	0x0	Loss of source XO

1.14 R14 Register (Address = 0xE) [Reset = 0x0]

R14 is shown in Table 1-16.

Return to the Summary Table.

Table 1-16. R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL	R	0x0	Loss of phase lock DPLL
6	LOFL_DPLL	R	0x0	Loss of frequency lock DPLL
5	HIST	R	0x0	Tuning word history update DPLL
4	HLDOVR	R	0x0	Holdover event DPLL

Table 1-16. R14 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	REFSWITCH	R	0x0	Reference switchover DPLL
2	LOR_MISSCLK	R	0x0	Loss of active reference missing clock DPLL
1	LOR_FREQ	R	0x0	Loss of active reference frequency DPLL
0	LOR_AMP	R	0x0	Loss of active reference amplitude DPLL

1.15 R15 Register (Address = 0xF) [Reset = 0x0]

R15 is shown in Table 1-17.

Return to the Summary Table.

Table 1-17. R15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	LOS_FDET_XO_MASK	R/W	0x0	Mask Loss of Source Freq Det XO When set to 1, interrupt output is not triggered.
3	LOL_PLL2_MASK	R/W	0x0	Mask Loss of Lock APLL2 When set to 1, interrupt output is not triggered.
2	LOL_PLL1_MASK	R/W	0x0	Mask Loss of Lock APLL1 When set to 1, interrupt output is not triggered.
1	RESERVED	R	0x0	Reserved
0	LOS_XO_MASK	R/W	0x0	Mask Loss of source XO When set to 1, interrupt output is not triggered.

1.16 R16 Register (Address = 0x10) [Reset = 0x0]

R16 is shown in Table 1-18.

Return to the Summary Table.

Table 1-18. R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL_MASK	R/W	0x0	Mask Loss of Phase Lock DPLL When set to 1, interrupt output is not triggered.
6	LOFL_DPLL_MASK	R/W	0x0	Mask Loss of Freq Lock DPLL When set to 1, interrupt output is not triggered.
5	HIST_MASK	R/W	0x0	Mask Tuning word history update DPLL When set to 1, interrupt output is not triggered.
4	HLDOVR_MASK	R/W	0x0	Mask Holdover event DPLL When set to 1, interrupt output is not triggered.
3	REFSWITCH_MASK	R/W	0x0	Mask Reference switchover DPLL When set to 1, interrupt output is not triggered.
2	LOR_MISSCLK_MASK	R/W	0x0	Mask Loss of active reference missing clk DPLL When set to 1, interrupt output is not triggered.
1	LOR_FREQ_MASK	R/W	0x0	Mask Loss of active reference freq DPLL When set to 1, interrupt output is not triggered.
0	LOR_AMP_MASK	R/W	0x0	Mask Loss of active reference amplitude DPLL When set to 1, interrupt output is not triggered.

1.17 R17 Register (Address = 0x11) [Reset = 0x0]

R17 is shown in Table 1-19.

Return to the Summary Table.

Table 1-19. R17 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	LOS_FDET_XO_POL	R/W	0x0	LOS_FDET_XO Flag Polarity
3	LOL_PLL2_POL	R/W	0x0	LOL_PLL2 Flag Polarity
2	LOL_PLL1_POL	R/W	0x0	LOL_PLL1 Flag Polarity
1	RESERVED	R	0x0	Reserved
0	LOS_XO_POL	R/W	0x0	LOS_XO Flag Polarity

1.18 R18 Register (Address = 0x12) [Reset = 0x0]

R18 is shown in Table 1-20.

Return to the Summary Table.

Table 1-20. R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL_POL	R/W	0x0	LOPL_DPLL Flag Polarity
6	LOFL_DPLL_POL	R/W	0x0	LOFL_DPLL Flag Polarity
5	HIST_POL	R/W	0x0	HIST Flag Polarity
4	HLDOVR_POL	R/W	0x0	HLDOVR Flag Polarity
3	REFSWITCH_POL	R/W	0x0	REFSWITCH Flag Polarity
2	LOR_MISSCLK_POL	R/W	0x0	LOR_MISSCLK Flag Polarity
1	LOR_FREQ_POL	R/W	0x0	LOR_FREQ Flag Polarity
0	LOR_AMP_POL	R/W	0x0	LOR_AMP Flag Polarity

1.19 R19 Register (Address = 0x13) [Reset = 0x0]

R19 is shown in Table 1-21.

Return to the Summary Table.

Table 1-21. R19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	LOS_FDET_XO_INTR	R/W0C	0x0	LOL_FDET_XO Interrupt Bit is set when an edge of the correct polarity is detected on the LOL_FDET_XO interrupt source. The bit is cleared by writing a 0.
3	LOL_PLL2_INTR	R/W0C	0x0	LOL_PLL2 Interrupt Bit is set when an edge of the correct polarity is detected on the LOL_PLL2 interrupt source. The bit is cleared by writing a 0.
2	LOL_PLL1_INTR	R/W0C	0x0	LOL_PLL1 Interrupt Bit is set when an edge of the correct polarity is detected on the LOL_PLL1 interrupt source.The bit is cleared by writing a 0.
1	RESERVED	R	0x0	Reserved
0	LOS_XO_INTR	R/W0C	0x0	LOS_XO Interrupt Bit is set when an edge of the correct polarity is detected on the LOS_XO interrupt source. The bit is cleared by writing a 0.

1.20 R20 Register (Address = 0x14) [Reset = 0x0]

R20 is shown in Table 1-22.

Return to the Summary Table.

Table 1-22. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL_INTR	R/W0C	0x0	LOPL_DPLL Interrupt Bt is set when an edge of the correct polarity is detected on the LOPL_DPLL interrupt source. The bit is cleared by writing a 0.
6	LOFL_DPLL_INTR	R/W0C	0x0	LOFL_DPLL Interrupt Bit is set when an edge of the correct polarity is detected on the LOFL_DPLL interrupt source. The bit is cleared by writing a 0.
5	HIST_INTR	R/W0C	0x0	HIST Interrupt Bit is set when an edge of the correct polarity is detected on the HIST interrupt source. The bit is cleared by writing a 0.
4	HLDOVR_INTR	R/W0C	0x0	HLDOVR Interrupt Bit is set when an edge of the correct polarity is detected on the HLDOVR interrupt source. The bit is cleared by writing a 0.
3	REFSWITCH_INTR	R/W0C	0x0	REFSWITCH Interrupt Bit is set when an edge of the correct polarity is detected on the REFSWITCH interrupt source. The bit is cleared by writing a 0.
2	LOR_MISSCLK_INTR	R/W0C	0x0	LOR_MISSCLK Interrupt Bit is set when an edge of the correct polarity is detected on the LOR_MISSCLK interrupt source. The bit is cleared by writing a 0.
1	LOR_FREQ_INTR	R/W0C	0x0	LOR_FREQ Interrupt Bit is set when an edge of the correct polarity is detected on the LOR_FREQ interrupt source. The bit is cleared by writing a 0.
0	LOR_AMP_INTR	R/W0C	0x0	LOR_AMP Interrupt Bit is set when an edge of the correct polarity is detected on the LOR_AMP interrupt source. The bit is cleared by writing a 0.

1.21 R21 Register (Address = 0x15) [Reset = 0x0]

R21 is shown in Table 1-23.

Return to the Summary Table.

Table 1-23. R21 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	INT_AND_OR	R/W	0x0	Interrupt Logical AND or OR Combination 0x0 = OR: Any un-masked interrupt flags can generate an interrupt. 0x1 = AND: All un-masked interrupt flags must be active in order to generate an interrupt.
0	INT_EN	R/W	0x0	Interrupt Enable

1.22 R22 Register (Address = 0x16) [Reset = 0x0]

R22 is shown in Table 1-24.

Return to the Summary Table.

Table 1-24. R22 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	STAT1_POL	R/W	0x0	STATUS1 Output Polarity Defines the polarity of information presented on the STATUS1 output. If STAT1_POL is set to 1 then STATUS1 is active high, if STAT1_POL is 0then STATUS1 is active low.
0	STAT0_POL	R/W	0x0	STATUS0 Output Polarity Defines the polarity of information presented on the STATUS0 output. If STAT0_POL is set to 1 then STATUS0 is active high, if STAT0_POL is 0then STATUS0 is active low.

1.23 R23 Register (Address = 0x17) [Reset = 0x0]

R23 is shown in Table 1-25.

Return to the Summary Table.

Table 1-25. R23 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CH3_MUTE_LVL	R/W	0x0	Output 3 Mute Level See CH0_MUTE_LVL for description and bit settings.
5:4	CH2_MUTE_LVL	R/W	0x0	Output 2 Mute Level See CH0_MUTE_LVL for description and bit settings.
3:2	CH1_MUTE_LVL	R/W	0x0	Output 1 Mute Level See CH0_MUTE_LVL for description and bit settings.
1:0	CH0_MUTE_LVL	R/W	0x0	Output 0 Mute Level Determines the configuration of the Output Driver during mute. 0x0 = Bypass Mute (Normal Operation) 0x1 = For DIFF or HCSL mute to differential Vocm. For LVCMOS, P is Bypass Mute and N is Mute Low. 0x2 = For DIFF or HCSL mute to differntial High. For LVCMOS, P is Mute Low and N is Bypass Mute. 0x3 = For DIFF or HCSL mute to differential Low. For LVCMOS, P is Mute Low and N is Mute Low.

1.24 R24 Register (Address = 0x18) [Reset = 0x0]

R24 is shown in Table 1-26.

Return to the Summary Table.

Table 1-26. R24 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CH7_MUTE_LVL	R/W	0x0	Output 7 Mute Level See CH0_MUTE_LVL for description and bit settings.
5:4	CH6_MUTE_LVL	R/W	0x0	Output 6 Mute Level See CH0_MUTE_LVL for description and bit settings.
3:2	CH5_MUTE_LVL	R/W	0x0	Output 5 Mute Level See CH0_MUTE_LVL for description and bit settings.
1:0	CH4_MUTE_LVL	R/W	0x0	Output 4 Mute Level See CH0_MUTE_LVL for description and bit settings.

1.25 R25 Register (Address = 0x19) [Reset = 0xFF]

R25 is shown in Table 1-27.

Return to the Summary Table.

Table 1-27. R25 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH7_MUTE	R/W	0x1	Output 7 Mute Control
6	CH6_MUTE	R/W	0x1	Output 6 Mute Control
5	CH5_MUTE	R/W	0x1	Output 5 Mute Control
4	CH4_MUTE	R/W	0x1	Output 4 Mute Control
3	CH3_MUTE	R/W	0x1	Output 3 Mute Control
2	CH2_MUTE	R/W	0x1	Output 2 Mute Control
1	CH1_MUTE	R/W	0x1	Output 1 Mute Control
0	CH0_MUTE	R/W	0x1	Output 0 Mute Control

1.26 R29 Register (Address = 0x1D) [Reset = 0x13]

R29 is shown in Table 1-28.

Return to the Summary Table.

Table 1-28. R29 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	MUTE_APLL2_LOCK	R/W	0x1	APLL2 mute enabled during PLL lock
3	RESERVED	R	0x0	Reserved
2	MUTE_DPLL_PHLOCK	R/W	0x0	DPLL mute enabled during phase lock
1	MUTE_DPLL_FLLOCK	R/W	0x1	DPLL mute enabled during DPLL lock
0	MUTE_APLL1_LOCK	R/W	0x1	APLL1 mute enabled during PLL lock

1.27 R36 Register (Address = 0x24) [Reset = 0x0]

R36 is shown in Table 1-29.

Return to the Summary Table.

Table 1-29. R36 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	GPIO_STAT1_OUT	R/W	0x0	STAT1 Driver Type Output 0x0 = NMOS Open-drain driver 0x1 = LVCMOS driver
0	GPIO_STAT0_OUT	R/W	0x0	STAT0 Driver Type Output 0x0 = NMOS Open-drain driver 0x1 = LVCMOS driver

1.28 R39 Register (Address = 0x27) [Reset = 0x0]

R39 is shown in Table 1-30.

Return to the Summary Table.

Table 1-30. R39 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:2	RESERVED	R/W	0x0	Reserved
1	GPIO2_OUT	R/W	0x0	GPIO2 Driver Type GPIO2 0x0 = NMOS Open-drain driver 0x1 = LVCMOS driver
0	APLL1_DEN_MODE	R/W	0x0	Programmable APLL1 denominator mode 0x0 = APLL1 uses programmable 40-bit numerator (R110, R111, R112, R113, R114) and fixed 40-bit denominator 0x1 = APLL1 uses programmable 24-bit numberator (R339, R110, R111) and programmable 24-bit denominator (R112, R113, R114)

1.29 R40 Register (Address = 0x28) [Reset = 0x0]

R40 is shown in Table 1-31.

Return to the Summary Table.

Table 1-31. R40 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0x0	Reserved

Table 1-31. R40 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	SECREF_DC_MODE	R/W	0x0	SECREF DC buffer mode 0x0 = SECREF is AC coupled internally 0x1 = SECREF is DC coupled internally
2	PRIREF_DC_MODE	R/W	0x0	PRIREF DC buffer mode 0x0 = PRIREF is AC coupled internally 0x1 = PRIREF is DC coupled internally
1	RESERVED	R/W	0x0	Reserved
0	APLL2_DEN_MODE	R/W	0x0	Programmable APLL2 denominator mode 0x0 = APLL2 uses fixed 24-bit denominator 0x1 = APLL2 uses programmable 24-bit denominator (R333, R334, R335)

1.30 R42 Register (Address = 0x2A) [Reset = 0x1]

R42 is shown in Table 1-32.

Return to the Summary Table.

Table 1-32. R42 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	OSCIN_DBLR_EN	R/W	0x0	Enable OSCIn doubler
3	XO_FDET_BYP	R/W	0x0	XO Frequency Detector Bypass If bypassed, the XO detector status is ignored and the XO input is considered valid by the PLL control state machines
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R/W	0x1	Reserved

1.31 R43 Register (Address = 0x2B) [Reset = 0x82]

R43 is shown in Table 1-33.

Return to the Summary Table.

Table 1-33. R43 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x1	Reserved
6:3	XO_TYPE	R/W	0x0	XO Input Type 0x0 = DC-Differential (external termination) 0x1 = AC-Differential (external termination) 0x3 = AC-Differential (internal termination 100-Ω) 0x4 = HCSL (internal termination 50-Ω) 0x8 = CMOS 0xC = Single-ended (internal termination 50-Ω)
2:0	RESERVED	R/W	0x2	Reserved

1.32 R44 Register (Address = 0x2C) [Reset = 0x1]

R44 is shown in Table 1-34.

Return to the Summary Table.

Table 1-34. R44 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved

Table 1-34. R44 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	OSCIN_RDIV	R/W	0x1	Oscillator Input Divider

1.33 R45 Register (Address = 0x2D) [Reset = 0x3]

R45 is shown in Table 1-35.

Return to the Summary Table.

Table 1-35. R45 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	SECREF_CMOS_SLEW	R/W	0x0	SECREF input buffer slew rate 0x0 = Select Amplitude Detector Mode 0x1 = Select CMOS Amplitude Detector Mode
2	PRIREF_CMOS_SLEW	R/W	0x0	PRIREF input buffer slew rate 0x0 = Select Amplitude Detector Mode 0x1 = Select CMOS Amplitude Detector Mode
1	SECREF_BUF_MODE	R/W	0x1	SECREF buffer mode. 0x0 = Set AC buffer hysteresis to 50 mV or enable DC buffer hysteresis 0x1 = Set AC buffer hysteresis to 200 mV or disable DC buffer hysteresis
0	PRIREF_BUF_MODE	R/W	0x1	PRIREF buffer mode 0x0 = Set AC buffer hysteresis to 50 mV or enable DC buffer hysteresis 0x1 = Set AC buffer hysteresis to 200 mV or disable DC buffer hysteresis

1.34 R46 Register (Address = 0x2E) [Reset = 0x0]

R46 is shown in Table 1-36.

Return to the Summary Table.

Table 1-36. R46 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	SECREF_TYPE	R/W	0x0	SECREF Input Type See PRIREF_TYPE for input type bit settings.
3:0	PRIREF_TYPE	R/W	0x0	PRIREF Input Type 0x0 = DC-Differential (external termination) 0x1 = AC-Differential (external termination) 0x3 = AC-Differential (internal termination 100-Ω) 0x4 = HCSL (internal termination 50-Ω) 0x8 = CMOS 0xC = Single-ended (internal termination 50-Ω)

1.35 R47 Register (Address = 0x2F) [Reset = 0x0]

R47 is shown in Table 1-37.

Return to the Summary Table.

Table 1-37. R47 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL2_RCLK_SEL	R/W	0x0	PLL2 Reference clock selection 0x0 = VCO1 - Cascaded Mode 0x1 = XO

Table 1-37. R47 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2:0	PLL1_VCO_TO_CNTRS_EN	R/W	0x0	PLL1 VCO to counters enable. Enables VCO1 output drivers to PLL1 N counter, DPLL, digital top, PLL2 R divider. Bit 0 enables VCO1 output for DPLL TDC, reference window detect, DPLL loop filter high speed clock and ppm checker clock. Bit 1 enables VCO1 output to PLL1 N counter Bit 2 enables the PLL1_P1 output to PLL2 R divider for loop-back mode.

1.36 R48 Register (Address = 0x30) [Reset = 0xA]

R48 is shown in Table 1-38.

Return to the Summary Table.

Table 1-38. R48 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved

Table 1-38. R48 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6:0	STAT0_SEL	R/W	0xA	STATUS0 Indicator Signal Select The output pin state of 1 indicates the status condition is true. 0x00 = XO Input Loss of Signal (LOS) 0x01 = Low 0x02 = Reserved 0x03 = PLL1 Digital Lock Detect (DLD) 0x04 = PLL1 VCO Calibration Active 0x05 = PLL1 N Divider, div-by-2 0x06 = PLL2 Digital Lock Detect (DLD) 0x07 = PLL2 VCO Calibration Active 0x08 = PLL2 N Divider, div-by-2 0x09 = EEPROM Active 0x0A = Interrupt (INTR) 0x0B = Reserved 0x0C = DPLL Phase Lock Detected (LOPL#) 0x0D = PRIREF Monitor Divider Output, div-by-2 0x0E = SECREF Monitor Divider Output, div-by-2 0x0F = PLL2 R Divider, div-by-2 0x10 = Reserved 0x11 = PRIREF Amplitude Monitor Fault 0x12 = SECREF Amplitude Monitor Fault 0x13 = Reserved 0x14 = Reserved 0x15 = PRIREF Frequency Monitor Fault 0x16 = SECREF Frequency Monitor Fault 0x17 = Reserved 0x18 = Reserved 0x19 = PRIREF Missing or Early Pulse Monitor Fault 0x1A = SECREF Missing or Early Pulse Monitor Fault 0x1B = Reserved 0x1C = Reserved 0x1D = PRIREF Validation Timer Active 0x1E = SECREF Validation Timer Active 0x1F = Reserved 0x20 = Reserved 0x21 = Reserved 0x22 = Reserved 0x23 = Reserved 0x24 = Reserved 0x25 = PRIREF Phase Validation Monitor Fault 0x26 = SECREF Phase Validation Monitor Fault 0x27 = Reserved 0x28 = Reserved 0x29 = PLL1 Lock Detected (LOL#) 0x2A = PLL2 Lock Detected (LOL#) 0x2B = Reserved 0x2C = Reserved 0x2D = Reserved 0x2E = Reserved 0x2F = Reserved 0x30 = Reserved 0x31 = Reserved 0x32 = Reserved 0x33 = Reserved 0x34 = Reserved 0x35 = Reserved 0x36 = Reserved 0x37 = Reserved 0x38 = Reserved 0x39 = Reserved 0x3A = Reserved 0x3B = Reserved 0x3C = Reserved 0x3D = Reserved 0x3E = Reserved 0x3F = Reserved 0x40 = DPLL R Divider, div-by-2 0x41 = DPLL FB Divider, div-by-2

Table 1-38. R48 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x42 = Reserved 0x43 = Reserved 0x44 = Reserved 0x45 = Reserved 0x46 = DPLL PRIREF Selected 0x47 = DPLL SECREF Selected 0x48 = Reserved 0x49 = Reserved 0x4A = DPLL Holdover Active 0x4B = DPLL Reference Switchover Event 0x4C = Reserved 0x4D = DPLL Tuning History Update 0x4E = DPLL Fast Lock Active 0x4F = Reserved 0x50 = DPLL Loss of Lock (LOFL)

1.37 R49 Register (Address = 0x31) [Reset = 0xA]

R49 is shown in Table 1-39.

Return to the Summary Table.

Table 1-39. R49 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	STAT1_SEL	R/W	0xA	STATUS1 Indicator Signal Select See STAT0_SEL for status signal and bit settings.

1.38 R50 Register (Address = 0x32) [Reset = 0x0]

R50 is shown in Table 1-40.

Return to the Summary Table.

Table 1-40. R50 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_FDEV_EN	R/W	0x0	Enable DCO Frequency When enabled, a rising edge on these pins will update the DCO frequency accordingly.
6	RESERVED	R	0x0	Reserved
5	CH7_PD	R/W	0x0	Channel 7 Powerdown When CH7_PD is 1 the regulator that supplies the divider and drivers for OUT7 will be disabled.
4	CH6_PD	R/W	0x0	Channel 6 Powerdown When CH6_PD is 1 the regulator that supplies the divider and drivers for OUT6 will be disabled.
3	CH5_PD	R/W	0x0	Channel 5 Powerdown When CH5_PD is 1 the regulator that supplies the divider and drivers for OUT5 will be disabled.
2	CH4_PD	R/W	0x0	Channel 4 Powerdown When CH4_PD is 1 the regulator that supplies the divider and drivers for OUT4 will be disabled.
1	CH2_3_PD	R/W	0x0	Channel 2 and 3 Powerdown When CH2_3_PD is 1 the regulator that supplies the divider and drivers for OUT2 and OUT3 will be disabled.
0	CH0_1_PD	R/W	0x0	Channel 0 and 1 Powerdown When CH0_1_PD is 1 the regulator that supplies the divider and drivers for OUT0 and OUT1 will be disabled.

1.39 R51 Register (Address = 0x33) [Reset = 0x18]

R51 is shown in Table 1-41.

Return to the Summary Table.

Table 1-41. R51 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CH0_1_MUX	R/W	0x0	Channel 0 and 1 Output Mux Selects frequency source for OUT0 and OUT1. 0x0 = APLL1 P1 0x1 = APLL1 P1 Inverted 0x2 = APLL2 P1 0x3 = APLL2 P2
5:0	OUT0_FMT	R/W	0x18	OUT0 Clock Format Values not desplayed below are reserved. 0x00 = Disabled 0x10 = AC-LVDS 0x14 = AC-CML 0x18 = AC-LVPECL 0x2C = HCSL (external termination 50-Ω) 0x2D = HCSL (internal termination 50-Ω)

1.40 R52 Register (Address = 0x34) [Reset = 0x18]

R52 is shown in Table 1-42.

Return to the Summary Table.

Table 1-42. R52 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	OUT1_FMT	R/W	0x18	OUT1 Clock Format See OUT0_FMT for bit settings.

1.41 R53 Register (Address = 0x35) [Reset = 0x7]

R53 is shown in Table 1-43.

Return to the Summary Table.

Table 1-43. R53 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT0_1_DIV	R/W	0x7	Channel 0 and Channel 1 Output Divider This is an 8-bit divider. The valid values for OUT0_1_DIV range from 1 to 255. Output Divider (ODOUT01) = OUT0_1_DIV + 1 Note: 0x00 is disabled.

1.42 R54 Register (Address = 0x36) [Reset = 0x18]

R54 is shown in Table 1-44.

Return to the Summary Table.

Table 1-44. R54 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CH2_3_MUX	R/W	0x0	Channel 2 and 3 Output Mux Selects frequency source for OUT2 and OUT3. See CH0_1_MUX for bit settings.

Table 1-44. R54 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	OUT2_FMT	R/W	0x18	OUT2 Clock Format See OUT0_FMT for bit settings.

1.43 R55 Register (Address = 0x37) [Reset = 0x18]

R55 is shown in Table 1-45.

Return to the Summary Table.

Table 1-45. R55 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	OUT3_FMT	R/W	0x18	OUT3 Clock Format See OUT0_FMT for bit settings.

1.44 R56 Register (Address = 0x38) [Reset = 0x7]

R56 is shown in Table 1-46.

Return to the Summary Table.

Table 1-46. R56 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT2_3_DIV	R/W	0x7	Channel 2 and Channel 3 Output Divider See OUT0_1_DIV for description and bit settings.

1.45 R57 Register (Address = 0x39) [Reset = 0x18]

R57 is shown in Table 1-47.

Return to the Summary Table.

Table 1-47. R57 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CH4_MUX	R/W	0x0	Channel 4 Output Mux Selects frequency source for OUT4. See CH0_1_MUX for bit settings.
5:0	OUT4_FMT	R/W	0x18	OUT4 Clock Format Values not desplayed below are reserved. 0x00 = Disabled 0x10 = AC-LVDS 0x14 = AC-CML 0x18 = AC-LVPECL 0x2C = HCSL (external termination 50-Ω) 0x2D = HCSL (internal termination 50-Ω) 0x30 = LVCMOS(HiZ/HiZ) 0x32 = LVCMOS(HiZ/-) 0x33 = LVCMOS(HiZ/+) 0x35 = LVCMOS(low/low) 0x38 = LVCMOS(-/HiZ) 0x3A = LVCMOS(-/-) 0x3B = LVCMOS(-/+) 0x3C = LVCMOS(+/HiZ) 0x3E = LVCMOS(+/-) 0x3F = LVCMOS(+/+)

1.46 R58 Register (Address = 0x3A) [Reset = 0x7]

R58 is shown in Table 1-48.

Return to the Summary Table.

Table 1-48. R58 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT4_DIV	R/W	0x7	Channel 4 Output Divider See OUT0_1_DIV for description and bit settings.

1.47 R59 Register (Address = 0x3B) [Reset = 0x18]

R59 is shown in Table 1-49.

Return to the Summary Table.

Table 1-49. R59 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CH5_MUX	R/W	0x0	Channel 5 Output Mux Selects frequency source for OUT5. See CH0_1_MUX for bit settings.
5:0	OUT5_FMT	R/W	0x18	OUT5 Clock Format See OUT4_FMT for bit settings.

1.48 R60 Register (Address = 0x3C) [Reset = 0x7]

R60 is shown in Table 1-50.

Return to the Summary Table.

Table 1-50. R60 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT5_DIV	R/W	0x7	Channel 5 Output Divider See OUT0_1_DIV for description and bit settings.

1.49 R61 Register (Address = 0x3D) [Reset = 0x18]

R61 is shown in Table 1-51.

Return to the Summary Table.

Table 1-51. R61 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CH6_MUX	R/W	0x0	Channel 6 Output Mux Selects frequency source for OUT6. See CH0_1_MUX for bit settings.
5:0	OUT6_FMT	R/W	0x18	OUT6 Clock Format See OUT4_FMT for bit settings.

1.50 R62 Register (Address = 0x3E) [Reset = 0x7]

R62 is shown in Table 1-52.

Return to the Summary Table.

Table 1-52. R62 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT6_DIV	R/W	0x7	Channel 6 Output Divider See OUT0_1_DIV for description and bit settings.

1.51 R63 Register (Address = 0x3F) [Reset = 0x18]

R63 is shown in Table 1-53.

Return to the Summary Table.

Table 1-53. R63 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	CH7_MUX	R/W	0x0	Channel 7 Output Mux Selects frequency source for OUT7. See CH0_1_MUX for bit settings.
5:0	OUT7_FMT	R/W	0x18	OUT7 Clock Format See OUT4_FMT for bit settings.

1.52 R64 Register (Address = 0x40) [Reset = 0x0]

R64 is shown in Table 1-54.

Return to the Summary Table.

Table 1-54. R64 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT7_STG2_DIV_23:16	R/W	0x0	Bits 23:16 of OUT7_STG2_DIV

1.53 R65 Register (Address = 0x41) [Reset = 0x0]

R65 is shown in Table 1-55.

Return to the Summary Table.

Table 1-55. R65 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT7_STG2_DIV_15:8	R/W	0x0	Bits 15:8 of OUT7_STG2_DIV

1.54 R66 Register (Address = 0x42) [Reset = 0x0]

R66 is shown in Table 1-56.

Return to the Summary Table.

Table 1-56. R66 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT7_STG2_DIV	R/W	0x0	Channel 7 Stage Two Output Divider OD2 = OUT7_STG2_DIV + 1 If OD2 > 1, then ODout7 must be ≥ 6. Total output 7 divide value = OD2 * ODout7.

1.55 R67 Register (Address = 0x43) [Reset = 0x7]

R67 is shown in Table 1-57.

Return to the Summary Table.

Table 1-57. R67 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OUT7_DIV	R/W	0x7	Channel 7 Output Divider This is an 8-bit divider. The valid values for OUT7_DIV range from 1 to 255. ODOUT7 = OUT7_DIV + 1. If OD2 > 1, then total output 7 divide value = OD2 * ODout7 where OD2 is OUT7 secondary output divider value. Note: 0x00 is disabled.

1.56 R68 Register (Address = 0x44) [Reset = 0xFF]

R68 is shown in Table 1-58.

Return to the Summary Table.

Table 1-58. R68 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0xF	Reserved
3:0	PLL1_CP_BAW	R/W	0xF	APLL1 Charge Pump Current Gain PLL1_CP_BAW ranges from 0 to 15. Gain = PLL1_CP_BAW x 100 µA.

1.57 R70 Register (Address = 0x46) [Reset = 0x0]

R70 is shown in Table 1-59.

Return to the Summary Table.

Table 1-59. R70 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2	PLL2_P2_SYNC_EN	R/W	0x0	Enable PLL2 P2 divider channel synchronizatrion
1	PLL2_P1_SYNC_EN	R/W	0x0	Enable PLL2 P1 divider channel synchronizatrion
0	PLL1_P1_SYNC_EN	R/W	0x0	Enable PLL1 P1 divider channel synchronizatrion

1.58 R71 Register (Address = 0x47) [Reset = 0x0]

R71 is shown in Table 1-60.

Return to the Summary Table.

Table 1-60. R71 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	CH7_SYNC_EN	R/W	0x0	Enable Channel 7 output synchronization
4	CH6_SYNC_EN	R/W	0x0	Enable Channel 6 output synchronization
3	CH5_SYNC_EN	R/W	0x0	Enable Channel 5 output synchronization
2	CH4_SYNC_EN	R/W	0x0	Enable Channel 4 output synchronization
1	CH2_3_SYNC_EN	R/W	0x0	Enable Channels 2 and 3 output synchronization
0	CH0_1_SYNC_EN	R/W	0x0	Enable Channels 0 and 1 output synchronization

1.59 R74 Register (Address = 0x4A) [Reset = 0x0]

R74 is shown in Table 1-61.

Return to the Summary Table.

Table 1-61. R74 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL1_PDN	R/W	0x0	PLL1 Power down The PLL1_PDN bit determines whether PLL1 is automatically enabled and calibrated after a hardware reset. 0x0 = PLL1 Enabled 0x1 = PLL1 Disabled

1.60 R79 Register (Address = 0x4F) [Reset = 0x11]

R79 is shown in Table 1-62.

Return to the Summary Table.

Table 1-62. R79 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	BAW_LOCKDET_EN	R/W	0x1	BAW Lock Detect Enable
3:0	RESERVED	R/W	0x1	Reserved

1.61 R80 Register (Address = 0x50) [Reset = 0x0]

R80 is shown in Table 1-63.

Return to the Summary Table.

Table 1-63. R80 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BAW_LOCK	R/W	0x0	BAW Lock Detect Status 0x0 = Unlocked 0x1 = Locked
6:0	BAW_LOCK_DET_1	R/W	0x0	BAW VCO Lock Detection

1.62 R81 Register (Address = 0x51) [Reset = 0x0]

R81 is shown in Table 1-64.

Return to the Summary Table.

Table 1-64. R81 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_LOCK_DET_2	R/W	0x0	BAW VCO Lock Detection

1.63 R82 Register (Address = 0x52) [Reset = 0x0]

R82 is shown in Table 1-65.

Return to the Summary Table.

Table 1-65. R82 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	BAW_LOCK_DET_3	R/W	0x0	BAW VCO Lock Detection

1.64 R83 Register (Address = 0x53) [Reset = 0x0]

R83 is shown in Table 1-66.

Return to the Summary Table.

Table 1-66. R83 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_LOCK_DET_4	R/W	0x0	BAW VCO Lock Detection

1.65 R84 Register (Address = 0x54) [Reset = 0x0]

R84 is shown in Table 1-67.

Return to the Summary Table.

Table 1-67. R84 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_LOCK_DET_5	R/W	0x0	BAW VCO Lock Detection

1.66 R85 Register (Address = 0x55) [Reset = 0x0]

R85 is shown in Table 1-68.

Return to the Summary Table.

Table 1-68. R85 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_LOCK_DET_6	R/W	0x0	BAW VCO Lock Detection

1.67 R86 Register (Address = 0x56) [Reset = 0x0]

R86 is shown in Table 1-69.

Return to the Summary Table.

Table 1-69. R86 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	BAW_LOCK_DET_7	R/W	0x0	BAW VCO Lock Detection

1.68 R87 Register (Address = 0x57) [Reset = 0x0]

R87 is shown in Table 1-70.

Return to the Summary Table.

Table 1-70. R87 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_LOCK_DET_8	R/W	0x0	BAW VCO Lock Detection

1.69 R88 Register (Address = 0x58) [Reset = 0x0]

R88 is shown in Table 1-71.

Return to the Summary Table.

Table 1-71. R88 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_LOCK_DET_9	R/W	0x0	BAW VCO Lock Detection

1.70 R89 Register (Address = 0x59) [Reset = 0x0]

R89 is shown in Table 1-72.

Return to the Summary Table.

Table 1-72. R89 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_LOCK_DET_10	R/W	0x0	BAW VCO Lock Detection

1.71 R90 Register (Address = 0x5A) [Reset = 0x0]

R90 is shown in Table 1-73.

Return to the Summary Table.

Table 1-73. R90 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	BAW_UNLK_DET_1	R/W	0x0	BAW VCO Unlock Detection

1.72 R91 Register (Address = 0x5B) [Reset = 0x0]

R91 is shown in Table 1-74.

Return to the Summary Table.

Table 1-74. R91 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_UNLK_DET_2	R/W	0x0	BAW VCO Unlock Detection

1.73 R92 Register (Address = 0x5C) [Reset = 0x0]

R92 is shown in Table 1-75.

Return to the Summary Table.

Table 1-75. R92 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	BAW_UNLK_DET_3	R/W	0x0	BAW VCO Unlock Detection

1.74 R93 Register (Address = 0x5D) [Reset = 0x0]

R93 is shown in Table 1-76.

Return to the Summary Table.

Table 1-76. R93 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_UNLK_DET_4	R/W	0x0	BAW VCO Unlock Detection

1.75 R94 Register (Address = 0x5E) [Reset = 0x0]

R94 is shown in Table 1-77.

Return to the Summary Table.

Table 1-77. R94 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_UNLK_DET_5	R/W	0x0	BAW VCO Unlock Detection

1.76 R95 Register (Address = 0x5F) [Reset = 0x0]

R95 is shown in Table 1-78.

Return to the Summary Table.

Table 1-78. R95 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_UNLK_DET_6	R/W	0x0	BAW VCO Unlock Detection

1.77 R96 Register (Address = 0x60) [Reset = 0x0]

R96 is shown in Table 1-79.

Return to the Summary Table.

Table 1-79. R96 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	BAW_UNLK_DET_7	R/W	0x0	BAW VCO Unlock Detection

1.78 R97 Register (Address = 0x61) [Reset = 0x0]

R97 is shown in Table 1-80.

Return to the Summary Table.

Table 1-80. R97 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_UNLK_DET_8	R/W	0x0	BAW VCO Unlock Detection

1.79 R98 Register (Address = 0x62) [Reset = 0x0]

R98 is shown in Table 1-81.

Return to the Summary Table.

Table 1-81. R98 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_UNLK_DET_9	R/W	0x0	BAW VCO Unlock Detection

1.80 R99 Register (Address = 0x63) [Reset = 0x0]

R99 is shown in Table 1-82.

Return to the Summary Table.

Table 1-82. R99 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	BAW_UNLK_DET_10	R/W	0x0	BAW VCO Unlock Detection

1.81 R100 Register (Address = 0x64) [Reset = 0x1]

R100 is shown in Table 1-83.

Return to the Summary Table.

Table 1-83. R100 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	PLL2_RDIV_SEC	R/W	0x0	APLL2 secondary reference divider in cascaded APLL2 mode Divider value ranges from 1-32. Divider value = PLL2_RDIV_SEC + 1.
2:1	PLL2_RDIV_PRE	R/W	0x0	APLL2 primary reference divider in cascaded APLL2 mode
0	PLL2_PDN	R/W	0x1	PLL2 Power down The PLL2_PDN bit determines whether PLL2 is automatically enabled and calibrated after a hardware reset. 0x0 = PLL2 Enabled 0x1 = PLL2 Disabled

1.82 R101 Register (Address = 0x65) [Reset = 0x2]

R101 is shown in Table 1-84.

Return to the Summary Table.

Table 1-84. R101 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1:0	PLL2_CP	R/W	0x2	PLL2 Charge Pump Gain 0x0 = 1.6 mA 0x1 = 3.2 mA 0x2 = 4.8 mA 0x3 = 6.4 mA

1.83 R102 Register (Address = 0x66) [Reset = 0x22]

R102 is shown in Table 1-85.

Return to the Summary Table.

Table 1-85. R102 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:4	PLL2_P2	R/W	0x2	PLL2 Post-Divider2 Note: A RESET is required after changing Divider values. See PLL2_P1 for bit settings.
3	RESERVED	R	0x0	Reserved

Table 1-85. R102 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	PLL2_P1	R/W	0x2	PLL2 Post-Divider1 Note: A RESET is required after changing Divider values. 0x0 = Invalid 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7 0x7 = Invalid

1.84 R104 Register (Address = 0x68) [Reset = 0x0]

R104 is shown in Table 1-86.

Return to the Summary Table.

Table 1-86. R104 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	PLL2_RBLEED_CP	R/W	0x0	PLL2 Bleed resistor selection (Ω) 0x0 = Open (high impedance) 0x1 = 23713.2 0x2 = 11875.2 0x3 = 7915.62 0x4 = 5843.79 0x5 = 4753.58 0x6 = 3963.08 0x7 = 3393.52 0x8 = 2970.14 0x9 = 2638.54 0xA = 2375.04 0xB = 2158.91 0xC = 1980.99 0xD = 1827.03 0xE = 1696.76 0xF = 1584.26 0x10 = 1486.55 0x11 = 1397.73 0x12 = 1320.66 0x13 = 1249.6 0x14 = 1187.43 0x15 = 1131.17 0x16 = 1077.88 0x17 = 1033.47 0x18 = 991.03 0x19 = 950.53 0x1A = 913.52 0x1B = 879.47 0x1C = 848.38 0x1D = 818.77 0x1E = 792.13 0x1F = 766.96

1.85 R105 Register (Address = 0x69) [Reset = 0x0]

R105 is shown in Table 1-87.

Return to the Summary Table.

Table 1-87. R105 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-87. R105 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3:2	PLL2_CLSDWAIT	R/W	0x0	Closed Loop Wait Period VCO calibration time per step (up to 7 steps). 0x0 = 0.3 ms 0x1 = 3 ms 0x2 = 30 ms 0x3 = 300 ms
1:0	RESERVED	R/W	0x0	Reserved

1.86 R108 Register (Address = 0x6C) [Reset = 0x0]

R108 is shown in Table 1-88.

Return to the Summary Table.

Table 1-88. R108 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PLL1_NDIV_11:8	R/W	0x0	Bits 11:8 of PLL1_NDIV

1.87 R109 Register (Address = 0x6D) [Reset = 0x64]

R109 is shown in Table 1-89.

Return to the Summary Table.

Table 1-89. R109 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NDIV	R/W	0x64	PLL1 N Divider

1.88 R110 Register (Address = 0x6E) [Reset = 0x0]

R110 is shown in Table 1-90.

Return to the Summary Table.

Table 1-90. R110 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_39:32	R/W	0x0	Bits 39:32 of PLL1_NUM, or bits 15:8 of PLL1_24B_NUM

1.89 R111 Register (Address = 0x6F) [Reset = 0x0]

R111 is shown in Table 1-91.

Return to the Summary Table.

Table 1-91. R111 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_31:24	R/W	0x0	Bits 31:24 of PLL1_NUM, or bits 7:0 of PLL1_24B_NUM

1.90 R112 Register (Address = 0x70) [Reset = 0x0]

R112 is shown in Table 1-92.

Return to the Summary Table.

Table 1-92. R112 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_23:16	R/W	0x0	Bits 23:16 of PLL1_NUM, or bits 23:16 of PLL1_24B_DEN

1.91 R113 Register (Address = 0x71) [Reset = 0x0]

R113 is shown in Table 1-93.

Return to the Summary Table.

Table 1-93. R113 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_15:8	R/W	0x0	Bits 15:8 of PLL1_NUM, or bits 15:8 of PLL1_24B_DEN

1.92 R114 Register (Address = 0x72) [Reset = 0x0]

R114 is shown in Table 1-94.

Return to the Summary Table.

Table 1-94. R114 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM	R/W	0x0	Bits 7:0 of PLL1_NUM, or bits 7:0 of PLL1_24B_DEN

1.93 R115 Register (Address = 0x73) [Reset = 0x0]

R115 is shown in Table 1-95.

Return to the Summary Table.

Table 1-95. R115 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	Reserved
4:3	PLL1_DTHRMODE	R/W	0x0	APLL1 SDM Dither Mode 0x0 = Weak 0x1 = Medium 0x2 = Strong 0x3 = Disabled
2:0	PLL1_ORDER	R/W	0x0	APLL1 SDM Order 0x0 = Integer Mode 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th

1.94 R116 Register (Address = 0x74) [Reset = 0x1]

R116 is shown in Table 1-96.

Return to the Summary Table.

Table 1-96. R116 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:1	RESERVED	R/W	0x0	Reserved

Table 1-96. R116 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PLL1_MODE	R/W	0x1	PLL1 operational mode 0x0 = Free-run mode (APLL only) 0x1 = DPLL mode

1.95 R123 Register (Address = 0x7B) [Reset = 0x0]

R123 is shown in Table 1-97.

Return to the Summary Table.

Table 1-97. R123 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_STAT_39:32	R	0x0	Bits 39:32 of PLL1_NUM_STAT

1.96 R124 Register (Address = 0x7C) [Reset = 0x0]

R124 is shown in Table 1-98.

Return to the Summary Table.

Table 1-98. R124 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_STAT_31:24	R	0x0	Bits 31:24 of PLL1_NUM_STAT

1.97 R125 Register (Address = 0x7D) [Reset = 0x0]

R125 is shown in Table 1-99.

Return to the Summary Table.

Table 1-99. R125 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_STAT_23:16	R	0x0	Bits 23:16 of PLL1_NUM_STAT

1.98 R126 Register (Address = 0x7E) [Reset = 0x0]

R126 is shown in Table 1-100.

Return to the Summary Table.

Table 1-100. R126 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_STAT_15:8	R	0x0	Bits 15:8 of PLL1_NUM_STAT

1.99 R127 Register (Address = 0x7F) [Reset = 0x0]

R127 is shown in Table 1-101.

Return to the Summary Table.

Table 1-101. R127 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_NUM_STAT	R	0x0	APLL1 Numerator Status Byte

1.100 R129 Register (Address = 0x81) [Reset = 0x18]

R129 is shown in Table 1-102.

Return to the Summary Table.

Table 1-102. R129 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-102. R129 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL1_LF_R2	R/W	0x18	PLL1 Loop Filter R2 (Ω) 0x00 = 0 0x01 = 414 0x02 = 880 0x03 = 1294 0x04 = 1625 0x05 = 2039 0x06 = 2505 0x07 = 2919 0x08 = 3250 0x09 = 3664 0x0A = 4130 0x0B = 4544 0x0C = 4875 0x0D = 5289 0x0E = 5755 0x0F = 6169 0x10 = 6400 0x11 = 6814 0x12 = 7280 0x13 = 7694 0x14 = 8025 0x15 = 8439 0x16 = 8905 0x17 = 9319 0x18 = 9650 0x19 = 10064 0x1A = 10530 0x1B = 10944 0x1C = 11275 0x1D = 11689 0x1E = 12155 0x1F = 12569 0x20 = 12800 0x21 = 13214 0x22 = 13680 0x23 = 14094 0x24 = 14425 0x25 = 14839 0x26 = 15305 0x27 = 15719 0x28 = 16050 0x29 = 16464 0x2A = 16930 0x2B = 17344 0x2C = 17675 0x2D = 18089 0x2E = 18555 0x2F = 18969 0x30 = 19200 0x31 = 19614 0x32 = 20080 0x33 = 20494 0x34 = 20825 0x35 = 21239 0x36 = 21705 0x37 = 22119 0x38 = 22450 0x39 = 22864 0x3A = 23330 0x3B = 23744 0x3C = 24075 0x3D = 24489 0x3E = 24955 0x3F = 25369

1.101 R131 Register (Address = 0x83) [Reset = 0x18]

R131 is shown in Table 1-103.

Return to the Summary Table.

Table 1-103. R131 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-103. R131 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL1_LF_R3	R/W	0x18	PLL1 Loop Filter R3 (Ω) 0x0 = 0 0x1 = 200 0x2 = 580 0x3 = 148.7 0x4 = 700 0x5 = 155.6 0x6 = 317.2 0x7 = 122.7 0x8 = 800 0x9 = 1000 0xA = 1380 0xB = 948.7 0xC = 1500 0xD = 955.6 0xE = 1117.2 0xF = 922.7 0x10 = 1600 0x11 = 1800 0x12 = 2180 0x13 = 1748.7 0x14 = 2300 0x15 = 1755.6 0x16 = 1917.2 0x17 = 1722.7 0x18 = 2400 0x19 = 2600 0x1A = 2980 0x1B = 2548.7 0x1C = 3100 0x1D = 2555.6 0x1E = 2717.2 0x1F = 2522.7 0x20 = 3200 0x21 = 3400 0x22 = 3780 0x23 = 3348.7 0x24 = 3900 0x25 = 3355.6 0x26 = 3517.2 0x27 = 3322.7 0x28 = 4000 0x29 = 4200 0x2A = 4580 0x2B = 4148.7 0x2C = 4700 0x2D = 4155.6 0x2E = 4317.2 0x2F = 4122.7 0x30 = 4800 0x31 = 5000 0x32 = 5380 0x33 = 4948.7 0x34 = 5500 0x35 = 4955.6 0x36 = 5117.2 0x37 = 4922.7 0x38 = 5600 0x39 = 5800 0x3A = 6180 0x3B = 5748.7 0x3C = 6300 0x3D = 5755.6 0x3E = 5917.2 0x3F = 5722.7

1.102 R132 Register (Address = 0x84) [Reset = 0x18]

R132 is shown in Table 1-104.

Return to the Summary Table.

Table 1-104. R132 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	PLL1_LF_R4	R/W	0x18	PLL1 Loop Filter R4 See PLL1_LF_R3 for bit settings.

1.103 R134 Register (Address = 0x86) [Reset = 0x0]

R134 is shown in Table 1-105.

Return to the Summary Table.

Table 1-105. R134 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	PLL2_NDIV_8:8	R/W	0x0	Bit 8 of PLL2_NDIV

1.104 R135 Register (Address = 0x87) [Reset = 0x64]

R135 is shown in Table 1-106.

Return to the Summary Table.

Table 1-106. R135 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NDIV	R/W	0x64	Bits 7:0 of PLL2 N Divider

1.105 R136 Register (Address = 0x88) [Reset = 0x0]

R136 is shown in Table 1-107.

Return to the Summary Table.

Table 1-107. R136 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_23:16	R/W	0x0	Bits 23:16 of PLL2_NUM

1.106 R137 Register (Address = 0x89) [Reset = 0x0]

R137 is shown in Table 1-108.

Return to the Summary Table.

Table 1-108. R137 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM_15:8	R/W	0x0	Bits 15:8 of PLL2_NUM

1.107 R138 Register (Address = 0x8A) [Reset = 0x0]

R138 is shown in Table 1-109.

Return to the Summary Table.

Table 1-109. R138 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_NUM	R/W	0x0	PLL2 Fractional Divider Numerator

1.108 R139 Register (Address = 0x8B) [Reset = 0x0]

R139 is shown in Table 1-110.

Return to the Summary Table.

Table 1-110. R139 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	Reserved
4:3	PLL2_DTHRMODE	R/W	0x0	SDM Dither Mode 0x0 = Weak 0x1 = Medium 0x2 = Strong 0x3 = Disabled
2:0	PLL2_ORDER	R/W	0x0	APLL2 SDM Order 0x0 = Integer Mode 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th

1.109 R140 Register (Address = 0x8C) [Reset = 0x18]

R140 is shown in Table 1-111.

Return to the Summary Table.

Table 1-111. R140 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-111. R140 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5:0	PLL2_LF_R2	R/W	0x18	PLL2 Loop Filter R2 (Ohm) 0x00 = 0 0x01 = 200 0x02 = 300 0x03 = 120 0x04 = 580 0x05 = 148.7 0x06 = 197.7 0x07 = 99.4 0x08 = 1067 0x09 = 168.4 0x0A = 234.2 0x0B = 107.9 0x0C = 375.7 0x0D = 130.5 0x0E = 166.8 0x0F = 91 0x10 = 800 0x11 = 1000 0x12 = 1100 0x13 = 920 0x14 = 1380 0x15 = 948.7 0x16 = 997.7 0x17 = 899.4 0x18 = 1867 0x19 = 968.4 0x1A = 1034.2 0x1B = 907.9 0x1C = 1175.7 0x1D = 930.5 0x1E = 966.8 0x1F = 891 0x20 = 1600 0x21 = 1800 0x22 = 1900 0x23 = 1720 0x24 = 2180 0x25 = 1748.7 0x26 = 1797.7 0x27 = 1699.4 0x28 = 2667 0x29 = 1768.4 0x2A = 1834.2 0x2B = 1707.9 0x2C = 1975.7 0x2D = 1730.5 0x2E = 1766.8 0x2F = 1691 0x30 = 2400 0x31 = 2600 0x32 = 2700 0x33 = 2520 0x34 = 2980 0x35 = 2548.7 0x36 = 2597.7 0x37 = 2499.4 0x38 = 3467 0x39 = 2568.4 0x3A = 2634.2 0x3B = 2507.9 0x3C = 2775.7 0x3D = 2530.5 0x3E = 2566.8 0x3F = 2491

1.110 R142 Register (Address = 0x8E) [Reset = 0x18]

R142 is shown in Table 1-112.

Return to the Summary Table.

Table 1-112. R142 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	PLL2_LF_R3	R/W	0x18	PLL2 Loop Filter R3 See PLL1_LF_R3 for bit settings.

1.111 R143 Register (Address = 0x8F) [Reset = 0x18]

R143 is shown in Table 1-113.

Return to the Summary Table.

Table 1-113. R143 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	PLL2_LF_R4	R/W	0x18	PLL2 Loop Filter R4 See PLL1_LF_R3 for bit settings.

1.112 R144 Register (Address = 0x90) [Reset = 0x0]

R144 is shown in Table 1-114.

Return to the Summary Table.

Table 1-114. R144 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:4	PLL2_LF_C4	R/W	0x0	PLL2 Loop Filter C4 See PLL2_LF_C3 for bit settings.
3	RESERVED	R	0x0	Reserved
2:0	PLL2_LF_C3	R/W	0x0	PLL2 Loop Filter C3 0x0 = 0 pF 0x1 = 40 pF 0x2 = 20 pF 0x3 = 60 pF 0x4 = 10 pF 0x5 = 50 pF 0x6 = 30 pF 0x7 = 70 pF

1.113 R145 Register (Address = 0x91) [Reset = 0x5]

R145 is shown in Table 1-115.

Return to the Summary Table.

Table 1-115. R145 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:3	RESERVED	R/W	0x0	Reserved

Table 1-115. R145 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	XO_TIMER	R/W	0x5	XO Input Wait Timer Sets the startup time for the oscillator input. 0x0 = 1.6 ms 0x1 = 3.3 ms 0x2 = 6.6 ms 0x3 = 13.1 ms 0x4 = 26.2 ms 0x5 = 52.4 ms 0x6 = 104.9 ms 0x7 = Reserved

1.114 R156 Register (Address = 0x9C) [Reset = 0x0]

R156 is shown in Table 1-116.

Return to the Summary Table.

Table 1-116. R156 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMCNT	R	0x0	NVM Program Count The NVMCNT increments automatically after every EEPROM Erase/Program Cycle (after a subsequent power-cycle or hard reset). The NVMCNT value is retrieved automatically after reset or after a NVM Commit operation.

1.115 R157 Register (Address = 0x9D) [Reset = 0x0]

R157 is shown in Table 1-117.

Return to the Summary Table.

Table 1-117. R157 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6	REGCOMMIT	RH/W1S	0x0	REG Commit to NVM SRAM Array The REGCOMMIT bit is used to initiate a transfer from the on-chip registers back to the corresponding location in the NVM SRAM Array. The REGCOMMIT bit is automatically cleared to 0 when the transfer is complete.
5	NVMCRCERR	R	0x0	NVM CRC Error Indication This bit will read 1 when a CRC Error has been detected reading back from on-chip EEPROM during device initialization, where the NVMLCRC value does not match NVMSCRC. This bit can only be cleared by successful EEPROM programming and power-on/reset cycle, such that the NVMLCRC value matches NVMSCRC.
4	RESERVED	R/W	0x0	Reserved
3	NVMCOMMIT	RH/W1S	0x0	NVM Commit to Registers The NVMCOMMIT bit is used to initiate a transfer of the on-chip EEPROM contents to internal registers. The transfer happens automatically after reset or when NVMCOMMIT is set to 1. The NVMCOMMIT bit is automatically cleared to 0. The registers cannot be read while a NVM Commit operation is taking place.
2	NVMBUSY	R	0x0	NVM Program Busy Indication This bit will read 1 when an EEPROM Erase/Program cycle is active, during which the EEPROM cannot be accessed.

Table 1-117. R157 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	NVM_ERASE_PROG	RH/W1S	0x0	NVM Erase/Program Start This bit field is used to initiate an internal EEPROM Erase/ Programsequence. The sequence is only executed if the immediately preceding register transaction was a write to the NVMUNLK register with the appropriate unlock code. The NVM Erase/Program sequence takes about 230 ms total (115 ms for Erase or Program). 0x0 = NVM Idle 0x3 = Start NVM Erase/Program

1.116 R159 Register (Address = 0x9F) [Reset = 0x0]

R159 is shown in Table 1-118.

Return to the Summary Table.

Table 1-118. R159 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	MEMADR_12:8	R/W	0x0	Bits 12:8 of MEMADR

1.117 R160 Register (Address = 0xA0) [Reset = 0x0]

R160 is shown in Table 1-119.

Return to the Summary Table.

Table 1-119. R160 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	MEMADR	R/W	0x0	Memory Address The MEMADR value determines the starting address for access to the on-chip memories. NVMDAT register = NVM EEPROM Data Array (Read only) RAMDAT register = NVM SRAM Data Array (Read/Write) ROMDAT register = ROM Data Array (Read only)

1.118 R161 Register (Address = 0xA1) [Reset = 0x0]

R161 is shown in Table 1-120.

Return to the Summary Table.

Table 1-120. R161 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMDAT	R	0x0	EEPROM Read Data

1.119 R162 Register (Address = 0xA2) [Reset = 0x0]

R162 is shown in Table 1-121.

Return to the Summary Table.

Table 1-121. R162 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RAMDAT	R/W	0x0	RAM Read/Write Data

1.120 R164 Register (Address = 0xA4) [Reset = 0x0]

R164 is shown in Table 1-122.

Return to the Summary Table.

Table 1-122. R164 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	NVMUNLK	R/W	0x0	NVM Program Unlock To perform an EEPROM erase and program operation, this register must be written with a value of 0xEA (unlock code) immediately before setting the NVM_ERASE_PROG bits to 0x3 on the next register write.

1.121 R180 Register (Address = 0xB4) [Reset = 0x0]

R180 is shown in Table 1-123.

Return to the Summary Table.

Table 1-123. R180 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_TUNING_FREE_RUN_37:32	R/W	0x0	Bits 37:32 of DPLL_TUNING_FREE_RUN

1.122 R181 Register (Address = 0xB5) [Reset = 0x0]

R181 is shown in Table 1-124.

Return to the Summary Table.

Table 1-124. R181 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_TUNING_FREE_RUN_31:24	R/W	0x0	Bits 31:24 of DPLL_TUNING_FREE_RUN

1.123 R182 Register (Address = 0xB6) [Reset = 0x0]

R182 is shown in Table 1-125.

Return to the Summary Table.

Table 1-125. R182 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_TUNING_FREE_RUN_23:16	R/W	0x0	Bits 23:16 of DPLL_TUNING_FREE_RUN

1.124 R183 Register (Address = 0xB7) [Reset = 0x0]

R183 is shown in Table 1-126.

Return to the Summary Table.

Table 1-126. R183 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_TUNING_FREE_RUN_15:8	R/W	0x0	Bits 15:8 of DPLL_TUNING_FREE_RUN

1.125 R184 Register (Address = 0xB8) [Reset = 0x0]

R184 is shown in Table 1-127.

Return to the Summary Table.

Table 1-127. R184 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_TUNING_FREE_RUN	R/W	0x0	DPLL Free-run tuning word

1.126 R185 Register (Address = 0xB9) [Reset = 0x0]

R185 is shown in Table 1-128.

Return to the Summary Table.

Table 1-128. R185 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	DPLL_REF_HIST_INTMD	R/W	0x0	Controls intermediate updates to DPLL REF tuning history Updates only occur during first averaging period Tavg after reset. Programming restriction: DPLL_REF_HIST_INTMD ≤ DPLL_REF_HISTCNT. 0x0 = No intermediate update 0x1 = 1 intermediate update at Tavg/2 0x2 = 2 intermediate update at Tavg/4 and Tavg/2 0x3 = 3 intermediate updates at Tavg/8, Tavg/4 and Tavg/2 0xF = 15 intermediate updates at Tavg/32768, Tavg/16384, ... Tavg/4 and Tavg/2.
3	RESERVED	R	0x0	Reserved
2:1	RESERVED	R/W	0x0	Reserved
0	DPLL_REF_HIST_EN	R/W	0x0	Enables DPLL REF tuning history monitor

1.127 R186 Register (Address = 0xBA) [Reset = 0x0]

R186 is shown in Table 1-129.

Return to the Summary Table.

Table 1-129. R186 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL_REF_HISTCNT	R/W	0x0	DPLL REF Tuning History Timer Valid range is 0 to 30.

1.128 R187 Register (Address = 0xBB) [Reset = 0x0]

R187 is shown in Table 1-130.

Return to the Summary Table.

Table 1-130. R187 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	DPLL_REF_HISTDLY_30:24	R/W	0x0	Bits 30:24 of DPLL_REF_HISTDLY

1.129 R188 Register (Address = 0xBC) [Reset = 0x0]

R188 is shown in Table 1-131.

Return to the Summary Table.

Table 1-131. R188 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_HISTDLY_23:16	R/W	0x0	Bits 23:16 of DPLL_REF_HISTDLY

1.130 R189 Register (Address = 0xBD) [Reset = 0x0]

R189 is shown in Table 1-132.

Return to the Summary Table.

Table 1-132. R189 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_HISTDLY_15:8	R/W	0x0	Bits 15:8 of DPLL_REF_HISTDLY

1.131 R190 Register (Address = 0xBE) [Reset = 0x0]

R190 is shown in Table 1-133.

Return to the Summary Table.

Table 1-133. R190 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_HISTDLY	R/W	0x0	DPLL REF Tuning History delay

1.132 R192 Register (Address = 0xC0) [Reset = 0x55]

R192 is shown in Table 1-134.

Return to the Summary Table.

Table 1-134. R192 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	DETECT_MODE_SECREF	R/W	0x1	SECREF Input Energy Detector Mode Control Determines the method for Energy Detection on the SECREF Input. See DETECT_MODE_PRIREF for bit settings.
5:4	DETECT_MODE_PRIREF	R/W	0x1	PRIREF Input Energy Detector Mode Control Determines the method for Energy Detection on the PRIREF Input. 0x0 = Rising Slew Rate Detector 0x1 = Rising and Falling Slew Rate Detector 0x2 = Falling Slew Rate Detector 0x3 = VIH/VIL Level Detector
3:2	SECREF_LVL_SEL	R/W	0x1	SECREF Input Amplitude Detector See PRIREF_LVL_SEL for description and bit settings.
1:0	PRIREF_LVL_SEL	R/W	0x1	PRIREF Input Amplitude Detector Specifies the minimum differential input peak-to-peak swing to be qualified. 0x0 = Vid is 200 mV Differential or 400 mVpp Single-Ended 0x1 = Vid is 250 mV Differential or 500 mVpp Single-Ended 0x2 = Vid is 300 mV Differential or 600 mVpp Single-Ended 0x3 = Vid is 300 mV Differential or 600 mVpp Single-Ended

1.133 R193 Register (Address = 0xC1) [Reset = 0x0]

R193 is shown in Table 1-135.

Return to the Summary Table.

Table 1-135. R193 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	PRIREF_EARLY_DET_EN	R/W	0x0	PRIREF Early Clock Detect Enable
4	PRIREF_PH_VALID_EN	R/W	0x0	PRIREF Phase Valid Detect Enable
3	PRIREF_VALTMR_EN	R/W	0x0	PRIREF Validation Timer Enable
2	PRIREF_PPM_EN	R/W	0x0	PRIREF Frequency ppm Detect Enable
1	PRIREF_MISSCLK_EN	R/W	0x0	PRIREF Missing Clock Detect Enable
0	PRIREF_AMPDET_EN	R/W	0x0	PRIREF Amplitude Detect Enable

1.134 R194 Register (Address = 0xC2) [Reset = 0x0]

R194 is shown in Table 1-136.

Return to the Summary Table.

Table 1-136. R194 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	SECREF_EARLY_DET_EN	R/W	0x0	SECREF Early Clock Detect Enable
4	SECREF_PH_VALID_EN	R/W	0x0	SECREF Phase Valid Detect Enable
3	SECREF_VALTMR_EN	R/W	0x0	SECREF Validation Timer Enable
2	SECREF_PPM_EN	R/W	0x0	SECREF Frequency ppm Detect Enable
1	SECREF_MISSCLK_EN	R/W	0x0	SECREF Missing Clock Detect Enable
0	SECREF_AMPDET_EN	R/W	0x0	SECREF Amplitude Detect Enable

1.135 R195 Register (Address = 0xC3) [Reset = 0x0]

R195 is shown in Table 1-137.

Return to the Summary Table.

Table 1-137. R195 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	PRIREF_MISSCLK_DET_1	R/W	0x0	PRIREF Missing Clock Detection

1.136 R196 Register (Address = 0xC4) [Reset = 0x0]

R196 is shown in Table 1-138.

Return to the Summary Table.

Table 1-138. R196 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_MISSCLK_DET_2	R/W	0x0	PRIREF Missing Clock Detection

1.137 R197 Register (Address = 0xC5) [Reset = 0x0]

R197 is shown in Table 1-139.

Return to the Summary Table.

Table 1-139. R197 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_MISSCLK_DET_3	R/W	0x0	PRIREF Missing Clock Detection

1.138 R198 Register (Address = 0xC6) [Reset = 0x0]

R198 is shown in Table 1-140.

Return to the Summary Table.

Table 1-140. R198 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	SECREF_MISSCLK_DET_1	R/W	0x0	SECREF Missing Clock Detection

1.139 R199 Register (Address = 0xC7) [Reset = 0x0]

R199 is shown in Table 1-141.

Return to the Summary Table.

Table 1-141. R199 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_MISSCLK_DET_2	R/W	0x0	SECREF Missing Clock Detection

1.140 R200 Register (Address = 0xC8) [Reset = 0x0]

R200 is shown in Table 1-142.

Return to the Summary Table.

Table 1-142. R200 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_MISSCLK_DET_3	R/W	0x0	SECREF Missing Clock Detection

1.141 R201 Register (Address = 0xC9) [Reset = 0x0]

R201 is shown in Table 1-143.

Return to the Summary Table.

Table 1-143. R201 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	SECREF_WINDOW_DET	R/W	0x0	SECREF Window Detection
0	PRIREF_WINDOW_DET	R/W	0x0	PRIREF Window Detection

1.142 R202 Register (Address = 0xCA) [Reset = 0x0]

R202 is shown in Table 1-144.

Return to the Summary Table.

Table 1-144. R202 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	PRIREF_EARLYCLK_DET_1	R/W	0x0	PRIREF Early Clock Detection

1.143 R203 Register (Address = 0xCB) [Reset = 0x0]

R203 is shown in Table 1-145.

Return to the Summary Table.

Table 1-145. R203 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_EARLYCLK_DET_2	R/W	0x0	PRIREF Early Clock Detection

1.144 R204 Register (Address = 0xCC) [Reset = 0x0]

R204 is shown in Table 1-146.

Return to the Summary Table.

Table 1-146. R204 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_EARLYCLK_DET_3	R/W	0x0	PRIREF Early Clock Detection

1.145 R205 Register (Address = 0xCD) [Reset = 0x0]

R205 is shown in Table 1-147.

Return to the Summary Table.

Table 1-147. R205 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	SECREF_EARLYCLK_DET_1	R/W	0x0	SECREF Early Clock Detection

1.146 R206 Register (Address = 0xCE) [Reset = 0x0]

R206 is shown in Table 1-148.

Return to the Summary Table.

Table 1-148. R206 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_EARLYCLK_DET_2	R/W	0x0	SECREF Early Clock Detection

1.147 R207 Register (Address = 0xCF) [Reset = 0x0]

R207 is shown in Table 1-149.

Return to the Summary Table.

Table 1-149. R207 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_EARLYCLK_DET_3	R/W	0x0	SECREF Early Clock Detection

1.148 R208 Register (Address = 0xD0) [Reset = 0x0]

R208 is shown in Table 1-150.

Return to the Summary Table.

Table 1-150. R208 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	PRIREF_FREQ_DET_1	R/W	0x0	PRIREF Frequency Detection

1.149 R209 Register (Address = 0xD1) [Reset = 0x0]

R209 is shown in Table 1-151.

Return to the Summary Table.

Table 1-151. R209 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_FREQ_DET_2	R/W	0x0	PRIREF Frequency Detection

1.150 R210 Register (Address = 0xD2) [Reset = 0x0]

R210 is shown in Table 1-152.

Return to the Summary Table.

Table 1-152. R210 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	PRIREF_FREQ_DET_3	R/W	0x0	PRIREF Frequency Detection

1.151 R211 Register (Address = 0xD3) [Reset = 0x0]

R211 is shown in Table 1-153.

Return to the Summary Table.

Table 1-153. R211 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_FREQ_DET_4	R/W	0x0	PRIREF Frequency Detection

1.152 R212 Register (Address = 0xD4) [Reset = 0x0]

R212 is shown in Table 1-154.

Return to the Summary Table.

Table 1-154. R212 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	SECREF_FREQ_DET_1	R/W	0x0	SECREF Frequency Detection

1.153 R213 Register (Address = 0xD5) [Reset = 0x0]

R213 is shown in Table 1-155.

Return to the Summary Table.

Table 1-155. R213 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_FREQ_DET_2	R/W	0x0	SECREF Frequency Detection

1.154 R214 Register (Address = 0xD6) [Reset = 0x0]

R214 is shown in Table 1-156.

Return to the Summary Table.

Table 1-156. R214 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	SECREF_FREQ_DET_3	R/W	0x0	SECREF Frequency Detection

1.155 R215 Register (Address = 0xD7) [Reset = 0x0]

R215 is shown in Table 1-157.

Return to the Summary Table.

Table 1-157. R215 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_FREQ_DET_4	R/W	0x0	SECREF Frequency Detection

1.156 R217 Register (Address = 0xD9) [Reset = 0x0]

R217 is shown in Table 1-158.

Return to the Summary Table.

Table 1-158. R217 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PRIREF_FREQ_DET_5	R/W	0x0	PRIREF Frequency Detection

1.157 R218 Register (Address = 0xDA) [Reset = 0x0]

R218 is shown in Table 1-159.

Return to the Summary Table.

Table 1-159. R218 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_FREQ_DET_6	R/W	0x0	PRIREF Frequency Detection

1.158 R219 Register (Address = 0xDB) [Reset = 0x0]

R219 is shown in Table 1-160.

Return to the Summary Table.

Table 1-160. R219 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_FREQ_DET_7	R/W	0x0	PRIREF Frequency Detection

1.159 R220 Register (Address = 0xDC) [Reset = 0x0]

R220 is shown in Table 1-161.

Return to the Summary Table.

Table 1-161. R220 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_FREQ_DET_8	R/W	0x0	PRIREF Frequency Detection

1.160 R221 Register (Address = 0xDD) [Reset = 0x0]

R221 is shown in Table 1-162.

Return to the Summary Table.

Table 1-162. R221 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	PRIREF_FREQ_DET_9	R/W	0x0	PRIREF Frequency Detection

1.161 R222 Register (Address = 0xDE) [Reset = 0x0]

R222 is shown in Table 1-163.

Return to the Summary Table.

Table 1-163. R222 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_FREQ_DET_10	R/W	0x0	PRIREF Frequency Detection

1.162 R223 Register (Address = 0xDF) [Reset = 0x0]

R223 is shown in Table 1-164.

Return to the Summary Table.

Table 1-164. R223 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_FREQ_DET_11	R/W	0x0	PRIREF Frequency Detection

1.163 R224 Register (Address = 0xE0) [Reset = 0x0]

R224 is shown in Table 1-165.

Return to the Summary Table.

Table 1-165. R224 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_FREQ_DET_12	R/W	0x0	PRIREF Frequency Detection

1.164 R225 Register (Address = 0xE1) [Reset = 0x0]

R225 is shown in Table 1-166.

Return to the Summary Table.

Table 1-166. R225 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SECREF_FREQ_DET_5	R/W	0x0	SECREF Frequency Detection

1.165 R226 Register (Address = 0xE2) [Reset = 0x0]

R226 is shown in Table 1-167.

Return to the Summary Table.

Table 1-167. R226 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_FREQ_DET_6	R/W	0x0	SECREF Frequency Detection

1.166 R227 Register (Address = 0xE3) [Reset = 0x0]

R227 is shown in Table 1-168.

Return to the Summary Table.

Table 1-168. R227 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_FREQ_DET_7	R/W	0x0	SECREF Frequency Detection

1.167 R228 Register (Address = 0xE4) [Reset = 0x0]

R228 is shown in Table 1-169.

Return to the Summary Table.

Table 1-169. R228 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_FREQ_DET_8	R/W	0x0	SECREF Frequency Detection

1.168 R229 Register (Address = 0xE5) [Reset = 0x0]

R229 is shown in Table 1-170.

Return to the Summary Table.

Table 1-170. R229 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	SECREF_FREQ_DET_9	R/W	0x0	SECREF Frequency Detection

1.169 R230 Register (Address = 0xE6) [Reset = 0x0]

R230 is shown in Table 1-171.

Return to the Summary Table.

Table 1-171. R230 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_FREQ_DET_10	R/W	0x0	SECREF Frequency Detection

1.170 R231 Register (Address = 0xE7) [Reset = 0x0]

R231 is shown in Table 1-172.

Return to the Summary Table.

Table 1-172. R231 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_FREQ_DET_11	R/W	0x0	SECREF Frequency Detection

1.171 R232 Register (Address = 0xE8) [Reset = 0x0]

R232 is shown in Table 1-173.

Return to the Summary Table.

Table 1-173. R232 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_FREQ_DET_12	R/W	0x0	SECREF Frequency Detection

1.172 R233 Register (Address = 0xE9) [Reset = 0x0]

R233 is shown in Table 1-174.

Return to the Summary Table.

Table 1-174. R233 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	PRIREFVLDTMR	R/W	0x0	PRIREF Validation Timer Timer = 0.1 ms x $2^{\text{PRIREFVLDTMR}}$

1.173 R234 Register (Address = 0xEA) [Reset = 0x0]

R234 is shown in Table 1-175.

Return to the Summary Table.

Table 1-175. R234 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	SECREFVLDTMR	R/W	0x0	SECREF Validation Timer Timer = 0.1 ms x $2^{\text{SECREFVLDTMR}}$

1.174 R235 Register (Address = 0xEB) [Reset = 0x0]

R235 is shown in Table 1-176.

Return to the Summary Table.

Table 1-176. R235 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	PRIREF_PH_VALID_DET_1	R/W	0x0	PRIREF Phase-valid Detection

1.175 R236 Register (Address = 0xEC) [Reset = 0x0]

R236 is shown in Table 1-177.

Return to the Summary Table.

Table 1-177. R236 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_PH_VALID_DET_2	R/W	0x0	PRIREF Phase-valid Detection

1.176 R237 Register (Address = 0xED) [Reset = 0x0]

R237 is shown in Table 1-178.

Return to the Summary Table.

Table 1-178. R237 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_PH_VALID_DET_3	R/W	0x0	PRIREF Phase-valid Detection

1.177 R238 Register (Address = 0xEE) [Reset = 0x0]

R238 is shown in Table 1-179.

Return to the Summary Table.

Table 1-179. R238 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PRIREF_PH_VALID_DET_4	R/W	0x0	PRIREF Phase-valid Detection

1.178 R239 Register (Address = 0xEF) [Reset = 0x0]

R239 is shown in Table 1-180.

Return to the Summary Table.

Table 1-180. R239 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	SECREF_PH_VALID_DET_1	R/W	0x0	SECREF Phase-valid Detection

1.179 R240 Register (Address = 0xF0) [Reset = 0x0]

R240 is shown in Table 1-181.

Return to the Summary Table.

Table 1-181. R240 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_PH_VALID_DET_2	R/W	0x0	SECREF Phase-valid Detection

1.180 R241 Register (Address = 0xF1) [Reset = 0x0]

R241 is shown in Table 1-182.

Return to the Summary Table.

Table 1-182. R241 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_PH_VALID_DET_3	R/W	0x0	SECREF Phase-valid Detection

1.181 R242 Register (Address = 0xF2) [Reset = 0x0]

R242 is shown in Table 1-183.

Return to the Summary Table.

Table 1-183. R242 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	SECREF_PH_VALID_DET_4	R/W	0x0	SECREF Phase-valid Detection

1.182 R243 Register (Address = 0xF3) [Reset = 0x0]

R243 is shown in Table 1-184.

Return to the Summary Table.

Table 1-184. R243 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	PRIREF_PH_VALID_THR	R/W	0x0	PRIREF Phase Valid Threshold

1.183 R244 Register (Address = 0xF4) [Reset = 0x0]

R244 is shown in Table 1-185.

Return to the Summary Table.

Table 1-185. R244 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	SECREF_PH_VALID_THR	R/W	0x0	SECREF Phase Valid Threshold

1.184 R249 Register (Address = 0xF9) [Reset = 0x0]

R249 is shown in Table 1-186.

Return to the Summary Table.

Table 1-186. R249 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0x0	Reserved
5:4	DPLL_SECREF_AUTO_PRTY	R/W	0x0	Set priorty for SECREF See DPLL_PRIREF_AUTO_PRTY for bit settings.
3:2	RESERVED	R/W	0x0	Reserved
1:0	DPLL_PRIREF_AUTO_PRTY	R/W	0x0	Set priorty for PRIREF 0x1 = First priority 0x2 = Second priority

1.185 R251 Register (Address = 0xFB) [Reset = 0x0]

R251 is shown in Table 1-187.

Return to the Summary Table.

Table 1-187. R251 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0x0	Reserved
5	DPLL_REF_MAN_SEL	R/W	0x0	Controls source of manual selection 0x0 = Software register: DPLL_REF_MAN_REG_SEL 0x1 = Hardware pin: REFSEL
4	DPLL_REF_MAN_REG_SEL	R/W	0x0	Controls software manual Ref selection 0x0 = Primary Reference 0x1 = Secondary Reference
3:2	RESERVED	R	0x0	Reserved
1:0	DPLL_SWITCH_MODE	R/W	0x0	Controls switchover mode 0x0 = Auto non-revertive 0x1 = Auto revertive 0x2 = Manual fallback 0x3 = Manual holdover

1.186 R252 Register (Address = 0xFC) [Reset = 0x0]

R252 is shown in Table 1-188.

Return to the Summary Table.

Table 1-188. R252 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL_ZDM_SYNC_EN	R/W	0x0	DPLL Zero Delay Synchronization enable
6	RESERVED	R/W	0x0	Reserved
5	DPLL_SWITCHOVER_1	R/W	0x0	DPLL Switchover Timer
4	DPLL_FASTLOCK_ALWAYS	R/W	0x0	Enable DPLL fast lock
3	RESERVED	R/W	0x0	Reserved
2	DPLL_HLDOVR_MODE	R/W	0x0	DPLL Holdover mode when tuning word history unavailable 0x0 = Enter free-run mode 0x1 = Hold last control value prior to holdover
1	RESERVED	R	0x0	Reserved
0	DPLL_LOOP_EN	R/W	0x0	DPLL Enable

1.187 R253 Register (Address = 0xFD) [Reset = 0x0]

R253 is shown in Table 1-189.

Return to the Summary Table.

Table 1-189. R253 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL_SWITCHOVER_2	R/W	0x0	DPLL Switchover Timer

1.188 R254 Register (Address = 0xFE) [Reset = 0x0]

R254 is shown in Table 1-190.

Return to the Summary Table.

Table 1-190. R254 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	0x0	Reserved
2:0	DPLL_SWITCHOVER_3	R/W	0x0	DPLL Switchover Timer

1.189 R255 Register (Address = 0xFF) [Reset = 0x0]

R255 is shown in Table 1-191.

Return to the Summary Table.

Table 1-191. R255 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_SWITCHOVER_4	R/W	0x0	DPLL Switchover Timer

1.190 R256 Register (Address = 0x100) [Reset = 0x0]

R256 is shown in Table 1-192.

Return to the Summary Table.

Table 1-192. R256 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_PRIREF_RDIV_15:8	R/W	0x0	Bits 15:8 of DPLL_PRIREF_RDIV

1.191 R257 Register (Address = 0x101) [Reset = 0x0]

R257 is shown in Table 1-193.

Return to the Summary Table.

Table 1-193. R257 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_PRIREF_RDIV	R/W	0x0	DPLL PRIREF divider control

1.192 R258 Register (Address = 0x102) [Reset = 0x0]

R258 is shown in Table 1-194.

Return to the Summary Table.

Table 1-194. R258 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_SECREF_RDIV_15:8	R/W	0x0	Bits 15:8 of DPLL_SECREF_RDIV

1.193 R259 Register (Address = 0x103) [Reset = 0x0]

R259 is shown in Table 1-195.

Return to the Summary Table.

Table 1-195. R259 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_SECREF_RDIV	R/W	0x0	DPLL SECREF divider control

1.194 R260 Register (Address = 0x104) [Reset = 0x0]

R260 is shown in Table 1-196.

Return to the Summary Table.

Table 1-196. R260 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3:2	RESERVED	R	0x0	Reserved
1	DPLL_REF_AVOID_SLIP	R/W	0x0	Disable Cycle Slip
0	RESERVED	R/W	0x0	Reserved

1.195 R261 Register (Address = 0x105) [Reset = 0x0]

R261 is shown in Table 1-197.

Return to the Summary Table.

Table 1-197. R261 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL_REF_1	R/W	0x0	DPLL Reference Control
6:5	RESERVED	R	0x0	Reserved
4:0	RESERVED	R/W	0x0	Reserved

1.196 R262 Register (Address = 0x106) [Reset = 0x0]

R262 is shown in Table 1-198.

Return to the Summary Table.

Table 1-198. R262 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL_REF_2	R/W	0x0	DPLL Reference Control

1.197 R263 Register (Address = 0x107) [Reset = 0x0]

R263 is shown in Table 1-199.

Return to the Summary Table.

Table 1-199. R263 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_3	R/W	0x0	DPLL Reference Control

1.198 R264 Register (Address = 0x108) [Reset = 0x0]

R264 is shown in Table 1-200.

Return to the Summary Table.

Table 1-200. R264 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_4	R/W	0x0	DPLL Reference Control

1.199 R265 Register (Address = 0x109) [Reset = 0x0]

R265 is shown in Table 1-201.

Return to the Summary Table.

Table 1-201. R265 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_5	R/W	0x0	DPLL Reference Control

1.200 R266 Register (Address = 0x10A) [Reset = 0x0]

R266 is shown in Table 1-202.

Return to the Summary Table.

Table 1-202. R266 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_6	R/W	0x0	DPLL Reference Control

1.201 R267 Register (Address = 0x10B) [Reset = 0x0]

R267 is shown in Table 1-203.

Return to the Summary Table.

Table 1-203. R267 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0x0	Reserved
3	DPLL_REF_7	R/W	0x0	DPLL Reference Control
2:1	DPLL_REF_LF_1	R/W	0x0	DPLL Loop Filter
0	DPLL_REF_LF_2	R/W	0x0	DPLL Loop Filter

1.202 R268 Register (Address = 0x10C) [Reset = 0xF]

R268 is shown in Table 1-204.

Return to the Summary Table.

Table 1-204. R268 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	DPLL_REF_8	R/W	0x1	DPLL Reference Control
2	DPLL_REF_9	R/W	0x1	DPLL Reference Control
1	DPLL_REF_10	R/W	0x1	DPLL Reference Control
0	DPLL_REF_11	R/W	0x1	DPLL Reference Control

1.203 R269 Register (Address = 0x10D) [Reset = 0x0]

R269 is shown in Table 1-205.

Return to the Summary Table.

Table 1-205. R269 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL_REF_12	R/W	0x0	DPLL Reference Control

1.204 R270 Register (Address = 0x10E) [Reset = 0x0]

R270 is shown in Table 1-206.

Return to the Summary Table.

Table 1-206. R270 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL_REF_LF_3	R/W	0x0	DPLL Loop Filter

1.205 R271 Register (Address = 0x10F) [Reset = 0x1]

R271 is shown in Table 1-207.

Return to the Summary Table.

Table 1-207. R271 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_LF_4	R/W	0x1	DPLL Loop Filter

1.206 R272 Register (Address = 0x110) [Reset = 0x0]

R272 is shown in Table 1-208.

Return to the Summary Table.

Table 1-208. R272 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_REF_LF_5	R/W	0x0	DPLL Loop Filter

1.207 R273 Register (Address = 0x111) [Reset = 0x0]

R273 is shown in Table 1-209.

Return to the Summary Table.

Table 1-209. R273 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_REF_LF_6	R/W	0x0	DPLL Loop Filter

1.208 R274 Register (Address = 0x112) [Reset = 0x0]

R274 is shown in Table 1-210.

Return to the Summary Table.

Table 1-210. R274 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_REF_LF_7	R/W	0x0	DPLL Loop Filter

1.209 R275 Register (Address = 0x113) [Reset = 0x0]

R275 is shown in Table 1-211.

Return to the Summary Table.

Table 1-211. R275 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL_REF_LF_8	R/W	0x0	DPLL Loop Filter

1.210 R276 Register (Address = 0x114) [Reset = 0x0]

R276 is shown in Table 1-212.

Return to the Summary Table.

Table 1-212. R276 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL_REF_LF_9	R/W	0x0	DPLL Loop Filter

1.211 R277 Register (Address = 0x115) [Reset = 0x0]

R277 is shown in Table 1-213.

Return to the Summary Table.

Table 1-213. R277 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL_REF_LF_10	R/W	0x0	DPLL Loop Filter

1.212 R278 Register (Address = 0x116) [Reset = 0x0]

R278 is shown in Table 1-214.

Return to the Summary Table.

Table 1-214. R278 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL_REF_LF_11	R/W	0x0	DPLL Loop Filter

1.213 R279 Register (Address = 0x117) [Reset = 0x0]

R279 is shown in Table 1-215.

Return to the Summary Table.

Table 1-215. R279 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL_REF_LF_12	R/W	0x0	DPLL Loop Filter

1.214 R280 Register (Address = 0x118) [Reset = 0x0]

R280 is shown in Table 1-216.

Return to the Summary Table.

Table 1-216. R280 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL_REF_LF_13	R/W	0x0	DPLL Loop Filter

1.215 R281 Register (Address = 0x119) [Reset = 0x0]

R281 is shown in Table 1-217.

Return to the Summary Table.

Table 1-217. R281 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL_REF_LF_14	R/W	0x0	DPLL Loop Filter

1.216 R282 Register (Address = 0x11A) [Reset = 0x0]

R282 is shown in Table 1-218.

Return to the Summary Table.

Table 1-218. R282 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL_REF_LF_15	R/W	0x0	DPLL Loop Filter

1.217 R283 Register (Address = 0x11B) [Reset = 0x0]

R283 is shown in Table 1-219.

Return to the Summary Table.

Table 1-219. R283 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL_REF_LF_16	R/W	0x0	DPLL Loop Filter

1.218 R284 Register (Address = 0x11C) [Reset = 0x0]

R284 is shown in Table 1-220.

Return to the Summary Table.

Table 1-220. R284 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL_REF_LF_17	R/W	0x0	DPLL Loop Filter

1.219 R285 Register (Address = 0x11D) [Reset = 0x0]

R285 is shown in Table 1-221.

Return to the Summary Table.

Table 1-221. R285 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL_REF_LF_18	R/W	0x0	DPLL Loop Filter

1.220 R286 Register (Address = 0x11E) [Reset = 0x0]

R286 is shown in Table 1-222.

Return to the Summary Table.

Table 1-222. R286 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL_REF_LF_19	R/W	0x0	DPLL Loop Filter

1.221 R287 Register (Address = 0x11F) [Reset = 0x0]

R287 is shown in Table 1-223.

Return to the Summary Table.

Table 1-223. R287 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_LF_20	R/W	0x0	DPLL Loop Filter

1.222 R288 Register (Address = 0x120) [Reset = 0x0]

R288 is shown in Table 1-224.

Return to the Summary Table.

Table 1-224. R288 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL_REF_LF_21	R/W	0x0	DPLL Loop Filter

1.223 R289 Register (Address = 0x121) [Reset = 0x0]

R289 is shown in Table 1-225.

Return to the Summary Table.

Table 1-225. R289 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_LF_22	R/W	0x0	DPLL Loop Filter

1.224 R290 Register (Address = 0x122) [Reset = 0x0]

R290 is shown in Table 1-226.

Return to the Summary Table.

Table 1-226. R290 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL_PL_DET_1	R/W	0x0	DPLL Phase Lock Detection

1.225 R291 Register (Address = 0x123) [Reset = 0x0]

R291 is shown in Table 1-227.

Return to the Summary Table.

Table 1-227. R291 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_PL_DET_2	R/W	0x0	DPLL Phase Lock Detection

1.226 R292 Register (Address = 0x124) [Reset = 0x0]

R292 is shown in Table 1-228.

Return to the Summary Table.

Table 1-228. R292 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	DPLL_HITLESS_SW_1	R/W	0x0	Phase Cancellation for Hitless Switching

1.227 R293 Register (Address = 0x125) [Reset = 0x1]

R293 is shown in Table 1-229.

Return to the Summary Table.

Table 1-229. R293 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved

Table 1-229. R293 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RESERVED	R/W	0x0	Reserved
0	DPLL_HITLESS_SW_2	R/W	0x1	Phase Cancellation for Hitless Switching

1.228 R294 Register (Address = 0x126) [Reset = 0x0]

R294 is shown in Table 1-230.

Return to the Summary Table.

Table 1-230. R294 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1:0	DPLL_HITLESS_SW_3	R/W	0x0	Phase Cancellation for Hitless Switching

1.229 R295 Register (Address = 0x127) [Reset = 0x0]

R295 is shown in Table 1-231.

Return to the Summary Table.

Table 1-231. R295 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_HITLESS_SW_4	R/W	0x0	Phase Cancellation for Hitless Switching

1.230 R296 Register (Address = 0x128) [Reset = 0x0]

R296 is shown in Table 1-232.

Return to the Summary Table.

Table 1-232. R296 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_REF_LF_23	R/W	0x0	DPLL Loop Filter

1.231 R297 Register (Address = 0x129) [Reset = 0x0]

R297 is shown in Table 1-233.

Return to the Summary Table.

Table 1-233. R297 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_REF_LF_24	R/W	0x0	DPLL Loop Filter

1.232 R298 Register (Address = 0x12A) [Reset = 0x0]

R298 is shown in Table 1-234.

Return to the Summary Table.

Table 1-234. R298 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_REF_LF_25	R/W	0x0	DPLL Loop Filter

1.233 R300 Register (Address = 0x12C) [Reset = 0x0]

R300 is shown in Table 1-235.

Return to the Summary Table.

Table 1-235. R300 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL_PL_DET_3	R/W	0x0	DPLL Phase Lock Detection

1.234 R301 Register (Address = 0x12D) [Reset = 0x0]

R301 is shown in Table 1-236.

Return to the Summary Table.

Table 1-236. R301 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_PL_LOCK_THRESH	R/W	0x0	Phase lock declaration threshold

1.235 R302 Register (Address = 0x12E) [Reset = 0x0]

R302 is shown in Table 1-237.

Return to the Summary Table.

Table 1-237. R302 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_PL_UNLK_THRESH	R/W	0x0	Phase un-lock declaration threshold

1.236 R304 Register (Address = 0x130) [Reset = 0x0]

R304 is shown in Table 1-238.

Return to the Summary Table.

Table 1-238. R304 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3:0	DPLL_REF_FB_PRE_DIV	R/W	0x0	DPLL REF Feedback Pre Divider value Divider value ranges from 2 to 17. Divider value = DPLL_REF_FB_PRE_DIV + 2.

1.237 R305 Register (Address = 0x131) [Reset = 0x0]

R305 is shown in Table 1-239.

Return to the Summary Table.

Table 1-239. R305 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_REF_FB_DIV_29:24	R/W	0x0	Bits 29:24 of DPLL_REF_FB_DIV

1.238 R306 Register (Address = 0x132) [Reset = 0x0]

R306 is shown in Table 1-240.

Return to the Summary Table.

Table 1-240. R306 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_FB_DIV_23:16	R/W	0x0	Bits 23:16 of DPLL_REF_FB_DIV

1.239 R307 Register (Address = 0x133) [Reset = 0x0]

R307 is shown in Table 1-241.

Return to the Summary Table.

Table 1-241. R307 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_FB_DIV_15:8	R/W	0x0	Bits 15:8 of DPLL_REF_FB_DIV

1.240 R308 Register (Address = 0x134) [Reset = 0xC8]

R308 is shown in Table 1-242.

Return to the Summary Table.

Table 1-242. R308 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_FB_DIV	R/W	0xC8	DPLL REF Feedback Divider value

1.241 R309 Register (Address = 0x135) [Reset = 0x0]

R309 is shown in Table 1-243.

Return to the Summary Table.

Table 1-243. R309 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_NUM_39:32	R/W	0x0	Bits 39:32 of DPLL_REF_NUM

1.242 R310 Register (Address = 0x136) [Reset = 0x0]

R310 is shown in Table 1-244.

Return to the Summary Table.

Table 1-244. R310 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_NUM_31:24	R/W	0x0	Bits 31:24 of DPLL_REF_NUM

1.243 R311 Register (Address = 0x137) [Reset = 0x0]

R311 is shown in Table 1-245.

Return to the Summary Table.

Table 1-245. R311 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_NUM_23:16	R/W	0x0	Bits 23:16 of DPLL_REF_NUM

1.244 R312 Register (Address = 0x138) [Reset = 0x0]

R312 is shown in Table 1-246.

Return to the Summary Table.

Table 1-246. R312 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_NUM_15:8	R/W	0x0	Bits 15:8 of DPLL_REF_NUM

1.245 R313 Register (Address = 0x139) [Reset = 0x0]

R313 is shown in Table 1-247.

Return to the Summary Table.

Table 1-247. R313 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_NUM	R/W	0x0	DPLL REF FB Divider Numerator

1.246 R314 Register (Address = 0x13A) [Reset = 0x0]

R314 is shown in Table 1-248.

Return to the Summary Table.

Table 1-248. R314 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_DEN_39:32	R/W	0x0	Bits 39:32 of DPLL_REF_DEN

1.247 R315 Register (Address = 0x13B) [Reset = 0x0]

R315 is shown in Table 1-249.

Return to the Summary Table.

Table 1-249. R315 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_DEN_31:24	R/W	0x0	Bits 31:24 of DPLL_REF_DEN

1.248 R316 Register (Address = 0x13C) [Reset = 0x0]

R316 is shown in Table 1-250.

Return to the Summary Table.

Table 1-250. R316 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_DEN_23:16	R/W	0x0	Bits 23:16 of DPLL_REF_DEN

1.249 R317 Register (Address = 0x13D) [Reset = 0x0]

R317 is shown in Table 1-251.

Return to the Summary Table.

Table 1-251. R317 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_DEN_15:8	R/W	0x0	Bits 15:8 of DPLL_REF_DEN

1.250 R318 Register (Address = 0x13E) [Reset = 0x0]

R318 is shown in Table 1-252.

Return to the Summary Table.

Table 1-252. R318 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_DEN	R/W	0x0	DPLL REF FB Divider denominator

1.251 R319 Register (Address = 0x13F) [Reset = 0x18]

R319 is shown in Table 1-253.

Return to the Summary Table.

Table 1-253. R319 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:5	RESERVED	R/W	0x0	Reserved
4:3	DPLL_REF_13	R/W	0x3	DPLL Reference Control
2:0	DPLL_REF_14	R/W	0x0	DPLL Reference Control

1.252 R320 Register (Address = 0x140) [Reset = 0x0]

R320 is shown in Table 1-254.

Return to the Summary Table.

Table 1-254. R320 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	DPLL_LOCK_DET_1	R/W	0x0	DPLL DCO Lock Detection

1.253 R321 Register (Address = 0x141) [Reset = 0x0]

R321 is shown in Table 1-255.

Return to the Summary Table.

Table 1-255. R321 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_LOCK_DET_2	R/W	0x0	DPLL DCO Lock Detection

1.254 R322 Register (Address = 0x142) [Reset = 0x0]

R322 is shown in Table 1-256.

Return to the Summary Table.

Table 1-256. R322 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_LOCK_DET_3	R/W	0x0	DPLL DCO Lock Detection

1.255 R323 Register (Address = 0x143) [Reset = 0x0]

R323 is shown in Table 1-257.

Return to the Summary Table.

Table 1-257. R323 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_LOCK_DET_4	R/W	0x0	DPLL DCO Lock Detection

1.256 R324 Register (Address = 0x144) [Reset = 0x0]

R324 is shown in Table 1-258.

Return to the Summary Table.

Table 1-258. R324 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_LOCK_DET_5	R/W	0x0	DPLL DCO Lock Detection

1.257 R325 Register (Address = 0x145) [Reset = 0x0]

R325 is shown in Table 1-259.

Return to the Summary Table.

Table 1-259. R325 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_LOCK_DET_6	R/W	0x0	DPLL DCO Lock Detection

1.258 R326 Register (Address = 0x146) [Reset = 0x0]

R326 is shown in Table 1-260.

Return to the Summary Table.

Table 1-260. R326 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_LOCK_DET_7	R/W	0x0	DPLL DCO Lock Detection

1.259 R327 Register (Address = 0x147) [Reset = 0x0]

R327 is shown in Table 1-261.

Return to the Summary Table.

Table 1-261. R327 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_LOCK_DET_8	R/W	0x0	DPLL DCO Lock Detection

1.260 R328 Register (Address = 0x148) [Reset = 0x0]

R328 is shown in Table 1-262.

Return to the Summary Table.

Table 1-262. R328 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_LOCK_DET_9	R/W	0x0	DPLL DCO Lock Detection

1.261 R329 Register (Address = 0x149) [Reset = 0x0]

R329 is shown in Table 1-263.

Return to the Summary Table.

Table 1-263. R329 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_LOCK_DET_10	R/W	0x0	DPLL DCO Lock Detection

1.262 R330 Register (Address = 0x14A) [Reset = 0x0]

R330 is shown in Table 1-264.

Return to the Summary Table.

Table 1-264. R330 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved
6:0	DPLL_UNLK_DET_1	R/W	0x0	DPLL DCO Unlock Detection

1.263 R331 Register (Address = 0x14B) [Reset = 0x0]

R331 is shown in Table 1-265.

Return to the Summary Table.

Table 1-265. R331 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_UNLK_DET_2	R/W	0x0	DPLL DCO Unlock Detection

1.264 R332 Register (Address = 0x14C) [Reset = 0x0]

R332 is shown in Table 1-266.

Return to the Summary Table.

Table 1-266. R332 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_UNLK_DET_3	R/W	0x0	DPLL DCO Unlock Detection

1.265 R333 Register (Address = 0x14D) [Reset = 0x0]

R333 is shown in Table 1-267.

Return to the Summary Table.

Table 1-267. R333 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_DEN_23:16	R/W	0x0	Bits 23:16 of PLL2 denominator

1.266 R334 Register (Address = 0x14E) [Reset = 0x0]

R334 is shown in Table 1-268.

Return to the Summary Table.

Table 1-268. R334 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_DEN_15:8	R/W	0x0	Bits 15:8 of PLL2 denominator

1.267 R335 Register (Address = 0x14F) [Reset = 0x0]

R335 is shown in Table 1-269.

Return to the Summary Table.

Table 1-269. R335 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL2_DEN_7:0	R/W	0x0	Bits 7:0 of PLL2 denominator

1.268 R336 Register (Address = 0x150) [Reset = 0x0]

R336 is shown in Table 1-270.

Return to the Summary Table.

Table 1-270. R336 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_UNLK_DET_7	R/W	0x0	DPLL DCO Unlock Detection

1.269 R337 Register (Address = 0x151) [Reset = 0x0]

R337 is shown in Table 1-271.

Return to the Summary Table.

Table 1-271. R337 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_UNLK_DET_8	R/W	0x0	DPLL DCO Unlock Detection

1.270 R338 Register (Address = 0x152) [Reset = 0x0]

R338 is shown in Table 1-272.

Return to the Summary Table.

Table 1-272. R338 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_UNLK_DET_9	R/W	0x0	DPLL DCO Unlock Detection

1.271 R339 Register (Address = 0x153) [Reset = 0x0]

R339 is shown in Table 1-273.

Return to the Summary Table.

Table 1-273. R339 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	PLL1_24B_NUM_23:16	R/W	0x0	APLL1 24-bit numberator bits 23:16

1.272 R340 Register (Address = 0x154) [Reset = 0x0]

R340 is shown in Table 1-274.

Return to the Summary Table.

Table 1-274. R340 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	Reserved
4:0	DPLL_REF_SYNC_PH_OFFSET_44:40	R/W	0x0	Bits 44:40 of DPLL_REF_SYNC_PH_OFFSET

1.273 R341 Register (Address = 0x155) [Reset = 0x0]

R341 is shown in Table 1-275.

Return to the Summary Table.

Table 1-275. R341 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_SYNC_PH_OFFSET_39:32	R/W	0x0	Bits 39:32 of DPLL_REF_SYNC_PH_OFFSET

1.274 R342 Register (Address = 0x156) [Reset = 0x0]

R342 is shown in Table 1-276.

Return to the Summary Table.

Table 1-276. R342 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_SYNC_PH_OFFSET_31:24	R/W	0x0	Bits 31:24 of DPLL_REF_SYNC_PH_OFFSET

1.275 R343 Register (Address = 0x157) [Reset = 0x0]

R343 is shown in Table 1-277.

Return to the Summary Table.

Table 1-277. R343 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_SYNC_PH_OFFSET_23:16	R/W	0x0	Bits 23:16 of DPLL_REF_SYNC_PH_OFFSET

1.276 R344 Register (Address = 0x158) [Reset = 0x0]

R344 is shown in Table 1-278.

Return to the Summary Table.

Table 1-278. R344 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_SYNC_PH_OFFSET_15:8	R/W	0x0	Bits 15:8 of DPLL_REF_SYNC_PH_OFFSET

1.277 R345 Register (Address = 0x159) [Reset = 0x0]

R345 is shown in Table 1-279.

Return to the Summary Table.

Table 1-279. R345 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_REF_SYNC_PH_OFFSET	R/W	0x0	DPLL REF Zero Delay Mode Phase Offset

1.278 R346 Register (Address = 0x15A) [Reset = 0x0]

R346 is shown in Table 1-280.

Return to the Summary Table.

Table 1-280. R346 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	DPLL_FDEV_EN	R/W	0x0	DPLL Freq Incr/Decr enable via pin or reg control

1.279 R347 Register (Address = 0x15B) [Reset = 0x0]

R347 is shown in Table 1-281.

Return to the Summary Table.

Table 1-281. R347 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5:0	DPLL_FDEV_37:32	R/W	0x0	Bits 37:32 of DPLL_FDEV

1.280 R348 Register (Address = 0x15C) [Reset = 0x0]

R348 is shown in Table 1-282.

Return to the Summary Table.

Table 1-282. R348 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_FDEV_31:24	R/W	0x0	Bits 31:24 of DPLL_FDEV

1.281 R349 Register (Address = 0x15D) [Reset = 0x0]

R349 is shown in Table 1-283.

Return to the Summary Table.

Table 1-283. R349 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_FDEV_23:16	R/W	0x0	Bits 23:16 of DPLL_FDEV

1.282 R350 Register (Address = 0x15E) [Reset = 0x0]

R350 is shown in Table 1-284.

Return to the Summary Table.

Table 1-284. R350 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_FDEV_15:8	R/W	0x0	Bits 15:8 of DPLL_FDEV

1.283 R351 Register (Address = 0x15F) [Reset = 0x0]

R351 is shown in Table 1-285.

Return to the Summary Table.

Table 1-285. R351 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DPLL_FDEV	R/W	0x0	DPLL Freq Incr/Decr Numerator Step Word This step word is computed based on the desired DCO frequecy step size in ppb (parts-per-billion).

1.284 R352 Register (Address = 0x160) [Reset = 0x0]

R352 is shown in Table 1-286.

Return to the Summary Table.

Table 1-286. R352 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	Reserved
0	DPLL_FDEV_REG_UPDATE	R/W	0x0	DPLL Freq Incr/Decr register control Writing this register applies one FINC/FDEC of the Numerator as defined by the FDEV register.

1.285 R357 Register (Address = 0x165) [Reset = 0x0]

R357 is shown in Table 1-287.

Return to the Summary Table.

Table 1-287. R357 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved

Table 1-287. R357 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	PLL1_VM_INSIDE	R	0x0	PLL1 VCO Status Denotes if the PLL1 charge pump voltage is within operational range.
4:0	RESERVED	R	0x0	Reserved

1.286 R367 Register (Address = 0x16F) [Reset = 0x0]

R367 is shown in Table 1-288.

Return to the Summary Table.

Table 1-288. R367 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	0x0	Reserved
5	PLL2_VM_INSIDE	R	0x0	PLL2 VCO Status Denotes if the PLL2 charge pump voltage is within operational range.
4:0	RESERVED	R	0x0	Reserved

1.287 R411 Register (Address = 0x19B) [Reset = 0x0]

R411 is shown in Table 1-289.

Return to the Summary Table.

Table 1-289. R411 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R	0x0	Reserved
3	SECREF_VALSTAT	R	0x0	SECREF valid state
2	PRIREF_VALSTAT	R	0x0	PRIREF valid state
1	RESERVED	R	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

2 LMK05318B Register Maps

Table 2-1 lists the memory-mapped registers for the Device registers. All register offset addresses not listed in Table 2-1 should be considered as reserved locations and the register contents should not be modified.

Table 2-1. Device Registers

Address	Acronym	Register Name	Section
0x0	R0		Go
0x1	R1		Go
0x2	R2		Go
0x3	R3		Go
0x4	R4		Go
0x5	R5		Go
0x6	R6		Go
0x7	R7		Go
0x8	R8		Go
0x9	R9		Go
0xA	R10		Go
0xB	R11		Go
0xC	R12		Go
0xD	R13		Go
0xE	R14		Go
0xF	R15		Go
0x10	R16		Go
0x11	R17		Go
0x12	R18		Go
0x13	R19		Go
0x14	R20		Go
0x15	R21		Go
0x16	R22		Go
0x17	R23		Go
0x18	R24		Go
0x19	R25		Go
0x1A	R26		Go
0x1B	R27		Go
0x1C	R28		Go
0x1D	R29		Go
0x1E	R30		Go
0x1F	R31		Go
0x20	R32		Go
0x21	R33		Go
0x22	R34		Go
0x23	R35		Go

Table 2-1. Device Registers (continued)

Address	Acronym	Register Name	Section
0x24	R36		Go
0x25	R37		Go
0x26	R38		Go
0x27	R39		Go
0x28	R40		Go
0x29	R41		Go
0x2A	R42		Go
0x2B	R43		Go
0x2C	R44		Go
0x2D	R45		Go
0x2E	R46		Go
0x2F	R47		Go
0x30	R48		Go
0x31	R49		Go
0x32	R50		Go
0x33	R51		Go
0x34	R52		Go
0x35	R53		Go
0x36	R54		Go
0x37	R55		Go
0x38	R56		Go
0x39	R57		Go
0x3A	R58		Go
0x3B	R59		Go
0x3C	R60		Go
0x3D	R61		Go
0x3E	R62		Go
0x3F	R63		Go
0x40	R64		Go
0x41	R65		Go
0x42	R66		Go
0x43	R67		Go
0x44	R68		Go
0x45	R69		Go
0x46	R70		Go
0x47	R71		Go
0x48	R72		Go
0x49	R73		Go
0x4A	R74		Go
0x4B	R75		Go

Table 2-1. Device Registers (continued)

Address	Acronym	Register Name	Section
0x4C	R76		Go
0x4D	R77		Go
0x4E	R78		Go
0x4F	R79		Go
0x50	R80		Go
0x51	R81		Go
0x52	R82		Go
0x53	R83		Go
0x54	R84		Go
0x55	R85		Go
0x56	R86		Go
0x57	R87		Go
0x58	R88		Go
0x59	R89		Go
0x5A	R90		Go
0x5B	R91		Go
0x5C	R92		Go
0x5D	R93		Go
0x5E	R94		Go
0x5F	R95		Go
0x60	R96		Go
0x61	R97		Go
0x62	R98		Go
0x63	R99		Go
0x64	R100		Go
0x65	R101		Go
0x66	R102		Go
0x67	R103		Go
0x68	R104		Go
0x69	R105		Go
0x6A	R106		Go
0x6B	R107		Go
0x6C	R108		Go
0x6D	R109		Go
0x6E	R110		Go
0x6F	R111		Go
0x70	R112		Go
0x71	R113		Go
0x72	R114		Go
0x73	R115		Go

Table 2-1. Device Registers (continued)

Address	Acronym	Register Name	Section
0x74	R116		Go
0x75	R117		Go
0x76	R118		Go
0x77	R119		Go
0x78	R120		Go
0x79	R121		Go
0x7A	R122		Go
0x7B	R123		Go
0x7C	R124		Go
0x7D	R125		Go
0x7E	R126		Go
0x7F	R127		Go
0x80	R128		Go
0x81	R129		Go
0x82	R130		Go
0x83	R131		Go
0x84	R132		Go
0x85	R133		Go
0x86	R134		Go
0x87	R135		Go
0x88	R136		Go
0x89	R137		Go
0x8A	R138		Go
0x8B	R139		Go
0x8C	R140		Go
0x8D	R141		Go
0x8E	R142		Go
0x8F	R143		Go
0x90	R144		Go
0x91	R145		Go
0x92	R146		Go
0x93	R147		Go
0x94	R148		Go
0x95	R149		Go
0x96	R150		Go
0x97	R151		Go
0x98	R152		Go
0x99	R153		Go
0x9A	R154		Go
0x9B	R155		Go

Table 2-1. Device Registers (continued)

Address	Acronym	Register Name	Section
0x9C	R156		Go
0x9D	R157		Go
0x9E	R158		Go
0x9F	R159		Go
0xA0	R160		Go
0xA1	R161		Go
0xA2	R162		Go
0xA3	R163		Go
0xA4	R164		Go
0xA5	R165		Go
0xA6	R166		Go
0xA7	R167		Go
0xA8	R168		Go
0xA9	R169		Go
0xAA	R170		Go
0xAB	R171		Go
0xAC	R172		Go
0xAD	R173		Go
0xAE	R174		Go
0xAF	R175		Go
0xB0	R176		Go
0xB1	R177		Go
0xB2	R178		Go
0xB3	R179		Go
0xB4	R180		Go
0xB5	R181		Go
0xB6	R182		Go
0xB7	R183		Go
0xB8	R184		Go
0xB9	R185		Go
0xBA	R186		Go
0xBB	R187		Go
0xBC	R188		Go
0xBD	R189		Go
0xBE	R190		Go
0xBF	R191		Go
0xC0	R192		Go
0xC1	R193		Go
0xC2	R194		Go
0xC3	R195		Go

Table 2-1. Device Registers (continued)

Address	Acronym	Register Name	Section
0xC4	R196		Go
0xC5	R197		Go
0xC6	R198		Go
0xC7	R199		Go
0xC8	R200		Go
0xC9	R201		Go
0xCA	R202		Go
0xCB	R203		Go
0xCC	R204		Go
0xCD	R205		Go
0xCE	R206		Go
0xCF	R207		Go
0xD0	R208		Go
0xD1	R209		Go
0xD2	R210		Go
0xD3	R211		Go
0xD4	R212		Go
0xD5	R213		Go
0xD6	R214		Go
0xD7	R215		Go
0xD8	R216		Go
0xD9	R217		Go
0xDA	R218		Go
0xDB	R219		Go
0xDC	R220		Go
0xDD	R221		Go
0xDE	R222		Go
0xDF	R223		Go
0xE0	R224		Go
0xE1	R225		Go
0xE2	R226		Go
0xE3	R227		Go
0xE4	R228		Go
0xE5	R229		Go
0xE6	R230		Go
0xE7	R231		Go
0xE8	R232		Go
0xE9	R233		Go
0xEA	R234		Go
0xEB	R235		Go

Table 2-1. Device Registers (continued)

Address	Acronym	Register Name	Section
0xEC	R236		Go
0xED	R237		Go
0xEE	R238		Go
0xEF	R239		Go
0xF0	R240		Go
0xF1	R241		Go
0xF2	R242		Go
0xF3	R243		Go
0xF4	R244		Go
0xF5	R245		Go
0xF6	R246		Go
0xF7	R247		Go
0xF8	R248		Go
0xF9	R249		Go
0xFA	R250		Go
0xFB	R251		Go
0xFC	R252		Go
0xFD	R253		Go
0xFE	R254		Go
0xFF	R255		Go
0x100	R256		Go
0x101	R257		Go
0x102	R258		Go
0x103	R259		Go
0x104	R260		Go

Complex bit access types are encoded to fit into small table cells. Table 2-2 shows the codes that are used for access types in this section.

Table 2-2. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RN	R N	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
WA	W A	Write
Reset or Default Value		

Table 2-2. Device Access Type Codes (continued)

Access Type	Code	Description
-n		Value after reset or the default value

2.1 R0 Register (Address = 0x0) [reset = 0x10]

R0 is shown in Table 2-3.

Return to Summary Table.

Table 2-3. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VNDRID_15:8	R	0x10	Bits 15:8 of VNDRID

2.2 R1 Register (Address = 0x1) [reset = 0xB]

R1 is shown in Table 2-4.

Return to Summary Table.

Table 2-4. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	VNDRID	R	0xB	Vendor Identification Number Unique 16-bit number assigned to chip vendors.

2.3 R2 Register (Address = 0x2) [reset = 0x35]

R2 is shown in Table 2-5.

Return to Summary Table.

Table 2-5. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRODID	R	0x35	Product Identification Number Unique 8-bit number used to identify the LMK05318.

2.4 R3 Register (Address = 0x3) [reset = 0x0]

R3 is shown in Table 2-6.

Return to Summary Table.

Table 2-6. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	REVID	R	0x0	Device Revision Number Used to identify the mask-set revision.

2.5 R4 Register (Address = 0x4) [reset = 0x0]

R4 is shown in Table 2-7.

Return to Summary Table.

Table 2-7. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRTID_31:24	R	0x0	Bits 31:24 of PRTID

2.6 R5 Register (Address = 0x5) [reset = 0x0]

R5 is shown in Table 2-8.

Return to Summary Table.

Table 2-8. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRTID_23:16	R	0x0	Bits 23:16 of PRTID

2.7 R6 Register (Address = 0x6) [reset = 0x0]

R6 is shown in Table 2-9.

Return to Summary Table.

Table 2-9. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRTID_15:8	R	0x0	Bits 15:8 of PRTID

2.8 R7 Register (Address = 0x7) [reset = 0x0]

R7 is shown in Table 2-10.

Return to Summary Table.

Table 2-10. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRTID	R	0x0	Part Identification Number 32-bit number used to serialize individual LMK05318 devices. Factory programmed. Cannot be modified by the user.

2.9 R8 Register (Address = 0x8) [reset = 0x0]

R8 is shown in Table 2-11.

Return to Summary Table.

Table 2-11. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
6	HW_SW_CTRL_MODE	R	0x0	HW_SW_CTRL Pin Configuration Reflects the values sampled on the HW_SW_CTRL pin during device power-on reset (POR). 0x0 = EEPROM/Soft Pin Mode 0x1 = ROM/Hard Pin Mode
5-4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved

Table 2-11. R8 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	OP_MODE	R	0x0	Operating Mode The OP_MODE fields reflects the device operating mode as determined by the input levels on the HW_SW_CTRL, STATUS0, and STATUS1 pins respectively during POR. 0x0 = Reserved 0x1 = Reserved 0x2 = EEPROM + I2C, Soft pin mode 0x3 = ROM + I2C, Hard pin mode 0x4 = EEPROM + SPI, Soft pin mode 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved

2.10 R9 Register (Address = 0x9) [reset = 0x20]

R9 is shown in Table 2-12.

Return to Summary Table.

Table 2-12. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-4	RESERVED	R	0x2	Reserved
3	RESERVED	R	0x0	
2-0	GPIO_HW_MODE	R	0x0	GPIO[2:0] Hard Pin Configuration Mode Reflects the value sampled on the GPIO[2:0] pins when HW_SW_CTRL = 1. This corresponds to the ROM page.

2.11 R10 Register (Address = 0xA) [reset = 0xC8]

R10 is shown in Table 2-13.

Return to Summary Table.

Table 2-13. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	SLAVEADR_GPIO1_SW	R	0x19	7-bit I2C Slave Address The five MSBs (base address bits) are programmable in EEPROM, which is 11001b for generic factory devices. The two LSBs are determined by control input pin levels. When the HW_SW_CTRL pin is 1, the two LSBs are fixed to 00b. When the HW_SW_CTRL pin is 0, the 2 LSBs are determined the GPIO1 input state (3-level) during POR.
2-0	RESERVED	R	0x0	

2.12 R11 Register (Address = 0xB) [reset = 0x0]

R11 is shown in Table 2-14.

Return to Summary Table.

Table 2-14. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EEREV	R	0x0	EEPROM Image Revision ID EEPROM Image Revision ID is automatically retrieved from EEPROM and reflected in the EEREV register after a reset or after a NVM commit operation. This register is user programmable. EEPROM register 11 can be written through the SRAM.

2.13 R12 Register (Address = 0xC) [reset = 0x39]

R12 is shown in Table 2-15.

Return to Summary Table.

Table 2-15. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET_SW	R/W	0x0	Software Reset ALL functions Writing a 1 will cause the device to return to its power-up state apart from the registers and the configuration controller. The configuration controller is excluded to prevent a re-transfer of EEPROM data to on-chip registers.
6	SYNC_SW	R/W	0x0	Output Synchronization (SYNC) Assert bit
5	SYNC_AUTO_DPLL	R/W	0x1	Reserved, Don't Care bit.
4	SYNC_AUTO_APLL	R/W	0x1	Enable Automatic Output SYNC after PLL lock
3	SYNC_MUTE	R/W	0x1	Determines if the output drivers are muted during a SYNC event 0x0 = Do not mute any outputs during SYNC 0x1 = Mute all outputs during SYNC
2	RESERVED	R	0x0	
1	PLLSTRTMODE	R/W	0x0	PLL Startup Mode . When using cascade mode, PLL1 is fixed to a center value while PLL2 locks. Then PLL1 performs final lock.
0	AUTOSTRT	R/W	0x1	Autostart If AUTOSTRT is set to 1, the device will automatically initiate the PLL and output start-up sequence after a device reset. A device reset can be triggered by the power-on-reset, PDN pin, or by writing to the RESET_SW bit. If AUTOSTRT is 0, the device will halt after the configuration phase; a subsequent write to set the AUTOSTRT bit will initiate the start-up sequence. In Test mode, the AUTOSTRT bit is ignored after device reset, but start-up can be triggered by a subsequent write to set the AUTOSTART bit.

2.14 R13 Register (Address = 0xD) [reset = 0x0]

R13 is shown in Table 2-16.

Return to Summary Table.

Table 2-16. R13 Register Field Descriptions

Bit	Field	Type	Reset	Description
4	LOS_FDET_XO	R	0x0	Loss of source freq detection XO
3	LOL_PLL2	R	0x0	Loss of Lock APLL2
2	LOL_PLL1	R	0x0	Loss of Lock APLL1
1	RESERVED	R	0x0	

Table 2-16. R13 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LOS_XO	R	0x0	Loss of source XO

2.15 R14 Register (Address = 0xE) [reset = 0x0]

R14 is shown in Table 2-17.

Return to Summary Table.

Table 2-17. R14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL	R	0x0	Loss of phase lock DPLL
6	LOFL_DPLL	R	0x0	Loss of frequency lock DPLL
5	HIST	R	0x0	Tuning word history update DPLL
4	HLDOVR	R	0x0	Holdover event DPLL
3	REFSWITCH	R	0x0	Reference switchover DPLL
2	LOR_MISSCLK	R	0x0	Loss of active reference missing clock DPLL
1	LOR_FREQ	R	0x0	Loss of active reference frequency DPLL
0	LOR_AMP	R	0x0	Loss of active reference amplitude DPLL

2.16 R15 Register (Address = 0xF) [reset = 0x0]

R15 is shown in Table 2-18.

Return to Summary Table.

Table 2-18. R15 Register Field Descriptions

Bit	Field	Type	Reset	Description
4	LOS_FDET_XO_MASK	R/W	0x0	Mask Loss of Source Freq Det XO
3	LOL_PLL2_MASK	R/W	0x0	Mask Loss of Lock APLL2
2	LOL_PLL1_MASK	R/W	0x0	Mask Loss of Lock APLL1
1	RESERVED	R	0x0	
0	LOS_XO_MASK	R/W	0x0	Mask Loss of source XO

2.17 R16 Register (Address = 0x10) [reset = 0x0]

R16 is shown in Table 2-19.

Return to Summary Table.

Table 2-19. R16 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL_MASK	R/W	0x0	Mask Loss of Phase Lock DPLL
6	LOFL_DPLL_MASK	R/W	0x0	Mask Loss of Freq Lock DPLL
5	HIST_MASK	R/W	0x0	Mask Tuning word history update DPLL
4	HLDOVR_MASK	R/W	0x0	Mask Holdover event DPLL
3	REFSWITCH_MASK	R/W	0x0	Mask Reference switchover DPLL
2	LOR_MISSCLK_MASK	R/W	0x0	Loss of active reference missing clk DPLL
1	LOR_FREQ_MASK	R/W	0x0	Loss of active reference freq DPLL
0	LOR_AMP_MASK	R/W	0x0	Mask Loss of active reference amplitude DPLL

2.18 R17 Register (Address = 0x11) [reset = 0x0]

R17 is shown in Table 2-20.

Return to Summary Table.

Table 2-20. R17 Register Field Descriptions

Bit	Field	Type	Reset	Description
4	LOS_FDET_XO_POL	R/W	0x0	LOS_FDET_XO Flag Polarity
3	LOL_PLL2_POL	R/W	0x0	LOL_PLL2 Flag Polarity
2	LOL_PLL1_POL	R/W	0x0	LOL_PLL1 Flag Polarity
1	RESERVED	R	0x0	
0	LOS_XO_POL	R/W	0x0	LOS_XO Flag Polarity

2.19 R18 Register (Address = 0x12) [reset = 0x0]

R18 is shown in Table 2-21.

Return to Summary Table.

Table 2-21. R18 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL_POL	R/W	0x0	LOPL_DPLL Flag Polarity
6	LOFL_DPLL_POL	R/W	0x0	LOFL_DPLL Flag Polarity
5	HIST_POL	R/W	0x0	HIST Flag Polarity
4	HLDOVR_POL	R/W	0x0	HLDOVR Flag Polarity
3	REFSWITCH_POL	R/W	0x0	REFSWITCH Flag Polarity
2	LOR_MISSCLK_POL	R/W	0x0	LOR_MISSCLK Flag Polarity
1	LOR_FREQ_POL	R/W	0x0	LOR_FREQ Flag Polarity
0	LOR_AMP_POL	R/W	0x0	LOR_AMP Flag Polarity

2.20 R19 Register (Address = 0x13) [reset = 0x0]

R19 is shown in Table 2-22.

Return to Summary Table.

Table 2-22. R19 Register Field Descriptions

Bit	Field	Type	Reset	Description
4	LOS_FDET_XO_INTR	R	0x0	LOL_FDET_XO Interrupt Bit is set when an edge of the correct polarity is detected on the LOL_FDET_XO interrupt source. The bit is cleared by writing a 0.
3	LOL_PLL2_INTR	R	0x0	LOL_PLL2 Interrupt Bit is set when an edge of the correct polarity is detected on the LOL_PLL2 interrupt source. The bit is cleared by writing a 0.
2	LOL_PLL1_INTR	R	0x0	LOL_PLL1 Interrupt Bit is set when an edge of the correct polarity is detected on the LOL_PLL1 interrupt source. The bit is cleared by writing a 0.
1	RESERVED	R	0x0	
0	LOS_XO_INTR	R	0x0	LOS_XO Interrupt Bit is set when an edge of the correct polarity is detected on the LOS_XO interrupt source. The bit is cleared by writing a 0.

2.21 R20 Register (Address = 0x14) [reset = 0x0]

R20 is shown in Table 2-23.

Return to Summary Table.

Table 2-23. R20 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	LOPL_DPLL_INTR	R	0x0	LOPL_DPLL Interrupt Bt is set when an edge of the correct polarity is detected on the LOPL_DPLL interrupt source. The bit is cleared by writing a 0.
6	LOFL_DPLL_INTR	R	0x0	LOFL_DPLL Interrupt Bit is set when an edge of the correct polarity is detected on the LOFL_DPLL interrupt source. The bit is cleared by writing a 0.
5	HIST_INTR	R	0x0	HIST Interrupt Bit is set when an edge of the correct polarity is detected on the HIST interrupt source. The bit is cleared by writing a 0.
4	HLDOVR_INTR	R	0x0	HLDOVR Interrupt Bit is set when an edge of the correct polarity is detected on the HLDOVR interrupt source. The bit is cleared by writing a 0.
3	REFSWITCH_INTR	R	0x0	REFSWITCH Interrupt Bit is set when an edge of the correct polarity is detected on the REFSWITCH interrupt source. The bit is cleared by writing a 0.
2	LOR_MISSCLK_INTR	R	0x0	LOR_MISSCLK Interrupt Bit is set when an edge of the correct polarity is detected on the LOR_MISSCLK interrupt source. The bit is cleared by writing a 0.
1	LOR_FREQ_INTR	R	0x0	LOR_FREQ Interrupt Bit is set when an edge of the correct polarity is detected on the LOR_FREQ interrupt source. The bit is cleared by writing a 0.
0	LOR_AMP_INTR	R	0x0	LOR_AMP Interrupt Bit is set when an edge of the correct polarity is detected on the LOR_AMP interrupt source. The bit is cleared by writing a 0.

2.22 R21 Register (Address = 0x15) [reset = 0x0]

R21 is shown in Table 2-24.

Return to Summary Table.

Table 2-24. R21 Register Field Descriptions

Bit	Field	Type	Reset	Description
1	INT_AND_OR	R/W	0x0	Interrupt Logical AND or OR Combination 0x0 = OR: Any un-masked interrupt flags can generate an interrupt. 0x1 = AND: All un-masked interrupt flags must be active in order to generate an interrupt.
0	INT_EN	R/W	0x0	Interrupt Enable

2.23 R22 Register (Address = 0x16) [reset = 0x0]

R22 is shown in Table 2-25.

Return to Summary Table.

Table 2-25. R22 Register Field Descriptions

Bit	Field	Type	Reset	Description
1	STAT1_POL	R/W	0x0	STATUS1 Output Polarity Defines the polarity of information presented on the STATUS1 output. If STAT1_POL is set to 1 then STATUS1 is active high, if STAT1_POL is 0 then STATUS1 is active low.
0	STAT0_POL	R/W	0x0	STATUS0 Output Polarity Defines the polarity of information presented on the STATUS0 output. If STAT0_POL is set to 1 then STATUS0 is active high, if STAT0_POL is 0then STATUS0 is active low.

2.24 R23 Register (Address = 0x17) [reset = 0x0]

R23 is shown in Table 2-26.

Return to Summary Table.

Table 2-26. R23 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH3_MUTE_LVL	R/W	0x0	Output 3 Mute Level See CH0_MUTE_LVL for description and bit settings.
5-4	CH2_MUTE_LVL	R/W	0x0	Output 2 Mute Level See CH0_MUTE_LVL for description and bit settings.
3-2	CH1_MUTE_LVL	R/W	0x0	Output 1 Mute Level See CH0_MUTE_LVL for description and bit settings.
1-0	CH0_MUTE_LVL	R/W	0x0	Output 0 Mute Level Determines the configuration of the Output Driver during mute. 0x0 = Bypass Mute (Normal Operation) 0x1 = For DIFF or HCSL mute to differential Vocm. For LVCMOS, P is Bypass Mute and N is Mute Low. 0x2 = For DIFF or HCSL mute to differntial High. For LVCMOS, P is Mute Low and N is Bypass Mute. 0x3 = For DIFF or HCSL mute to differential Low. For LVCMOS, P is Mute Low and N is Mute Low.

2.25 R24 Register (Address = 0x18) [reset = 0x0]

R24 is shown in Table 2-27.

Return to Summary Table.

Table 2-27. R24 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH7_MUTE_LVL	R/W	0x0	Output 7 Mute Level See CH0_MUTE_LVL for description and bit settings.
5-4	CH6_MUTE_LVL	R/W	0x0	Output 6 Mute Level See CH0_MUTE_LVL for description and bit settings.
3-2	CH5_MUTE_LVL	R/W	0x0	Output 5 Mute Level See CH0_MUTE_LVL for description and bit settings.
1-0	CH4_MUTE_LVL	R/W	0x0	Output 4 Mute Level See CH0_MUTE_LVL for description and bit settings.

2.26 R25 Register (Address = 0x19) [reset = 0xFF]

R25 is shown in Table 2-28.

Return to Summary Table.

Table 2-28. R25 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CH7_MUTE	R/W	0x1	Output 7 Mute Control
6	CH6_MUTE	R/W	0x1	Output 6 Mute Control
5	CH5_MUTE	R/W	0x1	Output 5 Mute Control
4	CH4_MUTE	R/W	0x1	Output 4 Mute Control
3	CH3_MUTE	R/W	0x1	Output 3 Mute Control
2	CH2_MUTE	R/W	0x1	Output 2 Mute Control
1	CH1_MUTE	R/W	0x1	Output 1 Mute Control
0	CH0_MUTE	R/W	0x1	Output 0 Mute Control

2.27 R26 Register (Address = 0x1A) [reset = 0x0]

R26 is shown in Table 2-29.

Return to Summary Table.

Table 2-29. R26 Register Field Descriptions

Bit	Field	Type	Reset	Description
1-0	XO_HTIMER	R/W	0x0	XO Input Hysteresis Timer Hysteresis Timer determines the time interval between reacting to successive changes on the XO oscillator status.

2.28 R27 Register (Address = 0x1B) [reset = 0x5]

R27 is shown in Table 2-30.

Return to Summary Table.

Table 2-30. R27 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	SPARE_NVMBASE1	R/W	0x0	Spare NVM register 1 located in Base
3-2	DETECT_MODE_XO	R/W	0x1	XO Single-ended Input Energy Detector Mode.
1-0	RESERVED	R/W	0x1	Reserved

2.29 R28 Register (Address = 0x1C) [reset = 0x5]

R28 is shown in Table 2-31.

Return to Summary Table.

Table 2-31. R28 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0x0	Reserved
3-2	DETECT_MODE_XO_DIFF	R/W	0x1	XO differential Input Energy Detector Mode Control. The DETECT_MODE_XO field determines the method for Energy Detection on the XO Input as follows. 0=Rising Slew Rate Detector 1=Rising and Falling Slew Rate Detector 2=Falling Slew Rate Detector 3=VIH/VIL Level Detector

Table 2-31. R28 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	LVL_SEL_XO_DIFF	R/W	0x1	XO Input Amplitude Detector Specifies the minimum differential input peak-to-peak swing to be qualified.

2.30 R29 Register (Address = 0x1D) [reset = 0x13]

R29 is shown in Table 2-32.

Return to Summary Table.

Table 2-32. R29 Register Field Descriptions

Bit	Field	Type	Reset	Description
4	MUTE_APLL2_LOCK	R/W	0x1	APLL2 mute enabled during PLL lock
3	RESERVED	R	0x0	
2	MUTE_DPLL_PHLOCK	R/W	0x0	DPLL mute enabled during phase lock
1	MUTE_DPLL_FRLOCK	R/W	0x1	DPLL mute enabled during DPLL lock
0	MUTE_APLL1_LOCK	R/W	0x1	APLL1 mute enabled during PLL lock

2.31 R30 Register (Address = 0x1E) [reset = 0x40]

R30 is shown in Table 2-33.

Return to Summary Table.

Table 2-33. R30 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	LDOTMRSCALE	R/W	0x2	LDO Timer Scale. The LDOTMRSCALE field allows all LDO startup times to be scaled as follows.0 = 0.25 1 = 0.5 2 = 1.0 3 = 2.0 4 = 4.0 5 to 7 = Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

2.32 R31 Register (Address = 0x1F) [reset = 0x0]

R31 is shown in Table 2-34.

Return to Summary Table.

Table 2-34. R31 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved

Table 2-34. R31 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RESERVED	R/W	0x0	Reserved

2.33 R32 Register (Address = 0x20) [reset = 0x44]

R32 is shown in Table 2-35.

Return to Summary Table.

Table 2-35. R32 Register Field Descriptions

Bit	Field	Type	Reset	Description
6-4	PLL2_LDO_TRIM	R/W	0x4	PLL2 MASH LDO Trim.
3	RESERVED	R	0x0	
2-0	PLL1_LDO_TRIM	R/W	0x4	PLL1 MASH LDO Trim.

2.34 R33 Register (Address = 0x21) [reset = 0x0]

R33 is shown in Table 2-36.

Return to Summary Table.

Table 2-36. R33 Register Field Descriptions

Bit	Field	Type	Reset	Description
6-4	RESERVED	R/W	0x0	Reserved
3-1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

2.35 R34 Register (Address = 0x22) [reset = 0x0]

R34 is shown in Table 2-37.

Return to Summary Table.

Table 2-37. R34 Register Field Descriptions

Bit	Field	Type	Reset	Description
6-4	RESERVED	R/W	0x0	Reserved
3-1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

2.36 R35 Register (Address = 0x23) [reset = 0x0]

R35 is shown in Table 2-38.

Return to Summary Table.

Table 2-38. R35 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VCO2LDOFASTCHRG	R/W	0x0	VCO2 LDO Fast Charge Control. Enabled by VCO2LDOFASTCHRGMAN. 1 = Fast Charging of the LDO Filter Cap enabled 0 = Fast Charging is disabled.
6	VCO2LDOFASTCHRGMAN	R/W	0x0	VCO2 LDO Fast Charge Manual Control Enable. 1 = The VCO2LDOFASTCHRG register bit can be used to force fast charging of the VCO2 LDO Filter CAP. 0 = The operation is automatic.
5	VCO2LDOHOLD	R/W	0x0	VCO2 LDO Hold Voltage Control. Enabled by VCO2LDOHOLDMAN. 1 = The VCO2 LDO Hold Voltage is enabled.

Table 2-38. R35 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	VCO2LDOHOLDMAN	R/W	0x0	VCO2 LDO Hold Voltage Manual Control Enable. 1 = The VCO2LDOHOLD register bit can be used to force a holding voltage on the output of the VCO2 LDO. 0 = The operation is automatic.
3	VCO1LDOFASTCHRG	R/W	0x0	VCO1 LDO Fast Charge Control. Enabled by VCO1LDOFASTCHRGMAN. 1 = Fast Charging of the LDO Filter Cap is enabled.
2	VCO1LDOFASTCHRGMAN	R/W	0x0	VCO1 LDO Fast Charge Manual Control Enable. 1 = The VCO1LDOFASTCHRG register bit can be used to force fast charging of the VCO1 LDO Filter CAP. 0 =The operation is automatic.
1	VCO1LDOHOLD	R/W	0x0	VCO1 LDO Hold Voltage Control. Enabled by VCO1LDOHOLDMAN. Enabled and Set to 1 = VCO1 LDO Hold Voltage Enabled and Clear to 0 = VCO1 LDO Hold Voltage Enabled
0	VCO1LDOHOLDMAN	R/W	0x0	VCO1 LDO Hold Voltage Manual Control Enable. If VCO1LDOHOLDMAN is set to 1 then the VCO1LDOHOLD register bit can be used to force a holding voltage on the output of the VCO1 LDO. If VCO1LDOHOLDMAN is 0 then the operation is automatic.

2.37 R36 Register (Address = 0x24) [reset = 0x0]

R36 is shown in Table 2-39.

Return to Summary Table.

Table 2-39. R36 Register Field Descriptions

Bit	Field	Type	Reset	Description
1	GPIO_STAT1_OUT	R/W	0x0	STAT1 Driver Type Output 0x0 = NMOS Open-drain driver 0x1 = LVCMOS driver
0	GPIO_STAT0_OUT	R/W	0x0	STAT0 Driver Type Output 0x0 = NMOS Open-drain driver 0x1 = LVCMOS driver

2.38 R37 Register (Address = 0x25) [reset = 0x4]

R37 is shown in Table 2-40.

Return to Summary Table.

Table 2-40. R37 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STAT0OPEND	R/W	0x0	STATUS0 Open Drain Enable. 0=NMOS open drain (external pull-up) 1=CMOS
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x1	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

2.39 R38 Register (Address = 0x26) [reset = 0x4]

R38 is shown in Table 2-41.

Return to Summary Table.

Table 2-41. R38 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STAT1OPEND	R/W	0x0	STATUS1 Open Drain Enable. 0=NMOS open drain (external pull-up) 1=CMOS
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x1	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

2.40 R39 Register (Address = 0x27) [reset = 0x0]

R39 is shown in Table 2-42.

Return to Summary Table.

Table 2-42. R39 Register Field Descriptions

Bit	Field	Type	Reset	Description
4	RESERVED	R/W	0x0	Reserved
3-2	RESERVED	R/W	0x0	Reserved
1	GPIO2_OUT	R/W	0x0	GPIO2 Driver Type GPIO2 0x0 = NMOS Open-drain driver 0x1 = LVCMOS driver
0	APLL1_DEN_MODE	R/W	0x0	APLL1 denominator mode. 0: Fixed 40-bit APLL1 denominator (chosen if DPLL is enabled) 1: Programmable 24-bit numerator and 24-bit denominator for APLL1 (chosen only in free-running mode where DPLL is powered-down)

2.41 R40 Register (Address = 0x28) [reset = 0x0]

R40 is shown in Table 2-43.

Return to Summary Table.

Table 2-43. R40 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	SPARE_NVMBASE2_11:8	R/W	0x0	Bits 11:8 of SPARE_NVMBASE2
3	SECREF_DC_MODE	R/W	0x0	SECREF DC coupled input buffer mode. 0: AC coupled SECREF 1: DC coupled SECREF
2	PRIREF_DC_MODE	R/W	0x0	PRIREF DC coupled input buffer mode. 0: AC coupled PRIREF 1: DC coupled PRIREF
1	RESERVED	R/W	0x0	Reserved

Table 2-43. R40 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	APLL2_DEN_MODE	R/W	0x0	APLL2 denominator mode. 0: Fixed 24-bit APLL2 denominator 1: Programmable 24-bit APLL2 denominator

2.42 R41 Register (Address = 0x29) [reset = 0x0]

R41 is shown in Table 2-44.

Return to Summary Table.

Table 2-44. R41 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SPARE_NVMBASE2	R/W	0x0	Spare NVM register 2 located in Base

2.43 R42 Register (Address = 0x2A) [reset = 0x1]

R42 is shown in Table 2-45.

Return to Summary Table.

Table 2-45. R42 Register Field Descriptions

Bit	Field	Type	Reset	Description
4	OSCIN_DBLR_EN	R/W	0x0	Enable OSCIn doubler
3	XO_FDET_BYP	R/W	0x0	XO Frequency Detector Bypass If bypassed, the XO detector status is ignored and the XO input is considered valid by the PLL control state machines
2	XO_DETECT_BYP	R/W	0x0	XO Amplitude Detector Bypass If bypassed, the XO input is considered to be valid by the PLL control state machines. XO_DETECT_BYP bit has no effect on the Interrupt register or status outputs.
1	RESERVED	R	0x0	
0	XO_BUFSEL	R/W	0x1	XO Input Buffer Enable

2.44 R43 Register (Address = 0x2B) [reset = 0x82]

R43 is shown in Table 2-46.

Return to Summary Table.

Table 2-46. R43 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	XO_DIFF_BUFGAIN	R/W	0x1	RESERVED. Always set to 1.
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x1	Reserved
0	RESERVED	R/W	0x0	Reserved

2.45 R44 Register (Address = 0x2C) [reset = 0x1]

R44 is shown in Table 2-47.

Return to Summary Table.

Table 2-47. R44 Register Field Descriptions

Bit	Field	Type	Reset	Description
4-0	OSCIN_RDIV	R/W	0x1	Oscillator Input Divider

2.46 R45 Register (Address = 0x2D) [reset = 0x3]

R45 is shown in Table 2-48.

Return to Summary Table.

Table 2-48. R45 Register Field Descriptions

Bit	Field	Type	Reset	Description
4	RESERVED	R/W	0x0	Reserved
3	SECREF_CMOS_SLEW	R/W	0x0	SECREF input buffer slew rate 0x0 = Select Amplitude Detector Mode 0x1 = Select CMOS Amplitude Detector Mode
2	PRIREF_CMOS_SLEW	R/W	0x0	PRIREF input buffer slew rate 0x0 = Select Amplitude Detector Mode 0x1 = Select CMOS Amplitude Detector Mode
1	SECREF_BUF_MODE	R/W	0x1	SECREF buffer mode 0: set input hysteresis to 50 mV for AC coupled SECREF, or enable hysteresis for DC coupled SECREF 1: set input hysteresis to 200 mV for AC coupled SECREF, or disable hysteresis for DC coupled SECREF
0	PRIREF_BUF_MODE	R/W	0x1	PRIREF buffer mode 0: set input hysteresis to 50 mV for AC coupled PRIREF, or enable hysteresis for DC coupled PRIREF 1: set input hysteresis to 200 mV for AC coupled PRIREF, or disable hysteresis for DC coupled PRIREF

2.47 R46 Register (Address = 0x2E) [reset = 0x0]

R46 is shown in Table 2-49.

Return to Summary Table.

Table 2-49. R46 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

2.48 R47 Register (Address = 0x2F) [reset = 0x0]

R47 is shown in Table 2-50.

Return to Summary Table.

Table 2-50. R47 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL2_RCLK_SEL	R/W	0x0	PLL2 Reference clock selection 0x0 = VCO1 - Cascaded Mode 0x1 = XO
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R	0x0	
2	RESERVED	RN/WA	0x0	Reserved
1	RESERVED	RN/WA	0x0	Reserved
0	RESERVED	RN/WA	0x0	Reserved

2.49 R48 Register (Address = 0x30) [reset = 0xA]

R48 is shown in Table 2-51.

Return to Summary Table.

Table 2-51. R48 Register Field Descriptions

Bit	Field	Type	Reset	Description
6-0	STAT0_SEL	R/W	0xA	STATUS0 Indicator Signal Select The output pin state of 1 indicates the status condition is true. 0x00 = XO Input Loss of Signal (LOS) 0x01 = Reserved 0x02 = Reserved 0x03 = PLL1 Digital Lock Detect (DLD) 0x04 = PLL1 VCO Calibration Active 0x05 = PLL1 N Divider, div-by-2 0x06 = PLL2 Digital Lock Detect (DLD) 0x07 = PLL2 VCO Calibration Active 0x08 = PLL2 N Divider, div-by-2 0x09 = EEPROM Active 0x0A = Interrupt (INTR) 0x0B = Reserved 0x0C = DPLL Phase Locked (opposite of LOPL - Loss of Phase Lock) 0x0D = PRIREF Monitor Divider Output, div-by-2 0x0E = SECREF Monitor Divider Output, div-by-2 0x0F = PLL2 R Divider, div-by-2 0x10 = Reserved 0x11 = PRIREF Amplitude Monitor Fault 0x12 = SECREF Amplitude Monitor Fault 0x13 = Reserved 0x14 = Reserved 0x15 = PRIREF Frequency Monitor Fault 0x16 = SECREF Frequency Monitor Fault 0x17 = Reserved 0x18 = Reserved 0x19 = PRIREF Missing or Early Pulse Monitor Fault 0x1A = SECREF Missing or Early Pulse Monitor Fault 0x1B = Reserved 0x1C = Reserved 0x1D = PRIREF Validation Timer Active 0x1E = SECREF Validation Timer Active 0x1F = Reserved 0x20 = Reserved 0x21 = Reserved 0x22 = Reserved 0x23 = Reserved

Table 2-51. R48 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x24 = Reserved 0x25 = PRIREF Phase Validation Monitor Fault 0x26 = SECREF Phase Validation Monitor Fault 0x27 = Reserved 0x28 = Reserved 0x29 = PLL1 Locked (opposite of LOL - Loss of Lock) 0x2A = PLL2 Locked (opposite of LOL - Loss of Lock) 0x2B = Reserved 0x2C = Reserved 0x2D = Reserved 0x2E = Reserved 0x2F = Reserved 0x30 = Reserved 0x31 = Reserved 0x32 = Reserved 0x33 = Reserved 0x34 = Reserved 0x35 = Reserved 0x36 = Reserved 0x37 = Reserved 0x38 = Reserved 0x39 = Reserved 0x3A = Reserved 0x3B = Reserved 0x3C = Reserved 0x3D = Reserved 0x3E = Reserved 0x3F = Reserved 0x40 = DPLL R Divider, div-by-2 0x41 = DPLL FB Divider, div-by-2 0x42 = Reserved 0x43 = Reserved 0x44 = Reserved 0x45 = Reserved 0x46 = DPLL PRIREF Selected 0x47 = DPLL SECREF Selected 0x48 = Reserved 0x49 = Reserved 0x4A = DPLL Holdover Active

Table 2-51. R48 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x4B = DPLL Reference Switchover Event 0x4C = Reserved 0x4D = DPLL Tuning History Update 0x4E = DPLL Fast Lock Active 0x4F = Reserved 0x50 = DPLL Frequency Locked (opposite of LOFL - Loss of Frequency Lock) 0x51 = Reserved 0x52 = Reserved 0x53 = Reserved 0x54 = Reserved 0x55 = Reserved 0x56 = Reserved 0x57 = Reserved 0x58 = Reserved 0x59 = Reserved 0x5A = Reserved

2.50 R49 Register (Address = 0x31) [reset = 0xA]

R49 is shown in Table 2-52.

Return to Summary Table.

Table 2-52. R49 Register Field Descriptions

Bit	Field	Type	Reset	Description
6-0	STAT1_SEL	R/W	0xA	STATUS1 Indicator Signal Select See STAT0_SEL for status signal and bit settings.

2.51 R50 Register (Address = 0x32) [reset = 0x0]

R50 is shown in Table 2-53.

Return to Summary Table.

Table 2-53. R50 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO_FDEV_EN	R/W	0x0	Enable DCO Frequency When enabled, a rising edge on these pins will update the DCO frequency accordingly.
6	RESERVED	R	0x0	
5	CH7_PD	R/W	0x0	Channel 7 Power-down When CH7_PD is 1 the regulator that supplies the divider and drivers for OUT7 will be disabled.
4	CH6_PD	R/W	0x0	Channel 6 Power-down When CH6_PD is 1 the regulator that supplies the divider and drivers for OUT6 will be disabled.

Table 2-53. R50 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	CH5_PD	R/W	0x0	Channel 5 Power-down When CH5_PD is 1 the regulator that supplies the divider and drivers for OUT5 will be disabled.
2	CH4_PD	R/W	0x0	Channel 4 Power-down When CH4_PD is 1 the regulator that supplies the divider and drivers for OUT4 will be disabled.
1	CH2_3_PD	R/W	0x0	Channel 2 and 3 Power-down When CH2_3_PD is 1 the regulator that supplies the divider and drivers for OUT2 and OUT3 will be disabled.
0	CH0_1_PD	R/W	0x0	Channel 0 and 1 Power-down When CH0_1_PD is 1 the regulator that supplies the divider and drivers for OUT0 and OUT1 will be disabled.

2.52 R51 Register (Address = 0x33) [reset = 0x18]

R51 is shown in Table 2-54.

Return to Summary Table.

Table 2-54. R51 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH0_1_MUX	R/W	0x0	Channel 0 and 1 Output Mux Selects frequency source for OUT0 and OUT1. 0x0 = APLL1 P1 0x1 = APLL1 P1 Inverted 0x2 = APLL2 P1 0x3 = APLL2 P2
5-4	RESERVED	R/W	0x1	Reserved
3-2	RESERVED	R/W	0x2	Reserved
1-0	RESERVED	R/W	0x0	Reserved

2.53 R52 Register (Address = 0x34) [reset = 0x18]

R52 is shown in Table 2-55.

Return to Summary Table.

Table 2-55. R52 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-4	RESERVED	R/W	0x1	Reserved
3-2	RESERVED	R/W	0x2	Reserved
1-0	RESERVED	R/W	0x0	Reserved

2.54 R53 Register (Address = 0x35) [reset = 0x7]

R53 is shown in Table 2-56.

Return to Summary Table.

Table 2-56. R53 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT0_1_DIV	R/W	0x7	Channel 0 and Channel 1 Output Divider This is an 8-bit divider. The valid values for OUT0_1_DIV range from 1 to 256. 0x05 THROUGH 0XFF = Div by register value + 1 0x00 = Reserved 0x01 = Div by 2 0x02 = Div by 3 0x03 = Div by 4 0x04 = Div by 5

2.55 R54 Register (Address = 0x36) [reset = 0x18]

R54 is shown in Table 2-57.

Return to Summary Table.

Table 2-57. R54 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH2_3_MUX	R/W	0x0	Channel 2 and 3 Output Mux Selects frequency source for OUT2 and OUT3. See CH0_1_MUX for bit settings.
5-4	RESERVED	R/W	0x1	Reserved
3-2	RESERVED	R/W	0x2	Reserved
1-0	RESERVED	R/W	0x0	Reserved

2.56 R55 Register (Address = 0x37) [reset = 0x18]

R55 is shown in Table 2-58.

Return to Summary Table.

Table 2-58. R55 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-4	RESERVED	R/W	0x1	Reserved
3-2	RESERVED	R/W	0x2	Reserved
1-0	RESERVED	R/W	0x0	Reserved

2.57 R56 Register (Address = 0x38) [reset = 0x7]

R56 is shown in Table 2-59.

Return to Summary Table.

Table 2-59. R56 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT2_3_DIV	R/W	0x7	Channel 2 and Channel 3 Output Divider See OUT0_1_DIV for description and bit settings.

2.58 R57 Register (Address = 0x39) [reset = 0x18]

R57 is shown in Table 2-60.

Return to Summary Table.

Table 2-60. R57 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH4_MUX	R/W	0x0	Channel 4 Output Mux Selects frequency source for OUT4. See CH0_1_MUX for bit settings.
5-4	RESERVED	R/W	0x1	Reserved
3-2	RESERVED	R/W	0x2	Reserved
1-0	RESERVED	R/W	0x0	Reserved

2.59 R58 Register (Address = 0x3A) [reset = 0x7]

R58 is shown in Table 2-61.

Return to Summary Table.

Table 2-61. R58 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT4_DIV	R/W	0x7	Channel 4 Output Divider See OUT0_1_DIV for description and bit settings.

2.60 R59 Register (Address = 0x3B) [reset = 0x18]

R59 is shown in Table 2-62.

Return to Summary Table.

Table 2-62. R59 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH5_MUX	R/W	0x0	Channel 5 Output Mux Selects frequency source for OUT5. See CH0_1_MUX for bit settings.
5-4	RESERVED	R/W	0x1	Reserved
3-2	RESERVED	R/W	0x2	Reserved
1-0	RESERVED	R/W	0x0	Reserved

2.61 R60 Register (Address = 0x3C) [reset = 0x7]

R60 is shown in Table 2-63.

Return to Summary Table.

Table 2-63. R60 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT5_DIV	R/W	0x7	Channel 5 Output Divider See OUT0_1_DIV for description and bit settings.

2.62 R61 Register (Address = 0x3D) [reset = 0x18]

R61 is shown in Table 2-64.

Return to Summary Table.

Table 2-64. R61 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH6_MUX	R/W	0x0	Channel 6 Output Mux Selects frequency source for OUT6. See CH0_1_MUX for bit settings.

Table 2-64. R61 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	RESERVED	R/W	0x1	Reserved
3-2	RESERVED	R/W	0x2	Reserved
1-0	RESERVED	R/W	0x0	Reserved

2.63 R62 Register (Address = 0x3E) [reset = 0x7]

R62 is shown in Table 2-65.

Return to Summary Table.

Table 2-65. R62 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT6_DIV	R/W	0x7	Channel 6 Output Divider See OUT0_1_DIV for description and bit settings.

2.64 R63 Register (Address = 0x3F) [reset = 0x18]

R63 is shown in Table 2-66.

Return to Summary Table.

Table 2-66. R63 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CH7_MUX	R/W	0x0	Channel 7 Output Mux Selects frequency source for OUT7. See CH0_1_MUX for bit settings.
5-4	RESERVED	R/W	0x1	Reserved
3-2	RESERVED	R/W	0x2	Reserved
1-0	RESERVED	R/W	0x0	Reserved

2.65 R64 Register (Address = 0x40) [reset = 0x0]

R64 is shown in Table 2-67.

Return to Summary Table.

Table 2-67. R64 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT7_STG2_DIV_23:16	R/W	0x0	Bits 23:16 of OUT7_STG2_DIV

2.66 R65 Register (Address = 0x41) [reset = 0x0]

R65 is shown in Table 2-68.

Return to Summary Table.

Table 2-68. R65 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT7_STG2_DIV_15:8	R/W	0x0	Bits 15:8 of OUT7_STG2_DIV

2.67 R66 Register (Address = 0x42) [reset = 0x0]

R66 is shown in Table 2-69.

Return to Summary Table.

Table 2-69. R66 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT7_STG2_DIV	R/W	0x0	Channel 7 Stage Two Output Divider OD2 = OUT7_STG2_DIV + 1If OD2 > 1, then ODout7 must be ≥ 6. Total output 7 divide value = OD2 * ODout7.

2.68 R67 Register (Address = 0x43) [reset = 0x7]

R67 is shown in Table 2-70.

Return to Summary Table.

Table 2-70. R67 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUT7_DIV	R/W	0x7	Channel 7 Output Divider This is an 8-bit divider. The valid values for OUT7_DIV range from 1 to 255. ODOUT7 = OUT7_DIV + 1. If OD2 > 1, then total output 7 divide value = OD2 * ODout7 where OD2 is OUT7 secondary output divider value. Note: 0x00 is disabled.

2.69 R68 Register (Address = 0x44) [reset = 0xFF]

R68 is shown in Table 2-71.

Return to Summary Table.

Table 2-71. R68 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x1	Reserved
6	RESERVED	R/W	0x1	Reserved
5	RESERVED	R/W	0x1	Reserved
4	RESERVED	R/W	0x1	Reserved
3-0	PLL1_CP_BAW	R/W	0xF	APLL1 Charge Pump Current Gain PLL1_CP_BAW ranges from 0 to 15. Gain = PLL1_CP_BAW x 100 µA.

2.70 R69 Register (Address = 0x45) [reset = 0x0]

R69 is shown in Table 2-72.

Return to Summary Table.

Table 2-72. R69 Register Field Descriptions

Bit	Field	Type	Reset	Description
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

2.71 R70 Register (Address = 0x46) [reset = 0x0]

R70 is shown in Table 2-73.

Return to Summary Table.

Table 2-73. R70 Register Field Descriptions

Bit	Field	Type	Reset	Description
2	PLL2_P2_SYNC_EN	R/W	0x0	Enable PLL2 P2 divider channel synchronization
1	PLL2_P1_SYNC_EN	R/W	0x0	Enable PLL2 P1 divider channel synchronization
0	PLL1_P1_SYNC_EN	R/W	0x0	Enable PLL1 P1 divider channel synchronization

2.72 R71 Register (Address = 0x47) [reset = 0x0]

R71 is shown in Table 2-74.

Return to Summary Table.

Table 2-74. R71 Register Field Descriptions

Bit	Field	Type	Reset	Description
5	CH7_SYNC_EN	R/W	0x0	Enable Channel 7 output synchronization
4	CH6_SYNC_EN	R/W	0x0	Enable Channel 6 output synchronization
3	CH5_SYNC_EN	R/W	0x0	Enable Channel 5 output synchronization
2	CH4_SYNC_EN	R/W	0x0	Enable Channel 4 output synchronization
1	CH2_3_SYNC_EN	R/W	0x0	Enable Channels 2 and 3 output synchronization
0	CH0_1_SYNC_EN	R/W	0x0	Enable Channels 0 and 1 output synchronization

2.73 R72 Register (Address = 0x48) [reset = 0x0]

R72 is shown in Table 2-75.

Return to Summary Table.

Table 2-75. R72 Register Field Descriptions

Bit	Field	Type	Reset	Description
5	CH7_ACT	R	0x0	Channel 7 Output Active flag Reads 1 when output channel is powered-up and active.
4	CH6_ACT	R	0x0	Channel 6 Output Active flag Reads 1 when output channel is powered-up and active.
3	CH5_ACT	R	0x0	Channel 45 Output Active flag Reads 1 when output channel is powered-up and active.
2	CH4_ACT	R	0x0	Channel 23 Output Active flag Reads 1 when output channel is powered-up and active.
1	CH2_3_ACT	R	0x0	Channel 1 Output Active flag Reads 1 when output channel is powered-up and active.
0	CH0_1_ACT	R	0x0	Channel 0 Output Active flag Reads 1 when output channel is powered-up and active.

2.74 R73 Register (Address = 0x49) [reset = 0x0]

R73 is shown in Table 2-76.

Return to Summary Table.

Table 2-76. R73 Register Field Descriptions

Bit	Field	Type	Reset	Description
1	REF_BYPASS_EN	R/W	0x0	Reference Bypass Selection Enable When ref_bypass_en=1, the reference selected by ref_bypass_sel will be routed to the channel outputs instead of VCO1.

Table 2-76. R73 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	REF_BYPASS_SEL	R/W	0x0	Reference Bypass Selection Register When ref_bypass_en=1, ref_bypass_sel will select which reference input to drive channel outputs.

2.75 R74 Register (Address = 0x4A) [reset = 0x0]

R74 is shown in Table 2-77.

Return to Summary Table.

Table 2-77. R74 Register Field Descriptions

Bit	Field	Type	Reset	Description
0	PLL1_PDN	R/W	0x0	PLL1 Power down The PLL1_PDN bit determines whether PLL1 is automatically enabled and calibrated after a hardware reset. 0x0 = PLL1 Enabled 0x1 = PLL1 Disabled

2.76 R75 Register (Address = 0x4B) [reset = 0x2]

R75 is shown in Table 2-78.

Return to Summary Table.

Table 2-78. R75 Register Field Descriptions

Bit	Field	Type	Reset	Description
2	PLL1_VM_BYP	R/W	0x0	PLL1 Vtune Monitor Bypass
1-0	PLL1_CP	R/W	0x2	PLL1 Charge Pump Gain

2.77 R76 Register (Address = 0x4C) [reset = 0x2]

R76 is shown in Table 2-79.

Return to Summary Table.

Table 2-79. R76 Register Field Descriptions

Bit	Field	Type	Reset	Description
2-0	PLL1_P1	R/W	0x2	PLL1 Post-Divider1 Note: A RESET is required after changing Divider values.

2.78 R77 Register (Address = 0x4D) [reset = 0x3]

R77 is shown in Table 2-80.

Return to Summary Table.

Table 2-80. R77 Register Field Descriptions

Bit	Field	Type	Reset	Description
3-0	PLL1_DISABLE_3RD4TH	R/W	0x3	PLL1 Loop Filter Settings

2.79 R78 Register (Address = 0x4E) [reset = 0x0]

R78 is shown in Table 2-81.

Return to Summary Table.

Table 2-81. R78 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_RBLEED_CP	R/W	0x0	PLL1 Bleed resistor selection

2.80 R79 Register (Address = 0x4F) [reset = 0x10]

R79 is shown in Table 2-82.

Return to Summary Table.

Table 2-82. R79 Register Field Descriptions

Bit	Field	Type	Reset	Description
5	RESERVED	R/W	0x0	Reserved
4	BAW_LOCKDET_EN	R/W	0x1	BAW Lock Detect Enable
3-2	PLL1_CLSDWAIT	R/W	0x0	Closed Loop Wait Period VCO calibration time per step (up to 7 steps).
1-0	PLL1_VCOWAIT	R/W	0x0	VCO Wait Period Timeout counter before starting VCO calibration.

2.81 R80 Register (Address = 0x50) [reset = 0x0]

R80 is shown in Table 2-83.

Return to Summary Table.

Table 2-83. R80 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BAW_LOCK	R	0x0	BAW Lock Detect Status 0x0 = Unlocked 0x1 = Locked
6-0	BAW_LOCK_PPM_MAX_14:8	R/W	0x0	BAW VCO Lock Detection

2.82 R81 Register (Address = 0x51) [reset = 0x0]

R81 is shown in Table 2-84.

Return to Summary Table.

Table 2-84. R81 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_LOCK_PPM_MAX	R/W	0x0	BAW VCO Lock Detection

2.83 R82 Register (Address = 0x52) [reset = 0x0]

R82 is shown in Table 2-85.

Return to Summary Table.

Table 2-85. R82 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-0	BAW_LOCK_CNTSTRT_29:24	R/W	0x0	BAW VCO Lock Detection

2.84 R83 Register (Address = 0x53) [reset = 0x0]

R83 is shown in Table 2-86.

Return to Summary Table.

Table 2-86. R83 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_LOCK_CNTSTRT_23:16	R/W	0x0	BAW VCO Lock Detection

2.85 R84 Register (Address = 0x54) [reset = 0x0]

R84 is shown in Table 2-87.

Return to Summary Table.

Table 2-87. R84 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_LOCK_CNTSTRT_15:8	R/W	0x0	BAW VCO Lock Detection

2.86 R85 Register (Address = 0x55) [reset = 0x0]

R85 is shown in Table 2-88.

Return to Summary Table.

Table 2-88. R85 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_LOCK_CNTSTRT	R/W	0x0	BAW VCO Lock Detection

2.87 R86 Register (Address = 0x56) [reset = 0x0]

R86 is shown in Table 2-89.

Return to Summary Table.

Table 2-89. R86 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-0	BAW_LOCK_VCO_CNTSTRT_29:24	R/W	0x0	BAW VCO Lock Detection

2.88 R87 Register (Address = 0x57) [reset = 0x0]

R87 is shown in Table 2-90.

Return to Summary Table.

Table 2-90. R87 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_LOCK_VCO_CNTSTRT_23:16	R/W	0x0	BAW VCO Lock Detection

2.89 R88 Register (Address = 0x58) [reset = 0x0]

R88 is shown in Table 2-91.

Return to Summary Table.

Table 2-91. R88 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_LOCK_VCO_CNTSTRT_15:8	R/W	0x0	BAW VCO Lock Detection

2.90 R89 Register (Address = 0x59) [reset = 0x0]

R89 is shown in Table 2-92.

Return to Summary Table.

Table 2-92. R89 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_LOCK_VCO_CNTSTRT	R/W	0x0	BAW VCO Lock Detection

2.91 R90 Register (Address = 0x5A) [reset = 0x0]

R90 is shown in Table 2-93.

Return to Summary Table.

Table 2-93. R90 Register Field Descriptions

Bit	Field	Type	Reset	Description
6-0	BAW_UNLK_PPM_MAX_14:8	R/W	0x0	BAW VCO Unlock Detection

2.92 R91 Register (Address = 0x5B) [reset = 0x0]

R91 is shown in Table 2-94.

Return to Summary Table.

Table 2-94. R91 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_UNLK_PPM_MAX	R/W	0x0	BAW VCO Unlock Detection

2.93 R92 Register (Address = 0x5C) [reset = 0x0]

R92 is shown in Table 2-95.

Return to Summary Table.

Table 2-95. R92 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-0	BAW_UNLK_CNTSTRT_29:24	R/W	0x0	BAW VCO Unlock Detection

2.94 R93 Register (Address = 0x5D) [reset = 0x0]

R93 is shown in Table 2-96.

Return to Summary Table.

Table 2-96. R93 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_UNLK_CNTSTRT_23:16	R/W	0x0	BAW VCO Unlock Detection

2.95 R94 Register (Address = 0x5E) [reset = 0x0]

R94 is shown in Table 2-97.

Return to Summary Table.

Table 2-97. R94 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_UNLK_CNTSTRT_15:8	R/W	0x0	BAW VCO Unlock Detection

2.96 R95 Register (Address = 0x5F) [reset = 0x0]

R95 is shown in Table 2-98.

Return to Summary Table.

Table 2-98. R95 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_UNLK_CNTSTRT	R/W	0x0	BAW VCO Unlock Detection

2.97 R96 Register (Address = 0x60) [reset = 0x0]

R96 is shown in Table 2-99.

Return to Summary Table.

Table 2-99. R96 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-0	BAW_UNLK_VCO_CNTSTRT_29:24	R/W	0x0	BAW VCO Unlock Detection

2.98 R97 Register (Address = 0x61) [reset = 0x0]

R97 is shown in Table 2-100.

Return to Summary Table.

Table 2-100. R97 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_UNLK_VCO_CNTSTRT_23:16	R/W	0x0	BAW VCO Unlock Detection

2.99 R98 Register (Address = 0x62) [reset = 0x0]

R98 is shown in Table 2-101.

Return to Summary Table.

Table 2-101. R98 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_UNLK_VCO_CNTSTRT_15:8	R/W	0x0	BAW VCO Unlock Detection

2.100 R99 Register (Address = 0x63) [reset = 0x0]

R99 is shown in Table 2-102.

Return to Summary Table.

Table 2-102. R99 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BAW_UNLK_VCO_CNTSTRT	R/W	0x0	BAW VCO Unlock Detection

2.101 R100 Register (Address = 0x64) [reset = 0x1]

R100 is shown in Table 2-103.

Return to Summary Table.

Table 2-103. R100 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	PLL2_RDIV_SEC	R/W	0x0	APLL2 secondary reference divider in cascaded APLL2 mode Divider value ranges from 1-32. Divider value = PLL2_RDIV_SEC + 1.
2-1	PLL2_RDIV_PRE	R/W	0x0	APLL2 primary reference divider in cascaded APLL2 mode
0	PLL2_PDN	R/W	0x1	PLL2 Power down The PLL2_PDN bit determines whether PLL2 is automatically enabled and calibrated after a hardware reset. 0x0 = PLL2 Enabled 0x1 = PLL2 Disabled

2.102 R101 Register (Address = 0x65) [reset = 0x2]

R101 is shown in Table 2-104.

Return to Summary Table.

Table 2-104. R101 Register Field Descriptions

Bit	Field	Type	Reset	Description
2	PLL2_VM_BYP	R/W	0x0	PLL2 Vtune Monitor Bypass
1-0	PLL2_CP	R/W	0x2	PLL2 Charge Pump Gain 0x0 = 1.6 mA 0x1 = 3.2 mA 0x2 = 4.8 mA 0x3 = 6.4 mA

2.103 R102 Register (Address = 0x66) [reset = 0x22]

R102 is shown in Table 2-105.

Return to Summary Table.

Table 2-105. R102 Register Field Descriptions

Bit	Field	Type	Reset	Description
6-4	PLL2_P2	R/W	0x2	PLL2 Post-Divider2 Note: A RESET is required after changing Divider values. See PLL2_P1 for bit settings.
3	RESERVED	R	0x0	
2-0	PLL2_P1	R/W	0x2	PLL2 Post-Divider1 Note: A RESET is required after changing Divider values. 0x0 = Invalid 0x1 = 2 0x2 = 3 0x3 = 4 0x4 = 5 0x5 = 6 0x6 = 7 0x7 = Invalid

2.104 R103 Register (Address = 0x67) [reset = 0x3]

R103 is shown in Table 2-106.

Return to Summary Table.

Table 2-106. R103 Register Field Descriptions

Bit	Field	Type	Reset	Description
3-0	PLL2_DISABLE_3RD4TH	R/W	0x3	PLL2 Loop Filter Settings

2.105 R104 Register (Address = 0x68) [reset = 0x0]

R104 is shown in Table 2-107.

Return to Summary Table.

Table 2-107. R104 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-0	PLL2_RBLEED_CP	R/W	0x0	PLL2 Bleed resistor selection (Ω) 0x0 = Open (high impedance) 0x1 = 23713.2 0x2 = 11875.2 0x3 = 7915.62 0x4 = 5843.79 0x5 = 4753.58 0x6 = 3963.08 0x7 = 3393.52 0x8 = 2970.14 0x9 = 2638.54 0xA = 2375.04 0xB = 2158.91 0xC = 1980.99 0xD = 1827.03 0xE = 1696.76 0xF = 1584.26 0x10 = 1486.55 0x11 = 1397.73 0x12 = 1320.66 0x13 = 1249.6 0x14 = 1187.43 0x15 = 1131.17 0x16 = 1077.88 0x17 = 1033.47 0x18 = 991.03 0x19 = 950.53 0x1A = 913.52 0x1B = 879.47 0x1C = 848.38 0x1D = 818.77 0x1E = 792.13 0x1F = 766.96

2.106 R105 Register (Address = 0x69) [reset = 0x0]

R105 is shown in Table 2-108.

Return to Summary Table.

Table 2-108. R105 Register Field Descriptions

Bit	Field	Type	Reset	Description
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R	0x0	
3-2	PLL2_CLSDWAIT	R/W	0x0	Closed Loop Wait Period VCO calibration time per step (up to 7 steps). 0x0 = 0.3 ms 0x1 = 3 ms 0x2 = 30 ms 0x3 = 300 ms
1-0	PLL2_VCOWAIT	R/W	0x0	VCO Wait Period Timeout counter before starting VCO calibration.

2.107 R106 Register (Address = 0x6A) [reset = 0x0]

R106 is shown in Table 2-109.

Return to Summary Table.

Table 2-109. R106 Register Field Descriptions

Bit	Field	Type	Reset	Description
3-0	PLL1_NDLYDIV_11:8	R/W	0x0	Bits 11:8 of PLL1_NDLYDIV

2.108 R107 Register (Address = 0x6B) [reset = 0x64]

R107 is shown in Table 2-110.

Return to Summary Table.

Table 2-110. R107 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NDLYDIV	R/W	0x64	PLL1 N Delay Divider

2.109 R108 Register (Address = 0x6C) [reset = 0x0]

R108 is shown in Table 2-111.

Return to Summary Table.

Table 2-111. R108 Register Field Descriptions

Bit	Field	Type	Reset	Description
3-0	PLL1_NDIV_11:8	R/W	0x0	Bits 11:8 of PLL1_NDIV

2.110 R109 Register (Address = 0x6D) [reset = 0x64]

R109 is shown in Table 2-112.

Return to Summary Table.

Table 2-112. R109 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NDIV	R/W	0x64	PLL1 N Divider

2.111 R110 Register (Address = 0x6E) [reset = 0x0]

R110 is shown in Table 2-113.

Return to Summary Table.

Table 2-113. R110 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_39:32	R/W	0x0	1. If APLL1 has 40-bit fixed denominator, then this register is APLL1 numerator [39:32]. 2. If APLL1 has 24-bit programmable denominator, then this register is APLL1 numerator [15:8].

2.112 R111 Register (Address = 0x6F) [reset = 0x0]

R111 is shown in Table 2-114.

Return to Summary Table.

Table 2-114. R111 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_31:24	R/W	0x0	1. If APLL1 has 40-bit fixed denominator, then this register is APLL1 numerator [31:24]. 2. If APLL1 has 24-bit programmable denominator, then this register is APLL1 numerator [7:0].

2.113 R112 Register (Address = 0x70) [reset = 0x0]

R112 is shown in Table 2-115.

Return to Summary Table.

Table 2-115. R112 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_23:16	R/W	0x0	1. If APLL1 has 40-bit fixed denominator, then this register is APLL1 numerator [23:16]. 2. If APLL1 has 24-bit programmable denominator, then this register is APLL1 denominator [23:16].

2.114 R113 Register (Address = 0x71) [reset = 0x0]

R113 is shown in Table 2-116.

Return to Summary Table.

Table 2-116. R113 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_15:8	R/W	0x0	1. If APLL1 has 40-bit fixed denominator, then this register is APLL1 numerator [15:8]. 2. If APLL1 has 24-bit programmable denominator, then this register is APLL1 denominator [15:8].

2.115 R114 Register (Address = 0x72) [reset = 0x0]

R114 is shown in Table 2-117.

Return to Summary Table.

Table 2-117. R114 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM	R/W	0x0	1. If APLL1 has 40-bit fixed denominator, then this register is APLL1 numerator [7:0]. 2. If APLL1 has 24-bit programmable denominator, then this register is APLL1 denominator [7:0].

2.116 R115 Register (Address = 0x73) [reset = 0x0]

R115 is shown in Table 2-118.

Return to Summary Table.

Table 2-118. R115 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL1_DUAL_PH_EN	R/W	0x0	PLL1 DUAL PHASE functionality on the feedback path enabled
6	PLL1_MASHSEED1	R/W	0x0	Mash Engine seed for second stage
5	PLL1_MASHSEED0	R/W	0x0	Mash Engine seed for first stage
4-3	PLL1_DTHRMODE	R/W	0x0	APLL1 SDM Dither mode 0x0 = Weak 0x1 = Medium 0x2 = Strong 0x3 = Disabled
2-0	PLL1_ORDER	R/W	0x0	APLL1 SDM Order 0x0 = Integer mode 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th

2.117 R116 Register (Address = 0x74) [reset = 0x1]

R116 is shown in Table 2-119.

Return to Summary Table.

Table 2-119. R116 Register Field Descriptions

Bit	Field	Type	Reset	Description
2	PLL1_IGNORE_GPIO_PIN	R/W	0x0	Ignore PLL1 frequency increment or decrement updates via pins
1	PLL1_FDEV_EN	R/W	0x0	Enable PLL1 frequency increment or decrement via pins or registers
0	PLL1_MODE	R/W	0x1	PLL1 operational mode 0x0 = Free-run mode (APLL only) 0x1 = DPLL mode

2.118 R117 Register (Address = 0x75) [reset = 0x0]

R117 is shown in Table 2-120.

Return to Summary Table.

Table 2-120. R117 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-0	PLL1_FDEV_37:32	R/W	0x0	Bits 37:32 of PLL1_FDEV

2.119 R118 Register (Address = 0x76) [reset = 0x0]

R118 is shown in Table 2-121.

Return to Summary Table.

Table 2-121. R118 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_FDEV_31:24	R/W	0x0	Bits 31:24 of PLL1_FDEV

2.120 R119 Register (Address = 0x77) [reset = 0x0]

R119 is shown in Table 2-122.

Return to Summary Table.

Table 2-122. R119 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_FDEV_23:16	R/W	0x0	Bits 23:16 of PLL1_FDEV

2.121 R120 Register (Address = 0x78) [reset = 0x0]

R120 is shown in Table 2-123.

Return to Summary Table.

Table 2-123. R120 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_FDEV_15:8	R/W	0x0	Bits 15:8 of PLL1_FDEV

2.122 R121 Register (Address = 0x79) [reset = 0x0]

R121 is shown in Table 2-124.

Return to Summary Table.

Table 2-124. R121 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_FDEV	R/W	0x0	PLL1 Frequency Increment or Decrement Numerator

2.123 R122 Register (Address = 0x7A) [reset = 0x0]

R122 is shown in Table 2-125.

Return to Summary Table.

Table 2-125. R122 Register Field Descriptions

Bit	Field	Type	Reset	Description
0	PLL1_FDEV_REG_UPDATE	R/W	0x0	PLL1 Frequency Increment or Decrement Register Control Writing to this register increments or decrements the APLL1 numerator by one step size. The step size is defined by PLL1_FDEV register.

2.124 R123 Register (Address = 0x7B) [reset = 0x0]

R123 is shown in Table 2-126.

Return to Summary Table.

Table 2-126. R123 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_STAT_39:32	R	0x0	Bits 39:32 of PLL1_NUM_STAT

2.125 R124 Register (Address = 0x7C) [reset = 0x0]

R124 is shown in Table 2-127.

Return to Summary Table.

Table 2-127. R124 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_STAT_31:24	R	0x0	Bits 31:24 of PLL1_NUM_STAT

2.126 R125 Register (Address = 0x7D) [reset = 0x0]

R125 is shown in Table 2-128.

Return to Summary Table.

Table 2-128. R125 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_STAT_23:16	R	0x0	Bits 23:16 of PLL1_NUM_STAT

2.127 R126 Register (Address = 0x7E) [reset = 0x0]

R126 is shown in Table 2-129.

Return to Summary Table.

Table 2-129. R126 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_STAT_15:8	R	0x0	Bits 15:8 of PLL1_NUM_STAT

2.128 R127 Register (Address = 0x7F) [reset = 0x0]

R127 is shown in Table 2-130.

Return to Summary Table.

Table 2-130. R127 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL1_NUM_STAT	R	0x0	APLL1 Numerator Status Byte

2.129 R128 Register (Address = 0x80) [reset = 0x0]

R128 is shown in Table 2-131.

Return to Summary Table.

Table 2-131. R128 Register Field Descriptions

Bit	Field	Type	Reset	Description
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	PLL1_NUM_SAT_HI	R	0x0	PLL1 Numerator saturation high status
0	PLL1_NUM_SAT_LO	R	0x0	PLL1 Numerator saturation low status

2.130 R129 Register (Address = 0x81) [reset = 0x18]

R129 is shown in Table 2-132.

Return to Summary Table.

Table 2-132. R129 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-0	PLL1_LF_R2	R/W	0x18	PLL1 Loop Filter R2 (Ω) 0x00 = 0 0x01 = 414 0x02 = 880 0x03 = 1294 0x04 = 1625 0x05 = 2039 0x06 = 2505 0x07 = 2919 0x08 = 3250 0x09 = 3664 0x0A = 4130 0x0B = 4544 0x0C = 4875 0x0D = 5289 0x0E = 5755 0x0F = 6169 0x10 = 6400 0x11 = 6814 0x12 = 7280 0x13 = 7694 0x14 = 8025 0x15 = 8439 0x16 = 8905 0x17 = 9319 0x18 = 9650 0x19 = 10064 0x1A = 10530 0x1B = 10944 0x1C = 11275 0x1D = 11689 0x1E = 12155 0x1F = 12569 0x20 = 12800 0x21 = 13214 0x22 = 13680 0x23 = 14094 0x24 = 14425 0x25 = 14839

Table 2-132. R129 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x26 = 15305 0x27 = 15719 0x28 = 16050 0x29 = 16464 0x2A = 16930 0x2B = 17344 0x2C = 17675 0x2D = 18089 0x2E = 18555 0x2F = 18969 0x30 = 19200 0x31 = 19614 0x32 = 20080 0x33 = 20494 0x34 = 20825 0x35 = 21239 0x36 = 21705 0x37 = 22119 0x38 = 22450 0x39 = 22864 0x3A = 23330 0x3B = 23744 0x3C = 24075 0x3D = 24489 0x3E = 24955 0x3F = 25369

2.131 R130 Register (Address = 0x82) [reset = 0x0]

R130 is shown in Table 2-133.

Return to Summary Table.

Table 2-133. R130 Register Field Descriptions

Bit	Field	Type	Reset	Description
2-0	PLL1_LF_C1	R/W	0x0	PLL1 Loop Filter C1. Not Used, fixed 100 pF

2.132 R131 Register (Address = 0x83) [reset = 0x18]

R131 is shown in Table 2-134.

Return to Summary Table.

Table 2-134. R131 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-0	PLL1_LF_R3	R/W	0x18	PLL1 Loop Filter R3 (Ω) 0x0 = 0 0x1 = 200 0x2 = 580 0x3 = 148.7 0x4 = 700 0x5 = 155.6 0x6 = 317.2 0x7 = 122.7 0x8 = 800 0x9 = 1000 0xA = 1380 0xB = 948.7 0xC = 1500 0xD = 955.6 0xE = 1117.2 0xF = 922.7 0x10 = 1600 0x11 = 1800 0x12 = 2180 0x13 = 1748.7 0x14 = 2300 0x15 = 1755.6 0x16 = 1917.2 0x17 = 1722.7 0x18 = 2400 0x19 = 2600 0x1A = 2980 0x1B = 2548.7 0x1C = 3100 0x1D = 2555.6 0x1E = 2717.2 0x1F = 2522.7 0x20 = 3200 0x21 = 3400 0x22 = 3780 0x23 = 3348.7 0x24 = 3900 0x25 = 3355.6

Table 2-134. R131 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
				0x26 = 3517.2 0x27 = 3322.7 0x28 = 4000 0x29 = 4200 0x2A = 4580 0x2B = 4148.7 0x2C = 4700 0x2D = 4155.6 0x2E = 4317.2 0x2F = 4122.7 0x30 = 4800 0x31 = 5000 0x32 = 5380 0x33 = 4948.7 0x34 = 5500 0x35 = 4955.6 0x36 = 5117.2 0x37 = 4922.7 0x38 = 5600 0x39 = 5800 0x3A = 6180 0x3B = 5748.7 0x3C = 6300 0x3D = 5755.6 0x3E = 5917.2 0x3F = 5722.7

2.133 R132 Register (Address = 0x84) [reset = 0x18]

R132 is shown in Table 2-135.

Return to Summary Table.

Table 2-135. R132 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-0	PLL1_LF_R4	R/W	0x18	PLL1 Loop Filter R4 See PLL1_LF_R3 for bit settings.

2.134 R133 Register (Address = 0x85) [reset = 0x0]

R133 is shown in Table 2-136.

Return to Summary Table.

Table 2-136. R133 Register Field Descriptions

Bit	Field	Type	Reset	Description
6-4	PLL1_LF_C4	R/W	0x0	PLL1 Loop Filter C4 See PLL1_LF_C3 for bit settings.
3	RESERVED	R	0x0	
2-0	PLL1_LF_C3	R/W	0x0	PLL1 Loop Filter C3

2.135 R134 Register (Address = 0x86) [reset = 0x0]

R134 is shown in Table 2-137.

Return to Summary Table.

Table 2-137. R134 Register Field Descriptions

Bit	Field	Type	Reset	Description
0	PLL2_NDIV_8:8	R/W	0x0	Bit 8 of PLL2_NDIV

2.136 R135 Register (Address = 0x87) [reset = 0x64]

R135 is shown in Table 2-138.

Return to Summary Table.

Table 2-138. R135 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL2_NDIV	R/W	0x64	Bits 7:0 of PLL2 N Divider

2.137 R136 Register (Address = 0x88) [reset = 0x0]

R136 is shown in Table 2-139.

Return to Summary Table.

Table 2-139. R136 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL2_NUM_23:16	R/W	0x0	Bits 23:16 of PLL2_NUM

2.138 R137 Register (Address = 0x89) [reset = 0x0]

R137 is shown in Table 2-140.

Return to Summary Table.

Table 2-140. R137 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL2_NUM_15:8	R/W	0x0	Bits 15:8 of PLL2_NUM

2.139 R138 Register (Address = 0x8A) [reset = 0x0]

R138 is shown in Table 2-141.

Return to Summary Table.

Table 2-141. R138 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL2_NUM	R/W	0x0	PLL2 Fractional Divider Numerator

2.140 R139 Register (Address = 0x8B) [reset = 0x0]

R139 is shown in Table 2-142.

Return to Summary Table.

Table 2-142. R139 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL2_DUAL_PH_EN	R/W	0x0	PLL2 DUAL PHASE functionality on the feedback path enabled
6	PLL2_MASHSEED1	R/W	0x0	Mash Engine seed for second stage
5	PLL2_MASHSEED0	R/W	0x0	Mash Engine seed for first stage
4-3	PLL2_DTHRMODE	R/W	0x0	SDM Dither Mode 0x0 = Weak 0x1 = Medium 0x2 = Strong 0x3 = Disabled
2-0	PLL2_ORDER	R/W	0x0	APLL2 SDM Order 0x0 = Integer Mode 0x1 = 1st 0x2 = 2nd 0x3 = 3rd 0x4 = 4th

2.141 R140 Register (Address = 0x8C) [reset = 0x18]

R140 is shown in Table 2-143.

Return to Summary Table.

Table 2-143. R140 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-0	PLL2_LF_R2	R/W	0x18	PLL2 Loop Filter R2 See PLL1_LF_R2 for bit settings.

2.142 R141 Register (Address = 0x8D) [reset = 0x0]

R141 is shown in Table 2-144.

Return to Summary Table.

Table 2-144. R141 Register Field Descriptions

Bit	Field	Type	Reset	Description
2-0	PLL2_LF_C1	R/W	0x0	PLL2 Loop Filter C1. Not Used, fixed 100 pF

2.143 R142 Register (Address = 0x8E) [reset = 0x18]

R142 is shown in Table 2-145.

Return to Summary Table.

Table 2-145. R142 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-0	PLL2_LF_R3	R/W	0x18	PLL2 Loop Filter R3 See PLL1_LF_R3 for bit settings.

2.144 R143 Register (Address = 0x8F) [reset = 0x18]

R143 is shown in Table 2-146.

Return to Summary Table.

Table 2-146. R143 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-0	PLL2_LF_R4	R/W	0x18	PLL2 Loop Filter R4 See PLL1_LF_R3 for bit settings.

2.145 R144 Register (Address = 0x90) [reset = 0x0]

R144 is shown in Table 2-147.

Return to Summary Table.

Table 2-147. R144 Register Field Descriptions

Bit	Field	Type	Reset	Description
6-4	PLL2_LF_C4	R/W	0x0	PLL2 Loop Filter C4 See PLL2_LF_C3 for bit settings.
3	RESERVED	R	0x0	
2-0	PLL2_LF_C3	R/W	0x0	PLL2 Loop Filter C3 0x0 = 0 pF 0x1 = 40 pF 0x2 = 20 pF 0x3 = 60 pF 0x4 = 10 pF 0x5 = 50 pF 0x6 = 30 pF 0x7 = 70 pF

2.146 R145 Register (Address = 0x91) [reset = 0x5]

R145 is shown in Table 2-148.

Return to Summary Table.

Table 2-148. R145 Register Field Descriptions

Bit	Field	Type	Reset	Description
4-3	RESERVED	R/W	0x0	Reserved
2-0	XO_TIMER	R/W	0x5	XO Input Wait Timer Sets the startup time for the oscillator input. 0x0 = 1.6 ms 0x1 = 3.3 ms 0x2 = 6.6 ms 0x3 = 13.1 ms 0x4 = 26.2 ms 0x5 = 52.4 ms 0x6 = 104.9 ms 0x7 = Reserved

2.147 R146 Register (Address = 0x92) [reset = 0x84]

R146 is shown in Table 2-149.

Return to Summary Table.

Table 2-149. R146 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0x4	Reserved
4-0	RESERVED	R/W	0x4	Reserved

2.148 R147 Register (Address = 0x93) [reset = 0x0]

R147 is shown in Table 2-150.

Return to Summary Table.

Table 2-150. R147 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5-0	RESERVED	R/W	0x0	Reserved

2.149 R148 Register (Address = 0x94) [reset = 0x0]

R148 is shown in Table 2-151.

Return to Summary Table.

Table 2-151. R148 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.150 R149 Register (Address = 0x95) [reset = 0x0]

R149 is shown in Table 2-152.

Return to Summary Table.

Table 2-152. R149 Register Field Descriptions

Bit	Field	Type	Reset	Description
3-0	RESERVED	R/W	0x0	Reserved

2.151 R150 Register (Address = 0x96) [reset = 0x0]

R150 is shown in Table 2-153.

Return to Summary Table.

Table 2-153. R150 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PLL1_AMPCAL_TH_HI	R/W	0x0	Amplitude Calibration Upper Threshold.
3-0	PLL1_AMPCAL_TH_LO	R/W	0x0	Amplitude Calibration Lower Threshold.

2.152 R151 Register (Address = 0x97) [reset = 0x0]

R151 is shown in Table 2-154.

Return to Summary Table.

Table 2-154. R151 Register Field Descriptions

Bit	Field	Type	Reset	Description
1-0	RESERVED	R/W	0x0	Reserved

2.153 R152 Register (Address = 0x98) [reset = 0x0]

R152 is shown in Table 2-155.

Return to Summary Table.

Table 2-155. R152 Register Field Descriptions

Bit	Field	Type	Reset	Description
3-0	RESERVED	R/W	0x0	Reserved

2.154 R153 Register (Address = 0x99) [reset = 0x29]

R153 is shown in Table 2-156.

Return to Summary Table.

Table 2-156. R153 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PLL2_AMPCAL_TH_HI	R/W	0x2	Amplitude Calibration Upper Threshold.
3-0	PLL2_AMPCAL_TH_LO	R/W	0x9	Amplitude Calibration Lower Threshold.

2.155 R154 Register (Address = 0x9A) [reset = 0x24]

R154 is shown in Table 2-157.

Return to Summary Table.

Table 2-157. R154 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-3	REF_1P2V_LDO_TRIM	R/W	0x4	REF LDO trim bits.
2-0	LDO_TRIM	R/W	0x4	LDO Trim bits which is used as common for all different LDO trims.

2.156 R155 Register (Address = 0x9B) [reset = 0x0]

R155 is shown in Table 2-158.

Return to Summary Table.

Table 2-158. R155 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NVMSCRC	R	0x0	NVM Stored CRC

2.157 R156 Register (Address = 0x9C) [reset = 0x0]

R156 is shown in Table 2-159.

Return to Summary Table.

Table 2-159. R156 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NVMCNT	R	0x0	NVM Program Count The NVMCNT increments automatically after every EEPROM Erase/ Program Cycle (after a subsequent power-cycle or hard reset). The NVMCNT value is retrieved automatically after reset or after a NVM Commit operation.

2.158 R157 Register (Address = 0x9D) [reset = 0x0]

R157 is shown in Table 2-160.

Return to Summary Table.

Table 2-160. R157 Register Field Descriptions

Bit	Field	Type	Reset	Description
6	REGCOMMIT	R/W1C	0x0	REG Commit to NVM SRAM Array The REGCOMMIT bit is used to initiate a transfer from the on-chip registers back to the corresponding location in the NVM SRAM Array. The REGCOMMIT bit is automatically cleared to 0 when the transfer is complete.
5	NVMCRCERR	R	0x0	NVM CRC Error Indication This bit will read 1 when a CRC Error has been detected reading back from on-chip EEPROM during device initialization, where the NVMLCRC value does not match NVMSCRC. This bit can only be cleared by successful EEPROM programming and power-on/reset cycle, such that the NVMLCRC value matches NVMSCRC.
4	NVMAUTOCRC_DIS	R/W	0x0	NVM Automatic CRC Disable. 0 = The EEPROM Stored CRC byte is automatically calculated whenever a EEPROM program takes place.
3	NVMCOMMIT	R/W1C	0x0	NVM Commit to Registers The NVMCOMMIT bit is used to initiate a transfer of the on-chip EEPROM contents to internal registers. The transfer happens automatically after reset or when NVMCOMMIT is set to 1. The NVMCOMMIT bit is automatically cleared to 0. The registers cannot be read while a NVM Commit operation is taking place.
2	NVMBUSY	R	0x0	NVM Program Busy Indication This bit will read 1 when an EEPROM Erase/Program cycle is active, during which the EEPROM cannot be accessed.
1	NVMERASE	R/W1C	0x0	NVM Erase Start The NVMERASE bit is used to begin an on-chip EEPROM Erase cycle. The Erase cycle is only initiated if the immediately preceding I2C/SMBus transaction was a write to the NVMUNLK register with the appropriate code. The NVMERASE bit is automatically cleared to 0. In wafer sort mode the NVMERASE bit can be operated independently of the NVMPROG bit, however when not in wafer sort mode an erase can only take place as part of an ERASE/PROGRAM cycle. The NVM Erase operation takes around 115 ms.
0	NVMPROG	R/W1C	0x0	NVM Program Start The NVMPROG bit is used to begin an on-chip EEPROM Program cycle. The Program cycle is only initiated if the immediately preceding I2C/SMBus transaction was a write to the NVMUNLK register with the appropriate code. The NVMPROG bit is automatically cleared to 0. If the NVMERASE and NVMPROG bits are set simultaneously then an ERASE/PROGRAM cycle will be executed. If the NVMPROG is set when not in wafer sort mode an erase operation will also take place. The NVM Program operation takes around 115 ms.

2.159 R158 Register (Address = 0x9E) [reset = 0x0]

R158 is shown in Table 2-161.

Return to Summary Table.

Table 2-161. R158 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NVMLCRC	R	0x0	NVM Live CRC This field holds the Live CRC computed from the EEPROM data during device initialization. The internal EEPROM controller does a CRC check to compare the Live CRC value with the Stored CRC value written to EEPROM (NVMSCRC byte) in the last NVM program cycle during initialization. If the Live and Stored CRC values match (no CRC error), the EEPROM data is valid and the device controller allows normal start-up operation to continue; otherwise, if Live and Stored CRC do not match (CRC error detected), the EEPROM data is considered invalid and the controller halts start-up operation after register load (for example, PLL lock sequence and so forth). The CRC error status can be read from the NVMCRCERR bit.

2.160 R159 Register (Address = 0x9F) [reset = 0x0]

R159 is shown in Table 2-162.

Return to Summary Table.

Table 2-162. R159 Register Field Descriptions

Bit	Field	Type	Reset	Description
4-0	MEMADR_12:8	R/W	0x0	Bits 12:8 of MEMADR

2.161 R160 Register (Address = 0xA0) [reset = 0x0]

R160 is shown in Table 2-163.

Return to Summary Table.

Table 2-163. R160 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MEMADR	R/W	0x0	Memory Address The MEMADR value determines the starting address for access to the on-chip memories. NVMDAT register = NVM EEPROM Data Array (Read only) RAMDAT register = NVM SRAM Data Array (Read/Write) ROMDAT register = ROM Data Array (Read only)

2.162 R161 Register (Address = 0xA1) [reset = 0x0]

R161 is shown in Table 2-164.

Return to Summary Table.

Table 2-164. R161 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NVMDAT	R	0x0	EEPROM Read Data

2.163 R162 Register (Address = 0xA2) [reset = 0x0]

R162 is shown in Table 2-165.

Return to Summary Table.

Table 2-165. R162 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RAMDAT	R/W	0x0	RAM Read/Write Data

2.164 R163 Register (Address = 0xA3) [reset = 0x0]

R163 is shown in Table 2-166.

Return to Summary Table.

Table 2-166. R163 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R	0x0	Reserved

2.165 R164 Register (Address = 0xA4) [reset = 0x0]

R164 is shown in Table 2-167.

Return to Summary Table.

Table 2-167. R164 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NVMUNLK	R/W	0x0	NVM Program Unlock To perform an EEPROM erase and program operation, this register must be written with a value of 0xEA (unlock code) immediately before setting the NVM_ERASE_PROG bits to 0x3 on the next register write.

2.166 R165 Register (Address = 0xA5) [reset = 0x0]

R165 is shown in Table 2-168.

Return to Summary Table.

Table 2-168. R165 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NVMBASEUNLK	R/W	0x0	NVM BASE Unlock

2.167 R166 Register (Address = 0xA6) [reset = 0x0]

R166 is shown in Table 2-169.

Return to Summary Table.

Table 2-169. R166 Register Field Descriptions

Bit	Field	Type	Reset	Description
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R	0x0	
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

2.168 R167 Register (Address = 0xA7) [reset = 0x0]

R167 is shown in Table 2-170.

Return to Summary Table.

Table 2-170. R167 Register Field Descriptions

Bit	Field	Type	Reset	Description
1-0	RESERVED	R	0x0	Reserved

2.169 R168 Register (Address = 0xA8) [reset = 0x0]

R168 is shown in Table 2-171.

Return to Summary Table.

Table 2-171. R168 Register Field Descriptions

Bit	Field	Type	Reset	Description
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

2.170 R169 Register (Address = 0xA9) [reset = 0x0]

R169 is shown in Table 2-172.

Return to Summary Table.

Table 2-172. R169 Register Field Descriptions

Bit	Field	Type	Reset	Description
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2-0	RESERVED	R/W	0x0	Reserved

2.171 R170 Register (Address = 0xAA) [reset = 0x0]

R170 is shown in Table 2-173.

Return to Summary Table.

Table 2-173. R170 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R	0x0	
0	RESERVED	R/W	0x0	Reserved

2.172 R171 Register (Address = 0xAB) [reset = 0x0]

R171 is shown in Table 2-174.

Return to Summary Table.

Table 2-174. R171 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	Reserved
6-4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2-0	RESERVED	R/W	0x0	Reserved

2.173 R172 Register (Address = 0xAC) [reset = 0x0]

R172 is shown in Table 2-175.

Return to Summary Table.

Table 2-175. R172 Register Field Descriptions

Bit	Field	Type	Reset	Description
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved
4	RESERVED	R/W	0x0	Reserved
3-2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

2.174 R173 Register (Address = 0xAD) [reset = 0x0]

R173 is shown in Table 2-176.

Return to Summary Table.

Table 2-176. R173 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-0	RESERVED	R/W	0x0	Reserved

2.175 R174 Register (Address = 0xAE) [reset = 0x0]

R174 is shown in Table 2-177.

Return to Summary Table.

Table 2-177. R174 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.176 R175 Register (Address = 0xAF) [reset = 0x0]

R175 is shown in Table 2-178.

Return to Summary Table.

Table 2-178. R175 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.177 R176 Register (Address = 0xB0) [reset = 0x0]

R176 is shown in Table 2-179.

Return to Summary Table.

Table 2-179. R176 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.178 R177 Register (Address = 0xB1) [reset = 0x0]

R177 is shown in Table 2-180.

Return to Summary Table.

Table 2-180. R177 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.179 R178 Register (Address = 0xB2) [reset = 0x0]

R178 is shown in Table 2-181.

Return to Summary Table.

Table 2-181. R178 Register Field Descriptions

Bit	Field	Type	Reset	Description
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

2.180 R179 Register (Address = 0xB3) [reset = 0x0]

R179 is shown in Table 2-182.

Return to Summary Table.

Table 2-182. R179 Register Field Descriptions

Bit	Field	Type	Reset	Description
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

2.181 R180 Register (Address = 0xB4) [reset = 0x0]

R180 is shown in Table 2-183.

Return to Summary Table.

Table 2-183. R180 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-0	DPLL_TUNING_FREE_RUN_37:32	R/W	0x0	Bits 37:32 of DPLL_TUNING_FREE_RUN

2.182 R181 Register (Address = 0xB5) [reset = 0x0]

R181 is shown in Table 2-184.

Return to Summary Table.

Table 2-184. R181 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_TUNING_FREE_RUN_31:24	R/W	0x0	Bits 31:24 of DPLL_TUNING_FREE_RUN

2.183 R182 Register (Address = 0xB6) [reset = 0x0]

R182 is shown in Table 2-185.

Return to Summary Table.

Table 2-185. R182 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_TUNING_FREE_RUN_23:16	R/W	0x0	Bits 23:16 of DPLL_TUNING_FREE_RUN

2.184 R183 Register (Address = 0xB7) [reset = 0x0]

R183 is shown in Table 2-186.

Return to Summary Table.

Table 2-186. R183 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_TUNING_FREE_RUN_15:8	R/W	0x0	Bits 15:8 of DPLL_TUNING_FREE_RUN

2.185 R184 Register (Address = 0xB8) [reset = 0x0]

R184 is shown in Table 2-187.

Return to Summary Table.

Table 2-187. R184 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_TUNING_FREE_RUN	R/W	0x0	DPLL Free-Run Tuning Word

2.186 R185 Register (Address = 0xB9) [reset = 0x0]

R185 is shown in Table 2-188.

Return to Summary Table.

Table 2-188. R185 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DPLL_REF_HIST_INTMD	R/W	0x0	Controls intermediate updates to DPLL REF tuning history Updates only occur during first averaging period Tavg after reset. Programming restriction: DPLL_REF_HIST_INTMD ≤ DPLL_REF_HISTCNT. 0x0 = No intermediate update 0x1 = 1 intermediate update at Tavg/2 0x2 = 2 intermediate update at Tavg/4 and Tavg/2 0x3 = 3 intermediate updates at Tavg/8, Tavg/4 and Tavg/2 0xF = 15 intermediate updates at Tavg/32768, Tavg/16384 through Tavg/8, Tavg/4 and Tavg/2.
3	RESERVED	R	0x0	
2	DPLL_REF_HIST_HOLD	R/W	0x0	DPLL REF tuning history persistent bit 3br# if set, tuning history is not reset on holdover exit, switchover, or history software reset.
1	DPLL_REF_HIST_SWRST	R/W	0x0	Resets DPLL REF tuning history if persistent bit is not set
0	DPLL_REF_HIST_EN	R/W	0x0	Enables DPLL REF tuning history monitor

2.187 R186 Register (Address = 0xBA) [reset = 0x0]

R186 is shown in Table 2-189.

Return to Summary Table.

Table 2-189. R186 Register Field Descriptions

Bit	Field	Type	Reset	Description
4-0	DPLL_REF_HISTCNT	R/W	0x0	DPLL REF Tuning History Timer Valid range is 0 to 30.

2.188 R187 Register (Address = 0xBB) [reset = 0x0]

R187 is shown in Table 2-190.

Return to Summary Table.

Table 2-190. R187 Register Field Descriptions

Bit	Field	Type	Reset	Description
6-0	DPLL_REF_HISTDLY_30:24	R/W	0x0	Bits 30:24 of DPLL_REF_HISTDLY

2.189 R188 Register (Address = 0xBC) [reset = 0x0]

R188 is shown in Table 2-191.

Return to Summary Table.

Table 2-191. R188 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_HISTDLY_23:16	R/W	0x0	Bits 23:16 of DPLL_REF_HISTDLY

2.190 R189 Register (Address = 0xBD) [reset = 0x0]

R189 is shown in Table 2-192.

Return to Summary Table.

Table 2-192. R189 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_HISTDLY_15:8	R/W	0x0	Bits 15:8 of DPLL_REF_HISTDLY

2.191 R190 Register (Address = 0xBE) [reset = 0x0]

R190 is shown in Table 2-193.

Return to Summary Table.

Table 2-193. R190 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_REF_HISTDLY	R/W	0x0	DPLL REF Tuning History Delay

2.192 R191 Register (Address = 0xBF) [reset = 0x0]

R191 is shown in Table 2-194.

Return to Summary Table.

Table 2-194. R191 Register Field Descriptions

Bit	Field	Type	Reset	Description
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

2.193 R192 Register (Address = 0xC0) [reset = 0x55]

R192 is shown in Table 2-195.

Return to Summary Table.

Table 2-195. R192 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DETECT_MODE_SECREF	R/W	0x1	SECREF Input Energy Detector Mode Control Determines the method for energy detection on the SECREF Input. See DETECT_MODE_PRIREF for bit settings.
5-4	DETECT_MODE_PRIREF	R/W	0x1	PRIREF Input Energy Detector Mode Control Determines the method for energy detection on the PRIREF Input. 0x0 = Rising Slew Rate Detector 0x1 = Rising and Falling Slew Rate Detector 0x2 = Falling Slew Rate Detector 0x3 = VIH/VIL Level Detector
3-2	SECREF_LVL_SEL	R/W	0x1	SECREF Input Amplitude Detector See PRIREF_LVL_SEL for description and bit settings.
1-0	PRIREF_LVL_SEL	R/W	0x1	PRIREF Input Amplitude Detector Specifies the minimum differential input peak-to-peak swing to be qualified. 0x0 = Vid is 200 mV Differential or 400 mVpp Single-Ended 0x1 = Vid is 250 mV Differential or 500 mVpp Single-Ended 0x2 = Vid is 300 mV Differential or 600 mVpp Single-Ended 0x3 = Vid is 300 mV Differential or 600 mVpp Single-Ended

2.194 R193 Register (Address = 0xC1) [reset = 0x0]

R193 is shown in Table 2-196.

Return to Summary Table.

Table 2-196. R193 Register Field Descriptions

Bit	Field	Type	Reset	Description
5	PRIREF_EARLY_DET_EN	R/W	0x0	PRIREF Early Clock Detect Enable
4	PRIREF_PH_VALID_EN	R/W	0x0	PRIREF Phase Valid Detect Enable
3	PRIREF_VALTMR_EN	R/W	0x0	PRIREF Validation Timer Enable
2	RESERVED	R/W	0x0	Reserved
1	PRIREF_MISSCLK_EN	R/W	0x0	PRIREF Missing Clock Detect Enable
0	PRIREF_AMPDET_EN	R/W	0x0	PRIREF Amplitude Detect Enable

2.195 R194 Register (Address = 0xC2) [reset = 0x0]

R194 is shown in Table 2-197.

Return to Summary Table.

Table 2-197. R194 Register Field Descriptions

Bit	Field	Type	Reset	Description
5	SECREF_EARLY_DET_EN	R/W	0x0	SECREF Early Clock Detect Enable
4	SECREF_PH_VALID_EN	R/W	0x0	SECREF Phase Valid Detect Enable
3	SECREF_VALTMR_EN	R/W	0x0	SECREF Validation Timer Enable

Table 2-197. R194 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	RESERVED	R/W	0x0	Reserved
1	SECREF_MISSCLK_EN	R/W	0x0	SECREF Missing Clock Detect Enable
0	SECREF_AMPDET_EN	R/W	0x0	SECREF Amplitude Detect Enable

2.196 R195 Register (Address = 0xC3) [reset = 0x0]

R195 is shown in Table 2-198.

Return to Summary Table.

Table 2-198. R195 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-0	PRIREF_MISSCLK_DIV_21:16	R/W	0x0	PRIREF Missing Clock Detection

2.197 R196 Register (Address = 0xC4) [reset = 0x0]

R196 is shown in Table 2-199.

Return to Summary Table.

Table 2-199. R196 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_MISSCLK_DIV_15:8	R/W	0x0	PRIREF Missing Clock Detection

2.198 R197 Register (Address = 0xC5) [reset = 0x0]

R197 is shown in Table 2-200.

Return to Summary Table.

Table 2-200. R197 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_MISSCLK_DIV	R/W	0x0	PRIREF Missing Clock Detection

2.199 R198 Register (Address = 0xC6) [reset = 0x0]

R198 is shown in Table 2-201.

Return to Summary Table.

Table 2-201. R198 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-0	SECREF_MISSCLK_DIV_21:16	R/W	0x0	SECREF Missing Clock Detection

2.200 R199 Register (Address = 0xC7) [reset = 0x0]

R199 is shown in Table 2-202.

Return to Summary Table.

Table 2-202. R199 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_MISSCLK_DIV_15:8	R/W	0x0	SECREF Missing Clock Detection

2.201 R200 Register (Address = 0xC8) [reset = 0x0]

R200 is shown in Table 2-203.

Return to Summary Table.

Table 2-203. R200 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_MISSCLK_DIV	R/W	0x0	SECREF Missing Clock Detection

2.202 R201 Register (Address = 0xC9) [reset = 0x0]

R201 is shown in Table 2-204.

Return to Summary Table.

Table 2-204. R201 Register Field Descriptions

Bit	Field	Type	Reset	Description
1	SECREF_WINDOW_DET_DBLR_EN	R/W	0x0	SECREF Window Detection
0	PRIREF_WINDOW_DET_DBLR_EN	R/W	0x0	PRIREF Window Detection

2.203 R202 Register (Address = 0xCA) [reset = 0x0]

R202 is shown in Table 2-205.

Return to Summary Table.

Table 2-205. R202 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-0	PRIREF_EARLY_CLK_DIV_21:16	R/W	0x0	PRIREF Early Clock Detection

2.204 R203 Register (Address = 0xCB) [reset = 0x0]

R203 is shown in Table 2-206.

Return to Summary Table.

Table 2-206. R203 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_EARLY_CLK_DIV_15:8	R/W	0x0	PRIREF Early Clock Detection

2.205 R204 Register (Address = 0xCC) [reset = 0x0]

R204 is shown in Table 2-207.

Return to Summary Table.

Table 2-207. R204 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_EARLY_CLK_DIV	R/W	0x0	PRIREF Early Clock Detection

2.206 R205 Register (Address = 0xCD) [reset = 0x0]

R205 is shown in Table 2-208.

Return to Summary Table.

Table 2-208. R205 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-0	SECREF_EARLY_CLK_DIV_21:16	R/W	0x0	SECREF Early Clock Detection

2.207 R206 Register (Address = 0xCE) [reset = 0x0]

R206 is shown in Table 2-209.

Return to Summary Table.

Table 2-209. R206 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_EARLY_CLK_DIV_15:8	R/W	0x0	SECREF Early Clock Detection

2.208 R207 Register (Address = 0xCF) [reset = 0x0]

R207 is shown in Table 2-210.

Return to Summary Table.

Table 2-210. R207 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_EARLY_CLK_DIV	R/W	0x0	SECREF Early Clock Detection

2.209 R208 Register (Address = 0xD0) [reset = 0x0]

R208 is shown in Table 2-211.

Return to Summary Table.

Table 2-211. R208 Register Field Descriptions

Bit	Field	Type	Reset	Description
6-0	RESERVED	R/W	0x0	Reserved

2.210 R209 Register (Address = 0xD1) [reset = 0x0]

R209 is shown in Table 2-212.

Return to Summary Table.

Table 2-212. R209 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.211 R210 Register (Address = 0xD2) [reset = 0x0]

R210 is shown in Table 2-213.

Return to Summary Table.

Table 2-213. R210 Register Field Descriptions

Bit	Field	Type	Reset	Description
6-0	RESERVED	R/W	0x0	Reserved

2.212 R211 Register (Address = 0xD3) [reset = 0x0]

R211 is shown in Table 2-214.

Return to Summary Table.

Table 2-214. R211 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.213 R212 Register (Address = 0xD4) [reset = 0x0]

R212 is shown in Table 2-215.

Return to Summary Table.

Table 2-215. R212 Register Field Descriptions

Bit	Field	Type	Reset	Description
6-0	RESERVED	R/W	0x0	Reserved

2.214 R213 Register (Address = 0xD5) [reset = 0x0]

R213 is shown in Table 2-216.

Return to Summary Table.

Table 2-216. R213 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.215 R214 Register (Address = 0xD6) [reset = 0x0]

R214 is shown in Table 2-217.

Return to Summary Table.

Table 2-217. R214 Register Field Descriptions

Bit	Field	Type	Reset	Description
6-0	RESERVED	R/W	0x0	Reserved

2.216 R215 Register (Address = 0xD7) [reset = 0x0]

R215 is shown in Table 2-218.

Return to Summary Table.

Table 2-218. R215 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.217 R216 Register (Address = 0xD8) [reset = 0x0]

R216 is shown in Table 2-219.

Return to Summary Table.

Table 2-219. R216 Register Field Descriptions

Bit	Field	Type	Reset	Description
3-2	RESERVED	R/W	0x0	Reserved
1-0	RESERVED	R/W	0x0	Reserved

2.218 R217 Register (Address = 0xD9) [reset = 0x0]

R217 is shown in Table 2-220.

Return to Summary Table.

Table 2-220. R217 Register Field Descriptions

Bit	Field	Type	Reset	Description
3-0	RESERVED	R/W	0x0	Reserved

2.219 R218 Register (Address = 0xDA) [reset = 0x0]

R218 is shown in Table 2-221.

Return to Summary Table.

Table 2-221. R218 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.220 R219 Register (Address = 0xDB) [reset = 0x0]

R219 is shown in Table 2-222.

Return to Summary Table.

Table 2-222. R219 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.221 R220 Register (Address = 0xDC) [reset = 0x0]

R220 is shown in Table 2-223.

Return to Summary Table.

Table 2-223. R220 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.222 R221 Register (Address = 0xDD) [reset = 0x0]

R221 is shown in Table 2-224.

Return to Summary Table.

Table 2-224. R221 Register Field Descriptions

Bit	Field	Type	Reset	Description
3-0	RESERVED	R/W	0x0	Reserved

2.223 R222 Register (Address = 0xDE) [reset = 0x0]

R222 is shown in Table 2-225.

Return to Summary Table.

Table 2-225. R222 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.224 R223 Register (Address = 0xDF) [reset = 0x0]

R223 is shown in Table 2-226.

Return to Summary Table.

Table 2-226. R223 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.225 R224 Register (Address = 0xE0) [reset = 0x0]

R224 is shown in Table 2-227.

Return to Summary Table.

Table 2-227. R224 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.226 R225 Register (Address = 0xE1) [reset = 0x0]

R225 is shown in Table 2-228.

Return to Summary Table.

Table 2-228. R225 Register Field Descriptions

Bit	Field	Type	Reset	Description
3-0	RESERVED	R/W	0x0	Reserved

2.227 R226 Register (Address = 0xE2) [reset = 0x0]

R226 is shown in Table 2-229.

Return to Summary Table.

Table 2-229. R226 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.228 R227 Register (Address = 0xE3) [reset = 0x0]

R227 is shown in Table 2-230.

Return to Summary Table.

Table 2-230. R227 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.229 R228 Register (Address = 0xE4) [reset = 0x0]

R228 is shown in Table 2-231.

Return to Summary Table.

Table 2-231. R228 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.230 R229 Register (Address = 0xE5) [reset = 0x0]

R229 is shown in Table 2-232.

Return to Summary Table.

Table 2-232. R229 Register Field Descriptions

Bit	Field	Type	Reset	Description
3-0	RESERVED	R/W	0x0	Reserved

2.231 R230 Register (Address = 0xE6) [reset = 0x0]

R230 is shown in Table 2-233.

Return to Summary Table.

Table 2-233. R230 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.232 R231 Register (Address = 0xE7) [reset = 0x0]

R231 is shown in Table 2-234.

Return to Summary Table.

Table 2-234. R231 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.233 R232 Register (Address = 0xE8) [reset = 0x0]

R232 is shown in Table 2-235.

Return to Summary Table.

Table 2-235. R232 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.234 R233 Register (Address = 0xE9) [reset = 0x0]

R233 is shown in Table 2-236.

Return to Summary Table.

Table 2-236. R233 Register Field Descriptions

Bit	Field	Type	Reset	Description
4-0	PRIREFVLDTMR	R/W	0x0	PRIREF Validation Timer Timer = 0.1 ms x $2^{PRIREFVLDTMR}$

2.235 R234 Register (Address = 0xEA) [reset = 0x0]

R234 is shown in Table 2-237.

Return to Summary Table.

Table 2-237. R234 Register Field Descriptions

Bit	Field	Type	Reset	Description
4-0	SECREFVLDTMR	R/W	0x0	SECREF Validation Timer Timer = 0.1 ms x $2^{SECREFVLDTMR}$

2.236 R235 Register (Address = 0xEB) [reset = 0x0]

R235 is shown in Table 2-238.

Return to Summary Table.

Table 2-238. R235 Register Field Descriptions

Bit	Field	Type	Reset	Description
6-0	PRIREF_PH_VALID_CNT_30:24	R/W	0x0	PRIREF Phase-valid Detection

2.237 R236 Register (Address = 0xEC) [reset = 0x0]

R236 is shown in Table 2-239.

Return to Summary Table.

Table 2-239. R236 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_PH_VALID_CNT_23:16	R/W	0x0	PRIREF Phase-valid Detection

2.238 R237 Register (Address = 0xED) [reset = 0x0]

R237 is shown in Table 2-240.

Return to Summary Table.

Table 2-240. R237 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_PH_VALID_CNT_15:8	R/W	0x0	PRIREF Phase-valid Detection

2.239 R238 Register (Address = 0xEE) [reset = 0x0]

R238 is shown in Table 2-241.

Return to Summary Table.

Table 2-241. R238 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PRIREF_PH_VALID_CNT	R/W	0x0	PRIREF Phase-valid Detection

2.240 R239 Register (Address = 0xEF) [reset = 0x0]

R239 is shown in Table 2-242.

Return to Summary Table.

Table 2-242. R239 Register Field Descriptions

Bit	Field	Type	Reset	Description
6-0	SECREF_PH_VALID_CNT_30:24	R/W	0x0	SECREF Phase-valid Detection

2.241 R240 Register (Address = 0xF0) [reset = 0x0]

R240 is shown in Table 2-243.

Return to Summary Table.

Table 2-243. R240 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_PH_VALID_CNT_23:16	R/W	0x0	SECREF Phase-valid Detection

2.242 R241 Register (Address = 0xF1) [reset = 0x0]

R241 is shown in Table 2-244.

Return to Summary Table.

Table 2-244. R241 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_PH_VALID_CNT_15:8	R/W	0x0	SECREF Phase-valid Detection

2.243 R242 Register (Address = 0xF2) [reset = 0x0]

R242 is shown in Table 2-245.

Return to Summary Table.

Table 2-245. R242 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SECREF_PH_VALID_CNT	R/W	0x0	SECREF Phase-valid Detection

2.244 R243 Register (Address = 0xF3) [reset = 0x0]

R243 is shown in Table 2-246.

Return to Summary Table.

Table 2-246. R243 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-0	PRIREF_PH_VALID_THR	R/W	0x0	PRIREF Phase Valid Threshold

2.245 R244 Register (Address = 0xF4) [reset = 0x0]

R244 is shown in Table 2-247.

Return to Summary Table.

Table 2-247. R244 Register Field Descriptions

Bit	Field	Type	Reset	Description
5-0	SECREF_PH_VALID_THR	R/W	0x0	SECREF Phase Valid Threshold

2.246 R245 Register (Address = 0xF5) [reset = 0x0]

R245 is shown in Table 2-248.

Return to Summary Table.

Table 2-248. R245 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.247 R246 Register (Address = 0xF6) [reset = 0x0]

R246 is shown in Table 2-249.

Return to Summary Table.

Table 2-249. R246 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.248 R247 Register (Address = 0xF7) [reset = 0x0]

R247 is shown in Table 2-250.

Return to Summary Table.

Table 2-250. R247 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R/W	0x0	Reserved

2.249 R248 Register (Address = 0xF8) [reset = 0x0]

R248 is shown in Table 2-251.

Return to Summary Table.

Table 2-251. R248 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

2.250 R249 Register (Address = 0xF9) [reset = 0x0]

R249 is shown in Table 2-252.

Return to Summary Table.

Table 2-252. R249 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	Reserved
6	RESERVED	R/W	0x0	Reserved
5-4	DPLL_SECREF_AUTO_PRTY	R/W	0x0	Set priorty for SECREF See DPLL_PRIREF_AUTO_PRTY for bit settings.
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1-0	DPLL_PRIREF_AUTO_PRTY	R/W	0x0	Set priorty for PRIREF 0x1 = First priority 0x2 = Second priority

2.251 R250 Register (Address = 0xFA) [reset = 0x0]

R250 is shown in Table 2-253.

Return to Summary Table.

Table 2-253. R250 Register Field Descriptions

Bit	Field	Type	Reset	Description
1	DPLL_VAL_FL_EN	R/W	0x0	Assert reference valid for loopback mode immediately after frequency lock
0	DPLL_VAL_PL_EN	R/W	0x0	Assert reference valid for loopback mode after either phase lock or timeout counter

2.252 R251 Register (Address = 0xFB) [reset = 0x0]

R251 is shown in Table 2-254.

Return to Summary Table.

Table 2-254. R251 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0x0	Reserved
5	DPLL_REF_MAN_SEL	R/W	0x0	Controls source of manual selection 0x0 = Software register: DPLL_REF_MAN_REG_SEL 0x1 = Hardware pin: REFSEL
4	DPLL_REF_MAN_REG_SEL	R/W	0x0	Controls software manual reference selection 0x0 = Primary Reference 0x1 = Secondary Reference
3-2	RESERVED	R	0x0	
1-0	DPLL_SWITCH_MODE	R/W	0x0	Controls Switchover mode 0x0 = Auto non-revertive 0x1 = Auto revertive 0x2 = Manual fallback 0x3 = Manual holdover

2.253 R252 Register (Address = 0xFC) [reset = 0x0]

R252 is shown in Table 2-255.

Return to Summary Table.

Table 2-255. R252 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DPLL_ZDM_SYNC_EN	R/W	0x0	DPLL Zero Delay Synchronization enable
6	DPLL_ZDM_NDIV_RST_DIS	R/W	0x0	DPLL NDIV reset disable when ZDM mode is enabled
5	DPLL_SWITCHOVER_ALWAYS	R/W	0x0	DPLL Switchover Timer
4	DPLL_FASTLOCK_ALWAYS	R/W	0x0	Enable DPLL fast lock
3	RESERVED	R/W	0x0	Reserved
2	DPLL_HLDOVR_MODE	R/W	0x0	DPLL Holdover mode when tuning word history unavailable 0x0 = Enter free-run mode 0x1 = Hold last control value prior to holdover
1	RESERVED	R	0x0	
0	DPLL_LOOP_EN	R/W	0x0	DPLL Enable

2.254 R253 Register (Address = 0xFD) [reset = 0x0]

R253 is shown in Table 2-256.

Return to Summary Table.

Table 2-256. R253 Register Field Descriptions

Bit	Field	Type	Reset	Description
4-0	DPLL_SWITCHOVER_TMR_EXP	R/W	0x0	DPLL Switchover Timer

2.255 R254 Register (Address = 0xFE) [reset = 0x0]

R254 is shown in Table 2-257.

Return to Summary Table.

Table 2-257. R254 Register Field Descriptions

Bit	Field	Type	Reset	Description
2-0	DPLL_SWITCHOVER_TMR_MANT_10:8	R/W	0x0	DPLL Switchover Timer

2.256 R255 Register (Address = 0xFF) [reset = 0x0]

R255 is shown in Table 2-258.

Return to Summary Table.

Table 2-258. R255 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_SWITCHOVER_TMR_MANT	R/W	0x0	DPLL Switchover Timer

2.257 R256 Register (Address = 0x100) [reset = 0x0]

R256 is shown in Table 2-259.

Return to Summary Table.

Table 2-259. R256 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_PRIREF_RDIV_15:8	R/W	0x0	Bits 15:8 of DPLL_PRIREF_RDIV

2.258 R257 Register (Address = 0x101) [reset = 0x0]

R257 is shown in Table 2-260.

Return to Summary Table.

Table 2-260. R257 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_PRIREF_RDIV	R/W	0x0	DPLL PRIREF divider control

2.259 R258 Register (Address = 0x102) [reset = 0x0]

R258 is shown in Table 2-261.

Return to Summary Table.

Table 2-261. R258 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_SECREF_RDIV_15:8	R/W	0x0	Bits 15:8 of DPLL_SECREF_RDIV

2.260 R259 Register (Address = 0x103) [reset = 0x0]

R259 is shown in Table 2-262.

Return to Summary Table.

Table 2-262. R259 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DPLL_SECREF_RDIV	R/W	0x0	DPLL SECREF divider control

2.261 R260 Register (Address = 0x104) [reset = 0x0]

R260 is shown in Table 2-263.

Return to Summary Table.

Table 2-263. R260 Register Field Descriptions

Bit	Field	Type	Reset	Description
4	DPLL_TDC_SW_MODE	R/W	0x0	DPLL TDC Software Control Enable Value of TDC control word into the loop-filter is from register dpll_ref_frc_val[35:0].
3-0	RESERVED	R	0x0	

3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2020) to Revision A (April 2021)	Page
• Added register descriptions	1

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265