EVM User's Guide: LMK5B12212EVM

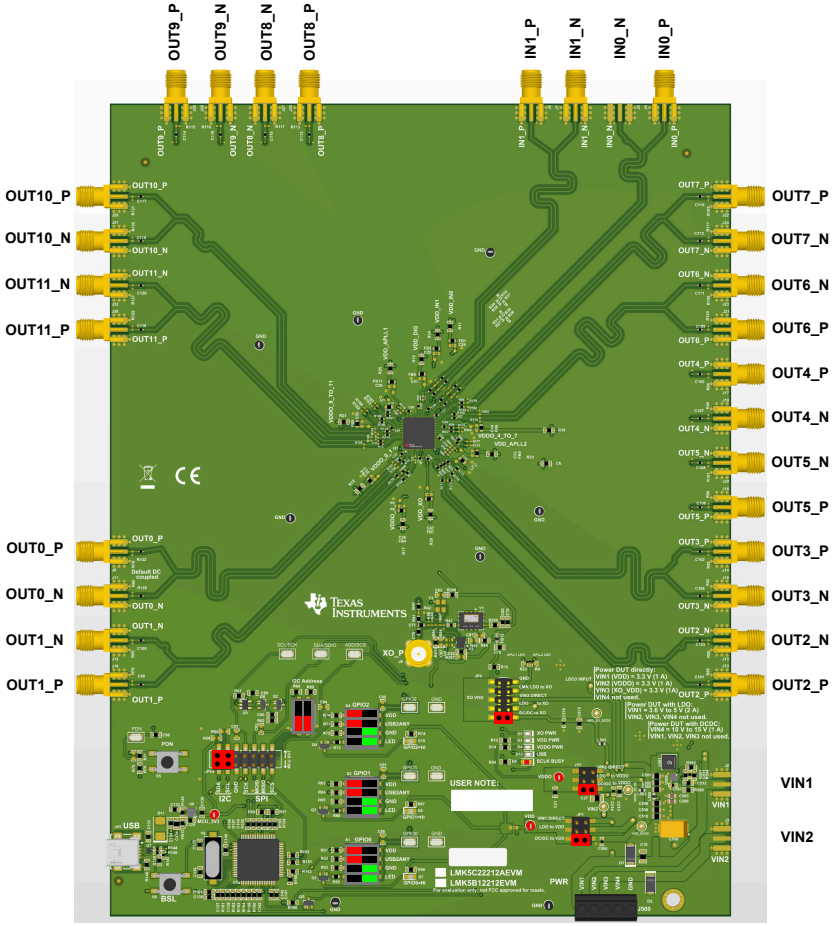
LMK5B12212 Evaluation Module User Guide

Description

The LMK5B12212EVM is an evaluation module for the LMK5B12212 Network Clock Generator and Synchronizer. The EVM can be used for device evaluation, compliance testing, and system prototyping.

Features

- One digital PLL (DPLL) with programmable bandwidths and two fractional analog PLLs (APLLs) for flexible clock generation.
- Two reference inputs to the DPLL supporting hitless switching and holdover 12 output clocks: outputs driven by BAW are capable of sub 50fs RMS phase jitter (12kHz to 20MHz).
- Flexible oscillator sources: onboard TCXO, or one of several footprints for other XO, TCXO, OCXO or external SMA input options.
- On-chip EEPROM for custom start-up clock configurations



1 Evaluation Module Overview

1.1 Introduction

The LMK5B12212EVM is an evaluation module for the LMK5B12212 Network Clock Generator and Synchronizer. The EVM can be used for device evaluation, compliance testing, and system prototyping. The LMK5B12212 integrates two Analog PLLs (APLL) and one Digital PLL (DPLL) with programmable loop bandwidth. The EVM includes SMA connectors for clock inputs, optional off-board APLL reference input, and clock outputs to interface the device with 50Ω test equipment. The onboard TCXO allows the LMK5B12212 to be evaluated in free-running, locked, or holdover mode of operation. The EVM can be configured through the onboard USB microcontroller (MCU) interface using a PC with TI's TICS Pro software graphical user interface (GUI). TICS Pro can be used to program the LMK5B12212 registers.

1.2 Kit Contents

- LMK5B12212EVM
- 3-ft. mini-USB cable (MPN 3021003-03)

1.3 Specification

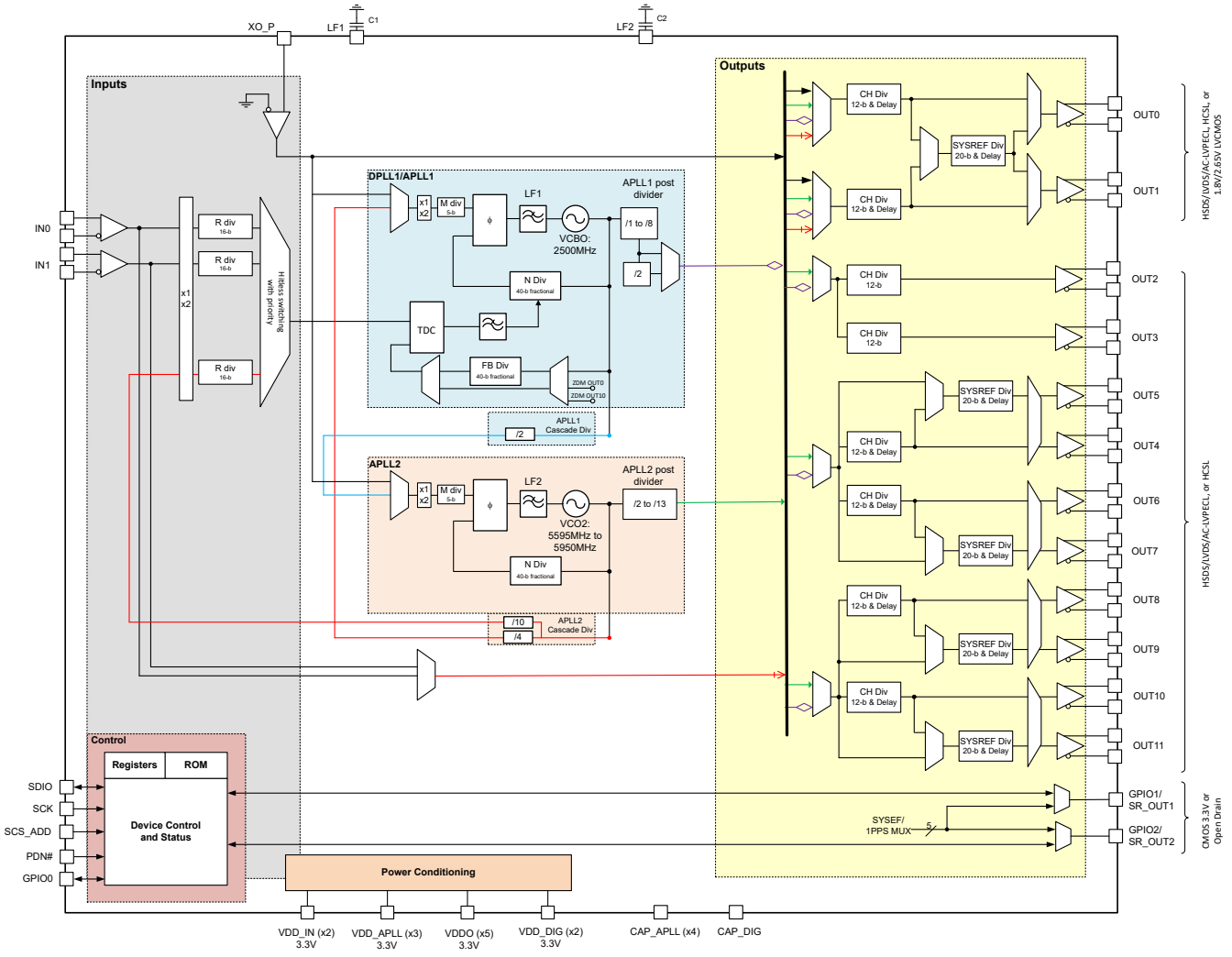


Figure 1-1. LMK5B12212 Top-Level Block Diagram

1.4 Device Information

The LMK5B12212 is a highly-configurable clock chip with multiple power domains, PLL domains, and clock input and output domains. To support a wide range of LMK5B12212 use cases, the EVM is designed with more flexibility and functionality than needed to implement the chip in a customer system application.

1.5 Using LMK5B12212EVM to evaluate LMK5C22212A

LMK5B12212 is populated on the LMK5B12212EVM by default, but the EVM can also be used to evaluate LMK5C22212A by replacing DUT U1. The two devices have the same package size and are pin-to-pin compatible. The difference is that LMK5C22212A has an extra DPLL2 compared to LMK5B12212 which has only one DPLL1. Beside that, LMK5C22212A has BAW VCO centered at 2457.6MHz supporting wireless applications.

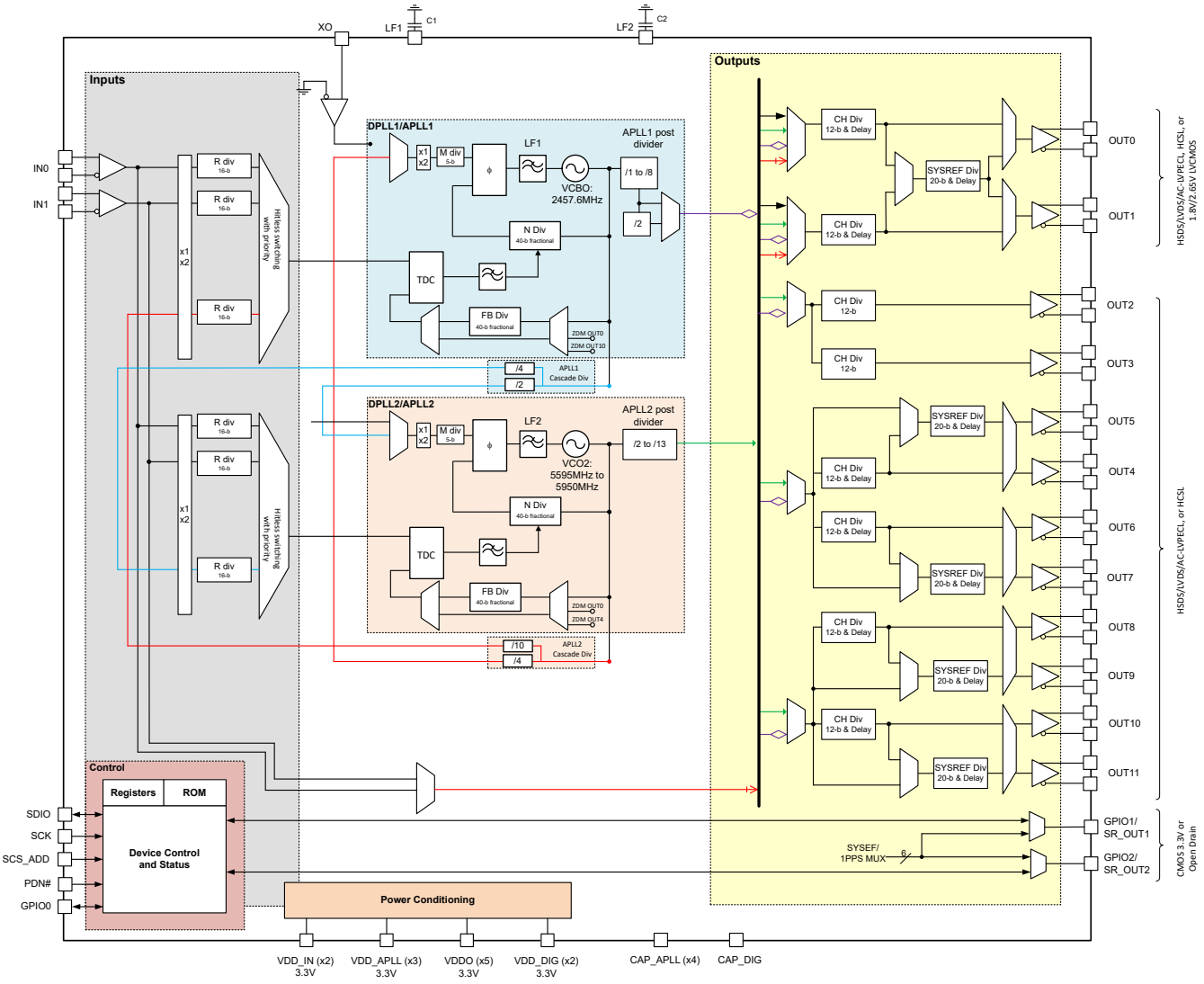


Figure 1-2. LMK5C22212A Top-Level Block Diagram

TICS Pro Software has LMK5C22212A profile to configure LMK5C22212A. Instructions to configure the profile is similar to LMK5B12212 profile as described in Software.

2 Hardware

2.1 Test Equipment Recommended

The following equipment are recommended to test with the LMK5B12212EVM configuration. Figure 2-1 illustrates an example test setup.

- For inputs:
  - DC power supply (12V, 1A for EVM default setting or 5V, 2A for other settings in Table 4-2)
  - Signal generator or other frequency sources for reference inputs
- For output measurements:
  - Phase noise analyzer
  - Real-time oscilloscope
  - Precision frequency counter

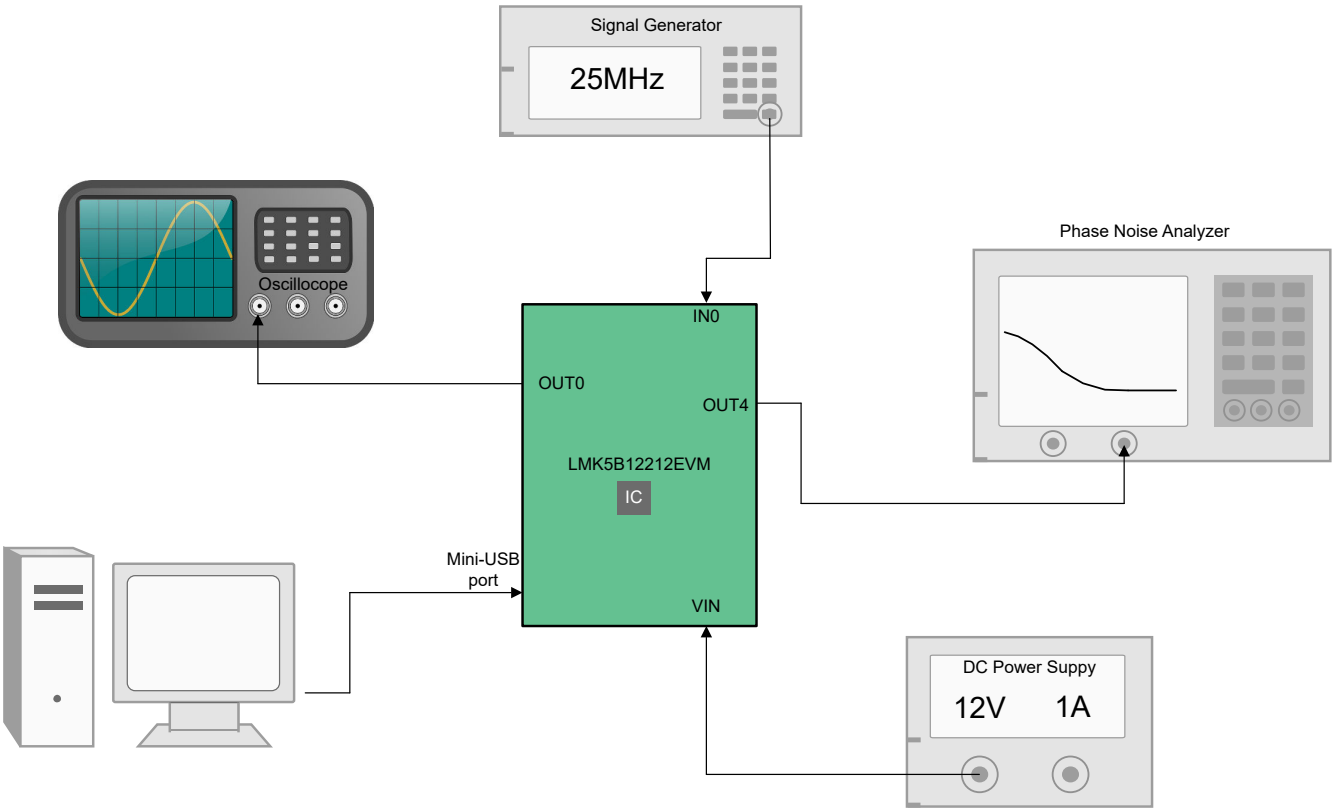


Figure 2-1. Test Setup Example

2.2 LMK5B12212EVM Default Settings

Figure 2-2 shows the jumper position with red markings. The DIP switch positions in either green boxes (for ON) or red boxes (for OFF) in the appropriate location.

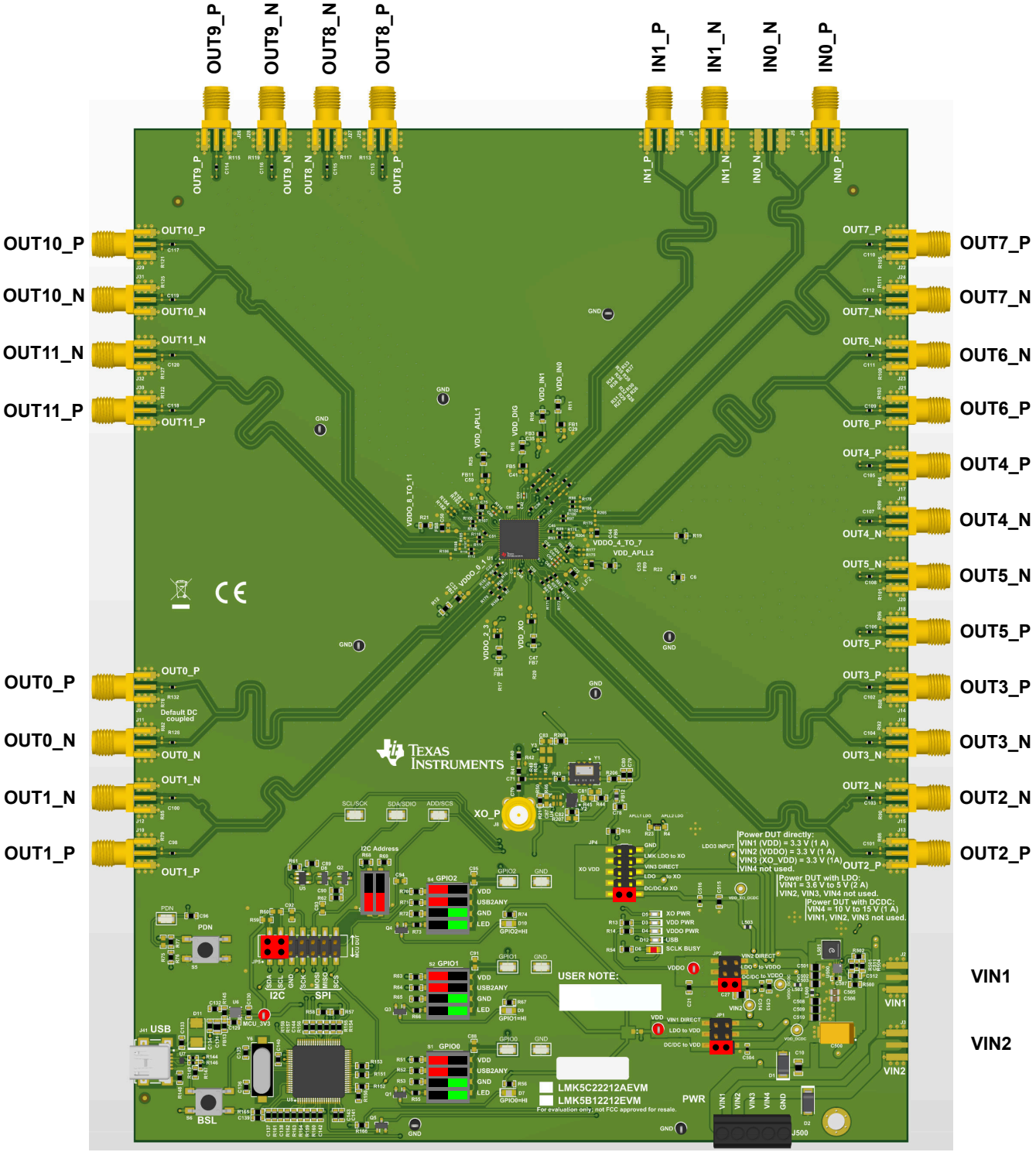


Figure 2-2. LMK5B12212EVM Default Setting of Jumpers and DIP Switches

Table 2-1 describes the default jumper positions for the EVM to power the device from a single 12V supply provided to VIN4. In positional information about jumpers, *adjacent designator* means the jumper is placed adjacent to the designator. *Opposite designator* means the jumper is placed opposite of the designator.

Table 2-1. Default Jumper and DIP Switch Settings

CATEGORY	REFERENCE DESIGNATOR	POSITION	DESCRIPTION
Power	JP1	1-2 (opposite designator)	LMK5B12212 VDD = 3.3V from DCDC provided by U500 on top of the PCB.
	JP2	1-2 (opposite designator)	LMK5B12212 VDDO = 3.3V from DCDC by U500 on top of the PCB.
	JP4	1-2 (opposite designator)	XO VCC = 3.3V from DCDC provided by U500 on top of PCB.
Communication	JP5	1-2, 3-4	Connect I^2C from onboard USB2ANY to LMK5B12212
LMK5B12212 Control Pins	S3	S3[1:2] = OFF	SCS_ADD = no pullup or pulldown.
	S1, S2, S4	Sx[1,2] = OFF Sx[3,4] = ON	Enable 3.9k pulldown on GPIO0, GPIO1, and GPIO2

2.3 EVM Quick Start

To begin using the LMK5B12212, follow the steps below.

1. Verify the EVM default jumper and DIP switch settings shown in .
2. Connect the 12V external power DC power supply (1A limit) to:
   a. VIN4 and GND terminals on header J500 (pins 4 and 5, see Figure 4-2.)
3. Connect references:
   a. 25MHz reference clock to IN0_P/N and/or,
   b. 25MHz reference clock to IN1_P/N
4. Connect the USB cable to the USB port at J41.

3 Software

3.1 Getting Started With TICS Pro

1. If not already installed, then install TICS Pro software from TI website: TICS Pro Software
2. If the MATLAB® R2015b (9.0)* 64-bit runtime is not already installed, download and install from MathWorks® website. While optional for programming and evaluating the default profile settings, the MATLAB Runtime is necessary for any application that needs to modify the DPLL loop filter settings. See MATLAB Runtime.
3. Start TICS Pro software.
4. Select the LMK5B12212 profile from *Select Device → Network Synchronizer Clock (Digital PLLs) → LMK5B12212*.
5. Confirm communications with the board by:
   a. Click *USB communications* from the menu bar.
   b. Click *Interface* to launch the *Communication Setup* pop-up window.
   c. Check these fields in the *Communication Setup* pop-up window:
      i. Make sure USB2ANY is selected as the interface.
      ii. In case of multiple USB2ANY, select desired interface. If a USB2ANY is currently in use in another TICS Pro, then users must release that interface by changing the interface setting to *DemoMode*.
      iii. Click *Identify* to blink LED shown in Figure 3-1. This confirms you are connected to the board you expect. Be aware that USB2ANY devices connected to the PC but not attached to by a TICS Pro instance can blink at a slow rate of 1 second on, 1 second off continuously. After clicking the *Identify* button, the LED flashes quickly at about 0.5 second on, 0.5 second off for about 5 seconds.

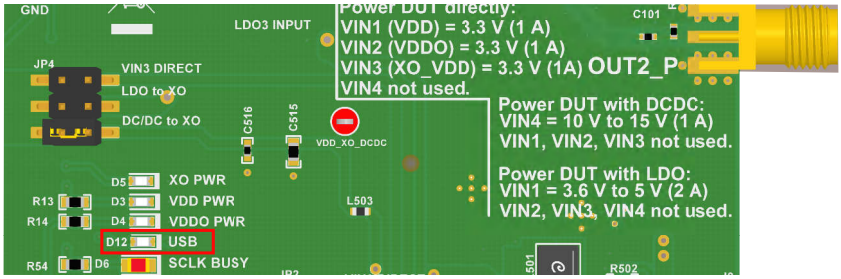


Figure 3-1. USB LED

3.2 Programming the LMK5B12212

1. Toggle the switch S5 (PDN/RESET).
2. Program all the registers:
   a. Press the *Write All Regs* button in toolbar,
   b. Select *USB Communications* in the menu bar, then select *Write All Registers*, or
   c. Press Ctrl + L.
3. Check the current consumption (maximum 1.3A).
4. Check LMK5B12212 Status as shown in Figure 3-2.
   a. Go to the *Status* page of the GUI.
   b. Click *Read Status Bits*.
   c. Make sure to clear the latched bits. To clear latched bits:
      i. Press the *Clear Latched Bits* button.
      ii. Select *Read Status Bits*.
   d. Wait to confirm the change. This can take some time for the DPLL status bits to reflect lock.

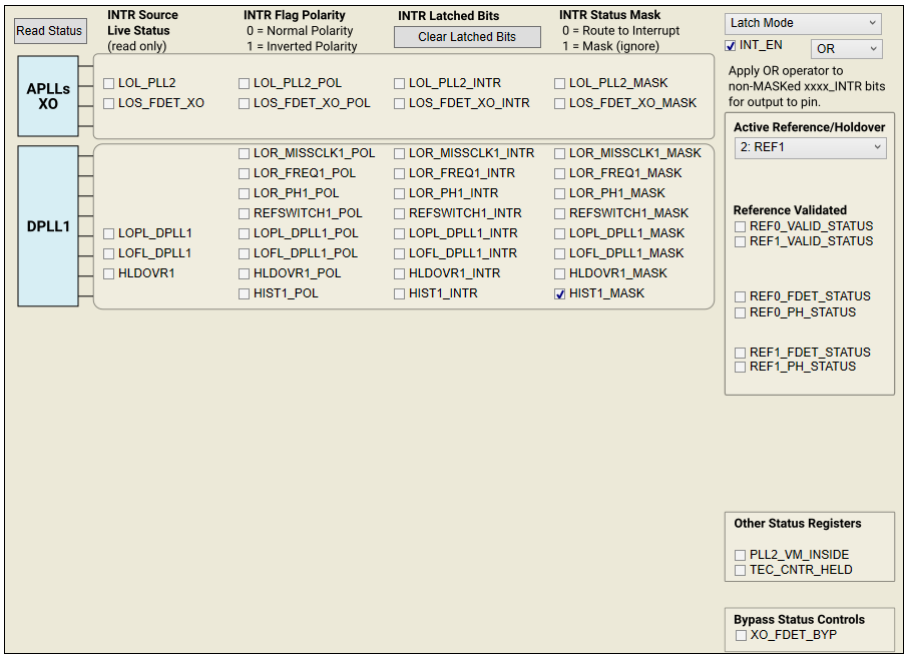


Figure 3-2. Read Status Bits

Measurements can now be made at the clock outputs.

3.3 Configuring TICS Pro

3.3.1 Using the Start Page

The Start page can be used to configure the PLLs for specific VCO frequencies and DPLL operation.

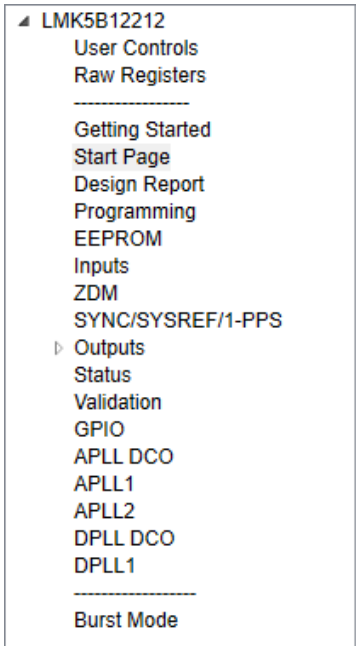


Figure 3-3. Start Page Location

3.3.1.1 Step 1

Set up the XO_P input frequency, interface type, and the XO frequency accuracy (ppm allowance).

3.3.1.2 Step 2

In Step 2, set up the clock input frequencies, interface types, and the frequency accuracies (ppm).

The ppm errors of XO and REFx are used to calculate the frequency validation according to the selected parameter located on the right side of this step.

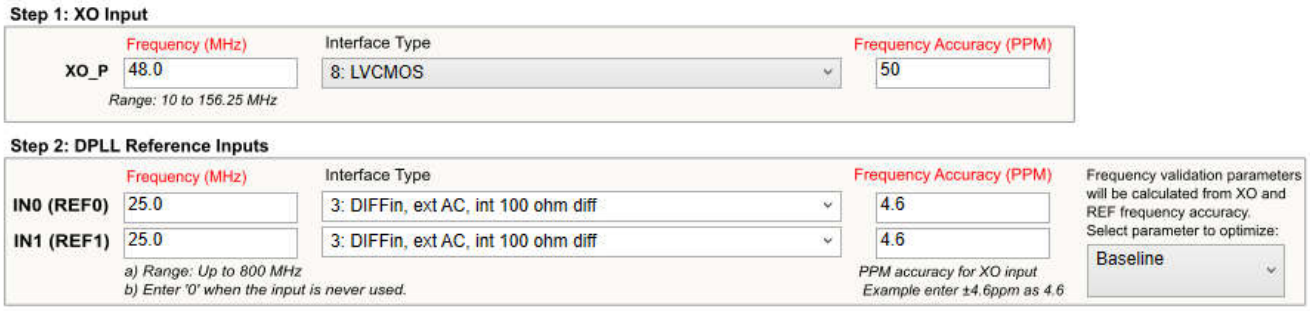


Figure 3-4. Step 1 and 2: XO Input and Clock Inputs

3.3.1.3 Step 3

Set the clock input select mode for the DPLL DPLLs, input priority, and maximum TDC frequency. The recommended Input Select Mode is *Auto Revertive*. REF0 and REF1 shown below correspond with IN0 and IN1, respectively. REF4 and REF5 priorities can be set if the DPLLs input is fed from one of the APLL post divider frequencies. The corresponding APLL is listed next to the REF4 and REF5. The REF with the highest priority is fed as the DPLL input.

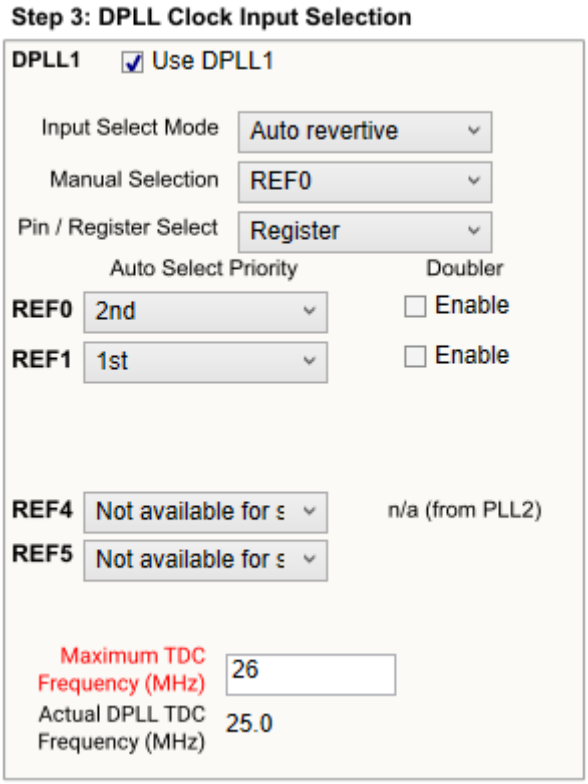


Figure 3-5. Step 3: DPLL Clock Input Selection

3.3.1.4 Step 4

Set the clock output for ZDM. The PLL drives the PLL source mux for the selected output set for ZDM.

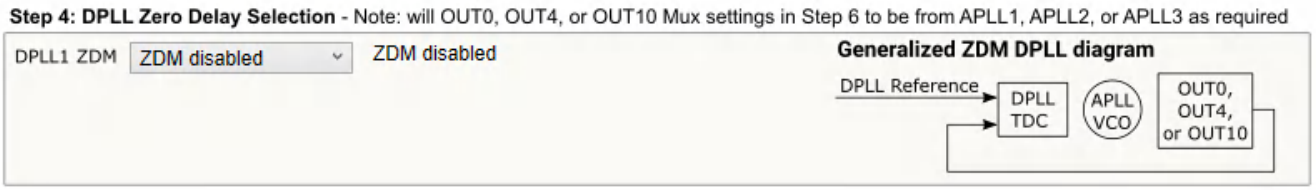


Figure 3-6. Step 4: Zero Delay Mode

3.3.1.5 Step 5

Set up the input to the APLLs by specifying the reference to each PLL. The phase detector frequency is also determined by the associated PLL R-divider and/or enabling doubler.

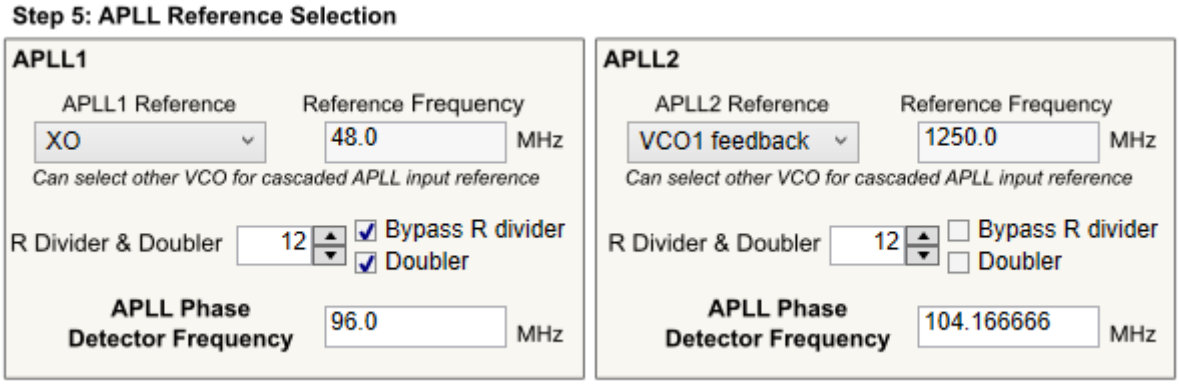


Figure 3-7. Step 5: APLL Reference Selection

3.3.1.6 Step 6

Enter desired target frequencies for each of the outputs as well as desired output format, output source, whether the output is SYSREF, and whether the output is being used or not.

Press *Calculate VCO Frequency Options* to generate a list of possible VCO frequency combinations.

Select a desired combination of VCO frequencies from the list of calculated values. If a specific VCO frequency is not in this list, a manual override can occur by selecting the *Enable User Override* checkbox and typing in the desired VCO frequencies. The *Copy to Selected VCO Frequency* box can also be used to copy the VCO frequency in the list selections to the VCO overrides.

Press the *Assign Selected VCO Settings to Device* button to update the VCO frequencies, then press the *Apply Output Clock Settings to Device* button. By default, the analog PLL frequencies are shown. The DPLL calculated frequency from step 7, however, results in exact output frequencies.

After the output frequency plan is calculated, make sure that a valid XO input is fed into the device so the APLLs can lock and generate the required frequencies. The device does not output any clocks until all enabled APLLs are locked.

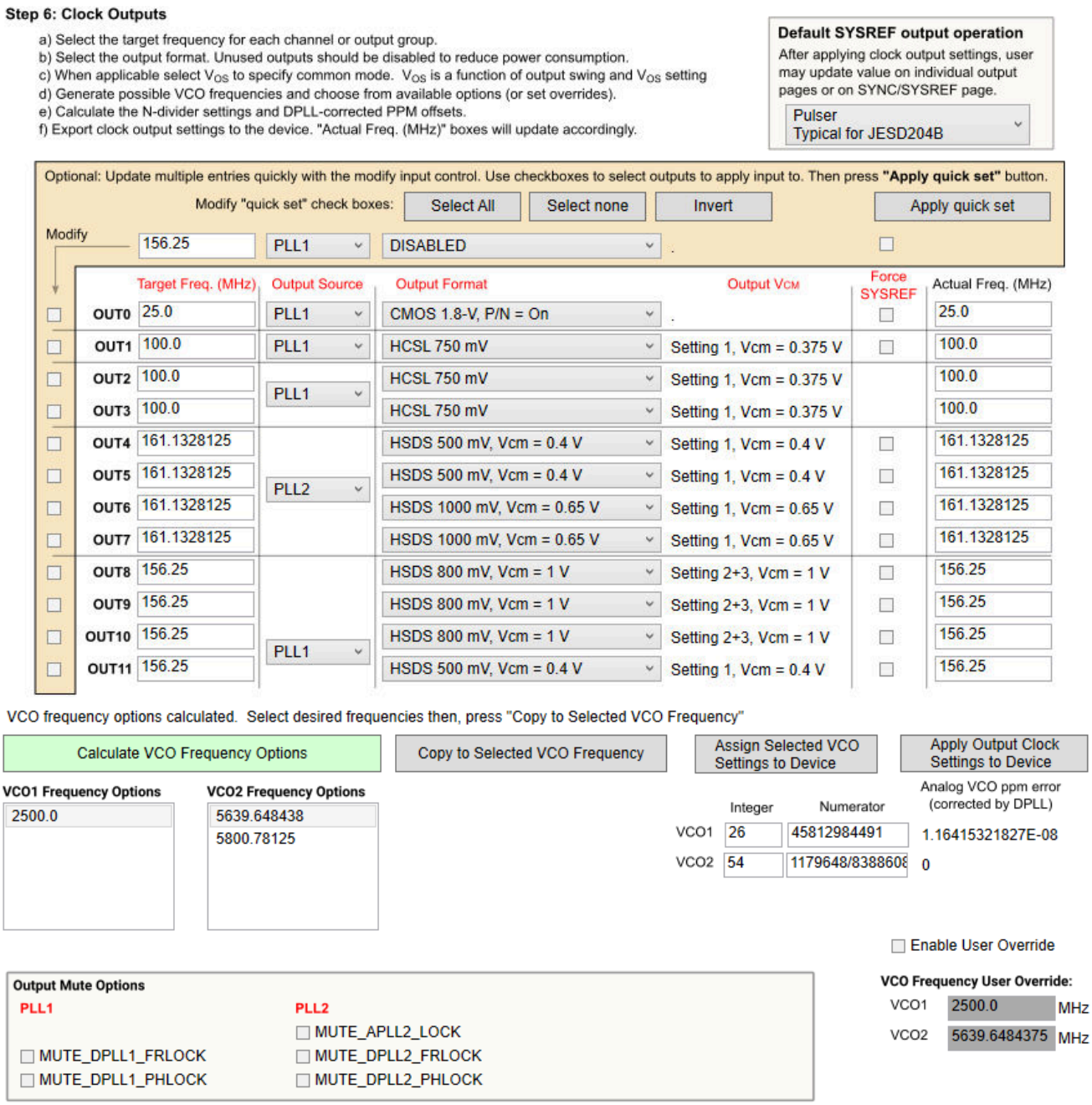


Figure 3-8. Step 6: Clock Outputs

3.3.1.7 Step 7

For step 7, simply enter the desired DPLL loop bandwidth.

Note

Any time an approximate symbol is shown, a tool tip allows exact output frequency to be seen by mousing over the control.

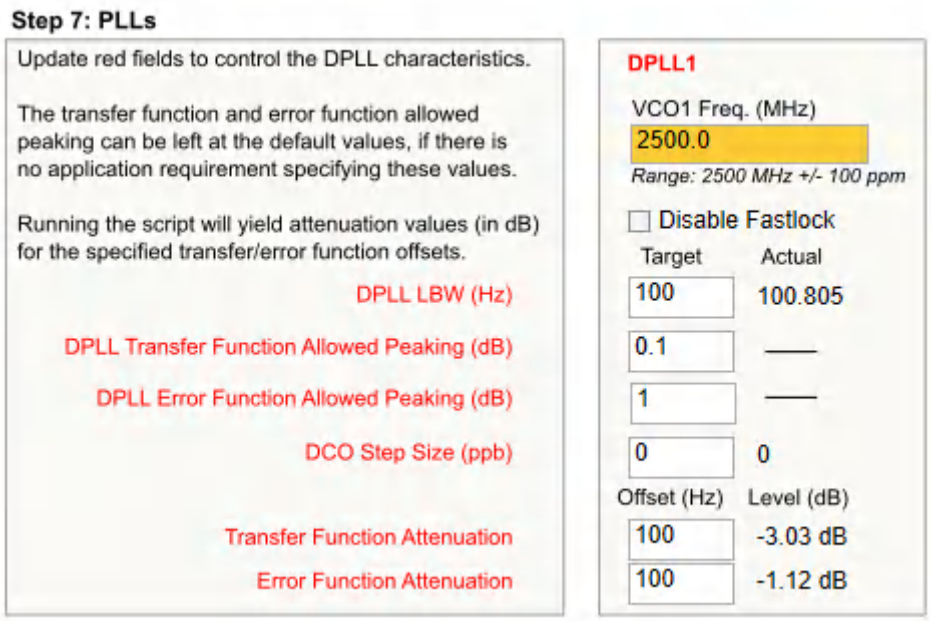


Figure 3-9. Step 7: PLLs

3.3.1.8 Step 8

To calculate the DPLL divider settings, select the DPLL loop filters and dividers to calculate and press the *Run Script* button. The software now runs and calculates the necessary loop filter settings.

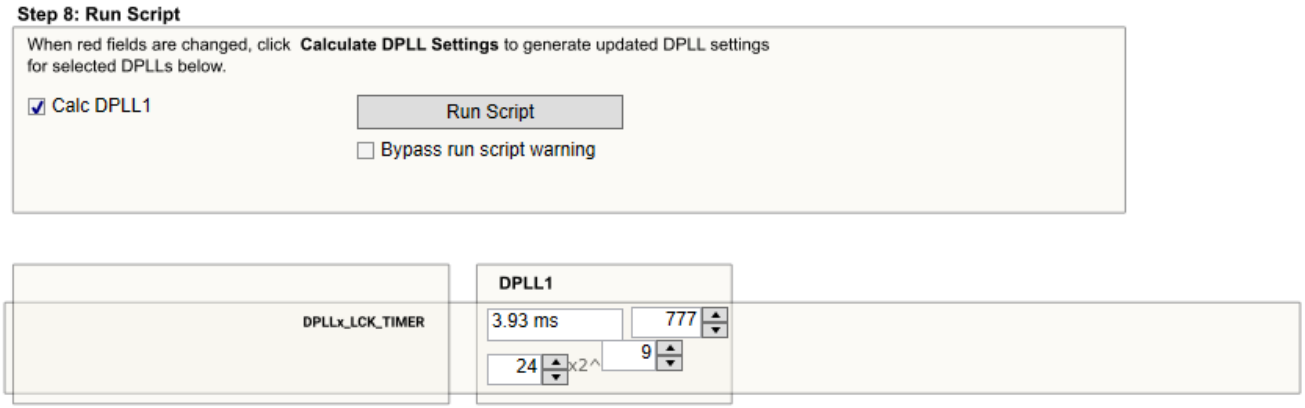


Figure 3-10. Step 8: Run Script

3.3.2 Using the Status Page

The Status page shows fields pertaining to the current status of the device. To update these fields, click the *Read Status Bits* button or the *Read RO Regs* button in the toolbar. The *Read RO Regs* button reads all read only registers which provides more information on other pages including the status fields but can take longer to read back. The read status bits just reads the status bits for this page.

For the DPLL to lock, a reference must be validated and selected in the *Active Reference/Holdover* and *Reference Validated* portions of the window shown in Figure 3-11.

As the DPLL locks, expect to see the LOPL_DPLLx as the last bit to become clear when the phase lock is acquired.

When INT_EN = 1, any live status flag, which occurs latch to the INTR Latched bit columns. These remain asserted until the *Clear Latched Bits* button is pressed. This gives additional insight into the behavior of the device.

Press the *Soft-chip reset* button in the toolbar to reset the device and restart the lock.

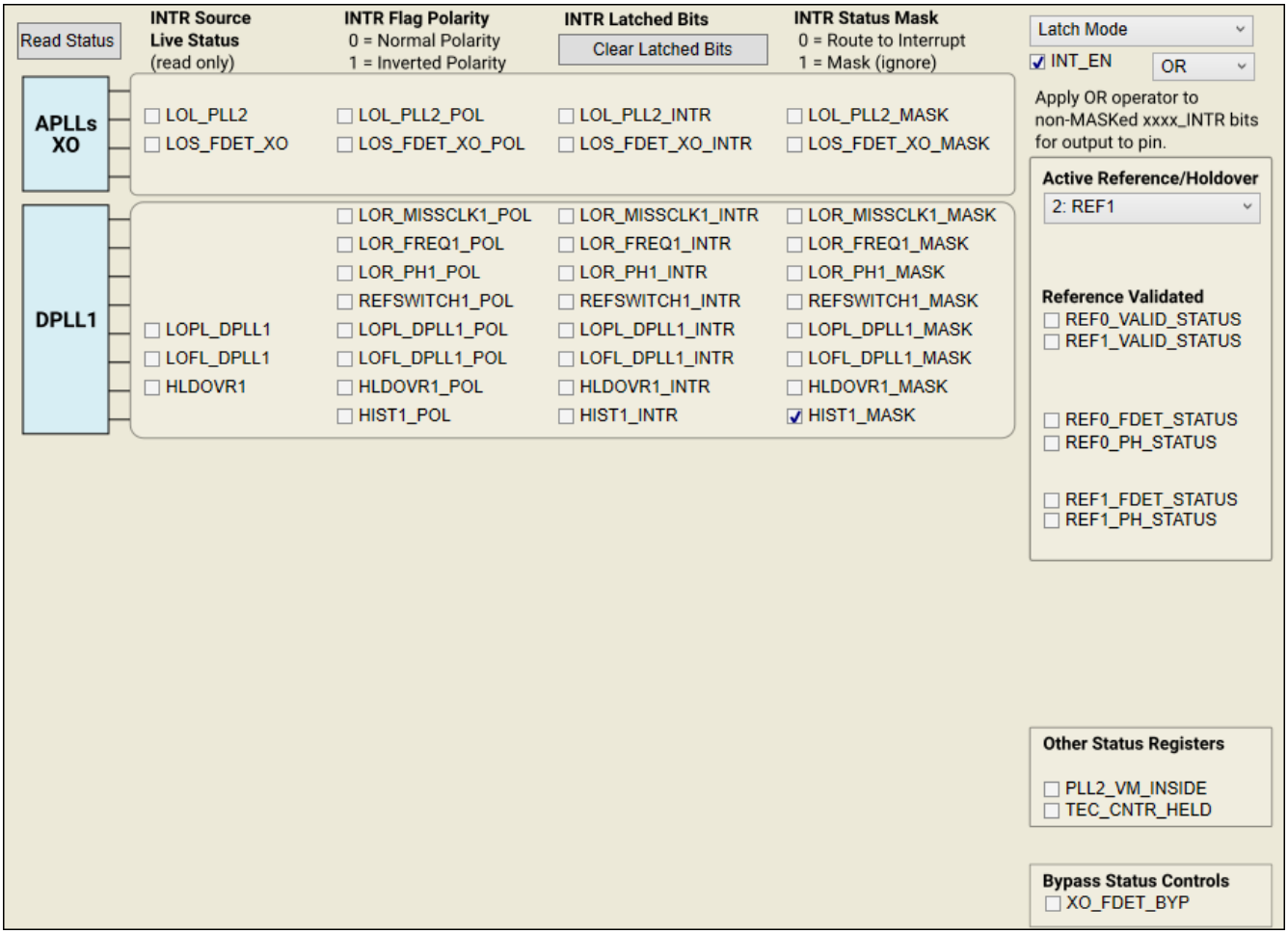


Figure 3-11. Status Page

3.3.3 Using the Input Page

The Input page provides a high-level view of all the inputs for the device, the APLL frequencies, and DPLL frequencies of the device.

When the DPLL dividers and loop filter are calculated by running the script in step 8 on the start page, this page displays the DPLL divider values which set the DPLL frequency. This is shown that the DPLL frequency is the exact desired frequency.

The DPLL supports two sets of DPLL dividers, which can be selected. At this time, the tool calculates the divider for FB Config 1 only. To use two different feedback dividers, the following procedure must be preformed:

1. Div #1 settings can be copied into Div #2 settings and selected for use by the *DPLL Div Select control*.
2. The references that require the Div #2 settings must be set to FB Config 2.
3. A second calculation can be run (re-perform a run script, step 8 on start page, of the DPLL), which repopulate Div #1 settings with the new values for FB Config 1.
   a. Div #2 settings remain the same as the ones initial copied over in step 1.

When using both feedback dividers, a requirement is not that the TDC rates are exactly the same; only that the TDC rates are within ±5% for the two DPLL feedback configurations.

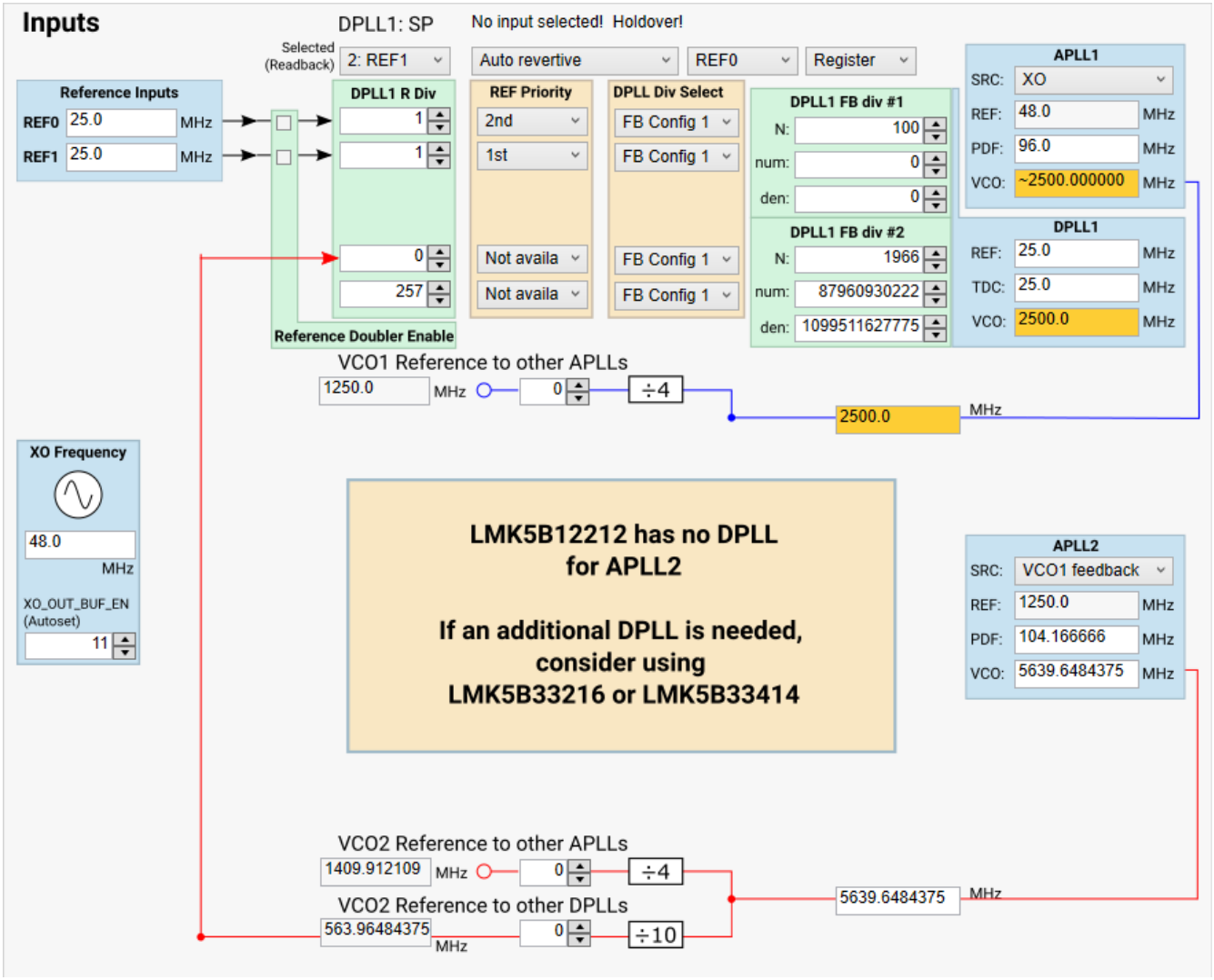


Figure 3-12. APLL or DPLL Frequency Selection

3.3.3.1 Cascaded Configurations

Cascaded configurations can be created using the input page, where the relevant VCO buffers and dividers are automatically enabled by inferring the state of source selection registers.

At least one PLL must always be active and set to XO reference source for cascaded configurations to be valid. APLL start-up priority automatically chooses XO-source APLLs to start up before all other PLLs whenever possible. Start-up priority cannot be properly inferred, therefore users must set this priority themselves in the *User Controls* page if in pin-selection mode. In the example below, APLL3 is referenced to the XO input and APLL1 and APLL2 are referenced from APLL3. Priority is controlled in ascending order, with 0 first and 1 last. APLLs can share priorities; if all APLL priorities are set to 0, then all APLLs starts up simultaneously.

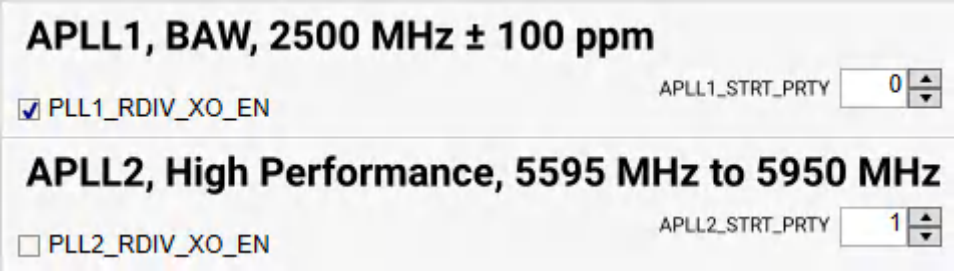
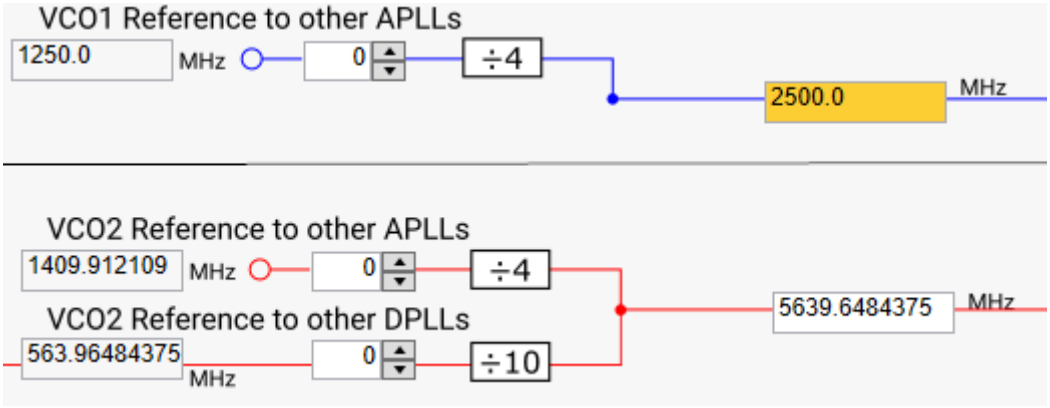


Figure 3-13. Cascade APLL Start Priorities

3.3.3.1.1 Cascade VCO to APLL Reference

Cascading APLLs is controlled by the APLL source box, shown in Figure 3-14. This box is programmed bitwise and is automatically set when generating a frequency plan. The XO_OUT_BUF_EN register in the *Input Control* section of the *User Controls* tab is automatically set to enable or disable the XO Output Buffer. The PLLx_RDIV_XO_EN is automatically checked/unchecked in each APLLx tab depending on whether each APLL is using the XO input.



Located on Inputs page

Figure 3-14. APLL Source Box

3.3.4 Using APLLx Pages

The APLL pages can be used to see detailed information on APLL behavior including the output dividers. A possibility is to type a VCO frequency into the PLL2 VCO frequency box (as shown in red circle) to have the fractional N value re-calculated.

When the DPLL is not used, the APLLs support an APLL-only mode with a programmable 24-bit denominator. Support for this mode is currently not implemented in the TICS Pro software.

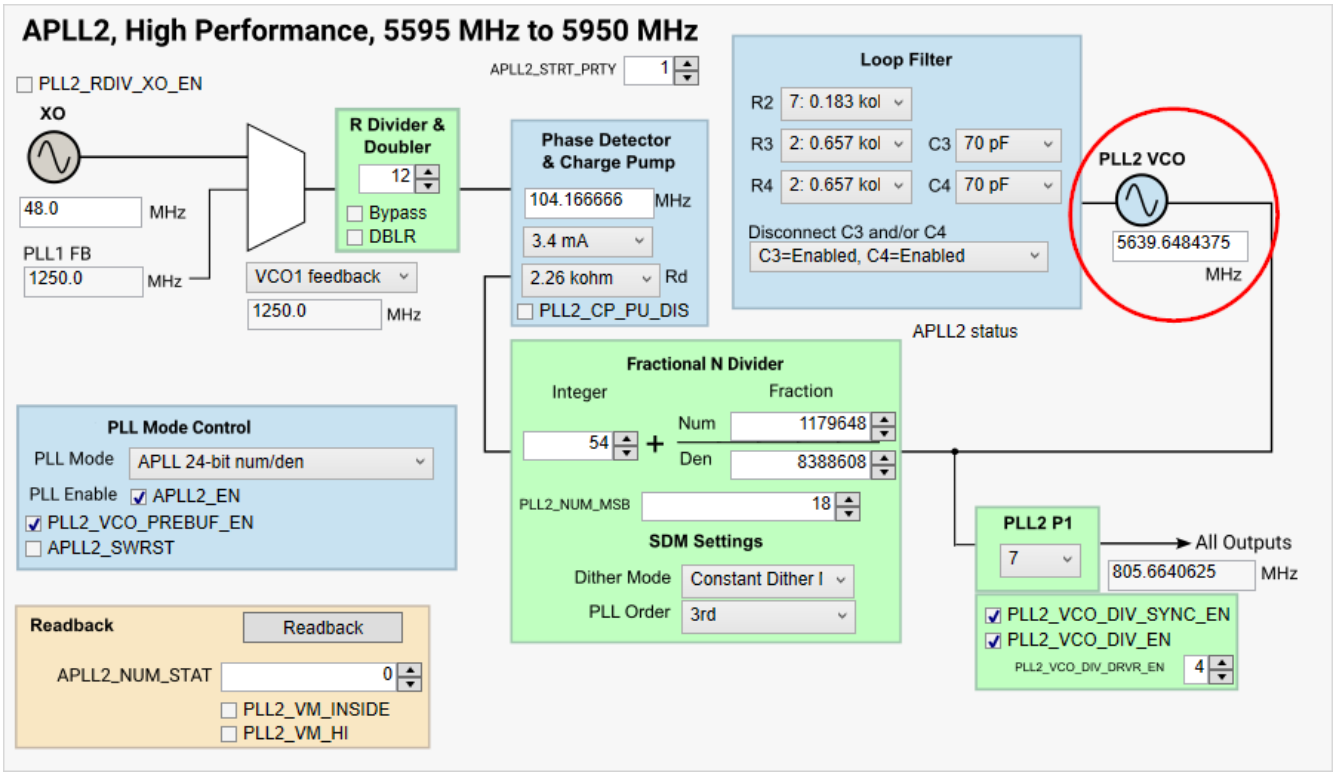


Figure 3-15. APLL2 Page

Figure 3-16 shows the post divider for PLL1. PLL1 supports all outputs of the LMK5B12212.

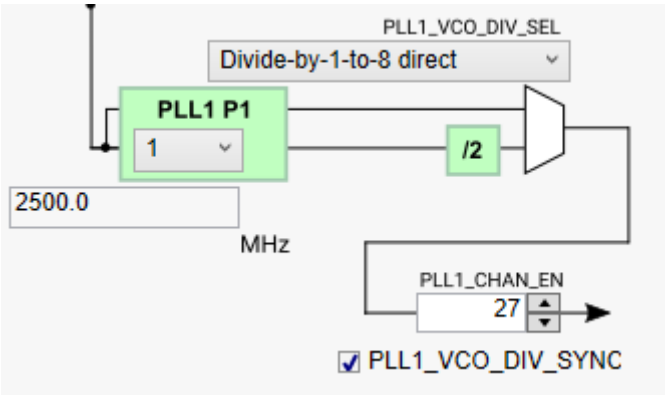


Figure 3-16. PLL1 Post Divider

3.3.4.1 APLL DCO

To use the DCO shift controls on a given APLL, enter the DCO ppb step value into the *DCO Step Size (ppb)* box shown below. The entered step size is used to calculate a numerator deviation and a 2s complement numerator deviation. To perform the shift, the increment or decrement button must be pressed. An increment writes the numerator deviation to the DPLLx_FREE_RUN control, which results in a positive frequency shift in the amount specified by the *DCO Step Size (ppb)*. An decrement writes the 2s complement numerator deviation to the DPLLx_FREE_RUN control, which results in a negative frequency shift in the amount specified by the *DCO Step Size (ppb)*.

The slew rate at which the adjustment occurs is set on the DPLLx_HOLD_SLEW_STEP control. Make sure the DPLLx_HOLD_SLEW_STEP is NOT equal to 0, otherwise the adjustment does not occur. The recommended DPLLx_HOLD_SLEW_STEP value is 63 (maximum value). A value of 63 results in the fastest adjustment.

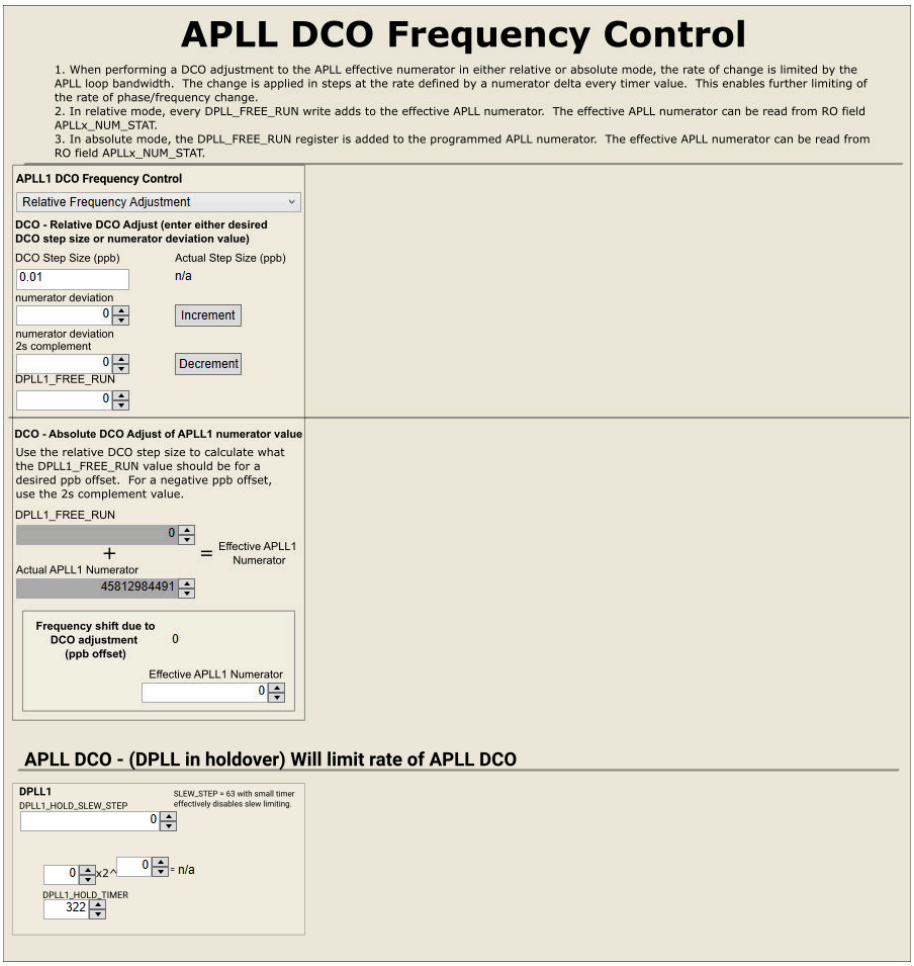


Figure 3-17. APLL DCO Controls

3.3.5 Using the DPLLx Page

The DPLL page contain many advanced controls that are normally set during the *Run Script* calculation.

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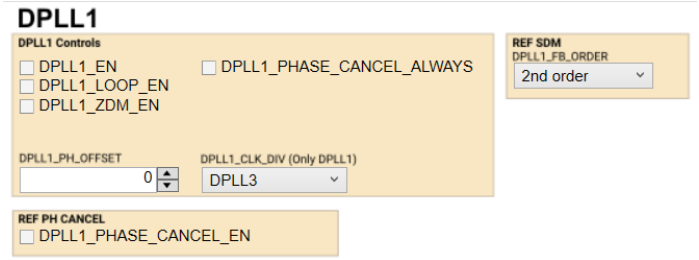

Figure 3-18. Primary DPLL Controls

3.3.5.1 DPLL DCO

To use the DCO shift controls on a given DPLL, enter the DCO ppb step value into the *DCO Step Size (ppb) box* shown below. The entered step size is used to calculate a frequency deviation that is applied to the DPLL numerator. This frequency deviation is shown in the DPLLx_FDEV control. To perform the shift, the increment or decrement button must be pressed.

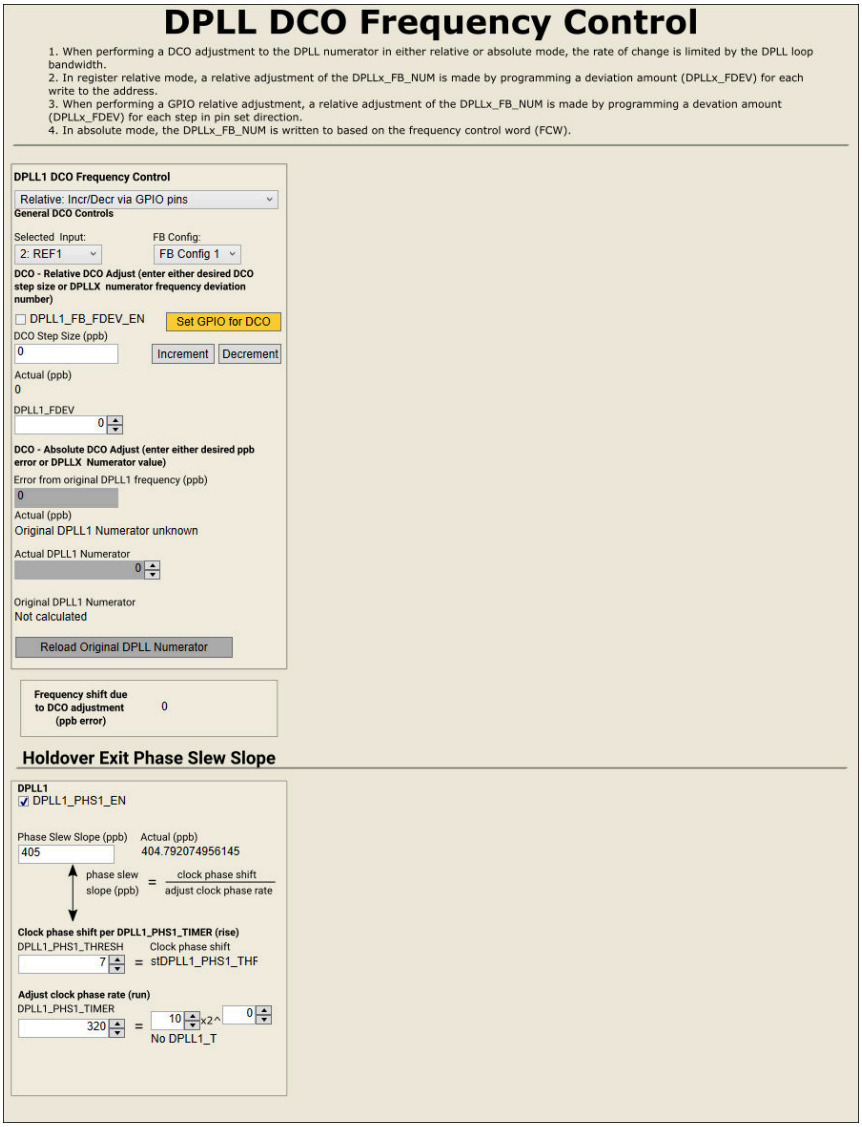

Figure 3-19. DPLL DCO Controls

3.3.6 Using the Validation Page

The Validation page allows the user to enable/disable different detectors for reference validation along with DPLL frequency and phase lock requirements. Press the *Reassign All* button at the top of the page to recalculate the validation values.

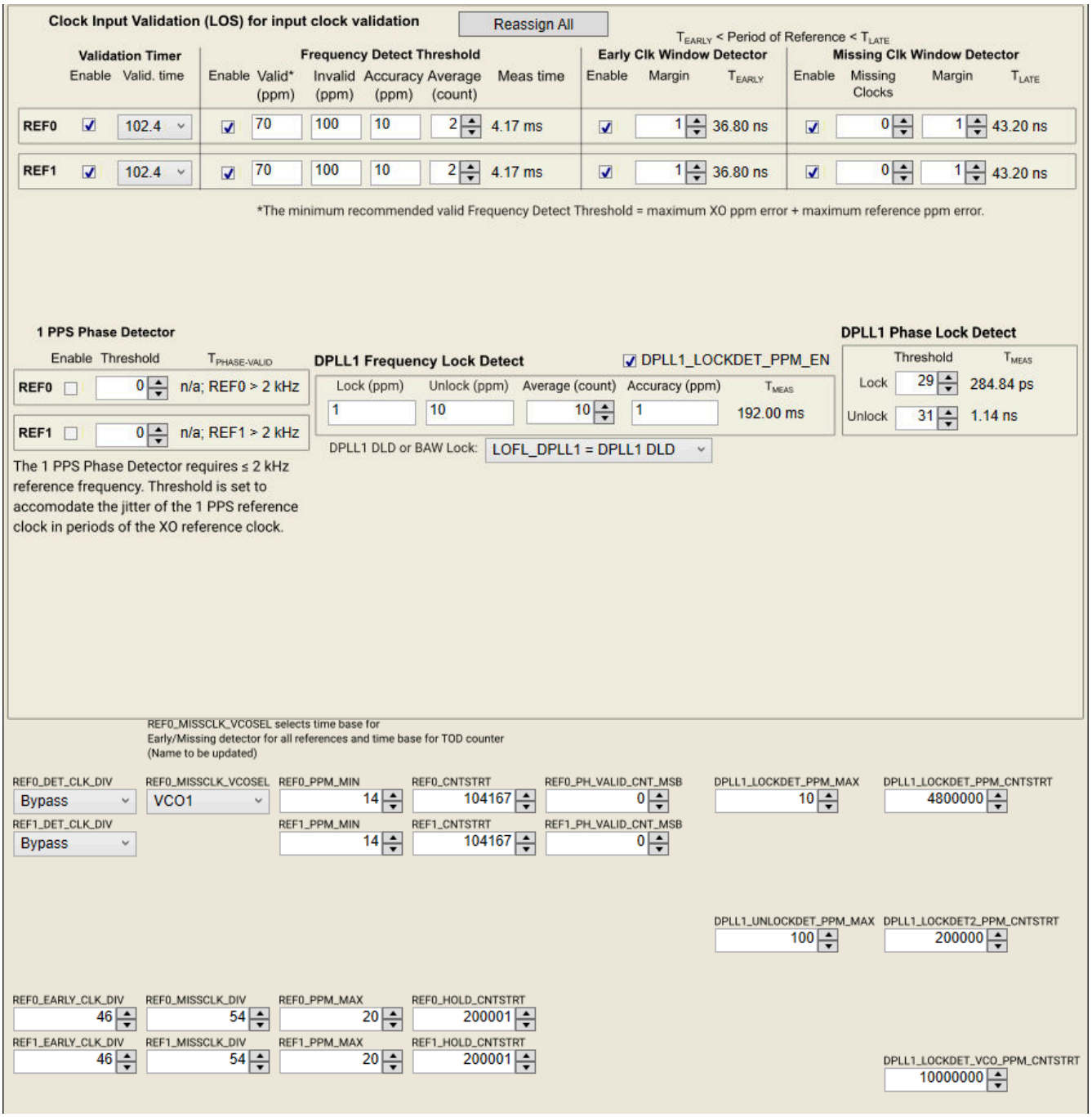

Figure 3-20. Validation Page

3.3.7 Using the GPIO Page

The GPIO page allows users to configure the GPIO0, GPIO1, and GPIO2 pins for different debugging purposes.

When using SPI readback on the EVM, GPIO2 must be configured as *STATUS or INT, Atcs as status or interrupt* and *SDO output*. When using the device in I^2C mode, refer to Section 4.1.3.

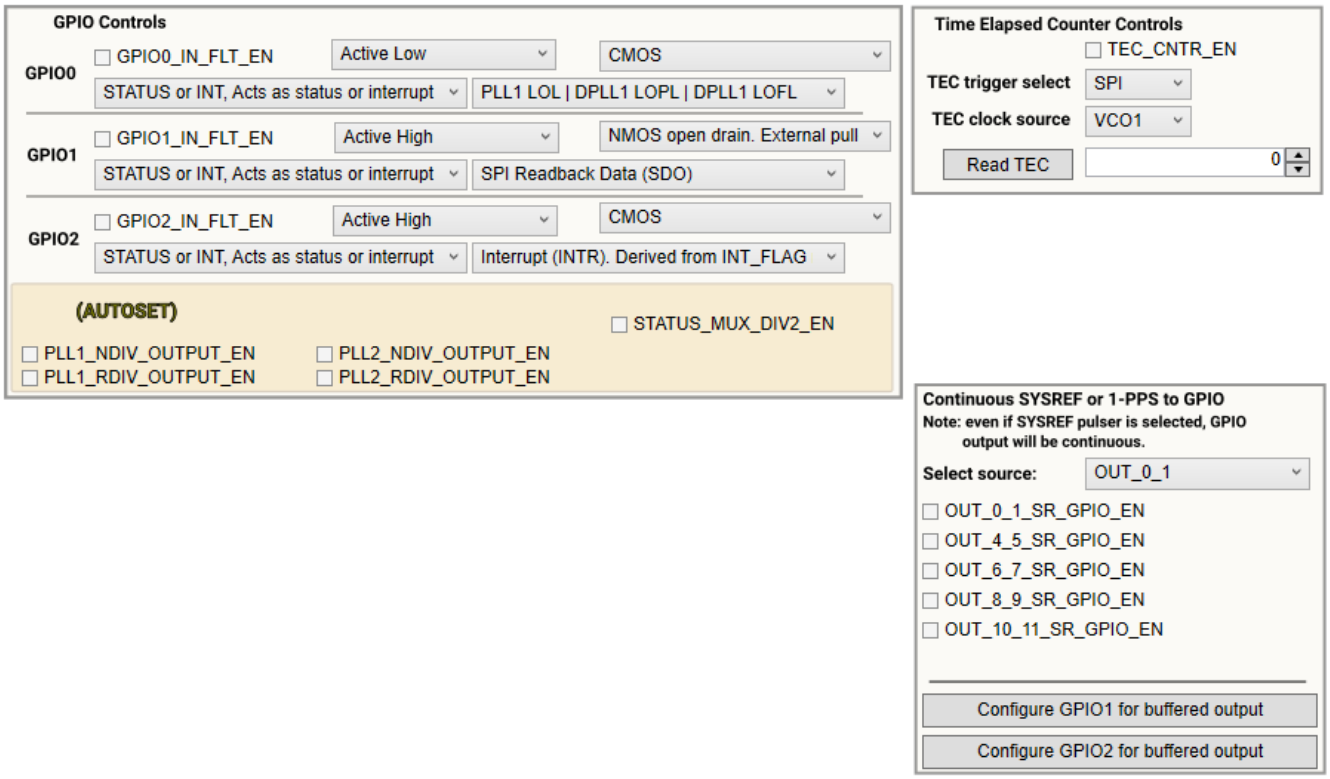

Figure 3-21. GPIO Page

3.3.7.1 SYNC/SYSREF/1-PPS Page

The SYNC/SYSREF/1-PPS page shows all the SYSREF block settings and allows for a continuous SYSREF or 1-PPS clock to be configured to be outputted from GPIO1 or GPIO2.

The SYSREF divider output signals can be replicated on either GPIO1 and GPIO2 to provide additional single ended 3.3V CMOS clocks after startup if desired. To configure the SYSREF/1PPS output replication, the GPIO must be enabled as an output (GPIOx_OUTEN = 1) and one of the SYSREF output to GPIO replication sources must be active. The SYSREF replication source comes from any one of the SYSREF dividers in use from OUT0/1, OUT4/5, OUT6/7, OUT/9, or OUT10/11 by register programming (OUT_x_y_SR_GPIO_EN = 1 and GPIO_SYSREF_SEL to the appropriate OUT_x_y). The GPIOx replicated SYSREF output is a continuous frequency. Pulsed SYSREF mode is not supported for the GPIOx replica outputs.

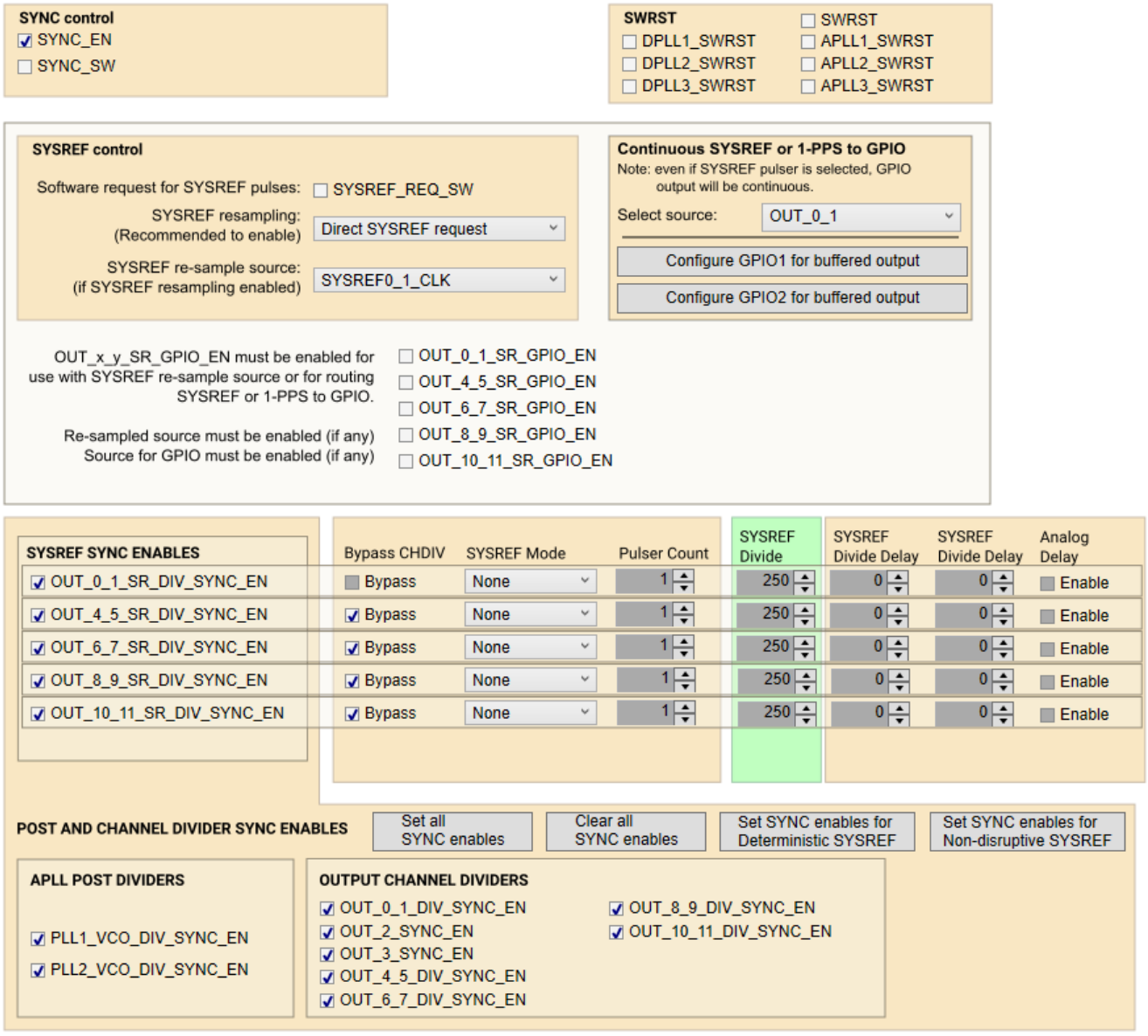

Figure 3-22. SYNC/SYSREF/1-PPS Page

3.3.8 Using the Outputs Page

The Outputs page shows all the possible source frequencies to the output channels. To simplify settings fields necessary to providing an output frequency, a source mux lists all possible sources for each output. Be sure to enable or disable the desired outputs on the right-hand side of the screen.

There are many detailed output pages beneath the Outputs page that show the individual controls for each set of outputs.

The black line between OUT2 to OUT3, OUT4 to OUT7, and OUT8 to OUT11 signifies that all these outputs must source from the same VCO.

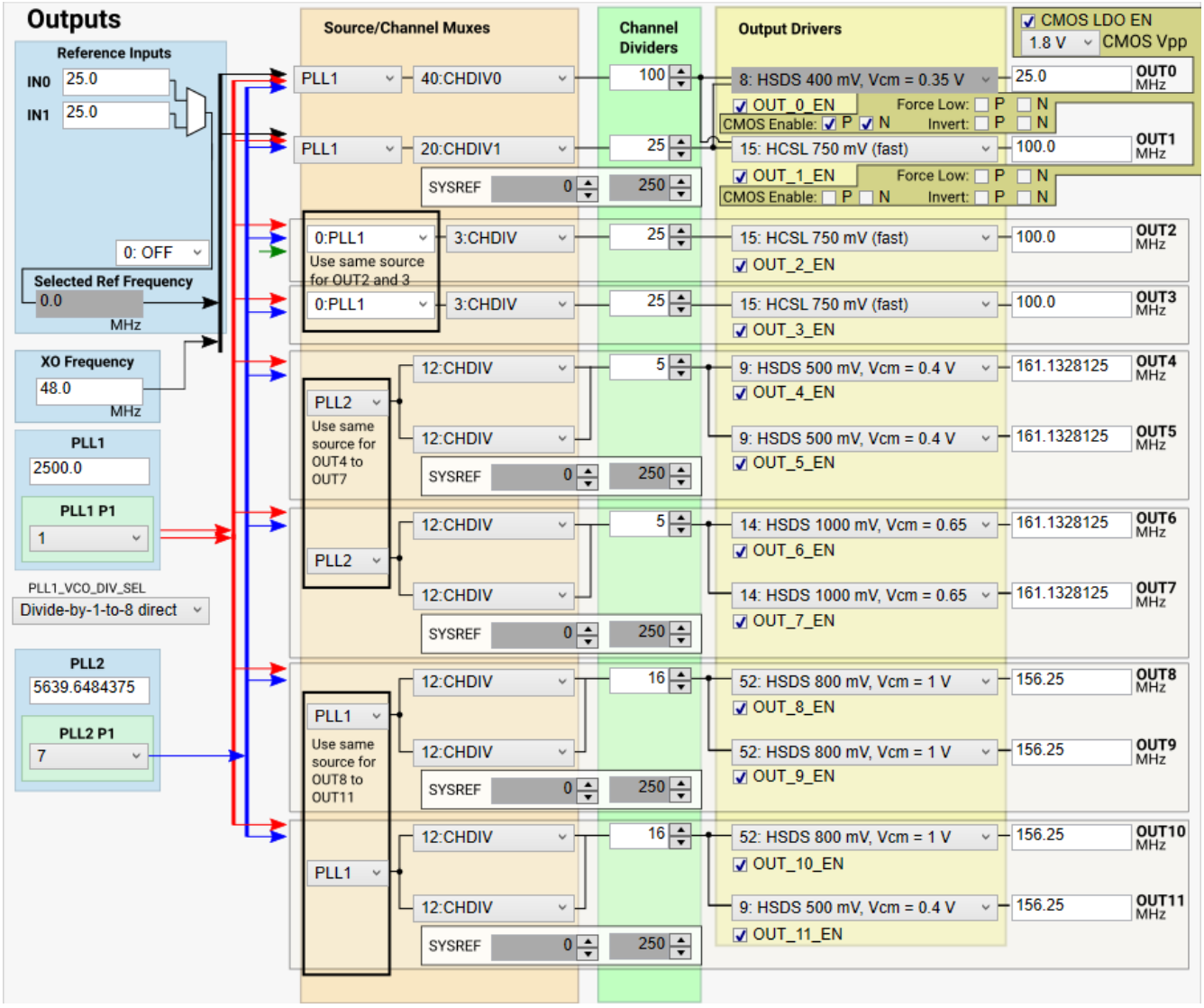

Figure 3-23. Outputs Page

3.3.9 EEPROM Page

The EEPROM page is used to write the currently loaded device settings into the device EEPROM. To program the EEPROM, press the *Program EEPROM* button.

By pressing the register commit method button, a sequence of registers is created. When this sequence is programmed onto a LMK5B12212, the sequence programs the EEPROM.

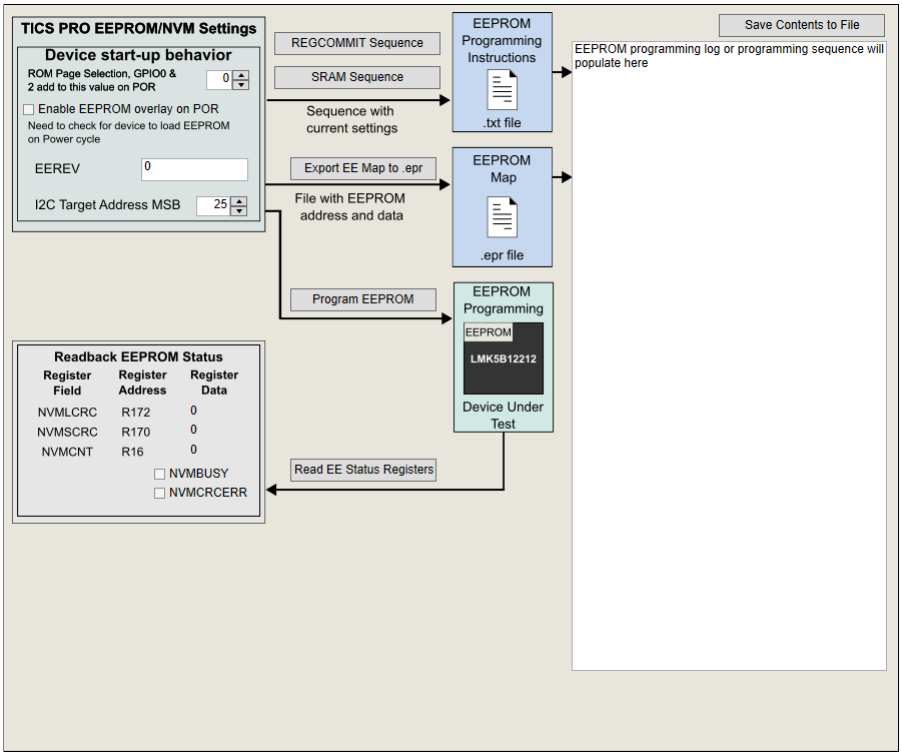

Figure 3-24. EEPROM Page

3.3.10 Design Report Page

The Design Report Page shows an overview of the current profile settings.

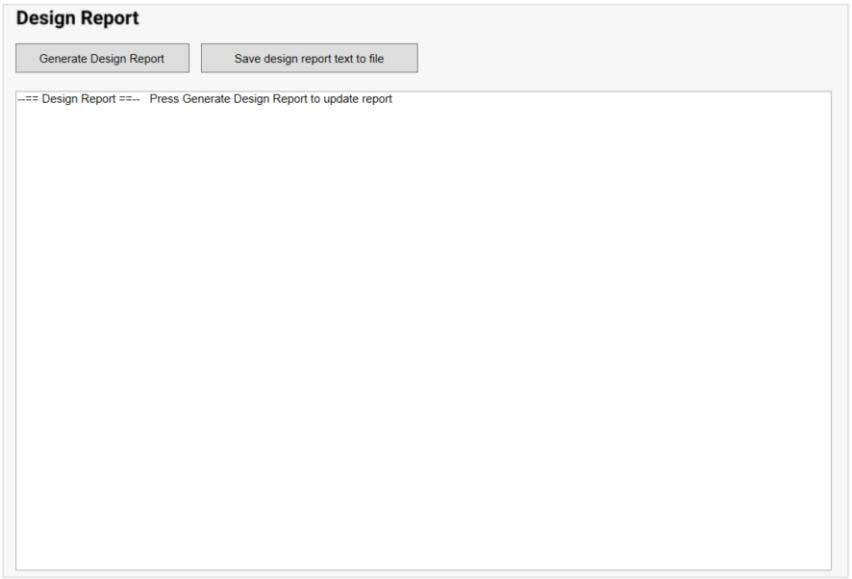

Figure 3-25. Design Report Page

4 EVM Configuration

4.1 Evaluation Setup

This section describes the power, logic, and clock input and output interfaces on the EVM, as well as how to connect, set up, and operate the EVM. Refer to Figure 4-1.

Table 4-1. Key Components Reference Designators and Descriptions

ITEM NO.		REFERENCE DESIGNATORS	DESCRIPTION
1		U1	LMK5B12212
2		J500 (VIN4 terminal block header)	External Supply, +12V DC using default configuration.
3	A	Y1	Onboard TCXO. Y1 provides improved holdover stability and allow narrower DPLL loop bandwidths to be used in comparison to the external XO input.
	B	J8	SMA connector for external XO. To use the external XO, remove the jumper from JP4.
4		J4/5, J6/7	SMA Ports for Clock Inputs (IN0_P/N and IN1_P/N). IN0_N is not populated and IN0_P is configured for single ended input. IN1 is configured for differential input.
5		J9/11, J10/12, J13/15, J14/16, J17/19, J18/20, J21/J23, J22/24, J25/27, J26/28, J29/31, J30/32, J33/35, J34/36, J37/39, J38/40	SMA Ports for Clock Outputs
6		S5	Normally open. Push button for device power down (PDN pin). R76 enables control of the PDN pin through the GUI. R76 is installed by default.
7		JP5	Jumper header for I^2C/SPI interface (MCU to LMK5B12212)
8		D6	SCL or SCK busy indication LED.
9		J41	USB Port for MCU

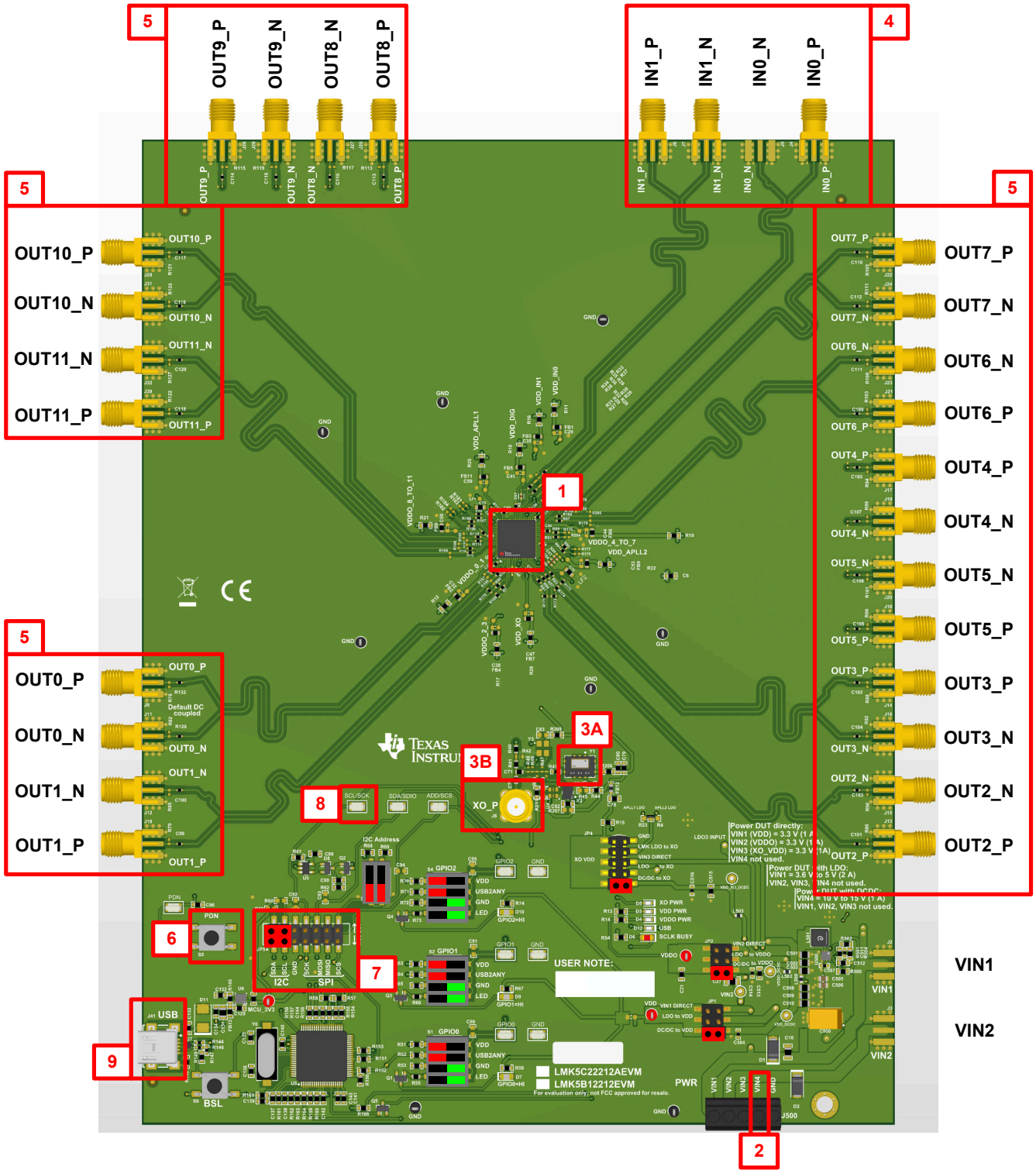

Figure 4-1. Key Components - EVM Top Side

4.1.1 Power Supply

The LMK5B12212 has VDD and VDDO supply pins that operate from 3.3V ± 5%.

J500 is the main power terminal to the external power supply. Power SMA port VIN1 (J2) provides an alternative connector style to apply power through coax cable. By default this SMA connector is not populated.

On the EVM, there are three methods for supplying power.

1. The default power configuration uses the onboard DC/DC supply (U500) to power all VDD and VDDO pins as well as the onboard XO from an external 12V supply input to VIN4 on J500.
2. The LDO power configuration uses three separate LDO regulators (U9, U10, and U11) to power the VDD, VDDO, and XO from an external 5V supply input to VIN1 on J500 (or J2).
3. The direct power configuration allows for separate voltage supplies for the VDD, VDDO, and XO. In the direct power configuration mode, an external 3.3V supply is provided to VIN1 to power the VDD pins, an external 3.3V supply is provided to VIN2 to power the VDDO pins, and an external 3.3V supply is provided to VIN3 to power the onboard XO.

Note

Not every power connection is used or required to operate the EVM. Other power configurations are possible. See the power schematics in Figure 5-1 and Figure 5-3.

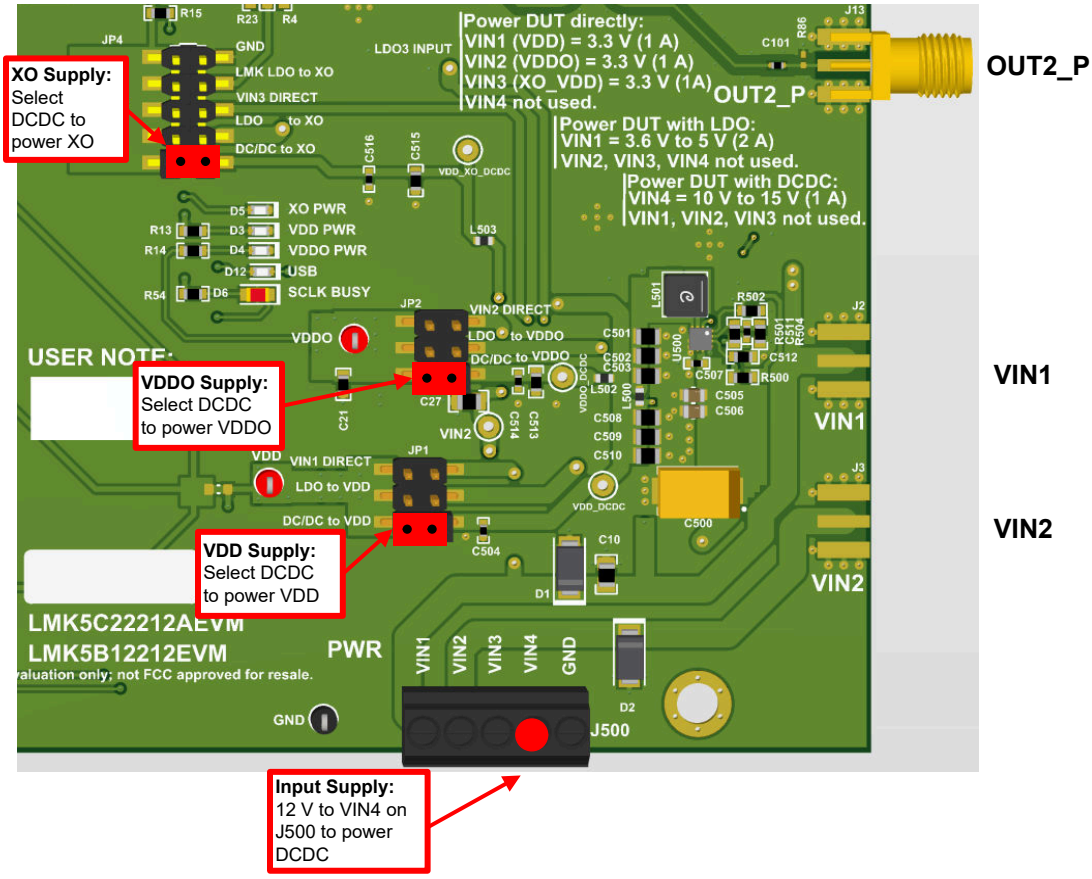

Figure 4-2. Default Power Jumper Configuration

Figure 4-2 shows the default power jumper locations and settings. Table 4-2 shows the suggested power configurations for the LMK5B12212

Table 4-2. Suggested Power Configurations

CONNECTION	NAME	ONBOARD DC/DC SUPPLY (DEFAULT) VDD = 3.3V (DCDC) VDDO = 3.3V (DCDC) XO = 3.3V (DCDC)	ONBOARD LDO REGULATORS VDD = 3.3V (LDO1) VDDO = 3.3V (LDO2) XO = 3.3V (LDO3)	DIRECT EXTERNAL SUPPLIES VDD = 3.3V (EXT. VIN1) VDDO = 3.3V (EXT. VIN2) XO = 3.3V (EXT. VIN3)
J500	PWR	• Pin 1 (VIN1): n/a • Pin 2 (VIN2): n/a • Pin 3 (VIN3): n/a • Pin 4 (VIN4): Connect to external 12V supply • Pin 5 (GND): Connect to supply ground	• Pin 1 (VIN1): Connect to external 5V supply • Pin 2 (VIN2): n/a • Pin 3 (VIN3): n/a • Pin 4 (VIN4): n/a • Pin 5 (GND): Connect to supply ground	• Pin 1 (VIN1): Connect to external 3.3V supply • Pin 2 (VIN2): Connect to external 3.3V supply • Pin 3 (VIN3): Connect to external 3.3V supply • Pin 4 (VIN4): n/a • Pin 5 (GND): Connect to supply ground
JP1	VDD	• Tie pins 1-2 (opposite to designator) to select 3.3V from DCDC to VDD Plane	• Tie pins 3-4 (middle pins) to select 3.3V from LDO1 to VDD Plane	• Tie pins 5-6 (adjacent to designator) to select external VIN1 to VDD Plane
JP2	VDDO	• Tie pins 1-2 (opposite to designator) to select 3.3V from DCDC to VDDO Plane	• Tie pins 3-4 (middle pins) to select 3.3V from LDO2 to VDDO Plane	• Tie pins 5-6 (adjacent to designator) to select external VIN2 to VDDO Plane
JP4	XO	• Tie pins 1-2 (opposite to designator) to select 3.3V from DCDC to XO supply	• Tie pins 3-4 (middle pins) to select 3.3V from LDO3 to XO supply	• Tie pins 5-6 (adjacent to designator) to select external VIN3 to XO supply

4.1.2 Logic Inputs and Outputs

The logic I/O pins of the LMK5B12212 support different functions depending on the device start-up mode chosen by the GPIO1 input level upon POR.

The default logic input pin states are determined by onboard pullup or pulldown resistors, but some input pins can be driven to high or low state by the MCU output or DIP switch control. The MCU can be controlled from a PC running TICS Pro software to program the device registers through I2C or SPI and also drive the LMK5B12212 logic inputs. To allow the MCU to control the pin input, SW[2] of the DIP switch correlating with controlled GPIO must be set to on.

See Table 4-3 for the logic pin mapping tables for the device start-up modes.

Table 4-3. Device Start-Up Modes

GPIO1 INPUT LEVEL(1)	START-UP MODE
Low	I^2C Mode
High	SPI Mode

(1) The input levels on these pins are sampled only during POR.

4.1.3 Switching Between I2C and SPI

To switch the EVM between I2C and SPI modes, the switches and jumpers must be configured as follows:

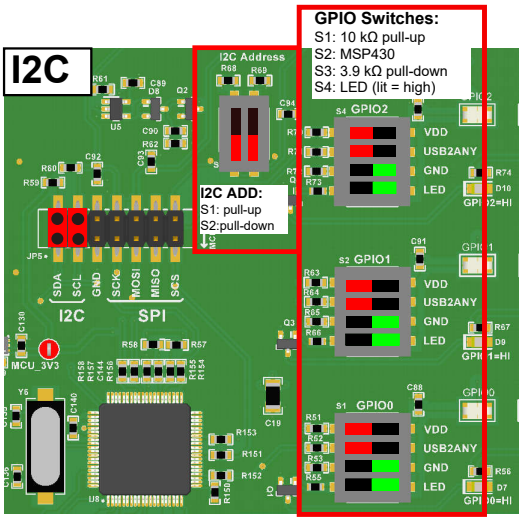

Figure 4-3. I2C Mode Jumper Configuration

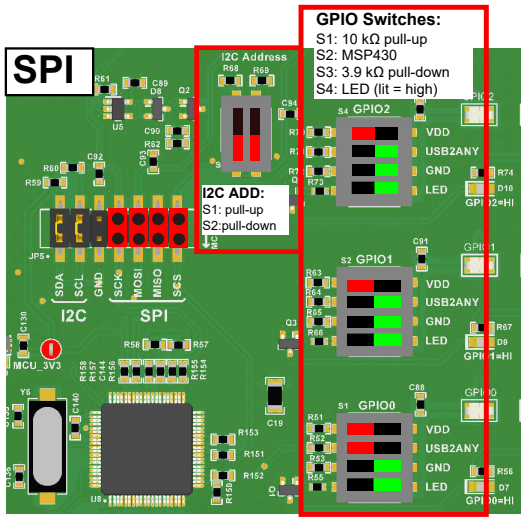

Figure 4-4. SPI Mode Jumper Configuration

In SPI mode, GPIO2 must also be configured as *STATUS or INT*, *SPI Readback Data (SDO)*, *Active High*, and *CMOS* to support SPI readback.

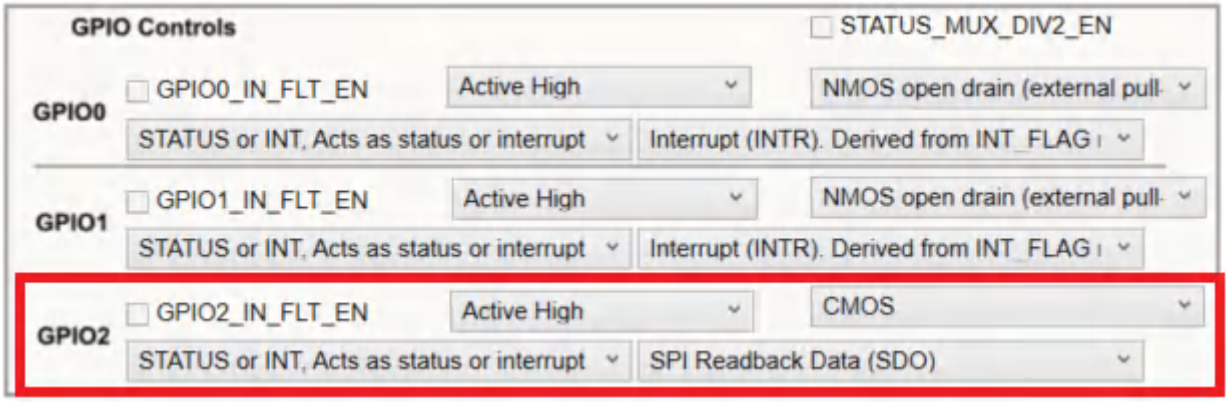

Figure 4-5. GPIO2 Setting for SPI Mode

Communication protocols must be set in TICS Pro. From the menu bar, select *USB communications → Interface* to get the *Communication Setup* window and change the protocol.

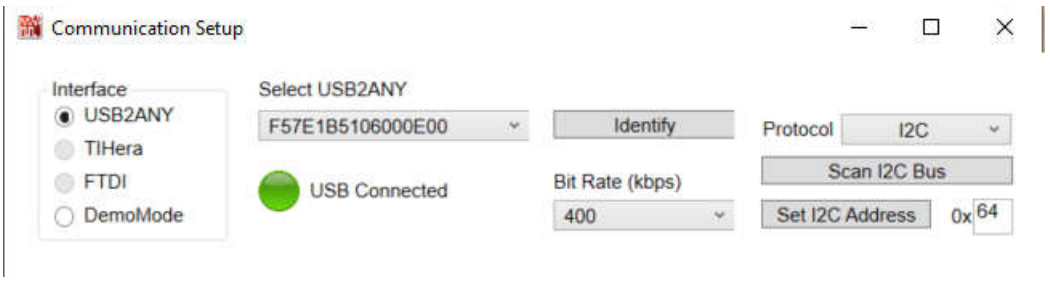

Figure 4-6. Communication Setup Window (Changing from I2C to SPI)

4.1.4 Generating SYSREF Request

A software request, GPIO0, or GPIO1 can be used to generate a SYSREF request. The TICS Pro software and EVM is designed to use GPIO2 for SPI readback (SDO). Accordingly, GPIO2 is not listed in the pins as is dedicated for SPI readback. In user application, any GPIO pin can be used.

Connect the desired GPIO pin to the MCU by setting S2 as ON on the switch block for the desired GPIO. Then, make sure the GPIO pin is configured for *SYSREF_REQ* on the GPIO tab of the GUI. A SYSREF Request can now be issued by toggling the GPIO buttons in the *Pins* section of the *User Controls* tab.

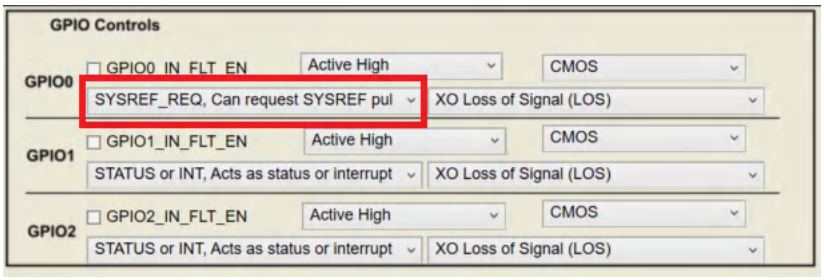

Figure 4-7. GPIO Setting for SYSREF Request

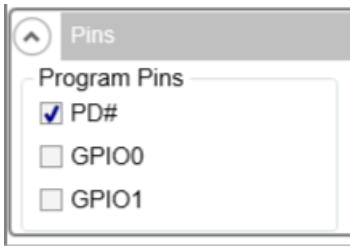

Figure 4-8. GPIO Pin Selection for SYSREF

4.1.5 XO Input

The LMK5B12212 has an XO input (XO pin) to accept a reference clock for the Fractional-N APLLs. The XO input determines the output frequency accuracy and stability in free-run or holdover modes. For synchronization applications like SyncE or IEEE 1588, the XO input is typically driven by a low-frequency TCXO or OCXO that conforms to the frequency accuracy and holdover stability requirements of the application. For proper DPLL operation, the XO frequency must have a non-integer frequency relationship with the VCO output frequency of any APLLs that uses the XO input as the reference. The non-integer relationship must be greater than 0.05 away from an integer boundary (meaning > 0.05 and < 0.95). When configuring the LMK5B12212 as a clock generator (DPLL not used), then the XO frequency can have an integer relationship with the APLL output frequency.

The XO input of the LMK5B12212 has programmable on-chip input termination and AC-coupled input biasing options to support any clock interface type.

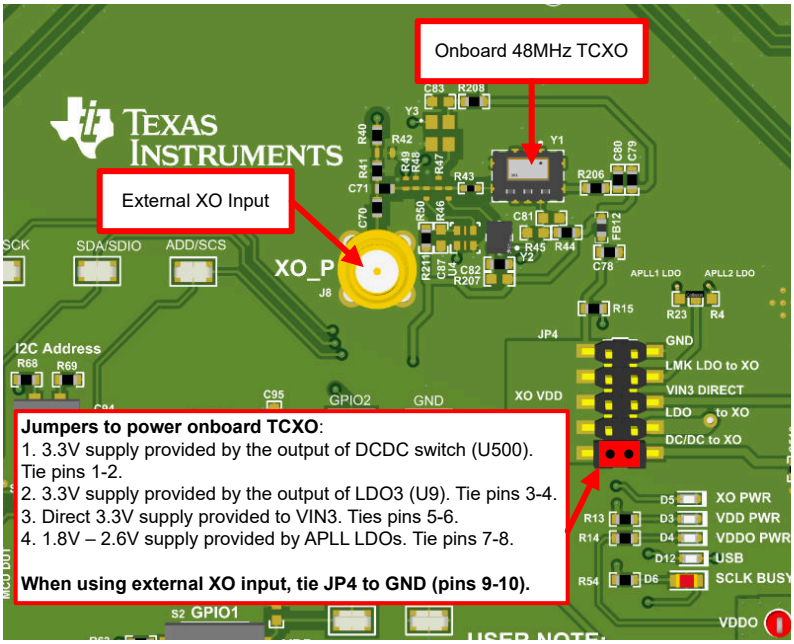

Figure 4-9. XO Input

4.1.5.1 48MHz TCXO (Default)

By default, the EVM is populated with a 48MHz, 3.3V LVCMOS, low-jitter TCXO, designated as Y1 (3.2mm x 2.5mm), which drives the XO input of the LMK5B12212 with the onboard termination and AC coupling. See Figure 4-9. All LMK5B12212 EVMs have a TXC 7N48071001 48MHz TCXO populated on Y1. Y1 can be used to evaluate various frequency configurations.

4.1.5.2 External Clock Input

Another option is to feed an external clock to the SMA port (J8) to drive the XO input. See Figure 4-9. This path can be connected to the XO input pins. Y1 must be powered down when using the external XO input path. To power down Y1 and use an external XO input, the jumper on JP4 must be removed. Suggested XO frequencies for best device performance are frequencies of 38.88MHz and 48MHz.

4.1.5.3 Additional XO Input Options

For flexibility, the EVM provides additional XO input options (use one at a time). C70 allows an external reference to be provided at SMA connector XO (J8). C71 allows one of the onboard XO/TCXO/OCXO footprints to be used.

By default, Y1 is populated with a 48MHz TCXO and selected with the populated R43 and R206. R43 provides the output clock of Y1 to the XO pin of the LMK5B12212 and R206 provides power to Y1.

Y2 (2.5mm × 2.0mm) is populated with TI high-performance 48MHz BAW oscillator LMK6C. This BAW oscillator is not connected to the LMK5B12212. R46 must be populated to provide the output of Y2 to the XO pin.

Additional PCB footprints are available to install alternate components for performance evaluation of specific oscillators. These additional footprints are Y3 (3.2mm × 2.5mm), Y4 (9.7mm × 7.5mm), Y5 (25mm × 22mm), and U4 (2.5mm × 2mm).

When using Y2, Y3, Y4, Y5, or U4, R43 and R206 must be removed to power down and isolate the output of Y1. When populating Y3, R47 must be populated to provide the output of Y3 to the XO pin. When populating Y4, R48 must be populated to provide the output of Y4 to the XO pin. When populating Y5, R49 must be populated to provide the output of Y5 to the XO pin. When populating U4, R50 must be populated to provide the output of U4 to the XO pin. Section 5.1.8 shows the components described above.

Take care if more than one device is installed to remove resistors to power down unused oscillators and isolate the outputs as described above.

4.1.5.4 APLL Reference Options

The LMK5B12212 APLLs can accept any other APLL output as a reference instead of the XO. The BAW on APLL1 provides a good option for a high-frequency cascaded APLL reference. Figure 3-4 shows how to configure the APLL reference to be cascaded from another APLL.

4.1.6 Reference Clock Inputs

The LMK5B12212 has two DPLL reference clock input pairs (IN0_P/N and IN1_P/N) with configurable input priority and input selection modes. The inputs have programmable input type, termination, and biasing options to support any clock interface type.

External LVCMOS or Differential reference clock inputs can be applied to the SMA ports, labeled IN0_P/N and IN1_P/N. All SMA inputs are routed through 50Ω single-ended traces and DC-coupled to the corresponding IN0_P/N and IN1_P/N pins of the LMK5B12212. Single-ended signals must be connected to the noninverting input, IN0_P or IN1_P. EVM default intends IN0 for single-ended input as the IN0_N SMA connector is not populated.

4.1.7 Clock Outputs

The LMK5B12212 has 12 clock output pairs (OUT[0:15]_P/N).

OUT0 is configured as DC-coupled for LVCMOS evaluation purposes. OUT1, OUT2, and OUT3 have 50Ω to GND followed by an AC-coupling capacitor for HCSL evaluation purposes. OUT4 to OUT11 are AC-coupled to the SMA ports for LVDS and HSDS evaluation purposes.

WARNING

DC-coupled clocks must not be directly connected to RF equipment, which can not accept DC voltage greater than 0V. For example, spectrum analyzers and phase noise analyzers.

4.1.8 Status Outputs and LEDS

Status outputs signals can be configured on the GPIO0, GPIO1, and GPIO2 pins. The status output types are 3.3V LVCMOS or NMOS open-drain.

4.1.9 Requirements for Making Measurements

When performing measurements with the LMK5B12212EVM, the following procedures must be completed:

1. Make sure all required outputs have proper termination components installed to match the desired output types. Figure 4-10 shows the recommended output terminations for each output format.

Driver	R_B (Ω)
LVDS	open
HSDS	open
HCSL	50

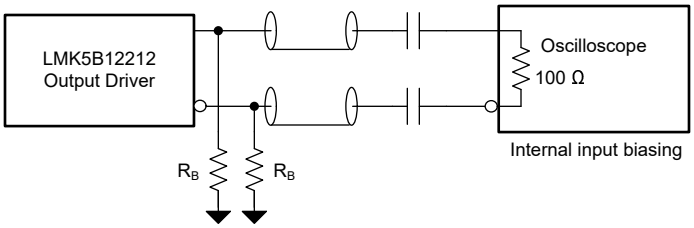

Figure 4-10. Output Termination Recommendations

2. Make sure all enabled outputs that are not connected to any test equipment have a 50Ω SMA termination. Figure 4-11 shows an example of a 50Ω SMA termination.

Figure 4-11. 50Ω SMA Termination

4.2 Typical Phase Noise Characteristics

These plots show the typical phase noise performance for common frequencies outputted from the BAW (VCO1).

The EVM configuration used to obtain these measurements is as follows:

1. XO frequency = 48MHz (Onboard TCXO)
2. Outputs are configured as HSDS outputs following the methods described in Section 4.1.9.

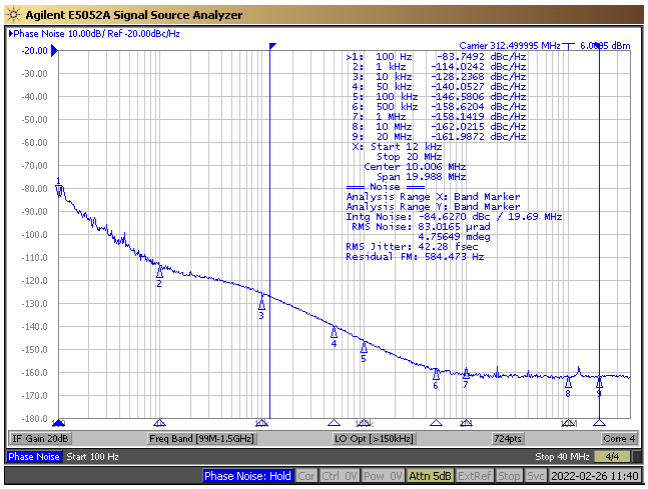

Figure 4-12. APLL1 312.5MHz Phase Noise Performance

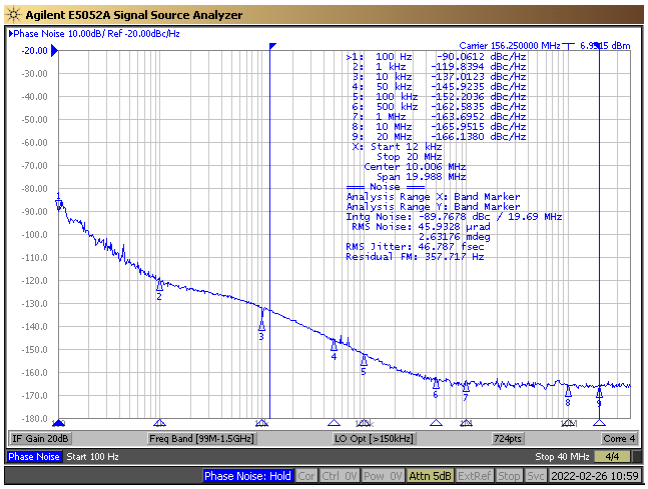

Figure 4-13. APLL1 156.25MHz Phase Noise Performance

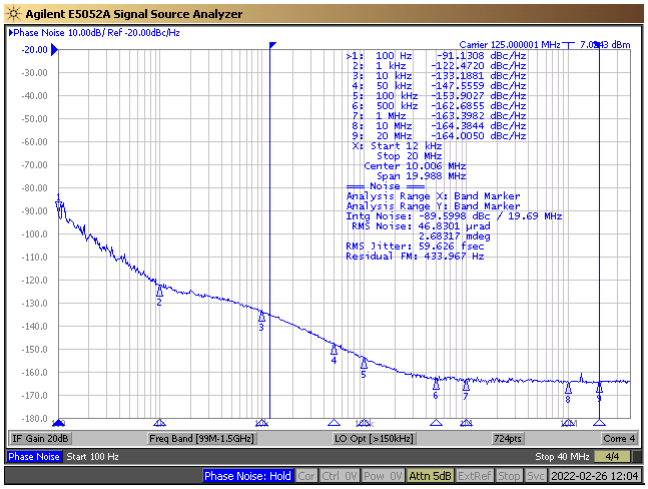

Figure 4-14. APLL1 125MHz Phase Noise Performance

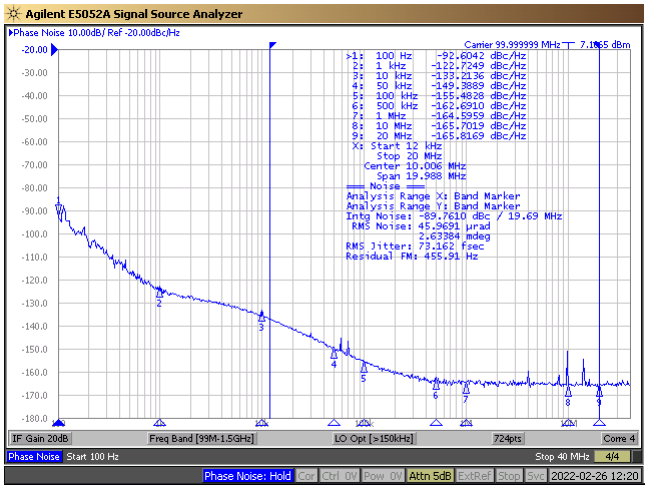

Figure 4-15. APLL1 100MHz Phase Noise Performance

5 Hardware Design Files

5.1 Schematics

5.1.1 Power Supply Schematic

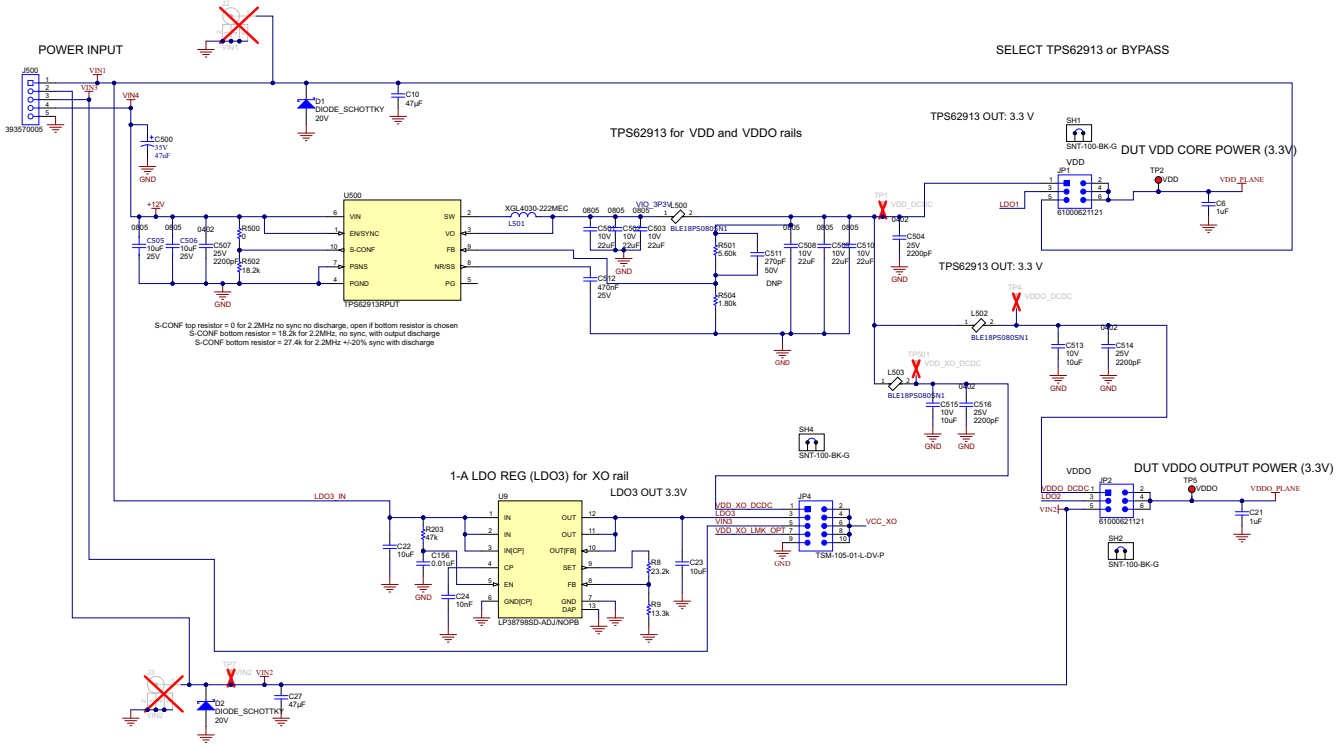

Figure 5-1. Power Supplies

5.1.2 Alternative Power Supply Schematic

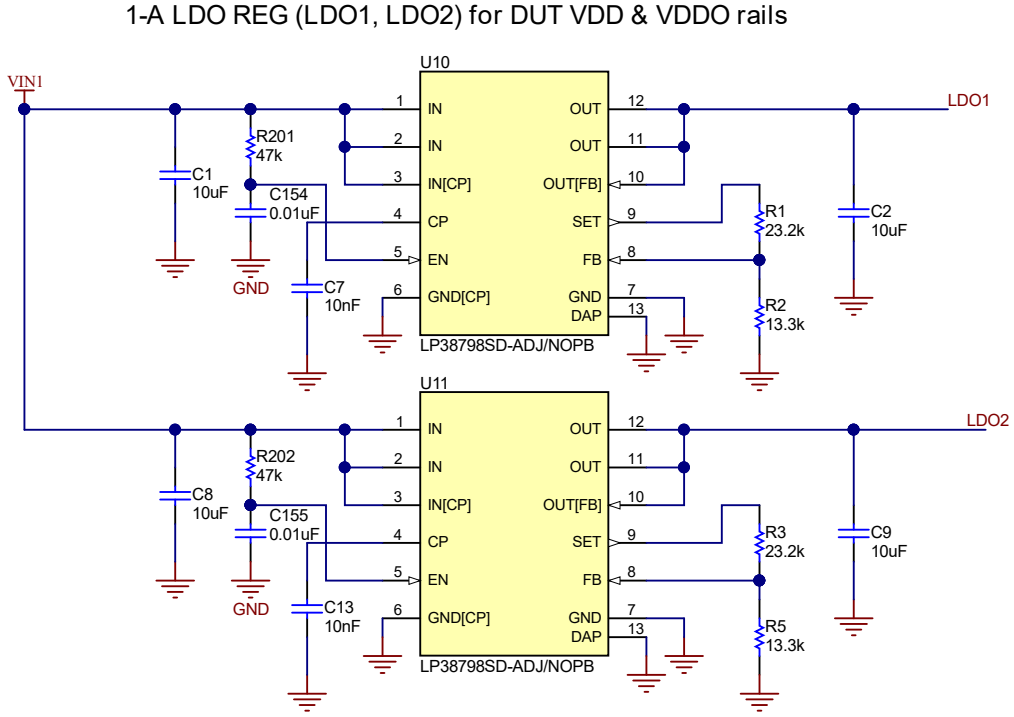

Figure 5-2. Alternative Power Supply

5.1.3 Power Distribution Schematic

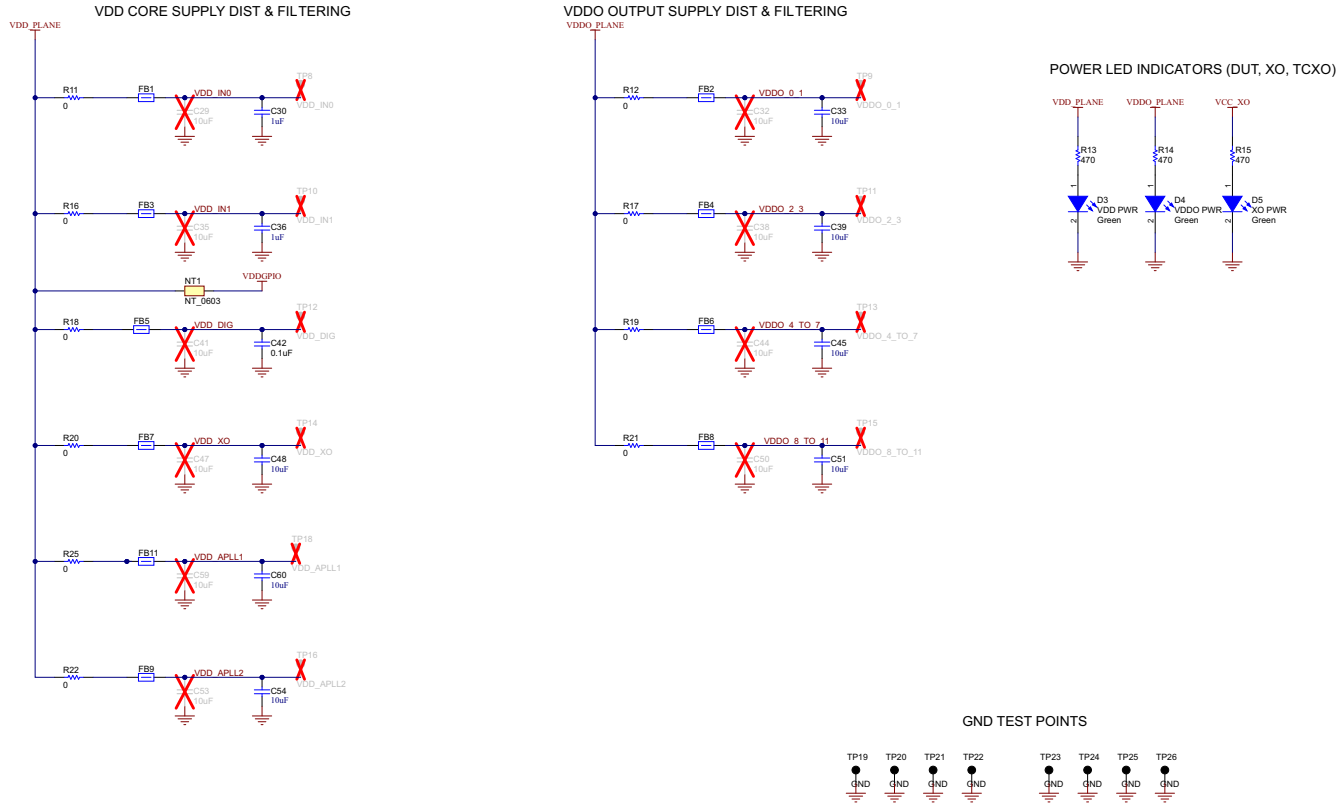

Figure 5-3. Power Distribution

5.1.4 LMK5B12212 and Input References IN0 to IN1 Schematic

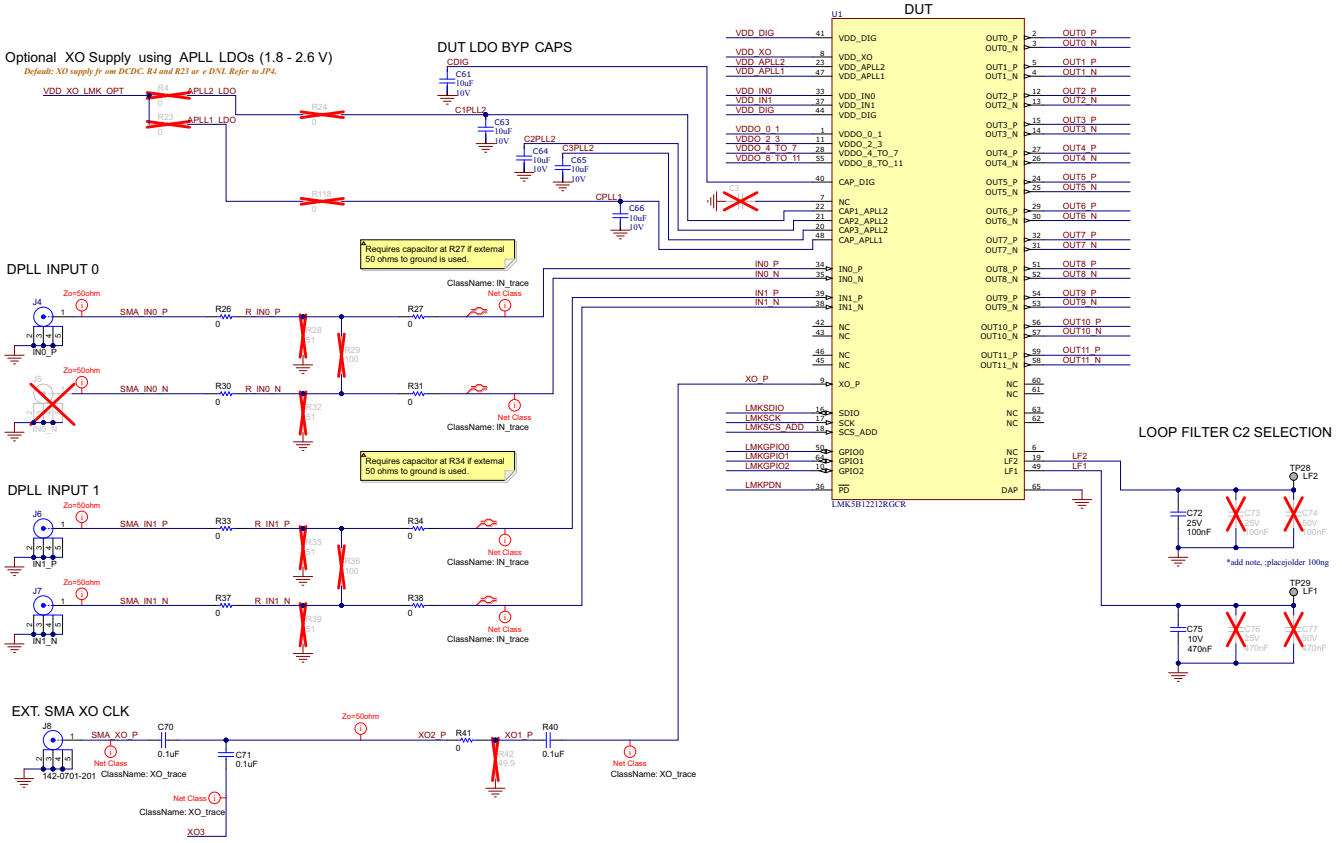

Figure 5-4. LMK5B12212 and Input Reference Inputs IN0 to IN1

5.1.5 Clock Outputs OUT0 to OUT3 Schematic

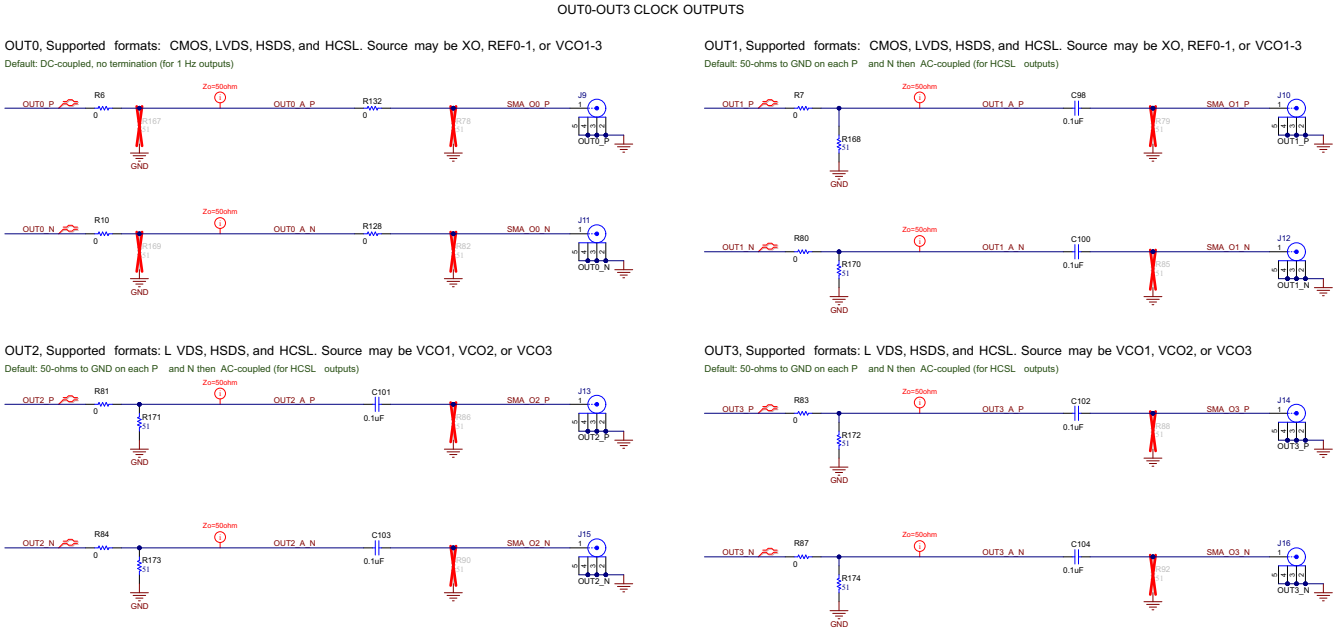

Figure 5-5. Clock Outputs OUT0 to OUT3

5.1.6 Clock Outputs OUT4 to OUT7 Schematic

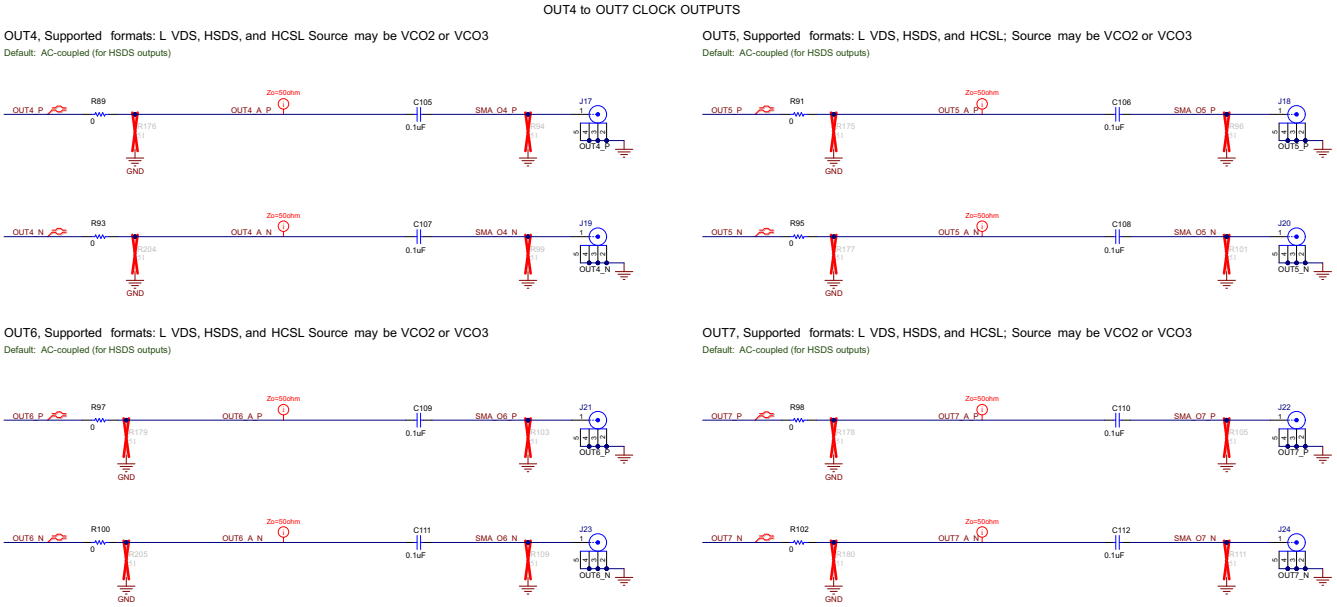

Figure 5-6. Clock Outputs OUT4 to OUT7

5.1.7 Clock Outputs OUT8 to OUT11 Schematic

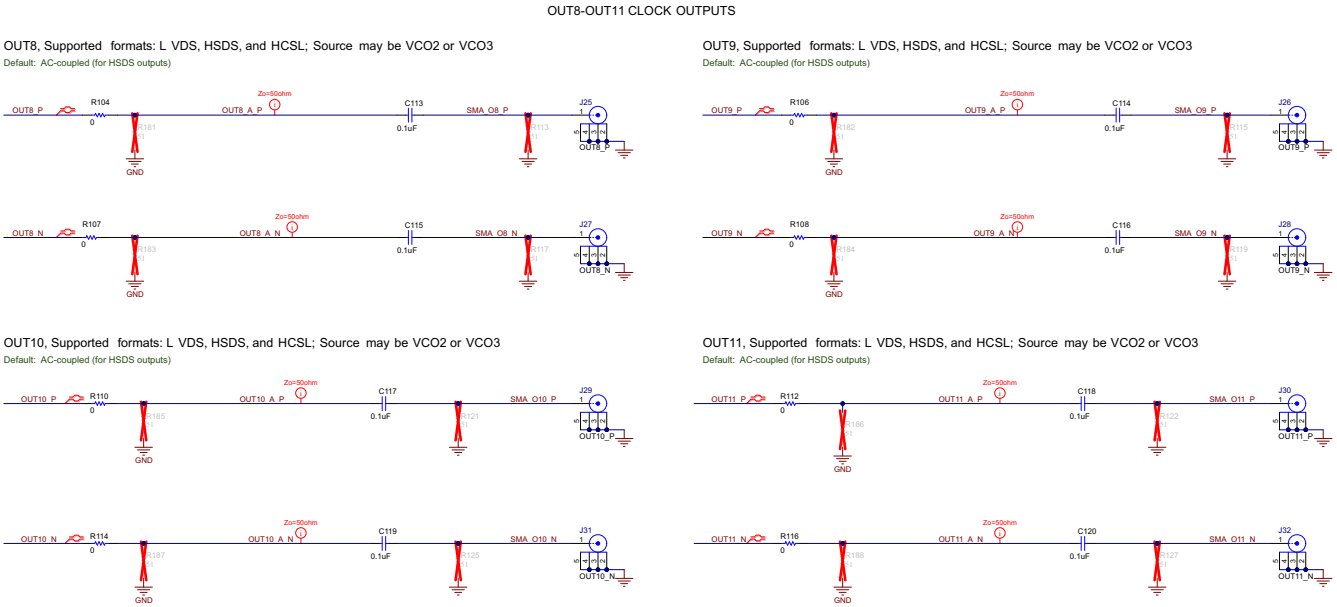

Figure 5-7. Clock Outputs OUT8 to OUT11

5.1.8 XO Schematic

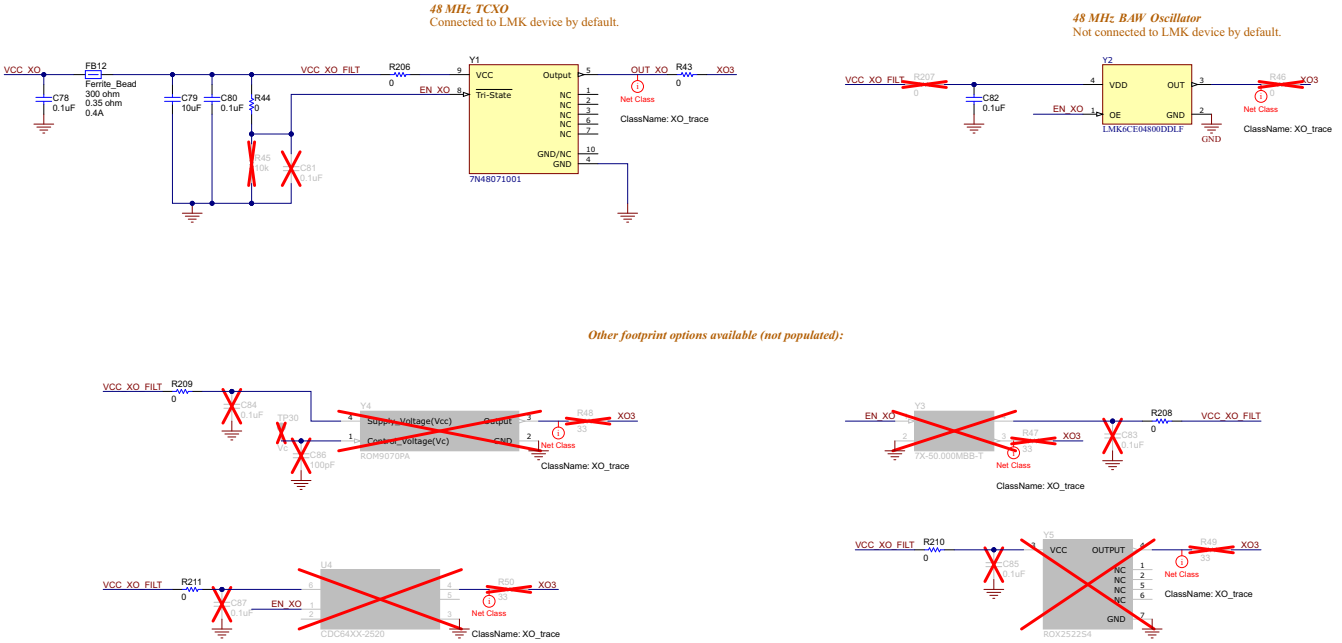

Figure 5-8. XO

5.1.9 Logic I/O Interfaces Schematic

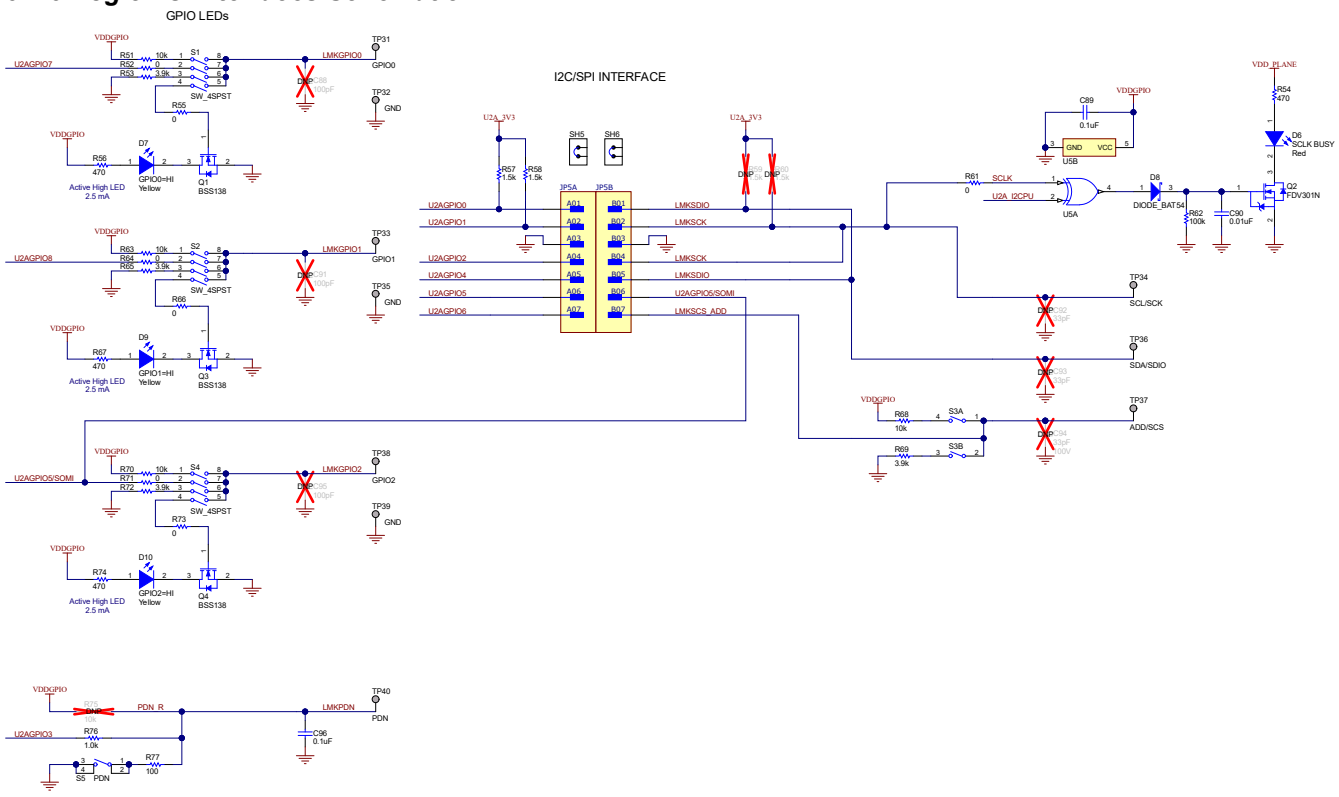

Figure 5-9. Logic I/O Interfaces

5.1.10 USB2ANY Schematic

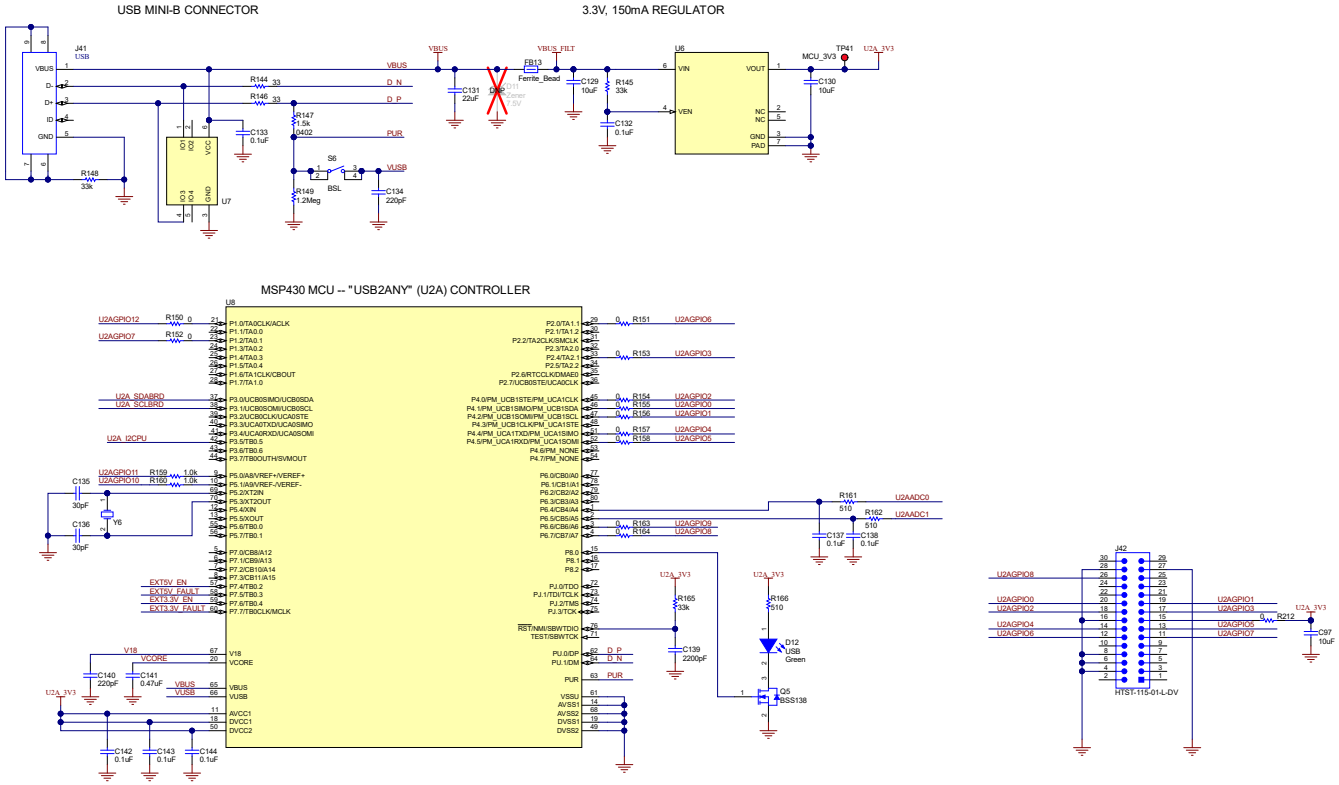

Figure 5-10. USB MCU

5.2 PCB Layouts

5.2.1 Layout Guidelines

- Isolate input, XO/OCXO/TCXO and output clocks from adjacent clocks with different frequencies and other nearby dynamic signals.
- Consider the XO/OCXO/TCXO placement and layout in terms of the supply/ground noise and thermal gradients from nearby circuitry (for example, power supplies, FPGA, ASIC) as well as system-level vibration and shock. These factors can affect the frequency stability/accuracy and transient performance of the oscillator.
- Avoid impedance discontinuities on controlled-impedance 50Ω single-ended (or 100Ω differential) traces for clock and dynamic logic signals.
- Place bypass capacitors close to the VDD and VDDO pins on the same side as the IC, or directly below the IC pins on the opposite side of the PCB. Larger decoupling capacitor values can be placed further away.
- Place external capacitors close to the CAP_x and LFx pins.
- Use multiple vias to connect wide supply traces to the respective power islands or planes if possible.
- Use at least a 6×6 through-hole via pattern to connect the IC ground/thermal pad to the PCB ground planes.
- See the Land Pattern Example, Solder Mask Details, and Solder Paste Example in *Mechanical, Packaging, and Orderable Information* section.

5.2.2 Layout Example

Below are printed circuit board (PCB) layout examples that show the application of thermal design practices and a low-inductance ground connection between the device DAP and the PCB. Place the ground return path for the supply decoupling capacitors close to the DAP. All OUTx pairs configured as differential signals must be routed differentially and meet the trace impedance requirements (typically 100 ohm differential).

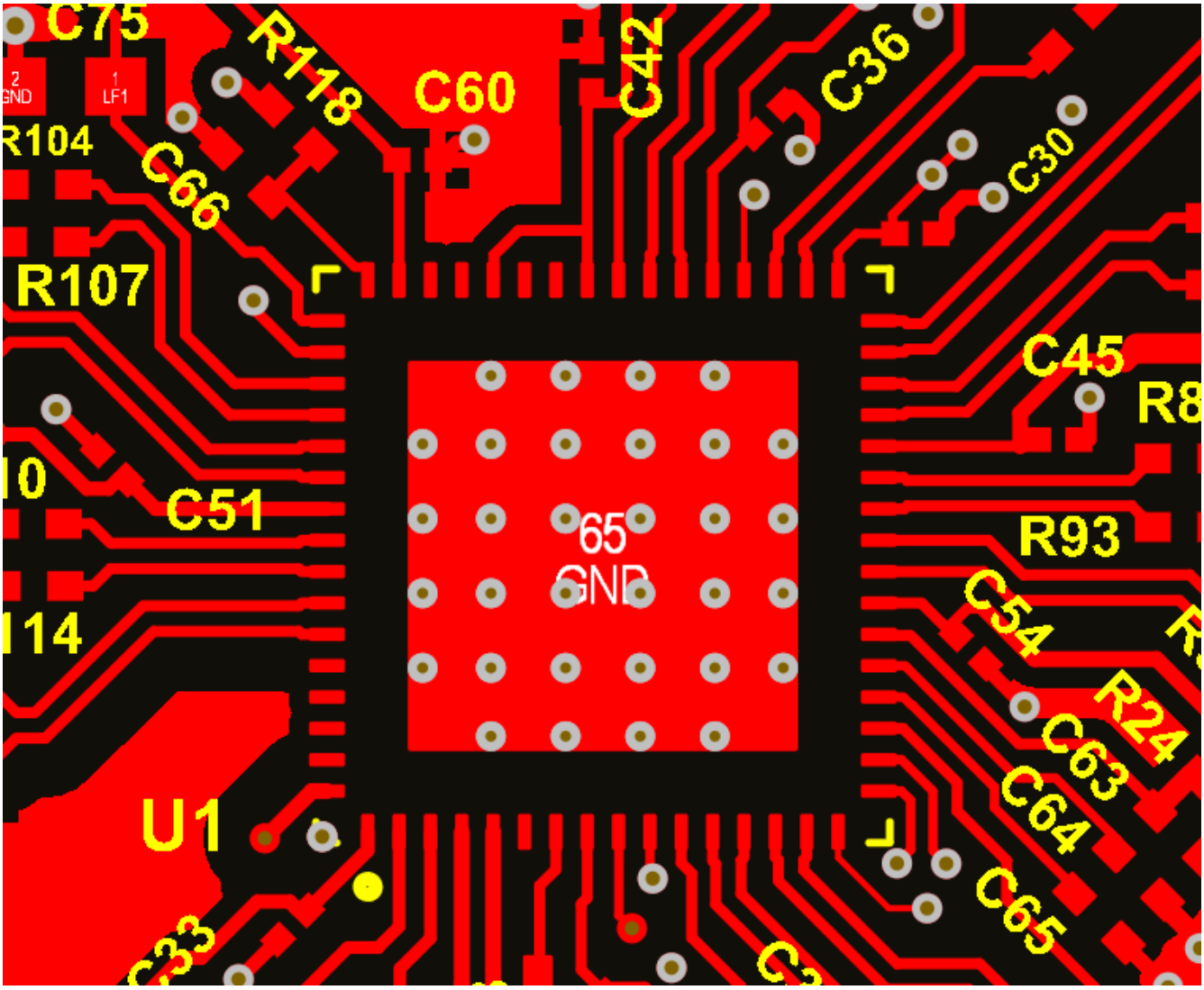

Figure 5-11. PCB Layout Example for LMK5B12212, Top Layer

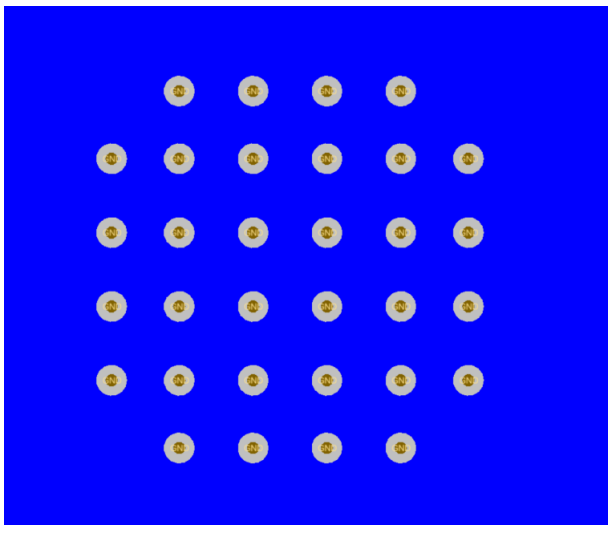

Figure 5-12. PCB Layout Example for LMK5B12212, Bottom Layer

5.2.3 Thermal Reliability

The LMK5B12212 is a high-performance device. To provide good electrical and thermal performance, TI recommends to design a thermally-enhanced interface between the IC ground or thermal pad and the PCB ground using at least a 6×6 through-hole through pattern connected to multiple PCB ground layers (see Figure 5-13).

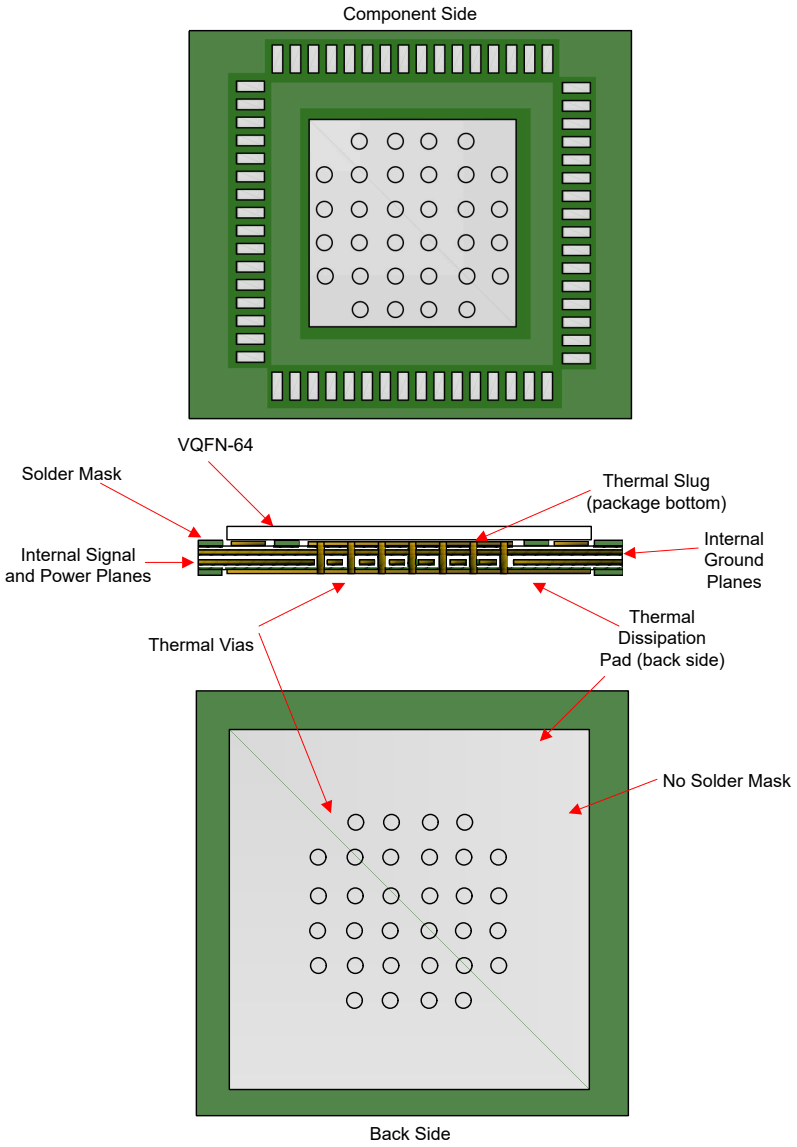

Figure 5-13. General PCB Ground Layout for Thermal Reliability (8+ Layers Recommended)

5.3 Bill of Materials (BOM)

Table 5-1. Bill of Materials (BOM)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER
C1, C2, C7, C8, C9, C13, C22, C23, C24, C79, C97, C129, C130	13	10uF	CAP, CERM, 10 uF, 10 V, +/- 20%, X5R, 0603	C1608X5R1A106M080AC	TDK
C3	0	10µF	10 µF ±20% 10V Ceramic Capacitor X5R 0402 (1005 Metric)	KGM05CR51A106MH	KYOCERA AVX
C6, C21	2	1uF	CAP, CERM, 1 uF, 10 V, +/- 10%, X5R, 0603	C0603C105K8PACTU	Kemet
C10, C27	2	47uF	CAP, CERM, 47 µF, 10 V,+/- 20%, X5R, 0805	GRM21BR61A476ME15L	MuRata
C29, C32, C35, C38, C41, C44, C47, C50, C53, C59	0	10uF	CAP, CERM, 10 uF, 10 V, +/- 20%, X5R, 0603	C1608X5R1A106M080AC	TDK
C30, C36	2	1uF	CAP, CERM, 1 uF, 10 V,+/- 10%, X6S, 0402	GRM155C81A105KA12D	MuRata
C33, C39, C45, C48, C51, C54, C60	7	10uF	CAP, CERM, 10 uF, 10 V, +/- 20%, X5R, 0402	GRM155R61A106ME11D	MuRata
C42	1	0.1uF	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X5R, 0402	C1005X5R1A104K050BA	TDK
C61, C63, C64, C65, C66	5	10µF	10 µF ±20% 10V Ceramic Capacitor X5R 0402 (1005 Metric)	KGM05CR51A106MH	KYOCERA AVX
C70, C71, C72, C78, C80, C82, C96, R40	8	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	C0603C104J3RACTU	Kemet
C73, C76	0	0.047uF	CAP, CERM, 0.047 µF, 25 V,+/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0805	C0805C473J3GACTU	Kemet
C74, C77	0	0.1uF	CAP, CERM, 0.1 µF, 50 V,+/- 5%, C0G/NP0, 1210	C3225C0G1H104J250AA	TDK
C75, C141	2	0.47uF	CAP, CERM, 0.47 uF, 10 V, +/- 10%, X7R, 0603	GRM188R71A474KA61D	MuRata
C81, C83, C84, C85, C87	0	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	C0603C104J3RACTU	Kemet
C86, C88, C91, C95	0	100pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	06035A101JAT2A	AVX
C89, C132, C133, C137, C138, C142, C143, C144	8	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 5%, X7R, 0603	C0603C104J4RACTU	Kemet
C90, C154, C155, C156	4	0.01uF	CAP, CERM, 0.01 uF, 50 V, +/- 5%, X7R, 0603	C0603C103J5RACTU	Kemet
C92, C93, C94	0	33pF	CAP, CERM, 33 pF, 100 V, +/- 5%, C0G/NP0, 0603	06031A330JAT2A	AVX
C98, C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C110, C111, C112, C113, C114, C115, C116, C117, C118, C119, C120	22	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0402	GRM155R71E104KE14D	MuRata
C131	1	22uF	CAP, CERM, 22 uF, 10 V, +/- 20%, X5R, 0805	LMK212BJ226MG-T	Taiyo Yuden
C134, C140	2	220pF	CAP, CERM, 220 pF, 50 V, +/- 1%, C0G/NP0, 0603	06035A221FAT2A	AVX

Table 5-1. Bill of Materials (BOM) (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER
C135, C136	2	30pF	CAP, CERM, 30 pF, 100 V, +/- 5%, C0G/NP0, 0603	GRM1885C2A300JA01D	MuRata
C139	1	2200pF	CAP, CERM, 2200 pF, 50 V, +/- 10%, X7R, 0603	C0603C222K5RACTU	Kemet
C500	1	47uF	CAP, TA, 47 uF, 35 V, +/- 10%, 0.3 ohm, SMD	T495X476K035ATE300	Kemet
C501, C502, C503, C508, C509, C510	6	22uF	CAP, CERM, 22 uF, 10 V, +/- 20%, X7S, 0805	C2012X7S1A226M125AC	TDK
C504, C507, C514, C516	4	2200pF	CAP, CERM, 2200 pF, 25 V, +/- 10%, X7R, 0402	GRM155R71E222KA01D	MuRata
C505, C506	2		10µF ±10% 25V Ceramic Capacitor X7S 0805 (2012 Metric)	C2012X7S1E106K125AC	TDK
C511	1		CAP CER 270PF 50V NP0 0402	UMK105CG271JV-F	Taiyo Yuden
C512	1	0.47uF	CAP, CERM, 0.47 µF, 25 V,+/- 10%, X7R, 0603	C1608X7R1E474K080AE	TDK
C513, C515	2	10uF	CAP, CERM, 10 uF, 10 V, +/- 20%, X7R, 0603	GRM188Z71A106MA73D	MuRata
D1, D2	2	20V	Diode, Schottky, 20 V, 2 A, SMA	B220A-13-F	Diodes Inc.
D3, D4, D5, D12	4	Green	LED, Green, SMD	LTST-C190GKT	Lite-On
D6	1	Red	LED, Red, SMD	LTST-C170KRKT	Lite-On
D7, D9, D10	3	Yellow	LED, Yellow , SMD	LTST-C170KSKT	Lite-On
D8	1	30V	Diode, Schottky, 30 V, 0.2 A, SOT-23	BAT54-7-F	Diodes Inc.
D11	0	7.5V	Diode, Zener, 7.5 V, 550 mW, SMB	1SMB5922BT3G	ON Semiconductor
FB1, FB2, FB3, FB4, FB5, FB6, FB7, FB8, FB9, FB11	10	220 ohm	Ferrite Bead, 220 ohm @ 100 MHz, 2.5 A, 0603	BLM18SG221TN1D	MuRata
FB12	1	300 ohm	Ferrite Bead, 300 ohm @ 100 MHz, 0.4 A, 1.6x0.8x0.95mm	LI0603D301R-10	Laird-Signal Integrity Products
FB13	1	60 ohm	Ferrite Bead, 60 ohm @ 100 MHz, 3.5 A, 0603	MPZ1608S600ATAH0	TDK
FID1, FID2, FID3, FID4, FID5, FID6	6		Fiducial mark. There is nothing to buy or mount.	N/A	N/A
H1, H2, H3, H4, H5, H6	6		BUMPER CYLIN 0.312" DIA	SJ61A6	3M
J2, J3, J5	0		CONN SMA JACK STR EDGE MNT	CON-SMA-EDGE-S	RF Solutions Ltd.
J4, J6, J7, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, J28, J29, J30, J31, J32	27		CONN SMA JACK STR EDGE MNT	CON-SMA-EDGE-S	RF Solutions Ltd.
J8	1		Connector, SMA, TH	142-0701-201	Cinch Connectivity
J41	1		Connector, Receptacle, Mini-USB Type B, R/A, Top Mount SMT	1734035-2	TE Connectivity
J42	1		Header, 2.54mm, 15x2, Gold, SMD	HTST-115-01-L-DV	Samtec
J500	1		Terminal Block, 3.5mm, 5x1, Tin, TH	393570005	Molex
JP1, JP2	2		Header, 2.54mm, 3x2, Gold, SMT	61000621121	Wurth Elektronik
JP4	1		Header, 2.54mm, 5x2, Gold, SMT	TSM-105-01-L-DV-P	Samtec
JP5	1		Connector Header Surface Mount 14 position 0.100" (2.54mm)	54202-G0807LF	Amphenol ICC
L500, L502, L503	3		Bead inductor BLE series, 8A	BLE18PS080SN1	Murata

Table 5-1. Bill of Materials (BOM) (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER
L501	1		Inductor Power Shielded Wirewound 2.2uH 20% 1MHz Composite 8.7A 15mOhm DCR Automotive T/R	XGL4030-222MEC	Coilcraft
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	THT-14-423-10	Brady
Q1, Q3, Q4, Q5	4	50V	MOSFET, N-CH, 50 V, 0.22 A, SOT-23	BSS138	Fairchild Semiconductor
Q2	1	25V	MOSFET, N-CH, 25 V, 0.22 A, SOT-23	FDV301N	Fairchild Semiconductor
R1, R3, R8	3	23.2k	RES, 23.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060323K2FKEA	Vishay-Dale
R2, R5, R9	3	13.3k	RES, 13.3 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060313K3FKEA	Vishay-Dale
R4, R23	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	ERJ-3GEY0R00V	Panasonic
R6, R7, R10, R80, R81, R83, R84, R87, R89, R91, R93, R95, R97, R98, R100, R102, R104, R106, R107, R108, R110, R112, R114, R116, R128, R132	26	0	RES, 0, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	RK73Z1ETTP	KOA Speer
R11, R12, R16, R17, R18, R19, R20, R21, R22, R25, R41, R52, R55, R61, R64, R66, R71, R73, R150, R151, R152, R153, R154, R155, R156, R157, R158, R163, R164, R212	30	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06030000Z0EA	Vishay-Dale
R13, R14, R15, R54, R56, R67, R74	7	470	RES, 470, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603470RJNEA	Vishay-Dale
R24, R46, R118	0	0	RES, 0, 0%, 0.2 W, AEC-Q200 Grade 0, 0402	CRCW04020000Z0EDHP	Vishay-Dale
R26, R27, R30, R31, R33, R34, R37, R38, R43	9	0	RES, 0, 0%, 0.2 W, AEC-Q200 Grade 0, 0402	CRCW04020000Z0EDHP	Vishay-Dale

Table 5-1. Bill of Materials (BOM) (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER
R28, R32, R35, R39, R78, R79, R82, R85, R86, R88, R90, R92, R94, R96, R99, R101, R103, R105, R109, R111, R113, R115, R117, R119, R121, R122, R125, R127, R167, R169, R175, R176, R177, R178, R179, R180, R181, R182, R183, R184, R185, R186, R187, R188, R204, R205	0	51	RES, 51, 5%, 0.0625 W, 0402	RC0402JR-0751RL	Yageo America
R29, R36	0	100	RES, 100, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603100RFKEA	Vishay-Dale
R42	0	49.9	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060349R9FKEA	Vishay-Dale
R44, R500	2	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	ERJ-3GEY0R00V	Panasonic
R45, R75	0	10k	RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060310K0JNEA	Vishay-Dale
R47, R48, R49, R50	0	33	RES, 33, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW040233R0JNED	Vishay-Dale
R51, R63, R68, R70	4	10k	RES, 10 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060310K0JNEA	Vishay-Dale
R53, R65, R69, R72	4	3.9k	RES, 3.9 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06033K90JNEA	Vishay-Dale
R57, R58	2	1.5k	RES, 1.5 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031K50JNEA	Vishay-Dale
R59, R60	0	1.5k	RES, 1.5 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031K50JNEA	Vishay-Dale
R62	1	100k	RES, 100 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603100KJNEA	Vishay-Dale
R76, R159, R160	3	1.0k	RES, 1.0 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031K00JNEA	Vishay-Dale
R77	1	100	RES, 100, 5%, 0.25 W, AEC-Q200 Grade 0, 0603	ESR03EZPJ101	Rohm
R144, R146	2	33	RES, 33, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW040233R0JNED	Vishay-Dale
R145, R148, R165	3	33k	RES, 33 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060333K0JNEA	Vishay-Dale
R147	1	1.5k	RES, 1.5 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW04021K50JNED	Vishay-Dale
R149	1	1.2Meg	RES, 1.2 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031M20JNEA	Vishay-Dale
R161, R162, R166	3	510	RES, 510, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603510RJNEA	Vishay-Dale
R168, R170, R171, R172, R173, R174	6	51	RES, 51, 5%, 0.0625 W, 0402	RC0402JR-0751RL	Yageo America
R201, R202, R203	3	47k	RES, 47 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060347K0JNEA	Vishay-Dale

Table 5-1. Bill of Materials (BOM) (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER
R206, R208, R209, R210, R211	5	0	RES, 0, 5%, 0.1 W, 0603	RC0603JR-070RL	Yageo
R207	0	0	RES, 0, 5%, 0.1 W, 0603	RC0603JR-070RL	Yageo
R501	1	5.60k	RES, 5.60 k, 0.1%, 0.1 W, 0603	RG1608P-562-B-T5	Susumu Co Ltd
R502	1	18.2k	RES, 18.2 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060318K2FKEA	Vishay-Dale
R504	1	1.80k	RES, 1.80 k, 0.1%, 0.1 W, 0603	RT0603BRD071K8L	Yageo America
S1, S2, S4	3		Switch, SPST 4 Pos, Top Actuated, SMT	219-4LPST	CTS Electrocomponents
S3	1		Switch, Slide, SPST 2 poles, SMT	219-2LPST	CTS Electrocomponents
S5, S6	2		Switch, Tactile, SPST-NO, 0.05A, 12V, SMT	FSM4JSMA	TE Connectivity
SH1, SH2, SH4, SH5, SH6	5	1x2	Shunt, 100mil, Gold plated, Black	SNT-100-BK-G	Samtec
TP1, TP4, TP7, TP501	0		Test Point, Miniature, Red, TH	5000	Keystone
TP2, TP5, TP41	3		Test Point, Miniature, Red, TH	5000	Keystone
TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26	8		Test Point, Miniature, Black, TH	5001	Keystone
TP30	0		Test Point, Miniature, SMT	5019	Keystone
TP31, TP32, TP33, TP34, TP35, TP36, TP37, TP38, TP39, TP40	10		Test Point, Miniature, SMT	5019	Keystone
U1	1		Ultra-Low Jitter Clock Synchronizer with JESD204B/C and BAW for Wired Communications	LMK5B12212RGCR	Texas Instruments
U4	0		CDC64XX-2520, DLF0006A (VSON-6)	CDC64XX-2520	Texas Instruments
U5	1		Single 2-Input Exclusive-OR Gate, DBV0005A (SOT-23-5)	SN74LVC1G86DBVR	Texas Instruments
U6	1		150-mA Ultra-Low Noise LDO for RF and Analog Circuits Requires No Bypass Capacitor, NGF0006A (WSON-6)	LP5900SD-3.3/NOPB	Texas Instruments
U7	1		4-Channel ESD Protection Array for High-Speed Data Interfaces, DRY0006A (USON-6)	TPD4E004DRYR	Texas Instruments
U8	1		25 MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85 degC, 80-pin QFP (PN), Green (RoHS & no Sb/Br)	MSP430F5529IPN	Texas Instruments
U9, U10, U11	3		800-mA Ultra-Low-Noise, High-PSRR LDO, DNT0012B (WSON-12)	LP38798SD-ADJ/NOPB	Texas Instruments
U500	1		3A Low Noise and Low Ripple buck converter, RPU0010A (VQFN-10)	TPS62913RPUT	Texas Instruments
Y1	1		SMD TCXO 7.0 * 5.0 48.000000MHz	7N48071001	TXC
Y2	1		High-Performance BAW Oscillator, LVCMOS; <1ps, +/- 50ppm; 2.5V/3.3V, -40C to 105C and DLE package	LMK6CE04800DDLF	Texas Instruments
Y3	0		Crystal, Sealed Locked 50 MHz, 15pF, SMD	7X-50.000MBB-T	TXC Corporation

Table 5-1. Bill of Materials (BOM) (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER
Y4	0		MERCURY+ 38.88MHz OCXO CMOS Oscillator 2.7 ~ 5V 4-SMD	ROM9070PA	Rakon
Y5	0		STANDARD OCXO 10MHz Frequency	ROX2522S4	Rakon
Y6	1		Crystal, 24.000 MHz, 20pF, SMD	ECS-240-20-5PX-TR	ECS Inc.

5.3.1 Loop Filter and Vibration Nonsensitive Capacitors

The capacitors used on the EVM use are X7R, which are ferromagnetic and, therefore, sensitive to vibration due to the piezoelectric effect. TI recommends to use non-ferromagnetic capacitors such as NP0, C0G, or Tantalum for applications in which the best performance is required in the presence of vibration.

At and below 47nF, C0G/NP0 capacitors are available in 0805 sized packages. For values 0.1µF and above Tantalum capacitors can be considered for vibration immune loop filter components.

Table 5-2. Examples of Substitute Capacitors Which are Vibration Immune

CAPACITOR VALUE	VIBRATION SENSITIVE, X7R	VIBRATION IMMUNE
3.3nF	C0603C332K5RACTU, 0603	GRM1885C1H332JA01D, C0G/NP0, 0603
33nF	C0603C333J3RACTU, 0603	C2012C0G1H333J125AA, C0G/NP0, 0805
47nF	06035C473JAT2A, 0603	C0805X473G3GEC7800, C0G/NP0, 0805 C0805C473J3GACTU, C0G/NP0, 0805
0.1µF	C0603C104J3RACTU, 0603	GRM31C5C1E104JA01L, C0G/NP0, 1206 TAJR104K020RNJ, Tantalum, 0805
0.47µF	GRM188R71A474KA61D, 0603	F921C474MPA, Tantalum, 0805

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2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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