Application Report
SNLA101A–March 2008–Revised April 2013

AN-1794 Using RMII Master Mode

ABSTRACT

Texas Instruments PHYTER® family of products incorporate the Reduced Media Independent Interface (RMII) as described in the RMII revision 1.2 specification from the RMII Consortium. This interface may be used to connect a PHY device to a MAC in 10/100 Mb/s systems using a reduced number of pins relative to standard MII. In this mode, data is transferred two bits at a time using a 50 MHz reference clock for both transmit and receive MAC interfaces.

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1 Introduction

The main advantage of RMII over standard MII is the reduced number of interface signals. This can improve printed circuit board (PCB) routing, and allows a PHY ASIC to be designed in a smaller package.

A disadvantage to standard RMII is the requirement for an Elasticity Buffer in the receiver. This requirement is due to the fact that the Receive Data interface signals in RMII are synchronous to the local reference clock instead of the recovered Receive Clock present in standard MII. The Elasticity Buffer serves as a FIFO between the recovered clock and the RMII reference clock and is used to prevent loss of data due to slight frequency mismatches between the two clocks.

The presence of the Elasticity Buffer introduces an uncertainty in the latency of the PHY receive datapath; this may be undesirable for systems requiring a high degree of determinism in the overall latency. As shown in Figure 1, the maximum supported packet size is a linear function of the nominal FIFO latency (bit depth).

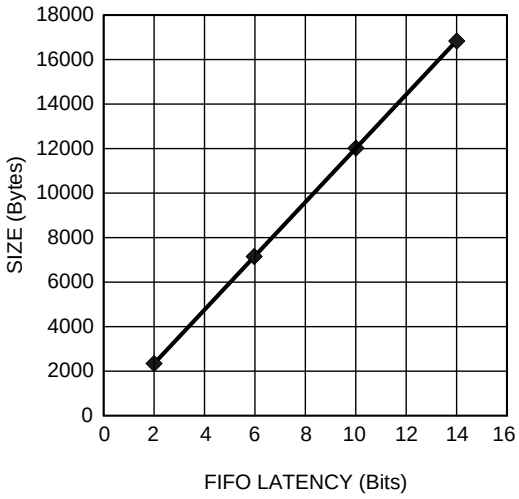

Figure 1. FIFO Latency vs. Maximum Packet Size

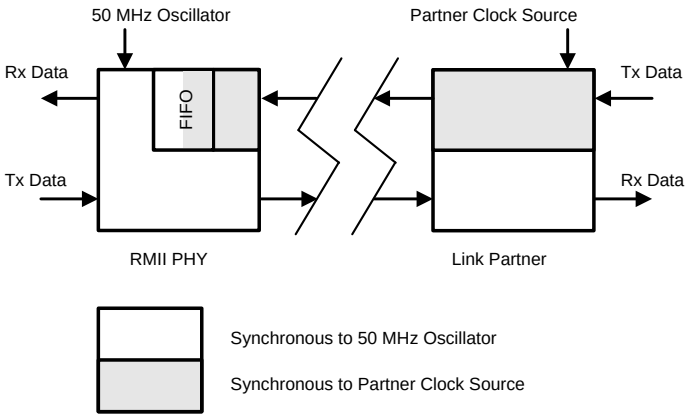

Figure 2. Standard RMII System Diagram

In the system shown in Figure 2, the MAC interface of the PHY device is operating in RMII mode. The mode of the Link Partner's MAC interface is immaterial to this discussion and is shown as MII for simplicity. As indicated in the diagram, there are two logical clock domains in a system comprising two linked physical layer devices: one synchronous to the 50 MHz oscillator and one synchronous to the partner clock source. The receiver of both devices recovers the frequency of its partner's local clock. In an RMII physical layer device, the MAC receive data interface is synchronous to the same clock as the MAC transmit data interface, i.e. the local 50 MHz oscillator.

This application report introduces two advanced features in Ti's DP83640 precision PHYTER® that address system clock distribution and synchronization issues.

2 RMII Master Mode

Texas Instruments DP83640 precision PHYTER® device implements a proprietary MAC interface mode known as RMII Master mode. In this mode, the 50 MHz Oscillator is replaced with a 25 MHz crystal, and the device generates three 50 MHz RMII reference clocks as outputs.

For more detail on the MAC/PHY interface, see *AN-1405 DP83848 Single 10/100 Mb/s Ethernet Transceiver Reduced Media Independent Interface™ (RMII™) Mode* (SNLA076).

A connection diagram is shown in Figure 3. The 50 MHz RMII clock is output on the RX_CLK, TX_CLK, and CLK_OUT pins. Note that the RMII Master mode is compatible with the standard RMII mode; therefore, it can be used with any MAC that has an RMII interface and an external 50 MHz RMII reference clock.

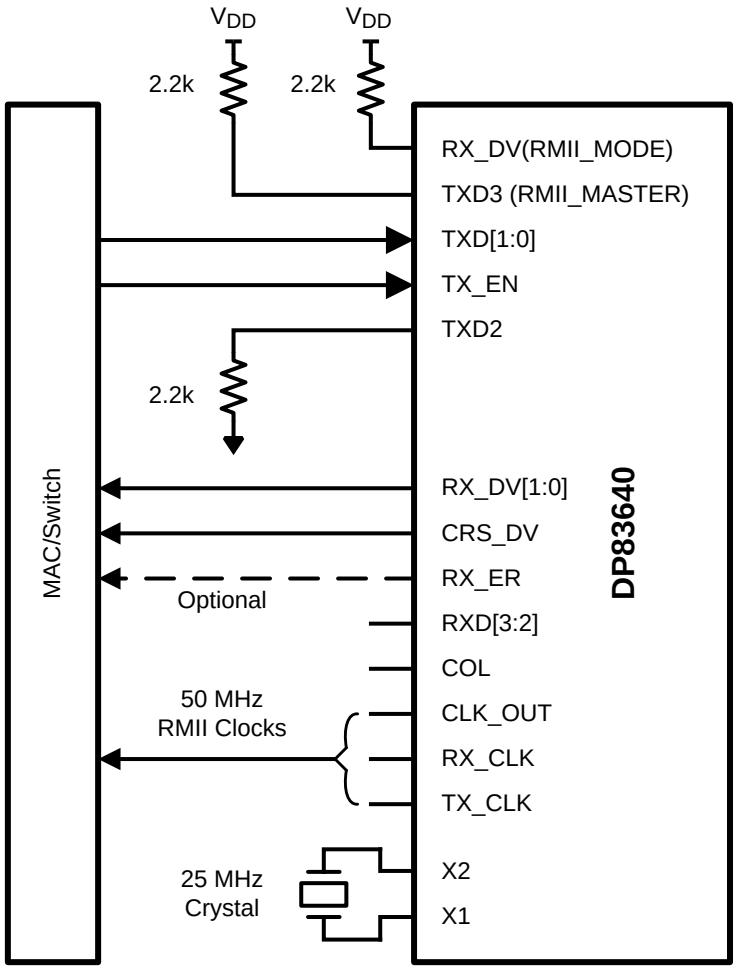

Figure 3. RMII Master Connection Diagram

There are three advantages to this setup:

- The system Bill of Materials (BOM) cost is reduced by the selection of a 25 MHz crystal instead of a 50 MHz oscillator.
- The extra 50 MHz clock outputs may be used as references for other system devices, thereby, reducing requirements for external clock buffering and further reducing the BOM cost.
- The MAC interface can be switched between RMII and MII modes with no component changes (50 MHz or 25 MHz clock sources). In addition, the DP83640 provides the transmit and receive data

reference clocks on the TX_CLK and RX_CLK signals in either MII or RMII mode. This can simplify the MAC design.

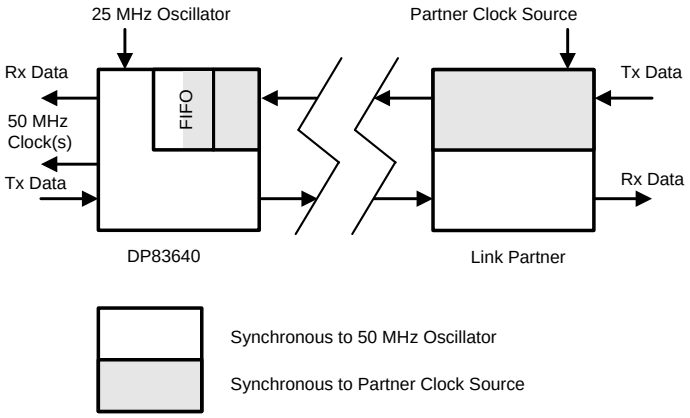

Figure 4. RMII Master System Diagram

The difference between the systems shown in Figure 2 and Figure 4 is the 50 MHz RMII reference clock source. In Figure 2, an external 50 MHz oscillator generates the clock, while in Figure 4 the DP83640 device takes a 25 MHz crystal input and generates the 50 MHz clock for use by both itself and the MAC. Note that since there are two logical clock domains in the system, the Elasticity Buffer is still required between the two domains in the receiver. However, since the IEEE-1588 Receive Timestamp Unit is prior to the Elasticity Buffer in the receive datapath, the Elasticity Buffer has no effect on the determinism of the captured timestamps.

2.1 Configuring RMII Master Mode

RMII Master mode may be configured in one of two ways:

- Strap the mode at power-up by pulling the RMII_MODE and RMII_MASTER straps high, or

1. Write 0x0 to Register 0x13 (PAGESEL).
2. Set bits 14 (RMII_MASTER) and 5 (RMII_MODE) to 1 in Register 0x17 (RBR).

In addition, if the CLK_OUT pin is to be used as a 50 MHz RMII clock, the default PTP clock output function must be disabled by clearing bit 15 (PTP_CLKOUT_EN) in register 0x14 (PTP_COC).

3 100Mb/s Synchronous Ethernet With RMII Master

In addition to RMII Master mode, Texas Instruments DP83640 precision PHYTER® implements a clocking option known as synchronous Ethernet mode, which is available in 100Mb/s operation, in which the reference clock for the transmitter is derived directly from the recovered receive clock.

For more information about synchronous Ethernet mode, see *AN-1730 DP83640 Synchronous Ethernet Mode: Achieving Sub-Nanosecond Accuracy in PTP Applications* (SNLA100).

As shown in Figure 5, the resulting system has only one logical clock domain. Therefore, the effects of the receive FIFO (latency non-determinism and packet size limiting) are eliminated. Note that the partner can be any 100Mb PHY and must not be operating in synchronous Ethernet mode since a master clock reference is required for the system to function.

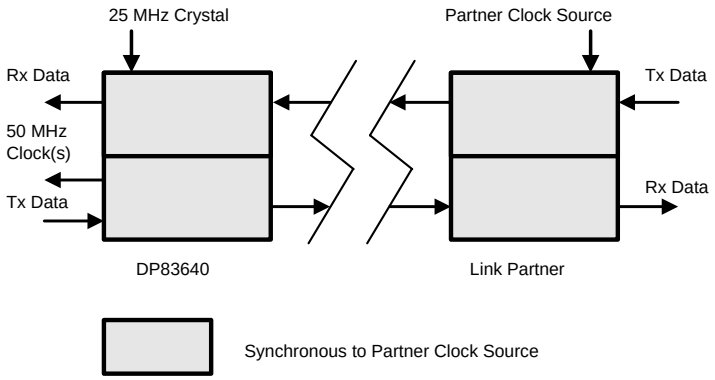

Figure 5. RMII Master/Synchronous 100Mb/s Ethernet System Diagram

This type of setup has an additional advantage to systems that require real-time operation, such as one that uses a Time Division Multiple Access (TDMA) protocol.

In addition, a link between two nodes in an IEEE-1588 Precision Time Protocol (PTP) would have essentially 0 ppm offset between the local and partner IEEE-1588 clocks, eliminating clock drift and improving precision. *AN-1730 DP83640 Synchronous Ethernet Mode: Achieving Sub-Nanosecond Accuracy in PTP Applications* (SNLA100) provides more detail regarding use of IEEE-1588 and the synchronous Ethernet mode.

Finally, the DP83640 device offers an additional clock distribution option that can be especially useful when the device is operating in RMII Master and 100Mb/s synchronous Ethernet mode. Instead of the 50 MHz RMII clocks appearing on the RX_CLK and TX_CLK signals, the 25 MHz MII clocks can be output. The RMII reference clock to the MAC is CLK_OUT, and the RX_CLK and TX_CLK signals are synchronous to CLK_OUT since all three clocks are derived from the link partner's transmit clock. For systems known to operate in 100Mb/s mode, this allows chaining several PHYs together using a single 25 MHz crystal to one of the PHYs (the "local clock master").

In addition, if the local clock master PHY is the uplink port of a switch, it can operate in synchronous Ethernet mode and can provide the reference clocks for all of the downlink port PHYs, thereby, facilitating synchronous downlink data transfer across a switch. If the link partners connected to the downlink PHYs are also operating in synchronous Ethernet mode, uplink data transfer will also be synchronous, creating a fully synchronous system. For more details, see Section 4.2.

Note that in this configuration, the local clock master PHY is connected to the 25 MHz crystal and operates in synchronous Ethernet mode; all other PHYs operate in standard (non-synchronous) Ethernet mode.

3.1 Configuring Synchronous Ethernet Mode

Synchronous Ethernet mode is configured as follows:

1. Write 0x0 to Register 0x13 (PAGESEL).
2. Set bit 13 (SYNC_ENET_EN) to 1 in Register 0x1C (PHYCR2).

3.2 Configuring MII Clock Output

Enable 25 MHz MII clock outputs in RMII Master mode as follows:

1. Write 0x0 to Register 0x13 (PAGESEL).
2. Set bit 6 (MII_CLOCK_EN) in Register 0x1B (CDCTRL1).

4 Clock Distribution Examples

Examples are provided in this section to facilitate understanding and implementation of RMII Master and synchronous Ethernet modes.

4.1 Three-Port Example

In a system comprising a three MAC functions plus three DP83640 devices, one PHY operates as the clock master and outputs the 50 MHz RMII reference clock on three separate pins. Such a system is shown in Figure 6. This allows the second and third PHYs in 50 MHz Slave Mode to use the same RMII reference clock as the 25 MHz Master PHY, thereby, allowing synchronous data transfer from all three PHYs to all three MACs. It is evident that this system uses only a single inexpensive 25 MHz crystal clock source, thus, saving the expense of three 50 MHz oscillators or several clock buffers. Since the RMII Master PHY provides three separately buffered copies of the RMII reference clock, this system removes the necessity for external clock distribution logic.

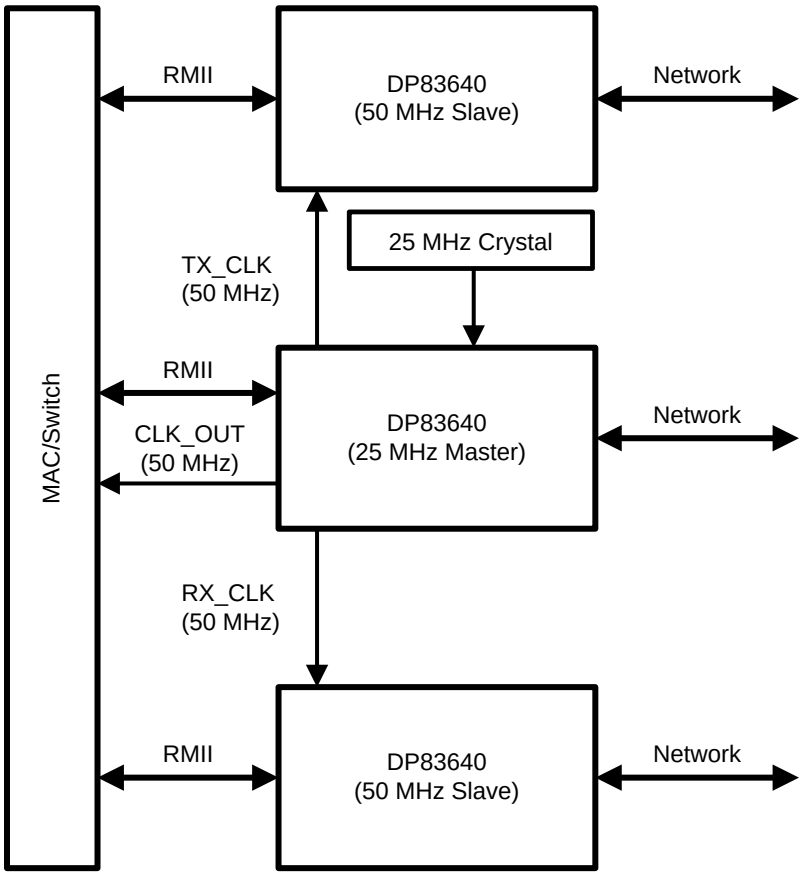

Figure 6. Three-Port Example

4.2 Five-Port Synchronous Switch

Figure 7 illustrates an example of a multi-port synchronous switch that takes advantage of RMII Master mode and 100Mb/s synchronous Ethernet mode. The TX_CLK and CLK_OUT outputs of the Uplink PHY are synchronous to its own Receive clock. Each subsequent PHY in the clock chain uses the TX_CLK signal from the previous PHY as its 25 MHz reference clock. In this manner, all data flowing downstream is synchronous. This is shown in Figure 8.

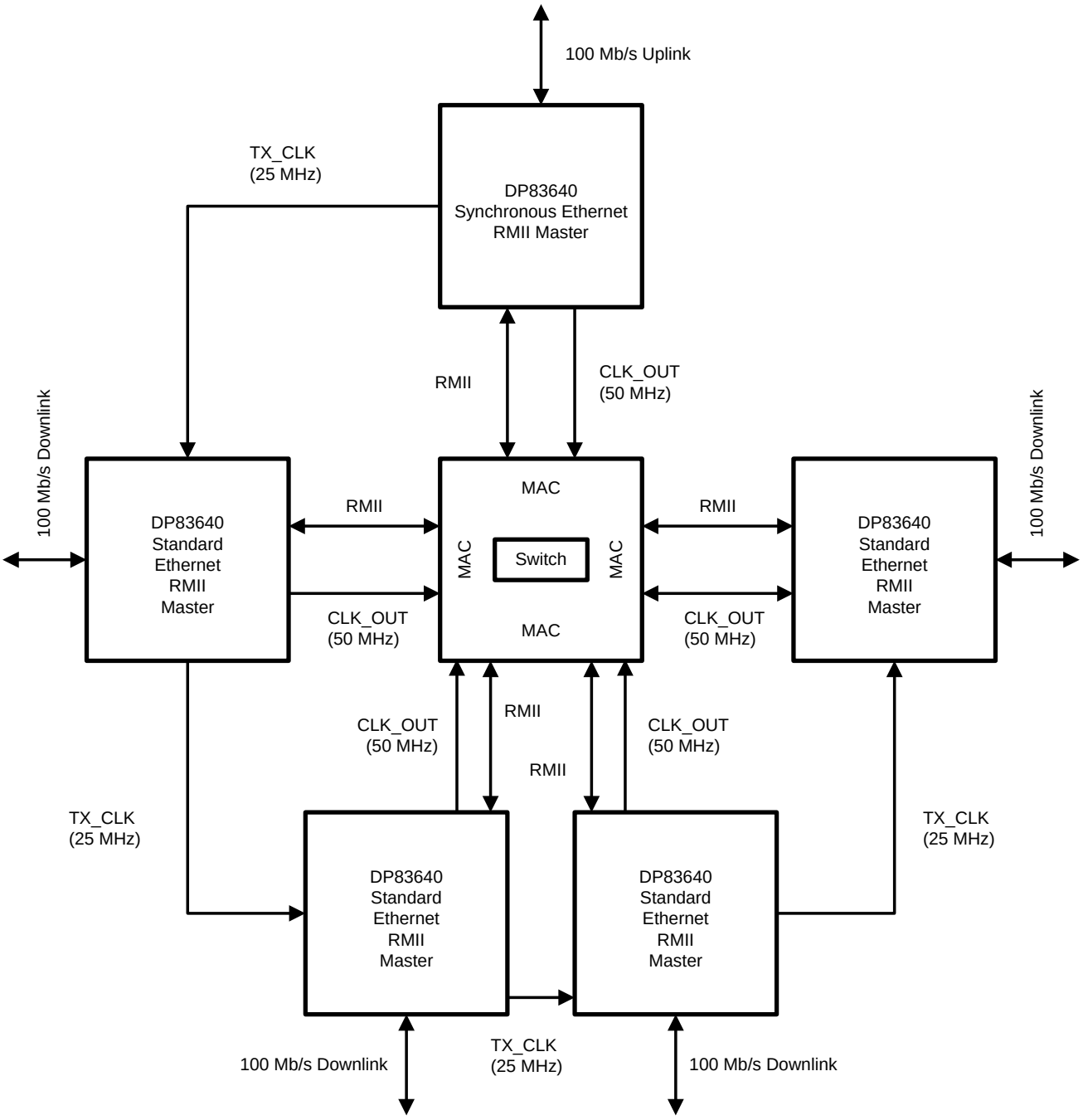

Figure 7. Five-Port Synchronous Switch

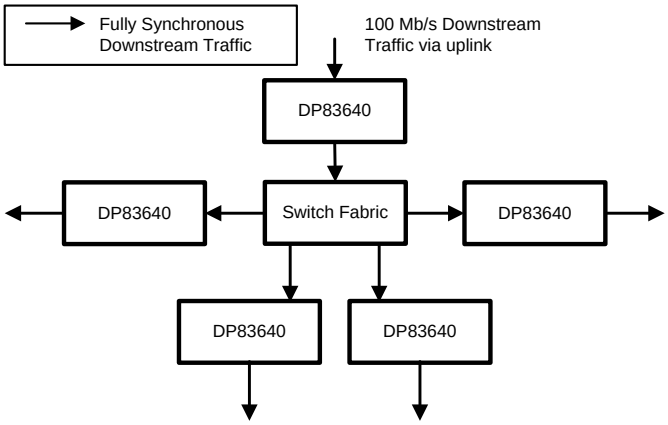

Figure 8. Synchronous Downstream Traffic

Note that this example can be extended to additional downlink ports by daisy-chaining more PHYs to the end of the PHY chain in the diagram via its TX_CLK output. When chaining reference clocks for the downlink PHYs, it is important that the TX_CLK signal be used as the reference clock for the next PHY in the chain since it is guaranteed to be synchronous and phase-locked to the PHY's own reference clock. If each downstream PHY's link partner node is a DP83640 in synchronous Ethernet mode, the system will be fully synchronous since the node's transmit clock is synchronous to its receive clock. This incorporates the switch in Figure 7 and is shown in Figure 9.

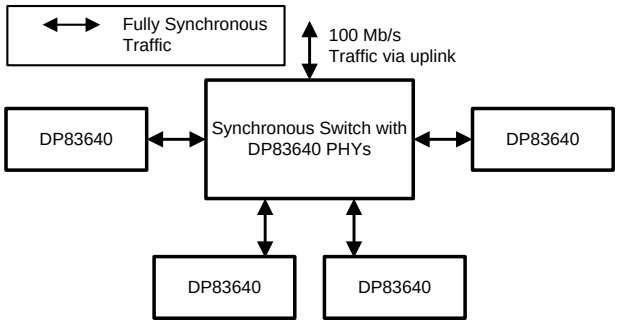

Figure 9. Fully Synchronous Traffic

5 Conclusions

The use of RMII as the interface between the MAC and PHY has seen increasing popularity due to its lower pin count. Up to now, however, RMII has had certain disadvantages that limit its usefulness in systems requiring highly deterministic latency or high tolerance to frequency offsets between the local and partner reference clocks. In addition, a standard RMII PHY device requires a 50 MHz oscillator that is expensive relative to a 25 MHz crystal.

Texas Instruments DP83640 precision PHYTER® supports two unique features which eliminate these RMII disadvantages. RMII Master mode allows the use of an inexpensive 25 MHz oscillator and generates multiple 50 MHz reference clocks. Synchronous Ethernet mode, when combined with RMII Master mode, eliminates the sensitivity to reference clock PPM offset between the two PHYs.

6 References

- *AN-1405 DP83848 Single 10/100 Mb/s Ethernet Transceiver Reduced Media Independent Interface™ (RMII™) Mode* (SNLA076)
- *AN-1729 DP83640 IEEE 1588 PTP Synchronized Clock Output* (SNLA099)
- *AN-1730 DP83640 Synchronous Ethernet Mode: Achieving Sub-Nanosecond Accuracy in PTP Applications* (SNLA100)

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