A New Driving Method to Compensate for Row Line Signal Propagation Delays in an AMLCD

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P-16: A New Driving Method to Compensate for Row Line Signal Propagation Delays in an AMLCD

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Abstract

The distributed capacitive and resistive nature of both the row and column lines in an AMLCD introduces significant propagation delays to their respective addressing signals. The row signal delay is conventionally accommodated by shortening the row select time, which requires lower TFT on-resistance to provide adequate charging ratios of the pixels. We present a new approach to column driving which results in a much-improved pixel-charging ratio. The benefit is of particular interest to large-area, high-resolution, wide-aspect-ratio, LCD TVs.

1.0 Background and History

The line-by-line, scan-and-hold feature of the active-matrix, TFT LCD means that each sub-pixel is operated as a sample-and-hold circuit. That is, when a row line is selected, all the sub-pixels on that row begin to acquire the voltage on their respective column lines. The sub-pixel charging time is designed to allow the sub-pixel voltage to equalize with the column line voltage before the end of the line time. At the end of the line time, the row signal falls latching this acquired voltage until the same line is addressed in the following frame.

In practice, it takes time for the row signal to propagate from the row driver, through the row line, to the other side of the panel. This is because the row line is electrically a distributed RC line. The propagation delay of the row signal through the RC line means that the latching of the sub-pixel on the far side of the panel will be slightly delayed from the latching of the sub-pixel near the row driver. This delay time is typically designed to be in the range of 1 to 3 microseconds.

In the conventional system, the column drivers transition from the voltage for the selected line to the voltage for the next line simultaneously, from one side of the panel to the other. That is, all column driver outputs on all the column drivers change at the same time. The 1 to 3 microsecond delay of the row line signal means that the column line signals must be held valid until the falling edge of the row signal reaches the far side of the panel. To prevent the column line voltages from changing before the row signal reaches the other end, the row pulse is shortened by an amount equal to the propagation time across the panel.

To shorten the row pulse, the row drivers provide a global output enable signal (OE) which when inactive forces all of the outputs to the de-select state (low). Since only one output is active at a time, this OE signal can be used to force a shortened row pulse signal on every line. In practice the electronic design engineer will adjust the width of the OE signal to tune the driving waveform to the particular panel design's propagation characteristics. Figure 1 shows how the row pulse signal width is shortened to allow for propagation of the falling edge to the far end of the line. Figure 2 shows the general concept of the OE signal. It should be noted that whenever OE is de-asserted, no row driver outputs are active. Therefore the portion of line time in which OE is de-asserted (low) is in a large sense a measure of how much of the row time is actually used for propagating the row signal rather than for charging the sub-pixel. Clearly we want to maximize the portion of the line time used to charge the sub-pixel [2].

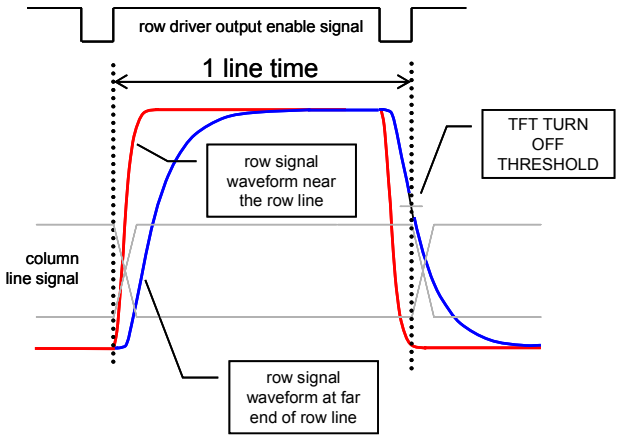

Figure 1. *The falling edge of the Row Signal takes time to propagate from the row driver to the far end of the row line. This requires the row pulse width to be shortened to assure that the signal reaches the far end of the row line before the column line data switches to the next line's voltage.*

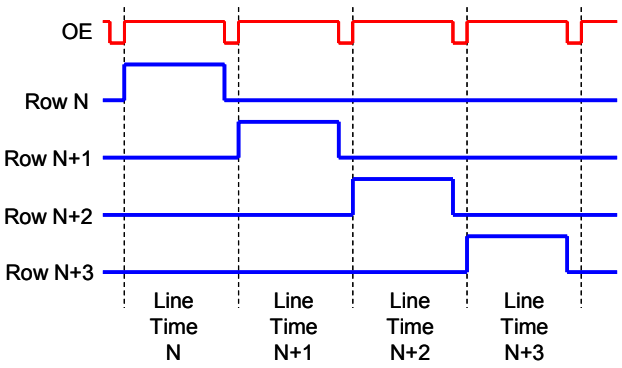

Figure 2. *Timing of the row signal's OE signal*

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2.0 Alternate Approach

Horizontal Line Delay Compensation (H-LDC) is an alternate method to compensate for the propagation delay of the row signal. Rather than transitioning all the outputs of all the column drivers simultaneously, each output of each column driver is delayed an amount that matches the propagating edge of the row signal as it passes that output. In other words, each column driver time staggers their output transitions, in step with the row signal propagation, to assure that the column driver changes states immediately after the row signal falls. This means that since no output must wait for the gate signal to propagate, whether the column driver output is near or far from the row driver, there is additional time to charge each pixel.

Notice in Figure 1 how the column driver signals near the row driver remain unchanged well after the row signal falls (red line). From the perspective of these column driver outputs, those near the row driver, the row driver signal could fall much later and provide additional time to charge the sub-pixel.

Figure 3 compares the driving waveforms of the conventional method for the row signal propagation compensation with the improved H-LDC method. Each of the three Figures, 3a, 3b and 3c have a common datum, the time at which the row driver signal begins to transition from low to high. This defines the beginning of a new line. In other words, notice that the time at which the row signal begins to transition from low to high is the same in Figures 3a, 3b and 3c. The row signals in Figure 3b and 3c are identically the same, the only differ in which end of the line is highlighted. Notice that the total on-time of the row select line is shorter in Figure 3a than it is in Figures 3b and 3c. This is a key benefit of H-LDC. The only difference between Figure 3b and 3c is when the column line signal transitions. In the conventional approach each column driver output must transition in unison with all the others. In H-LDC, each output of each column driver transitions independently and progressively later than the previous output (i.e. the one nearer the row line).

2.1 Implementation

One of the enabling technologies used to simplify the implementation of H-LDC is the PPDS™ architecture now being introduced by National Semiconductor into the market [1].

In the PPDS system, the Timing Controller communicates to each Column Driver separately through a single, point-to-point link rather than across a global, multi-drop bus. In addition to the video data sent across this link from the Timing Controller to the Column Driver, this link carries specific column driver control commands in a header of the packet of data that is sent with each new line.

With H-LDC the Column Driver outputs are divided into small banks which while they operate synchronously as a group, are small enough to approximate operation as individual outputs. One of two control parameters sent to each column driver to implement H-LDC is the number of PPDS link clock cycles to wait following the global, start-of-next-line signal before transitioning any output. The other parameter is the number link cycles to wait before starting each successive bank of grouped outputs. To program the column drivers in the PPDS™ system for H-LDC, the column driver nearest the row driver is told to wait 0 clock cycles following the new row strobe signal called LOAD. In addition, it is told to start the transition of each separate bank of outputs delayed from the previous bank by N clock cycles. Assuming that the column driver outputs are grouped into 8 separate banks, the next column driver away from the row driver is programmed with a start time of 8N clocks following the same global LOAD signal as well as a step size of M clock cycles. The remaining column drivers are programmed likewise thereby allowing each output of each column driver to transition approximately in step with the exact delay of the row signal falling edge at that outputs position along the row line.

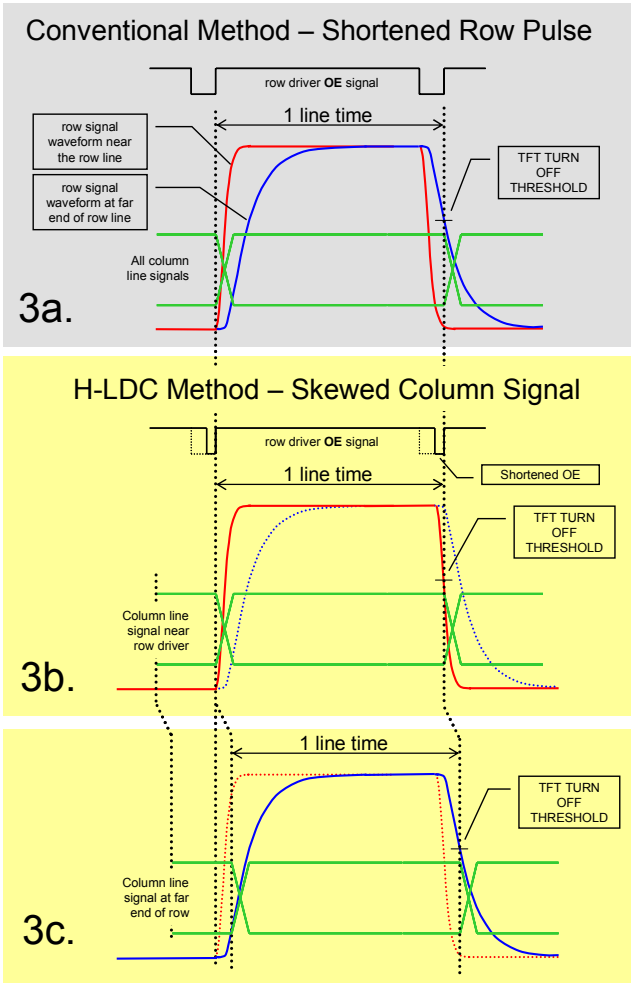

Figure 3. *Conventional shortened row pulse v.s. H-LDC signals. The conventional approach is shown in 3a. H-LDC signals near the row driver and far from the row driver are shown in 3b and 3c respectively*

3.0 Results

The data provided in the following figures was extracted from a SPICE model of an AMLCD. Figure 4 shows an example of the falling edge waveform as it propagates down the row line, away from the row driver on a representative row line. The graph shows signal amplitude as a percentage of the full-on voltage as a function of time for several equally spaced intervals across the row line. While the conduction characteristics of the TFT depends on the combined gate, source and drain voltages there is

some level of gate voltage under the worst-case of source and drain for which we can say the TFT is off.

An off-state threshold of 40 percent for example, is assumed for the purposes of this discussion example. Figure 5 is a reorganization of the data Figure 4 arranged to show how the same amplitude point on the falling edge waveform progresses down the row line.

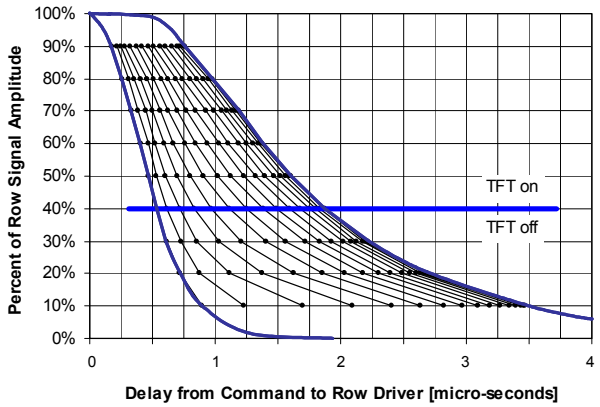

Figure 4. *The falling edge waveform for several equally spaced points along the row line. We can conceptually establish an on-off threshold, say 40%, for which we can say that below this voltage, under all conditions of Vgs and Vgd, the TFT is off.*

Figure 5 shows how the various points on the falling edge travel across the row line. In this graph the vertical gradicals are spaced to match the sixteen (16), 360 output, columns drivers (CDs) that might be used to drive a 1920 horizontal pixel panel. (Note that there are 3 column driver outputs per pixel, one for each of three primary colors). As described, the conventional approach to accommodate the propagation delay of the row signal threshold voltage is to shorten the row pulse to assure that the row line transitions everywhere across the line before the simultaneous transition of the column line signals. In our solution, we allow the column line outputs to transition progressively rather than simultaneously, in unison with the propagation of the threshold signal on the row line.

The dashed curve in Figure 5 shows how the 40% voltage threshold behaves as it progress from the row driver to the far end of the line. In the conventional solution, the OE de-select time would be made at least 1.9 micro-seconds to allow this point on the waveform to reach from one end of the row line to the other. This graph shows that when each column driver is programmed with H-LDC timing values that tune the column lines to transition from one state to another following the 40% curve with distance, OE can be reduced to just the time to be sure that the first column line nearest the row driver falls to 40% before the first column transitions. This means in this example, OE can be reduced to 0.2 microseconds or 200ns. This is a net increase of pixel charging time of 1.7us. Note that the more conservative we are in defining the on-off threshold, the more advantages H-LDC has. A threshold of 14 percent, for example, would have a minimum OE de-select time of 0.8 microseconds (compared with 0.2 microseconds for the previous example) but would provide an additional 2.4 microseconds of charge time per line over the conventional driving method.

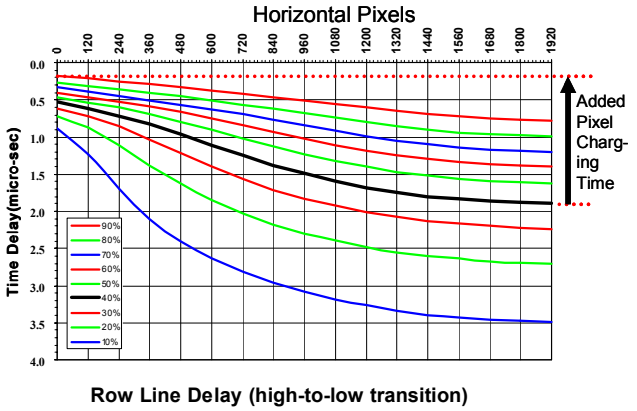

Figure 5. *The various points on the falling edge plotted over position along the row line (measured in pixels). When for example the 40% is taken as the off threshold, H-LDC compensation provides an addition 1.9 microseconds to charge the each sub-pixel.*

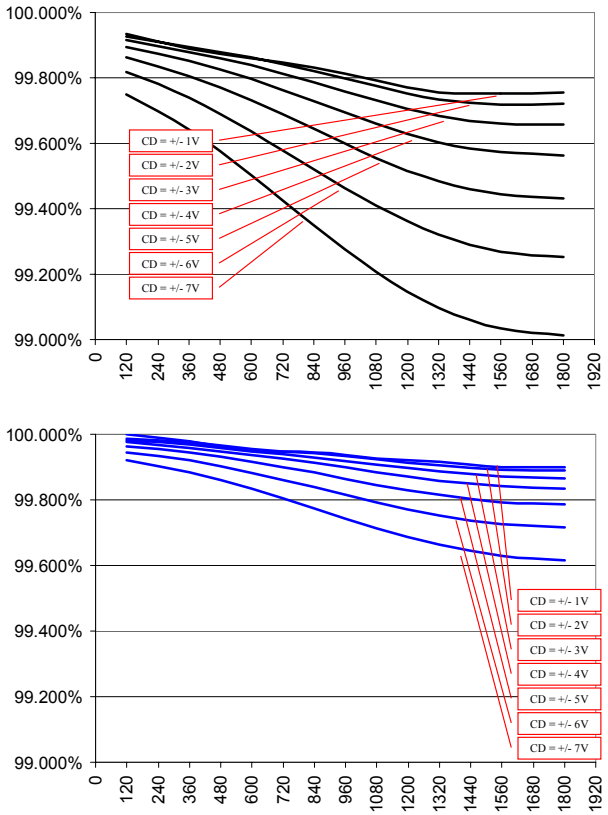

Figure 6a and 6b. *The charging ratio results from both the conventional, shortened gate pulse method (top) and using Horizontal Line Delay Compensation (bottom). Based on SPICE model.*

3.1 Charging Ratio

Figures 6a and 6b illustrate one of the key advantages of H-LDC, improved pixel charging ratio. Charging ratio is defined as the ratio of the peak voltage that appears on the pixel prior to the fall of the gate voltage to the asymptote, the ideal, intended voltage appearing on the column line. The improvement is substantial in

this case. Each sub-pixel benefits from a longer charging time and that benefit results in a more uniformly charged panel. This benefit can be spent as improved margin in the panel or allow a panel to achieve conventional charging rations with a smaller TFT.

In the example above, an HDTV panel (1920 by 1080) operated at 60Hz (with 5% vertical blanking time) has a line time of about 14.7 microseconds. With the conventional approach the effective charging time in the worst case would be 14.7 – 1.9 us, or 12.8 us. With H-LDC applied to this same example, the effective charge time would be increased from 12.8 us to 14.5 us (14.7 – 0.2). This provides enough additional margin for example, to operate the panel at 13% faster or up to 68Hz. This margin can be spent in several different ways. The need to provide additional margin is exasperated by wide formats (e.g. 16:9), higher pixel count formats (e.g. 1920 x 1200), larger sizes (> 40 inches) and black frame insertion methods (e.g. refreshing the panel in ½ the time to allow full display in the other half). To address these needs array designers relay on a number of methods including reduced pixel charging time constants, reduced row line time constants, reduced refresh rates and in some instances dual-end row drivers. While this method alone will not guarantee elimination of the need for any of these, it does provide added margin to lessen the need for these added features and in some cases could make the difference between needing a new feature and not. In any case however, H-LDC is compatible with both single and dual end drive and has no system penalty for its use.

4.0 Conclusions

The performance margin improvement resulting from application of this driving technique can be spent in any number of ways including faster refresh rates, higher apertures and/or better yields. The benefit is of particular interest in large-area, high-resolution, wide-aspect ratio panels, which tend to strain the limits of acceptable pixel-charging ratios. In particular, larger TV panels are sometimes designed to require dual-ended gate drive to improve the gate signal propagation time and maximize the pixel-charging dwell time. Other methods include lower resistance gate line materials including copper. Improvements in the margins due to this method could reduce the need for such expensive solutions in some cases. The method is compatible with both single and dual-ended drive providing substantial additional margin to the display.

In addition to the performance improvement resulting from this approach, the method will reduce EMI by reducing the peak surge current that occurs when all the column outputs and column lines of the panel transition simultaneously. This reduces peak power demands and improves the design margins of internal CD supply nodes. This reduced surge current is of particular importance in chip-on-glass (COG) and wire-on-array (WOA) applications. In these applications the reduced supply surge current helps to eliminate the need for local power supply de-coupling capacitors. In WOA the reduced peak surge currents helps to extend operation through highly resistive supply lines.

5.0 Acknowledgements

The SPICE simulation work used in this paper is based on an electrical model of the array developed by Korea University. This work was sponsored and directed by National Semiconductor and was done in collaboration with Samsung AMLCD. The Authors wish to thank the many engineers and scientists at Samsung for providing all the detailed parameters required for the model and in particular we wish to thank Dr. Sang-Soo Kim, Executive Vice President of Samsung AMLCD for his support of this research effort.

6.0 References

[1] McCartney and Bell, ASID ‘04 Digest, paper 2.2.2 - p. 82

[2] Lueder, Liquid Crystal Displays: Addressing Schemes & Electro-optical Effects, John Wiley and Sons Ltd., 23 April, 2001.

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