Application Report
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Adding Reset Delay to Voltage Detectors

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ABSTRACT

In many applications that have multiple power rails, power-up timing is critical to ensure proper system protection and functionality. In these cases, programmable reset time delay is a necessary feature to control the power-up timing and the reset output timing when returning from a fault condition. This application report explains a technique to add programmable reset time delay to voltage detectors.

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1 Introduction

In many applications that have multiple power rails, power-up timing is critical to ensure proper system protection and functionality. The normal operation of a voltage detector monitors a voltage rail and triggers a fault immediately when a fault in the monitored voltage occurs. This fault occurs due to either an undervoltage or overvoltage condition depending on the voltage detector used. When the fault condition is removed, voltage detectors return to normal operation after the inherent propagation delay from the output rising from logic low to high unlike voltage supervisors and reset ICs which have a fixed or programmable delay before returning to the normal operation from a fault condition. This document provides users with application techniques for adding reset time delay to voltage detectors with open-drain output topologies. Push-pull devices do not allow for additional reset time delay because the pull-up resistor is replaced with an internal MOSFET with very little resistance while the MOSFET is on, which causes the capacitor to be shorted out of the circuit preventing the additional delay at the output.

Not only is this useful for applications that require a reset time delay, but this can be useful for applications such as those from the automotive and industrial sectors that require wide input voltage (wide Vin), with reset time delay. TI's family of wide Vin voltage detectors such as those from the TPS37XX have 18V and 36V operating voltage range, and can monitor undervoltage and overvoltage conditions, but don't have a reset delay since they are voltage detectors. By following the technique explained in this document, programmable reset time delay can be added to the TPS37XX family as well as any other open-drain voltage detector.

2 Adding the External Programmable Reset Delay Circuitry

One way to implement such a solution is by adding a capacitor followed by a buffer at the output of the voltage detector as shown in Figure 1.

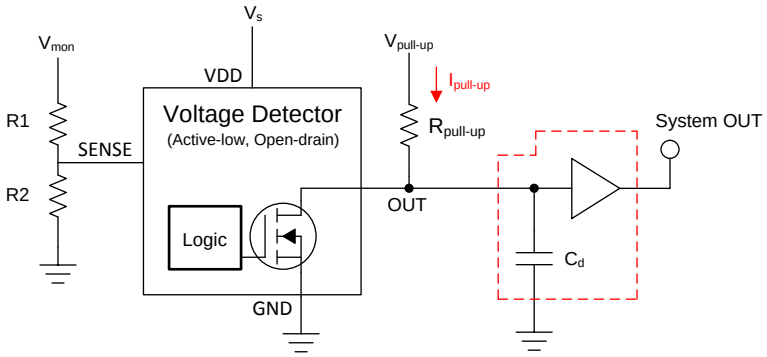

Figure 1. Adding Programmable Reset Time Delay to Detectors

The capacitor adds a programmable reset time delay on the rising edge because when the output rises, the capacitor needs time to charge via the pull-up resistor. This programmable reset time delay is calculated by using Equation 1 below and is derived from the relationship between voltage and current for capacitors:

$$I_{pull-up} = C_d \times \frac{\Delta V}{\Delta t} \quad (1)$$

where $I_{pull-up}$ is the current through the pull-up resistor, C_d is the programmable delay capacitor, ΔV is the rising voltage that triggers the buffer (V_{IH}), and Δt is the delay added by the capacitor. Solving Equation 1 for the delay gives Equation 2:

$$\Delta t = C_d \times \frac{\Delta V}{I_{pull-up}} \quad (2)$$

and rewritting to simpler terms gives Equation 3:

$$delay = C_d \times \frac{VIH_{buffer}}{V_{pull-up}/R_{pull-up}} \quad (3)$$

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During a fault condition at the monitored voltage, the internal MOSFET turns on and shorts OUT to ground effectively ignoring the impact of the capacitor, so no additional delay is added to the falling edge of the output during the fault detection. The effect of the capacitor and the buffer is shown in the timing diagram below Figure 2.

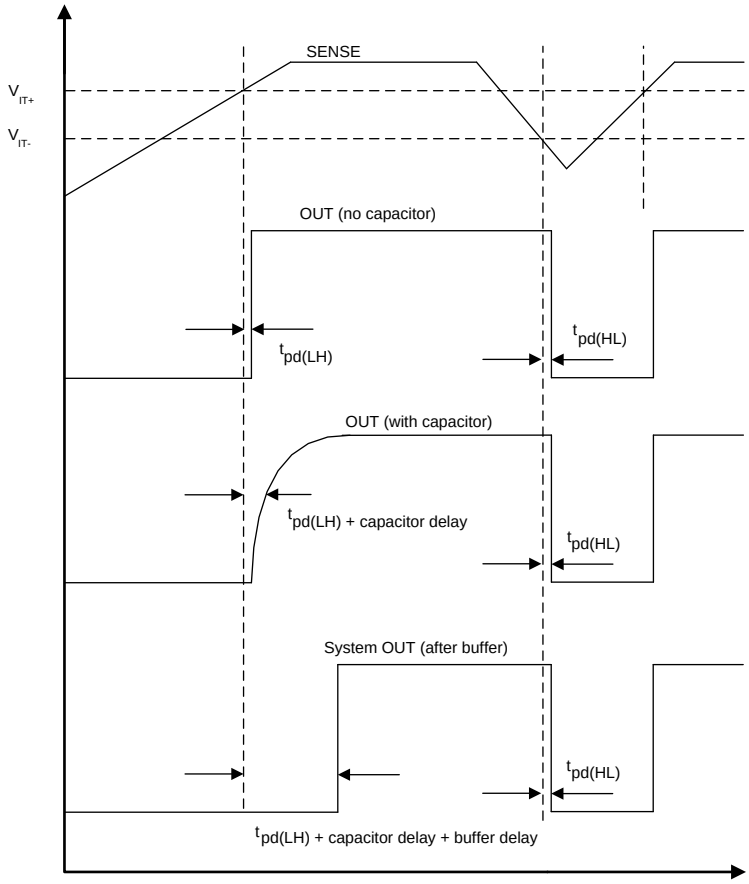

Figure 2. Programmable Reset Time Delay Timing Diagram

As shown in Figure 2, a voltage detector with no capacitor will have a rising propagation delay in the microsecond range, but by simply using a capacitor to add reset time delay and using a buffer to filter the output signal, any voltage detector with an open-drain output topology can be converted to a programmable reset delay voltage supervisor.

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3 Bench Testing

The effect of the capacitor and the buffer is shown by testing the TPS3700EVM-202 as shown in Figure 3

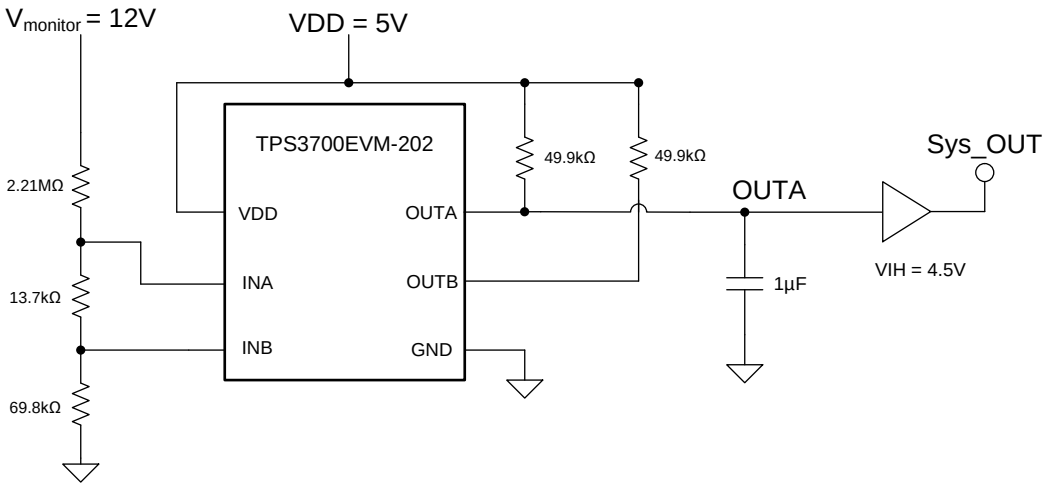

Figure 3. TPS3700EVM-202 Schematic with Capacitor and Buffer

No changes are made to the TPS3700 EVM except for adding the 1µF capacitor and the buffer. The buffer's logic "high" input voltage (V_{IH}) is specified as 90% of V_{DD}. Since V_{DD} = 5V for this test, the input voltage to trigger a logic "high" is 4.5V. Using Equation 3, the expected delay with a 1µF capacitor and a buffer with V_{IH} of 4.5V is calculated below in Equation 4:

$$delay = 1\mu F \times \frac{4.5V}{5V/49.9k\Omega} \tag{4}$$

The accuracy of the calculated delay is directly related to the tolerance of the capacitor and pull-up resistor so it is recommend to measure and use the actual component values when calculating the delay. The TPS3700 and buffer also provide additional propagation delays that must be accounted for and are specified in their datasheets. The TPS3700 provides an additional propagation delay of approximately 29µs (t_{PLH} from TPS3700 Datasheet) and the buffer provides an additional propagation delay of approximately 3.5ns (t_{pd} from SN74LVC1G07 Datasheet).

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4 Bench Results

The standard TPS3700EVM-202 output reset time delay is compared to the TPS3700EVM-202 output reset time delay with the additional capacitor and buffer in Figure 4 and Figure 5. The standard reset time delay with no capacitor or buffer is 34µs due to the inherent propagation delay of the TPS3700. With the additional 1µF capacitor and buffer, the reset time delay becomes 43ms.

Figure 4. Reset Time Delay with Standard TPS3700EVM-202

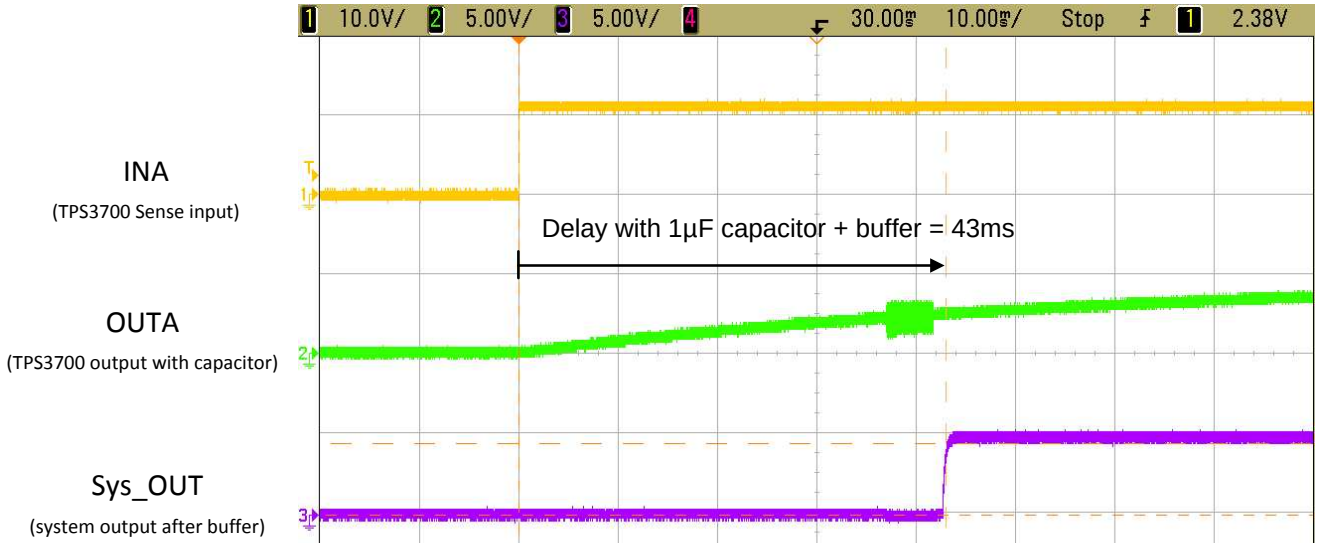

Figure 5. Reset Time Delay with TPS3700EVM-202 with Capacitor and Buffer

It is important to note that the additional capacitor and buffer do not have any significant impact on the voltage fault detection meaning the output still triggers to logic low quickly when a fault occurs. The additional programmable reset time delay is only added to the output rising edge when returning from the fault condition. Because the delay is only added when returning from the fault and not during fault detection, the device still functions properly. The standard fault detection time with no capacitor is compared to the fault detection time with the additional capacitor and buffer in Figure 6 and Figure 7.

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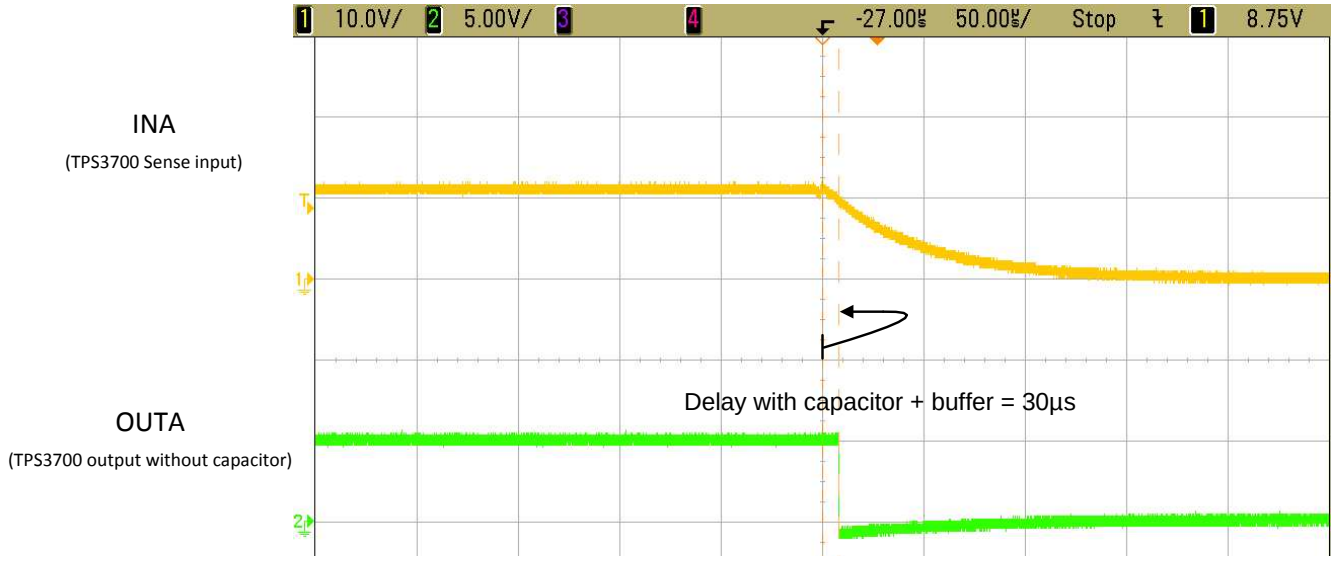

Figure 6. Standard Fault Detection Time with No Capacitor or Buffer

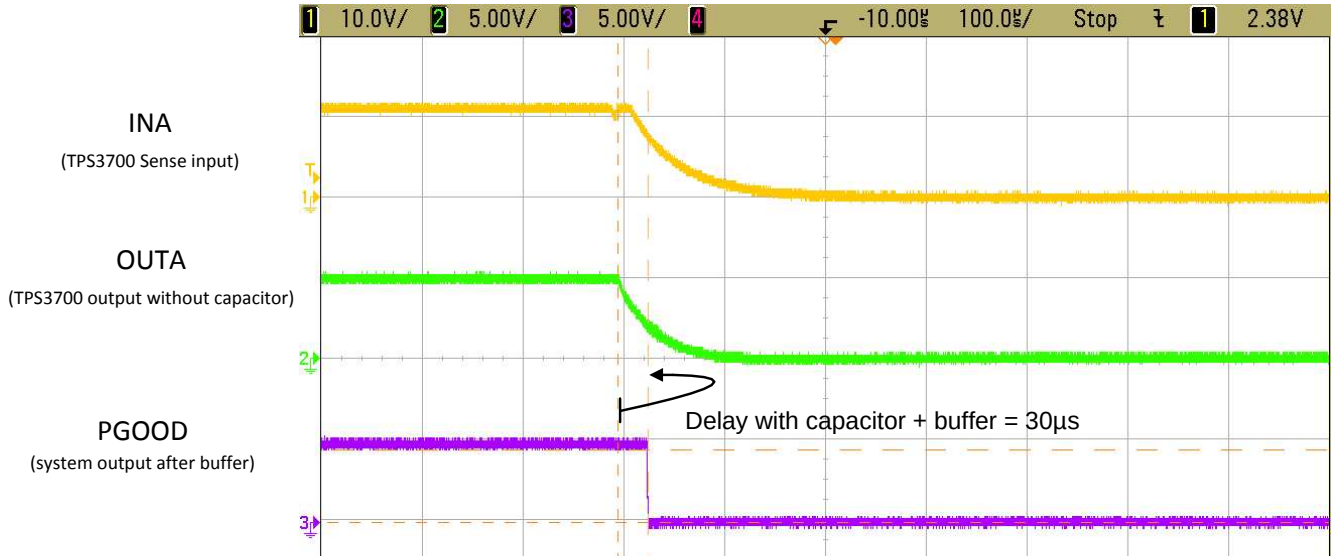

Figure 7. Fault Detection Time with Capacitor and Buffer

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5 Summary

There are applications that require both wide input voltage range and programmable reset delay, but most wide input voltage range voltage monitoring devices are voltage detectors without any reset time delay, and more importantly, without programmable reset time delay. Adding in a programmable reset time delay to a voltage detector simply requires a capacitor and a buffer connected to the output of an open-drain voltage detector. By following Equation 3 and selecting the appropriate capacitor, additional time delay can be achieved. Not only is this useful for applications where power-up timing is critical, but this method can also be used to achieve programmable reset time delay to TI's wide Vin voltage detectors: TPS3700, TPS3701, and TPS3702.

6 Resources

Table 1. Alternative Device Recommendations

Device	Description
TPS3700	18V input voltage, Window supervisor for overvoltage and undervoltage detection, high precision 0.25% accuracy
TPS701	36V input voltage, Window supervisor for overvoltage and undervoltage detection, high precision 0.25% accuracy
TPS3710	18V input voltage, voltage detector for undervoltage, high precision 0.25% accuracy
TPS3711	36V input voltage, voltage detector for undervoltage, high precision 0.25% accuracy

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