

# ***How to Begin Development Today With the TMS320C6414, TMS320C6415, and TMS320C6416 DSPs***

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## **ABSTRACT**

Development can begin now for the TMS320C6414, TMS320C6415, and TMS320C6416 highest-performance digital signal processor (DSP) systems. Because of the compatibility between TMS320C6000™ generation devices, existing C6000™ software tools and development platforms can be used to develop code for the C6414, C6415, C6416 and other future devices. This capability allows for systems to be up and running when silicon becomes available.

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## 1 How to Begin Development Today With the TMS320C641x DSP

The Texas Instruments TMS320C6000™ generation of high-performance digital signal processors (DSPs) now includes the TMS320C6414, TMS320C6415, and TMS320C6416. The C64x™ brings the highest level of performance in the C6000™ family of fixed-point DSPs. At clock rates of 1 GHz and greater, the C64x can process information at a rate of 8800+ MIPS or nearly nine billion instructions per second. Initial devices will be sampling in the 500 MHz-720 MHz range, giving performance levels of 4000-5760 MIPS.

Introduced in February 1997, the C6000 generation is based on TI's VelociTI™ architecture, an advanced very long instruction word (VLIW) architecture for DSPs. Advanced features of VelociTI architecture include instruction packing, conditional branching, and pre-fetched branching, all of which overcome problems that were associated with previous VLIW implementations. The architecture is highly deterministic, with few restrictions on how or when instructions are fetched, executed, or stored. This architectural flexibility is key to the breakthrough efficiency levels of the C6000 compiler.

The C64x employs VelociTI.2™ extension to the VelociTI architecture. The VelociTI.2 extension significantly improves performance with increased parallelism, orthogonality, packed data processing, and new instructions to accelerate performance in key applications.

The roadmap for fixed-point C6000 DSP platform shown in Figure 1 demonstrates TI's commitment to present highest performance DSPs.

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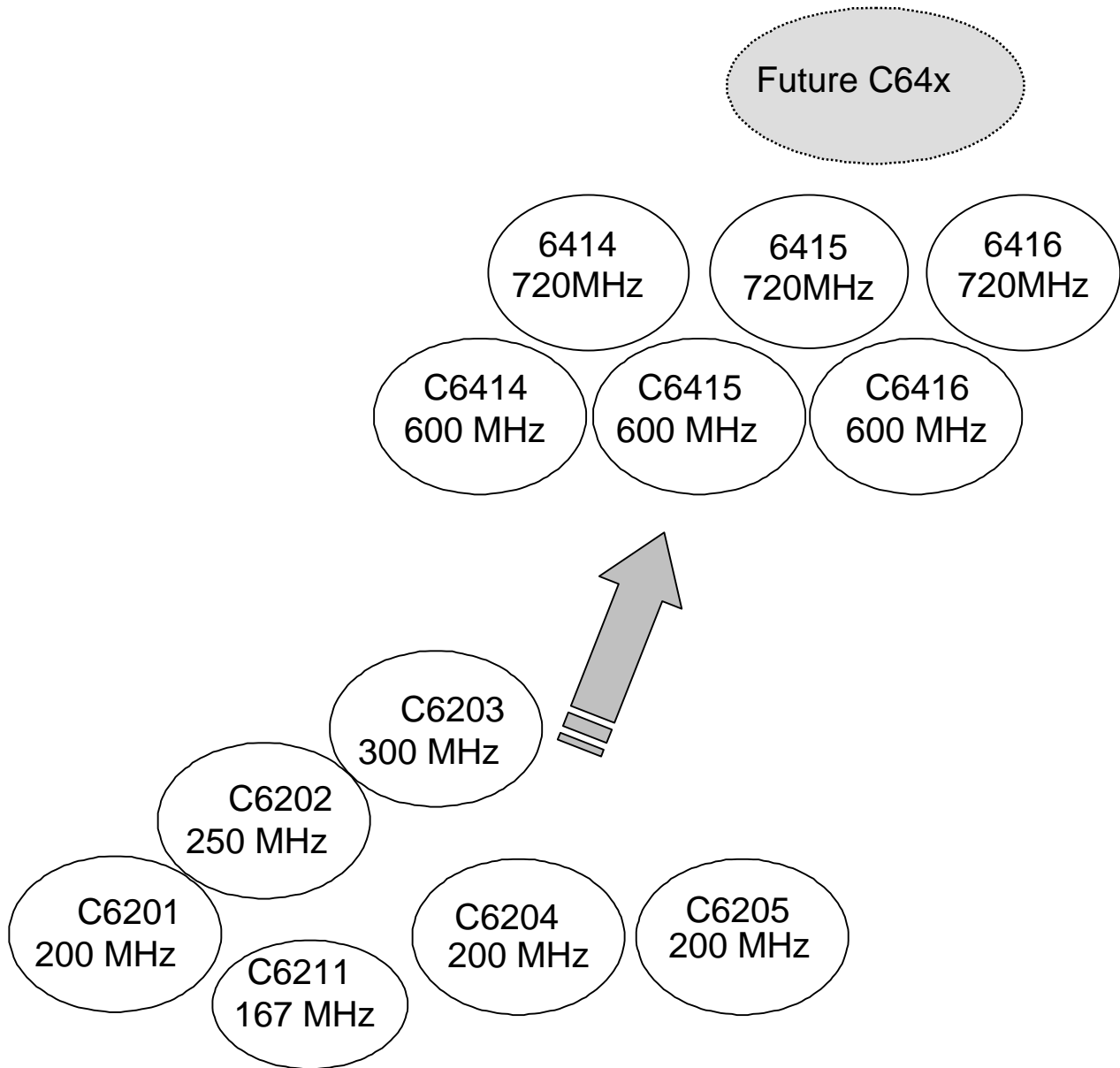


Figure 1. TMS320C6000 Highest Performance Fixed-Point DSP Roadmap

## 2 Highest Performance DSP

The TMS320C64x DSP core scales operating speeds beyond 1 GHz and achieves 10X performance improvements over the industry's previous DSP performance leader, the TMS320C62x DSP. Chips in development couple this processing performance with new memory and peripheral systems designed to accelerate real-time throughput for higher system performance.

The efficient on-chip cache architecture of the C641x allows system designers to use slower, cheaper external memory devices for data and program storage, while keeping the high performance capabilities of the device. In addition, a cache helps programmers to achieve their performance goals faster, shortening code development and accelerating time to market.

The enhanced direct memory access (EDMA) controller allows designers to optimize data organization in their systems. Capable of accessing any location in the C641x memory map, the EDMA controller transfers data in the background of DSP core operation. The EDMA controller can handle multiple transfers simultaneously and can interleave bursts. The EDMA controller offers 64 independent channels, with a separate RAM space to hold additional transfer configurations. Each EDMA controller channel is synchronized by an event to allow minimal intervention by the DSP core.

The on-chip memory is organized to allow design flexibility and ensure efficient memory usage. The C641x has 1056 Kbytes of on-chip memory, with 32 Kbytes serving as a level-one (L1) cache that the DSP core can directly access. The L1 cache is divided into 16 Kbytes of program (L1P) and 16 Kbytes of data (L1D) cache memory. The remaining 1024 Kbytes of on-chip memory is a unified program and data memory space. It can serve as memory-mapped SRAM, or a combination of SRAM and L2 cache.

L1P is direct-mapped, so that each instruction byte occupies a unique location in the cache. It has a 256-bit wide data path to the DSP core, so that the DSP core may fetch eight instructions (one fetch packet) every cycle.

L1D is two-way set associative, so that it can hold two different sets of information with independent address ranges. The L1D cache is a dual-ported memory that allows simultaneous accesses from both DSP core data ports, so that the DSP core can load or store two 64-bit values in a single L1D data cycle. The cache uses a least-recently-used (LRU) replacement scheme to select between the two possible cache locations on a cache miss.

The 1024 Kbytes L2 memory can be configured as memory-mapped SRAM, or a combination of SRAM and 4-way associative cache. The L2 memory can be programmed to be 0-, 32-, 64-, 96-, or 128-Kbyte 4-way associative cache, with the remaining set to memory-mapped SRAM. Blocks of L2 that are selected as cache are not included in the C6711 memory map. The mapability of L2 blocks as addressable locations allows critical code and data to be locked into internal memory.

TI has run extensive tests on this L1/L2 architecture to determine how it performs with an enhanced full-rate GSM vocoder, system-level applications in ADSL, V.90 modems, and other commonly used algorithms. For both data and program, TI's tests indicate L1 cache hit rates greater than 98 percent. In other words, only one instruction or data word in fifty needs to be fetched from L2 or external memory.

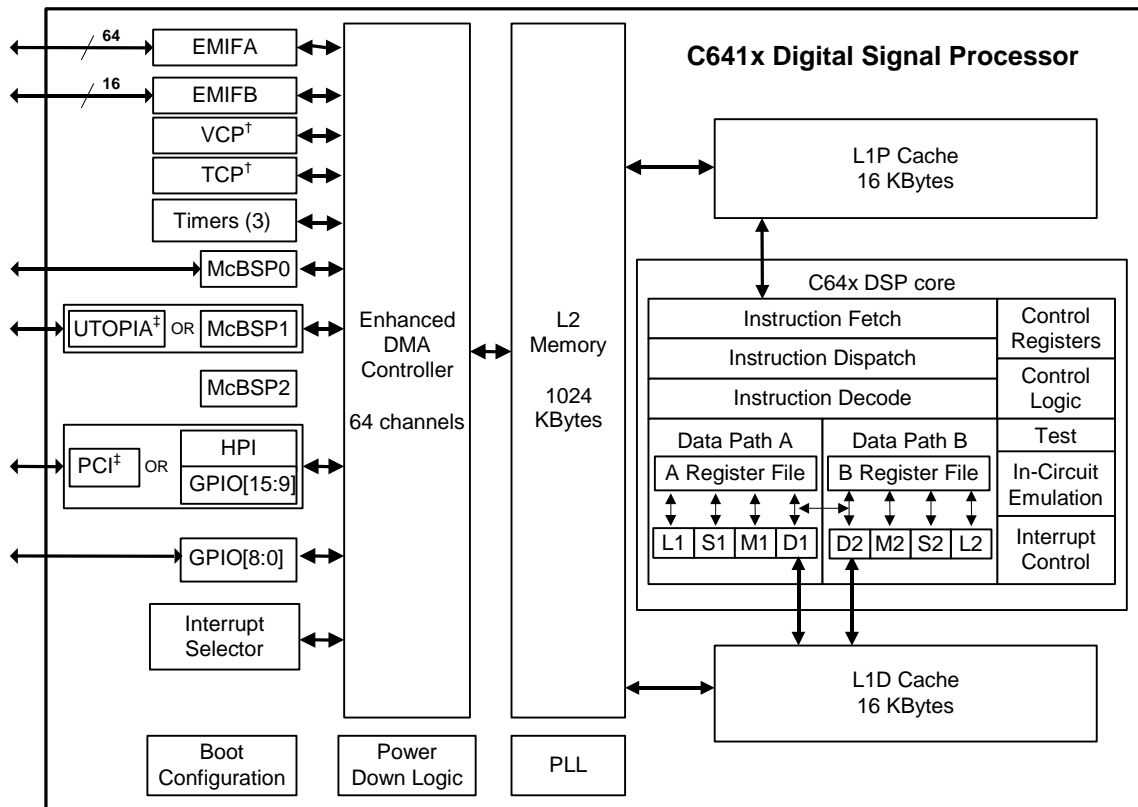
The high L1 hit rate, combined with the flexibility of L2 memory organization, means that this architecture can operate at more than 80 percent of the cycle performance of a more expensive device with a traditional memory organization where all system memory is on the chip. This high degree of efficiency allows systems to rely on inexpensive external memory for program and data storage, while at the same time performing high-speed number-crunching routines in real time.

### 3 TMS320C6000 Compatibility

All C6000 generation devices are code-compatible with one another, with the exception that there are some floating-point instructions that are only valid on the floating-point (C67x™) members. The C64x™ DSP core is enhanced over the C62x™ DSP core designed to achieve high performance through increased instruction-level parallelism. Surpassing the throughput of traditional superscalar designs, VelociTI.2 provides eight execution units, including two multipliers and six arithmetic logic units (ALUs). These units operate in parallel and can perform up to eight instructions during a single clock cycle—up to 5760 MIPS at 720MHz device clock speed.

This common architecture allows designers to begin development with existing C6000 software tools for those devices currently in development. This also allows for migration from one C6000 processor to another, as design specifications require.

In addition to the DSP core, many of the on-chip peripherals are common between C6000 devices. Figure 2 shows a block diagram of the C641x.



† The VCP/TCP coprocessors exist only on the C6416 device.

‡ The UTOPIA and PCI peripherals exist only on C6415 and C6416 devices.

**Figure 2. TMS320C641x DSP Block Diagram**

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### 3.1 C64x Advanced DSP Core

The C64x DSP core offers several enhancements over the C62x DSP core. They include:

- Register file enhancement
  - The register files have doubled in size. The C62x has 32 32-bit general-purpose registers and the C64x has 64 32-bit general-purpose registers.
  - Register A0 can be used as a condition registers on the C64x in addition to A1, A2, B0, B1, and B2 condition registers available on the C62x.
  - The C62x register file supports packed 16-, 32-, and 40-bit data types. The C64x register file extends this by supporting packed 8-, and 64-bit data types.
- Data path extensions
  - Each .D unit can load and store double words (64 bits) with a single instruction. The .D unit on the C62x cannot load and store 64-bit values with a single instruction.
  - The .D unit can now access operands via a data cross-path similar to the .L, .M and .S functional units. In the C62x, only address cross-paths on the .D unit are supported.
  - The C64x pipelines data cross path accesses. This allows the same register to be used as a data cross path operand by multiple functional units in the same execute packet. In the C62x, only one cross operand is allowed per side.
- Advanced Instruction Packing

The C62x VelociTI architecture contains instruction packing. Eight instructions are fetched every clock cycle. Of these instructions, any or all may be executed in parallel. To allow maximum usage of parallel instructions, the VelociTI architecture does not allow execute packets to cross-fetch packet boundaries. The code generation tools handled this limitation by padding fetch packets with NOP instructions. The C64x VelociTI.2 architecture extensions eliminate this limitation by including advanced instruction packing in the instruction dispatch unit. This improvement removes all execute packet boundary restrictions, thereby eliminating all of the NOPs added to pad fetch packets and helps to reduce code size.
- Packed data processing
  - Instructions have been added that operate directly on packed data to streamline data flow and increase instruction set efficiency. The C64x has a comprehensive collection of quad 8-bit and dual 16-bit instruction set extensions.
  - Extensive collection of pack and unpack instructions simplifies manipulation of packed data types.
- Additional Functional Unit Hardware
  - Each .M unit can now perform two 16x16 bit multiplies or four 8x8 bit multiplies every clock cycle.
  - The .D units can now access words and double words on any byte boundary by using non-aligned load and store instructions. The C62x only provides aligned load and store instructions.

- The .L units can perform byte shifts and the .M units can perform bi-directional variable shifts in addition to the .S unit's ability to do shifts. The bi-directional shifts directly assist voice-compression codecs (vocoders).
- The .L units can perform quad 8-bit subtracts with absolute value. This absolute difference instruction greatly aids motion estimation algorithms.
- Special communications-specific instructions, such as SHFL, DEAL and GMPY4 have been added to the .M unit to address common operations in error-correcting codes.
- Bit-count and Rotate hardware on the .M unit extends support for bit-level algorithms such as binary morphology, image metric calculations and encryption algorithms.
- Increased orthogonality
  - The .D unit can now perform 32-bit logical instructions in addition to the .S and .L units.
  - The .D unit now directly supports load and store instructions for double word data values. The C62x does not directly support loads and stores of double words and the C67x only directly supports loads of double words.
  - The .L, and .D units can now be used to load 5-bit constants in addition to the .S unit's ability to load 16-bit constants.
  - On the C62x, one long source and one long result per data path could occur every cycle. On the C64x, up to two long sources and two long results can be accessed on each data path every cycle.

### 3.2 Differences Between the C641x and C6211 DSPs

Significant enhancements have been made to the C641x over the C6211 to allow the C641x to be the highest performance DSP. These include:

- **DSP Core:** The C641x DSP features C64x DSP core, while the C6211 has C62x DSP core.
- **Coprocessors:** The C6416 has two high-performance, embedded coprocessors: Viterbi Decoder Coprocessor (VCP) and Turbo Decoder Coprocessor (TCP) that significantly speed up channel-decoding operations on chip.
- **Core Supply Voltage:** The C6211 requires 1.8V of core supply voltage. The C641x requires only 1.2V or 1.4V of core supply voltage, allowing high performance while still maintaining low power consumption.
- **Clock Rate:** The C6211 runs at 150 and 167 MHz, while C641x will run at 500-720 MHz.
- **Phase-Lock Loop (PLL):** The PLL circuitry on the C6211 supports clock multiplier factors x1 and x4; while on the C641x, multiplier factors of x1, x6, and x12 are supported.
- **Internal Memory:** To support the high performance of the DSP core, the L1/L2 caches in C64x have been increased in size over C62x, with 16 KB each in L1P and L1D caches, and 1024 KB in the unified L2 memory. Furthermore, the L2 memory in C641x can be configured as memory-mapped SRAM, or a combination of SRAM and L2 cache.
- **Enhanced Direct Memory Access (EDMA):** The C6211 has 16 independent EDMA channels. The C641x has the EDMA improved to 64 independent channels.

- **External Memory Interface (EMIF):** The C6211 has a 32-bit wide EMIF, while the C641x has two EMIFs; EMIFA and EMIFB, which are 64- and 16-bit wide respectively. In addition, the C641x EMIF offers additional flexibility by replacing the SBSRAM mode with a programmable synchronous interface, which supports glueless interfaces to the following:
  - Zero Bus Turnaround (ZBT) SRAM
  - Synchronous FIFOs
  - Pipeline and flow-through SBSRAM
- **Timers:** One 32-bit timer has been added to the C641x, bringing the total to three.
- **Multi-channel Buffered Serial Port (McBSP):** One McBSP has been added to the C641x, bringing the total to three. Additional new features include:
  - Enhanced multi-channel selection capability allows the McBSP to independently select up to 128 channels per phase frame.
  - Enhanced sample rate generator.
- **Host Port Interface (HPI):** The C6211 has a 16-bit HPI. The advanced 32-bit HPI available in the C641x allows 32- and 16-bit mode of operation.
- **Peripheral Component Interconnect (PCI):** The C6211 does not have a PCI. This peripheral is available in the C6415 and C6416. The PCI on the C6415 and C6416 has been improved over the PCI in C62x/C67x devices.
- **Universal Test and Operations Interface for ATM (UTOPIA):** This peripheral is featured only on the C6415 and C6416. This peripheral supports the UTOPIA Level 2 interface as a slave ATM controller. Both the CPU and EDMA are capable of servicing the UTOPIA peripheral.
- **General-Purpose Input/Output (GPIO):** On the C6211, GPIO pins are shared with timers and McBSP pins. The C641x extends this capability by adding a dedicated GPIO module, with 16 GPIO pins. The GPIO peripheral can be programmed to generate different CPU interrupts and EDMA events.
- **Device boot configurations:** The C6211 uses pull up/down resistors on the HPI pins to determine boot process and device configurations at reset. On the C641x, the pull up/down resistors on the EMIFB address bus determine boot process and device configurations.

### 3.3 Similarities Between the C6414, C6415, and C6416 DSPs

The following device components are identical between the C6414, C6415, and C6416 devices:

- C64x fixed-point DSP core
- Internal memory structure including L1 and L2 cache architectures
- Enhanced DMA (EDMA) Controller: 64 independent channels
- External Memory Interface (EMIF): 64-bit wide EMIFA and 16-bit wide EMIFB
- 32-bit timers
- Multichannel Buffered Serial Port (McBSP)
- Host Port Interface (HPI): 32-bit wide data bus, capable of 32- and 16-bit mode of operation.



- General-Purpose Input/Output (GPIO)
- Power down logic
- PLL

### 3.4 Differences Between the C6414, C6415, and C6416 DSPs

Featuring additional peripherals, the C6415 DSP can be viewed as the superset of C6414, and the C6416 DSP as the superset of C6415. The following is the list of differences between the C6414, C6415, and C6416 DSPs:

- **UTOPIA:** This peripheral exists only on the C6415 and C6416.
- **PCI:** This peripheral exists only on the C6415 and C6416.
- **VCP/TCP:** These coprocessors are featured only on the C6416.
- **Device boot configuration:** The UTOPIA and PCI peripherals on the C6415 are configurable only at reset by pull up/down resistors on external pins. They are mutually exclusive with other peripherals.
  - UTOPIA:  
The UTOPIA and McBSP1 are mutually exclusive. Only one of them is available for use after reset.
  - PCI vs. HPI/GPIO[9:15]  
Sixteen GPIO pins are available on the C6414, C6415, and C6416 DSPs. On the C6415 and C6416, GPIO 9 to 15, along with HPI, are only available when PCI is disabled. When PCI is enabled, HPI/GPIO[9:15] are not available.

Table 1 summarizes the peripheral differences between the C6211 and the C6414, C6415, and C6416 devices. For more information on device configurations, see *TMS320C6000 Peripherals Reference Guide* (SPRU190) and device-specific data sheets.

**Table 1. Peripheral Features on the C6211 and C641x**

Peripherals	C6211	C6414	C6415	C6416
L1P	4 KB Direct-mapped	16 KB Direct-mapped		
L1D	4 KB 2-way set-associative	16 KB 2-way set-associative		
L2	64 KB (SRAM/Cache)	1024 KB (SRAM/Cache)		
EMIF	32-bit bus width	EMIFA (16 bit) and EMIFB (64 bit)		
EDMA	16 channels	64 channels		
HPI	16 bit	32-/16-bit user-selectable		
McBSP	2	3		
Timers	2	3		
GPIO	Shared with Timer and McBSP pins	Dedicated GPIO module 16 GPIO pins		
UTOPIA	-	-	8-bit slave controller Up to 50 MHz	
PCI	-	-	32 bit, 33 MHz	
VCP/TCP Coprocessors	-	-	-	Over 500 7.95-kbps AMR Up to six 2-Mbps 3GPP

### 3.5 Pin Compatibility

The C6414, C6415, and C6416 devices are pin-for-pin compatible if the following conditions are met:

- They use the same peripherals

The C6414 is pin-for-pin compatible with the C6415/C6416 when the PCI and UTOPIA peripherals on the C6415/C6416 are disabled.

The C6415 is pin-for-pin compatible with the C6416 when they are in the same peripheral selection mode. For more information on peripheral selection, see the C6415/C6416 device-specific data sheet.

- The BEA[9:7] pins are properly configured.

For correct configuration of these BEA pins, see the Terminal Functions table in the device-specific data sheet.

## 4 Begin Writing Code for the C64x Today

Full object code compatibility with existing C6000 DSPs allows system developers to begin development of C64x DSP systems today. The code-compatible fixed-point DSP cores in the C6201, C6211, and C641x devices allow for code to be written for the C641x using existing C6000 tools. By taking advantage of the C6000 software and hardware tools currently available, C641x systems can have a running start for when silicon becomes available.

The C6000 compiler may be used for all members of the C6000 device platform. Fixed-point devices are object code compatible, so the C641x may use code written for the C6211.

The C6000 simulator may be used to provide a cycle-accurate account of device performance and to provide a good environment to learn the C6000 VLIW architecture. The C64x configuration of the simulator is available to model the C641x device. The C64x configuration also models the cache performance of the device. Using this configuration, it is possible to optimize code structure and data organization to take advantage of the C641x cache structure. C641x designs may be worked out in detail on the simulator prior to purchasing actual silicon.

For a development start in hardware, the C6211 DSP Starter Kit (DSK) may be used to understand the C6000 functionality. In this environment, code can be debugged while running in real time. Many of the peripherals on the C641x are, if not identical, enhanced versions of C6211 peripherals, so the DSK is a good tool to understand how to incorporate the peripherals into a real-time system. The identical architectures of the C6211 and C641x devices allow for many system-level issues to be resolved prior to obtaining C641x silicon. Applications running on the C6211 DSK will not be 100% cycle accurate to a C641x system, due to the difference in the internal memory architecture, EMIF, DSP core, clock rates, and other peripherals.

Using these development platforms, as well as the C6000 literature currently available will enable C641x systems to be completed soon after C641x silicon is made available.

### 4.1 C6000 Tools Support

C6000 tools are available now for use in all C6000 designs. The C6000 development tools available today for the C641x are:

- C6000 Simulator Software
- C6000 Optimizing C Compiler/Assembler
- TMS320C6711 DSP Starter Kit (DSK)
- XDS510 C6000 C Source Debugger Software
- XDS510 Emulator Hardware with JTAG Emulation Cable

### 4.2 C6000 Literature Available

A great deal of literature is available today for the C6000 devices.

- *TMS320C6000 CPU and Instruction Set Reference Guide* (SPRU189)
- *Manual Update Sheet for TMS320C6000 CPU and Instruction Set Reference Guide* (SPRZ168)
- *TMS320C6000 Peripherals Reference Guide* (SPRU190)
- *TMS320C6000 Technical Brief* (SPRU197)

- *TMS320C64x Technical Overview (SPRU395)*
- *Code Composer Studio User's Guide (SPRU328)*
- *TMS320C6000 Code Composer Studio Tutorial (SPRU301)*
- *TMS320C6000 Programmer's Guide (SPRU198)*
- *TMS320C6000 Evaluation Module User's Guide (SPRU269)*
- *TMS320C6000 Chip Support Library API Reference Guide (SPRU401)*
- *TMS320C6000 Peripheral Support Library Programmer's Reference (SPRU273)*
- *TMS320C6000 Assembly Language Tools User's Guide (SPRU186)*
- *TMS320C6000 Optimizing C Compiler User's Guide (SPRU187)*
- *TMS320C6000 C Source Debugger User's Guide (SPRU188)*
- *TMS320C6000 C Source Debugger For SPARCstations (SPRU224)*
- *TMS320C6000 DSP/BIOS User's Guide (SPRU303)*
- *TMS320C6000 DSP/BIOS Application Programming Interface (API) Reference Guide (SPRU403)*
- *DSP Algorithm Integration Standard (XDAIS) Rules and Guidelines (SPRU352)*
- *DSP Glossary (SPRU258)*
- *TMS320 DSP Standard Algorithm Developer's Guide (SPRU424)*

Many application notes also exist for assistance with C6711 applications.

- *Bit-Reverse/Digit-Reverse: Linear-Time Small Lookup Table Implementation-C6000 (SPRA440)*
- *Guidelines For Software Development Efficiency On the TMS320C6000 VelociTI Architecture (SPRA434)*
- *Implementation Of G.726 ADPCM On TMS320C62XX DSP (SPRA066)*
- *Implementing V.32BIS VITERBI Decoding on the TMS320C62XX DSP (SPRA444)*
- *Performance Analysis of Line Echo Cancellation Implementation Using TMS320C6201 (SPRA421)*
- *TMS320C6201 Power Supply (SPRA447)*
- *TMS320C6201 System Clock Circuit Example (SPRA430)*
- *TMS320C6000 EMIF to External SDRAM/SGRAM Interface (SPRA433)*
- *TMS320C6000 BGA Manufacturing Considerations (SPRA429)*

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- *TMS320C6000 Board Design: Considerations for Debug* (SPRA523)
  - *Reset Circuit for the TMS320C6000 DSP* (SPRA431)
  - *TMS320C6X Thermal Design Considerations* (SPRA432)
  - *Using the TMS320C6X McBSP as a High Speed Communication Port* (SPRA455)

**Note:** See <http://www.ti.com/sc/docs/dsps/products/c6000/index.htm> for more information.

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