

# Interfacing 5 V Sensors and Signals to 3.3 V Input SAR ADCs



## ABSTRACT

This application note covers designs and considerations for users interfacing 5 V inputs to Sitara™ AM2x microcontrollers.

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## 1 Introduction

TI's Sitara™ MCU products integrate SAR ADCs in advanced small geometry CMOS process nodes. In order to optimize for low cost and high performance and avoid high cost mask sets and/or larger die area which are required to support higher supply voltages for analog, input voltage range of these ADCs is limited to 3.3 V. For many applications this range is sufficient, however some applications, especially some legacy industrial or automotive sensors, may require higher ADC input ranges like 5 V.

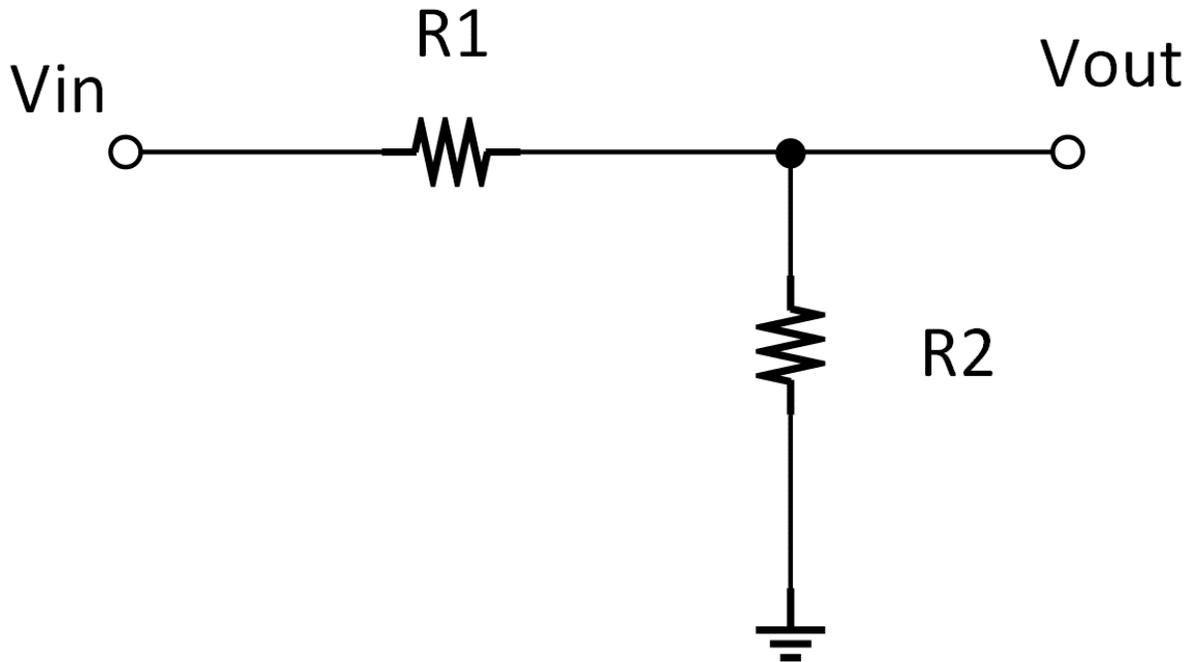
Depending on the application, there will be other design constraints, like the input source not being able to drive the sampling capacitor of the of the SAR ADC. Another design concern might be noise performance of the overall signal chain. This application note provides guidelines on how to approach the problem and interface different input sources with higher voltage rating than the Sitara™ MCU and the trade-offs.

## 2 Use-case Considerations

First, we need to check if the sensor really needs a 5 V ADC. Many sensors are rated for 5 V or works on a 5 V supply, but the analog output will not go beyond 3.3 V in the use case. As a good example the temperature sensor [LM50](#) operates on 5 V or higher supply but within the desired -40 C to 150 C operating window the maximum analog output voltage will be limited well below 3.3 V. So this sensor can easily be connected to Sitara™ ADC without any additional hardware.

### 3 Interfacing the High Voltage Sensor

The simplest and low cost method to attenuate a 5 V or any other higher voltage signal to 3.3 V is through a passive, resistor divider network as shown below. The diagram below is for single-ended implementation but can be easily extended for differential inputs as well.



**Figure 3-1. Resistive Attenuator**

$$V_{out} = V_{in} \times R2 / (R1 + R2) \quad (1)$$

If signal  $V_{in}$  has a 0-to-5 V swing and needs to drive a 0-to-3.3 V ADC input, then

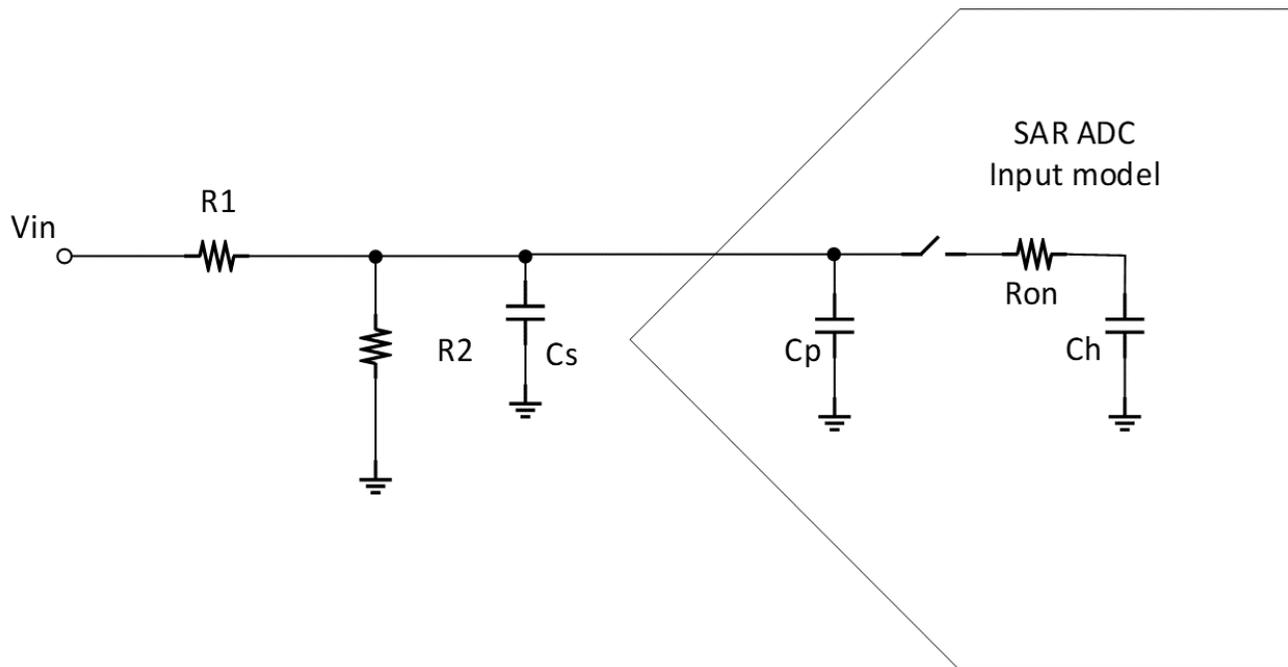
$$R2 \cong 1.94 \times R1 \quad (2)$$

If the source has any output impedance, that can be simply budgeted as part of the  $R1$ . The ground of the resistor ladder is best shorted to the clean analog ground (ADC ground or ADC negative reference) to eliminate unnecessary ground noise injection.

This simple method will work nicely but has few limitations. This limitations can be resolved by following the methods described in next few sections.

#### 3.1 Consideration for Proper ADC Sampling

During sampling window, the SAR ADC will have a capacitive network connected to the input and will sample the input voltage. This capacitive network does not provide any resistive loading and hence given enough sampling time, the input will always settle to the correct  $V_{out}$  voltage.



**Figure 3-2. ADC Interface**

TI's application note on [Charge Sharing Driving Circuits](#) gives an excellent tutorial on how to select source resistors and charge sharing capacitor to drive a SAR ADC.

$C_p$ ,  $R_{on}$ , and  $C_h$  and sampling time are ADC parameters that are given on the spec sheet of the ADC. Settling error (in LSBs), ADC driving source impedance ( $R_s = R1//R2$ ) and charge sharing capacitance value ( $C_s$ ) depend on the application and can be chosen following the guidelines on that application note. Page-30 provides an example on how to select external resistor and capacitor for a voltage divider at the input of a SAR ADC.

As a general guideline, the lower the value of  $R1$ ,  $R2$  and  $C_s$  the faster the response of the network. This guideline should be used for high bandwidth signal paths.

### 3.2 Handling High Impedance Sensor

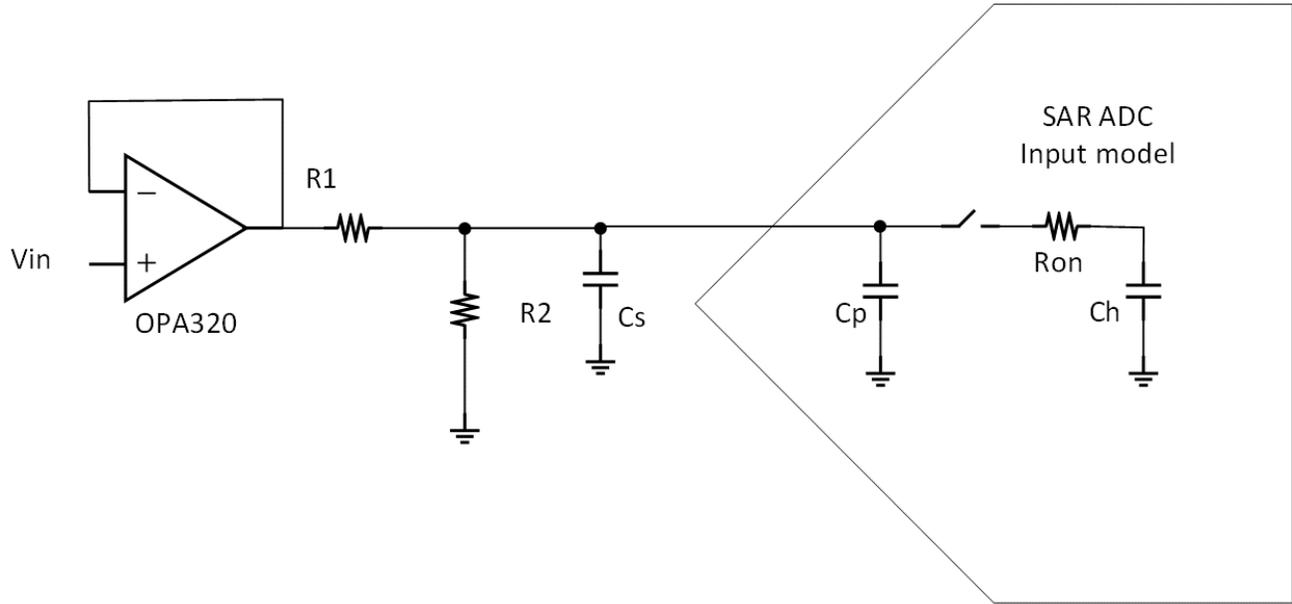
Certain applications require the ADC to sample a 5 V signal on a relatively high impedance sensor. Some of this sensor may not be able to drive or support a direct loading of  $R1+R2$  especially when they are not very high. To solve this problem, we can increase  $R1+R2$  till we meet the desired loading constraint and use a very large  $C_s$  to help in ADC sampling.

For example, we can use  $R1=1.7\text{ M}$  &  $R2=3.3\text{ M}$  along with a  $C_s=30\text{ nF}$  to provide a network which provides a 5 M impedance to the sensor while allowing clean ADC sampling even at highest sampling rate.

Care must be taken for the ADC input loading on the accuracy of the circuit when using high value for  $R1$  &  $R2$ . For example, in this use case if the ADC is configured to switch to this sensor and sample the Resistor ladder every 1  $\mu\text{s}$ , that will provide a worst-case average loading of  $R=1\text{ }\mu\text{s}/(C_p+C_h) \approx 100\text{ K}$  which is significant compared to the resistor ladder and hence will provide considerable error in measurement. To improve this error, we simply need to reduce the sample rate. If we sense this input at every 1 ms this impedance jumps to  $\approx 100\text{ M}$  and will not have any impact on the accuracy. This reduction of update rate is usually not a concern for high impedance sensors as they are inherently slow by nature. Additionally, this ladder network will also have an analog filter at  $\approx 4\text{ Hz}$ , so sampling at every 1  $\mu\text{s}$  is no different than sampling at every 1 ms. As an added benefit this filtering can help eliminate system noise in many use-cases.

A better but slightly costlier way to solve the problem is to use an OPAMP with a high input impedance, and a low output impedance. TI's high-performance low cost OPAMPS have a very wide selection and many application notes. One example with popular OPA320 or OPA320-Q1 is shown below. A high impedance unity

gain OPAMP with low output impedance is driving the resistor divider and providing isolation from the resistor divider and sampling capacitor.



**Figure 3-3. Opamp Drive Circuit**

## 4 Performance Considerations

The below sections look at performance metrics relating to reducing the dynamic range of the signal.

### 4.1 ADC Gain, Offset, INL & DNL

Assume the ADC has an offset  $m$  LSB. Now assume  $V1$  is the input voltage and  $LSB$  is the step size of the actual 3.3 V SAR ADC inside Sitara MCU ( $\approx 3.3/2^{12}$ ). The ADC generates an output code 'c' with input of 'V1' and has an offset of 'm' LSB.

$$V1 = c \times LSM + m \times LSB \quad (3)$$

$$c = (V1/LSB) + m \quad (4)$$

Now assume  $V2$  is applied at the input of the Resistor ladder, so at the input of ADC the voltage

$$V3 = V2 \times R1/(R1 + R2) \quad (5)$$

$$C2 = (V3/LSB) + m \quad (6)$$

$$V3 = C2 \times LSB + m \times LSB \quad (7)$$

$$V2 = C2 \times LSB \times (R1 + R2)/R1 + m \times LSB \times (R1 + R2)/R1 \quad (8)$$

Comparing the previous two equations, one can say the resistor ladder simply scales the LSB size and the offset effectively remains the 'same number of LSBs' as it was with the 3.3 V ADC. The gain error and INL, DNL also can be proven to be scaled in same way.

In simple words if the 3.3 V ADC has an offset error of 2 LSB (with  $LSB=3.3/4096$ ), then at the input of the resistor ladder it still has a 2 LSB offset error with a slightly larger  $LSB=5/4096$ .

### 4.2 SNR Consideration

For a **12b ADC**, 5 V to 3.3 V SNR degradation will cause about  $\frac{1}{2}$  **LSB SNR** loss, which is usually not very significant. The ideal 12 Bit ADC SNR will degrade from 74 dB to 70.6 dB with a 5 V to 3.3 V attenuation. The below definitions and equations explain the degradation.

**Source noise:** Any noise embedded in signal  $V_{in}$ , will also get attenuated with the resistor divider circuit, hence it will not affect overall Signal to Noise Ratio (SNR) performance.

**Common ground noise:** The common ground noise will not be attenuated by the resistor divider circuit, hence that will have an impact on the SNR. The SNR will be degraded by the attenuation factor. For a 5 V to 3.3 V signal attenuation, the SNR degradation will be:

$$3.3/5 = 0.66 \quad (9)$$

$$20 \log (0.66) \cong -3.6 \text{ dB} \quad (10)$$

An N bit ADC's ideal SNR is equal to

$$Ideal \text{ SNR} = 6.02 \times N + 1.76 \text{ dB} \quad (11)$$

### 4.3 Performance Advantage

The Sitara™ MCU has an ADC which operates in 3.3 V and has a step size which is much less ( $\approx 66\%$  less) than the step size of a similar 5 V ADC. With clever system design this can be used to a significant advantage. Most sensors have a wide operating range, but the use-case might limit the output variation to a limited range (see section 2). For example, let's consider a use case where we are using the LM35 temperature sensor and we are operating in room temperature (27 C). If the sensor is directly connected to Sitara™ MCU we get a step resolution of  $\approx 800 \mu\text{V}$  ( $\approx 3.3 \text{ V}/4096$ ) allowing a temperature resolution  $\approx 0.08 \text{ C}$  (each ADC LSB will be  $\approx 0.08 \text{ C}$ ), whereas if we connect an equivalent 5 V ADC (with step size =  $5 \text{ V}/4096 \approx 1.2 \text{ mV}$ ) we can only measure a temperature resolution  $\approx 0.12 \text{ C}$ .

## 5 Conclusion

Supporting a high voltage sensor does not always require a high voltage ADC. This document explains multiple points that must be taken into consideration before we move to a high voltage design. A 5 V to 3.3 V attenuator circuit is a low cost, efficient way of interfacing 5 V signals to a monolithic 3.3 V ADC of Sitara™ MCU products. Signal degradation is negligible for most applications.

## 6 References

- [Sitara MCU Device Portfolio](#)

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