TMS320DM646x DMSoC 64-Bit Timer

User's Guide



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Prefa	ce		5
1	Introd	uction	7
	1.1	Purpose of the Peripheral	7
	1.2	Features	7
	1.3	Functional Block Diagram	8
	1.4	Industry Standard Compatibility Statement	8
2	Archit	ecture	8
	2.1	Clock Control	8
	2.2	Signal Descriptions	9
	2.3	General-Purpose (GP) Timer Modes	10
	2.4	Watchdog Timer Mode	17
	2.5	Timer Pulse Generation	20
	2.6	Reset Considerations	20
	2.7	Interrupt Support	20
	2.8	EDMA Event Support	21
	2.9	Emulation Considerations	21
3	Regist	ters	22
	3.1	Peripheral Identification Register 12 (PID12)	22
	3.2	Emulation Management Register (EMUMGT)	23
	3.3	Timer Counter Registers (TIM12 and TIM34)	24
	3.4	Timer Period Registers (PRD12 and PRD34)	25
	3.5	Timer Control Register (TCR)	26
	3.6	Timer Global Control Register (TGCR)	28
	3.7	Watchdog Timer Control Register (WDTCR)	29
Appe	ndix A	Revision History	30



List of Figures

1	Timer Block Diagram	8
2	64-Bit Timer Mode Block Diagram	10
3	Dual 32-Bit Timers Chained Mode Block Diagram	12
4	Dual 32-Bit Timers Chained Mode Example	12
5	Dual 32-Bit Timers Unchained Mode Block Diagram	14
6	Dual 32-Bit Timers Unchained Mode Example	15
7	32-Bit Timer Counter Overflow Example	17
8	Watchdog Timer Mode Block Diagram	18
9	Watchdog Timer Operation State Diagram	19
10	Peripheral Identification Register 12 (PID12)	22
11	Emulation Management Register (EMUMGT)	23
12	Timer Counter Register 12 (TIM12)	24
13	Timer Counter Register 34 (TIM34)	24
14	Timer Period Register 12 (PRD12)	25
15	Timer Period Register 34 (PRD34)	25
16	Timer Control Register (TCR)	26
17	Timer Global Control Register (TGCR)	28
18	Watchdog Timer Control Register (WDTCR)	29

List of Tables

1	Supported Timer Features by Instantiation	7
2	Supported Timer Clock Sources	8
3	Timer Clock Source Selection	9
4	Timer Signals	9
5	64-Bit Timer Configurations	11
6	32-Bit Timer Chained Mode Configurations	13
7	32-Bit Timer Unchained Mode Configurations	16
8	Counter and Period Registers Used in GP Timer Modes	16
9	Timer Interrupts Generated	20
10	Timer Interrupts	21
11	Timer EDMA Events Generated	21
12	Timer Emulation Modes Selection	21
13	64-Bit Timer Registers	22
14	Peripheral Identification Register 12 (PID12) Field Descriptions	22
15	Emulation Management Register (EMUMGT) Field Descriptions	23
16	Timer Counter Register 12 (TIM12) Field Descriptions	24
17	Timer Counter Register 34 (TIM34) Field Descriptions	24
18	Timer Period Register (PRD12) Field Descriptions	25
19	Timer Period Register (PRD34) Field Descriptions	25
20	Timer Control Register (TCR) Field Descriptions	26
21	Timer Global Control Register (TGCR) Field Descriptions	28
22	Watchdog Timer Control Register (WDTCR) Field Descriptions	29
23	Document Revision History	30



Read This First

About This Manual

Describes the operation of the software-programmable 64-bit timer in the TMS320DM646x Digital Media System-on-Chip (DMSoC). Timer0 and Timer1 (controlled by the ARM or the DSP) are used as general-purpose (GP) timers and can be programmed in 64-bit mode, dual 32-bit unchained mode, or dual 32-bit chained mode; Timer2 (controller mainly by the ARM) is used only as a watchdog timer. The GP timer modes can be used to generate periodic interrupts or enhanced direct access (EDMA) synchronization events. The watchdog timer mode is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop. Chip implementation prevents Timer2 from being used as a general purpose timer. Although Timer0 and Timer1 may also be configured for watchdog timer mode, only Timer2 may generate a watchdog timer reset of the device.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
 - Each register figure shows a rectangle divided into fields that represent the fields of the register.
 Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
 - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320DM646x Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the Internet at <u>www.ti.com</u>. *Tip:* Enter the literature number in the search box provided at www.ti.com.

The current documentation that describes the DM646x DMSoC, related peripherals, and other technical collateral, is available in the C6000 DSP product folder at: www.ti.com/c6000.

<u>SPRUEP8</u> — *TMS320DM646x DMSoC DSP Subsystem Reference Guide.* Describes the digital signal processor (DSP) subsystem in the TMS320DM646x Digital Media System-on-Chip (DMSoC).

- SPRUEP9 TMS320DM646x DMSoC ARM Subsystem Reference Guide. Describes the ARM subsystem in the TMS320DM646x Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the DSP subsystem and a majority of the peripherals and external memories.
- SPRUEQ0 TMS320DM646x DMSoC Peripherals Overview Reference Guide. Provides an overview and briefly describes the peripherals available on the TMS320DM646x Digital Media System-on-Chip (DMSoC).
- SPRAA84 TMS320C64x to TMS320C64x+ CPU Migration Guide. Describes migrating from the Texas Instruments TMS320C64x digital signal processor (DSP) to the TMS320C64x+ DSP. The objective of this document is to indicate differences between the two cores. Functionality in the devices that is identical is not included.



- SPRU732 TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide. Describes the CPU architecture, pipeline, instruction set, and interrupts for the TMS320C64x and TMS320C64x+ digital signal processors (DSPs) of the TMS320C6000 DSP family. The C64x/C64x+ DSP generation comprises fixed-point devices in the C6000 DSP platform. The C64x+ DSP is an enhancement of the C64x DSP with added functionality and an expanded instruction set.
- SPRU871 TMS320C64x+ DSP Megamodule Reference Guide. Describes the TMS320C64x+ digital signal processor (DSP) megamodule. Included is a discussion on the internal direct memory access (IDMA) controller, the interrupt controller, the power-down controller, memory protection, bandwidth management, and the memory and cache.



64-Bit Timer/Watchdog Timer

1 Introduction

This document describes the operation of the software-programmable 64-bit timer in the TMS320DM646x Digital Media System-on-Chip (DMSoC). The DM646x DMSoC processor contains three software-programmable timers. Timer0 and Timer1 (general-purpose timers) can be controlled by the ARM or the DSP. Timer0 and Timer1 can be programmed in 64-bit mode, dual 32-bit unchained mode, or dual 32-bit chained mode. Timer2 is used as a watchdog timer and is mainly controlled by the ARM.

1.1 Purpose of the Peripheral

The timers support four modes of operation: a 64-bit general-purpose (GP) timer, dual unchained 32-bit GP timers, dual chained 32-bit timers, or a watchdog timer. The GP timer modes can be used to generate periodic interrupts or EDMA synchronization events. The watchdog timer mode is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop. The capabilities of each of the timers are summarized in Table 1.

Table 1. Supported Timer Features by Instantiation

Capability	Timer0	Timer1	Timer2
64-bit general-purpose timer		\checkmark	-
Dual 32-bit general-purpose timer (unchained)	\checkmark	\checkmark	-
Dual 32-bit general-purpose timer (chained)	\checkmark	\checkmark	-
External clock input	2 (TINP0L and TINP0U)	1 (TINP1I)	-
Watchdog timer	-	-	\checkmark

1.2 Features

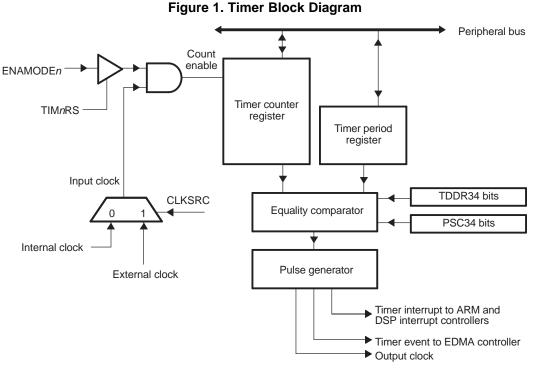
The 64-bit timer consists of the following features.

- 64-bit count-up counter
- Timer modes:
 - 64-bit general-purpose timer mode
 - Dual 32-bit general-purpose timer mode (chained or unchained)
 - Watchdog timer mode
- 2 possible clock sources:
 - Internal clock
 - External clock input via timer input pin
- 2 possible operation modes:
 - One-time operation (timer runs for one period then stops)
 - Continuous operation (timer automatically resets after each period)
- Generates interrupts to both the DSP and the ARM CPUs
- Generates sync event to EDMA
- Supports various output pulse generation modes



1.3 Functional Block Diagram

A block diagram of the timer is shown in Figure 1. Detailed information about the architecture and operation of the timers is in Section 2 and Section 2.4.



NOTE: TDDR34 and PSC34 apply only to Timer3:4.

1.4 Industry Standard Compatibility Statement

This peripheral is not intended to conform to any specific industry standard.

2 Architecture

This section describes the timer in the general-purpose (GP) timer mode and watchdog timer mode. Timer0 and Timer1 can be used in GP timer mode. Timer2 can only be used as a watchdog timer. To use Timer2 as a watchdog timer, see Section 2.4.

2.1 Clock Control

The timer can use an internal or external clock source for the counter period. The following sections explain how to select the clock source. Table 2 shows which clock sources are supported on each timer.

Clock Source	Timer0	Timer1	Timer2	
Internal clock source	\checkmark	\checkmark	\checkmark	
External clock input	2 (TINP0L and TINP0U)	1 (TINP1I)	-	

Table 2. Supported Timer Clock Sources



As shown in Table 3, the timer clock source is selected using the clock source (CLKSRC12 and CLKSRC34) bit in the timer control register (TCR). Two clock sources are available to drive the timer clock:

- internal clock, by setting CLKSRC12 = 0 and/or CLKSRC34 = 0.
- external clock, by setting CLKSRC12 = 1 and/or CLKSRC34 = 1. This input signal is synchronized internally.

At reset, the clock source is the internal clock. Details on each of the clock source configuration options are included in the following sections.

CLKSRC12/ CLKSRC34	Input Clock
0	Internal clock (default)
1	External clock

Table 3. Timer Clock Source Selection

2.1.1 Using the Internal Clock Source to the Timer

The internal clock source to the timer is SYSCLK3, which is the PLL0 clock divided by 4. For detailed information on the PLLs and clock distribution on the processor, see the *TMS320DM646x DMSoC ARM Subsystem Reference Guide* (SPRUEP9).

External clock sources can be provided to clock the timer via the TINP0L, TINP0U, and TINP1I pin. TINP0L is connected to TINP12 (timer 1:2 side) of Timer0; TINP0U is connected to TINP34 (timer 3:4 side) of Timer0; TINP1I is connected to TINP12 (timer 1:2 side) of Timer1.

The CLKSRC12 and CLKSRC34 parameter in the timer control register (TCR) controls whether the internal or external clock is used as the clock source for the timer. If the timer is configured in 64-bit mode or 32-bit chained mode, CLKSRC12 controls the clock source for the entire timer. If the timer is configured in dual 32-bit unchained mode (TIMMODE = 01 in TGCR), CLKSRC12 controls the timer 1:2 side of the Timer; and CLKSRC34 controls timer 3:4 side of the Timer. The timer 3:4 side of Timer1 must use the internal clock (CLKSRC34 = 0) because there is no external clock for timer 3:4 side of Timer1.

2.2 Signal Descriptions

The signals of the timer modules are shown in Table 4

Signal	I/O	Signal Explanation
TINP0L	I	Input clock to the timer 1:2 side of Timer0
TINP0U	I	Input clock to the timer 3:4 side of Timer0 (Only in 32-bit unchained mode)
TINP1I	I	Input clock to the timer 1:2 side of Timer1
TOUTOL	0	Output clock from the timer 1:2 side of Timer0
TOUT0U	0	Output clock from the timer 3:4 side of Timer0 (Only in 32-bit unchained mode)
TOUT1L	0	Output clock from the timer 1:2 side of Timer1
TOUT1U	0	Output clock from the timer 3:4 side of Timer1 (Only in 32-bit unchained mode)
TOUT2	0	Output clock from the timer 1:2 side of Timer2 (To signal WD timeout to off-chip devices)

Table 4. Timer Signals

2.3 General-Purpose (GP) Timer Modes

The following section describes the general-purpose (GP) timer modes. To use the timer as a watchdog timer (Timer2 only), see Section 2.4.

2.3.1 64-Bit Timer Mode (Timer0 and Timer1)

The general-purpose timers can each be configured as a 64-bit timer by clearing the TIMMODE bit in the timer global control register (TGCR) to 0. At reset, 0 is the default setting for the TIMMODE bit.

In this mode, the timer operates as a single 64-bit up-counter (Figure 2). The counter registers (TIM12 and TIM34) form a 64-bit timer counter register and the period registers (PRD12 and PRD34) form a 64-bit timer period register. When the timer is enabled, the timer counter starts incrementing by 1 at every timer input clock cycle. When the timer counter matches the timer period, a maskable timer interrupt and a timer EDMA event are generated. When the timer is configured in continuous mode, the timer counter is reset to 0 on the cycle after the timer counter reaches the timer period. The timer can be stopped, restarted, reset, or disabled using control bits in TGCR.

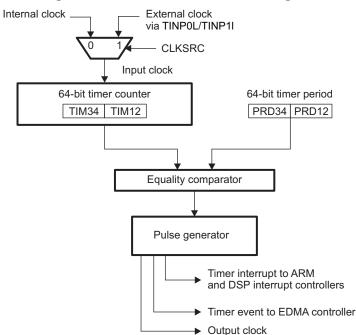


Figure 2. 64-Bit Timer Mode Block Diagram

2.3.1.1 Enabling the 64-Bit Timer

The TIM12RS and TIM34RS bits in TGCR control whether the timer is in reset or capable of operating. For the timer to operate in 64-bit timer mode, the TIM12RS and TIM34RS bits must be set to 1.

The ENAMODE12 bit in the timer control register (TCR) controls whether the timer is disabled, enabled to run once, or enabled to run continuously; the ENAMODE34 bit has no effect in 64-bit timer mode. When the timer is disabled (ENAMODE12 = 0), the timer does not run and maintains its current count value. When the timer is enabled for one time operation (ENAMODE12 = 1), it counts up until the counter value equals the period value and then stops. When the timer is enabled for continuous operation (ENAMODE12 = 2h), the counter counts up until it reaches the period value, then resets itself to zero and begins counting again.

Table 5 shows the bit values in TGCR to configure the 64-bit timer.

	TGC	TCR Bit	
64-Bit Timer Configuration	TIM12RS	TIM34RS	ENAMODE12
To place the 64-bit timer in reset	0	0	0
To disable the 64-bit timer (out of reset)	1h	1h	0
To enable the 64-bit timer for one-time operation	1h	1h	1h
To enable the 64-bit timer for continuous operation	1h	1h	2h

Table 5. 64-Bit Timer Configurations

Once the timer stops, if an external clock is used as the timer clock, the timer must remain disabled for at least one external clock period or the timer will not start counting again. When using the external clock, the count value is synchronized to the internal clock.

Note that when both the timer counter and timer period are cleared to 0, the timer can be enabled but the timer counter does not increment because the timer period is 0.

2.3.1.2 Reading the Counter Registers

When reading the timer count in 64-bit timer mode, the CPU must first read TIM12 followed by TIM34. When TIM12 is read, the timer copies TIM34 into a shadow register. When reading TIM34, the hardware logic forces the reads to read from the shadow register. This ensures that the values read from the registers are not affected by the fact that the timer may continue to run as the registers are read. When reading the timers in 32-bit mode, TIM12 and TIM34 may be read in either order.

2.3.1.3 64-Bit Timer Configuration Procedure

To configure the GP timer to operate as a 64-bit timer, follow the steps below:

- 1. Select 64-bit mode (TIMMODE bit in TGCR).
- 2. Remove the timer from reset (TIM12RS and TIM34RS bits in TGCR).
- 3. Select the desired timer period (PRD12 and PRD34).
- 4. Enable the timer (ENAMODE12 bit in TCR).

2.3.2 Dual 32-Bit Timer Modes (Timer0 and Timer1)

Each of the general-purpose timers can be configured as dual 32-bit timers by configuring the TIMMODE bit in the timer global control register (TGCR). In dual 32-bit timer mode, the two 32-bit timers can be operated independently (unchained mode) or in conjunction with each other (chained mode).

2.3.2.1 Chained Mode

The general-purpose timers can each be configured as a dual 32-bit chained timer by setting the TIMMODE bit in TGCR to 3h

In the chained mode (Figure 3), one 32-bit timer (timer 3:4) is used as a 32-bit prescaler and the other 32-bit timer (timer 1:2) is used as a 32-bit timer. The 32-bit prescaler is used to clock the 32-bit timer. The 32-bit prescaler uses one counter register (TIM34) to form a 32-bit prescale counter register and one period register (PRD34) to form a 32-bit prescale period register.

When the timer is enabled, the prescale counter starts incrementing by 1 at every timer input clock cycle. One cycle after the prescale counter matches the prescale period, a clock signal is generated and the prescale counter register is reset to 0 (see the example in Figure 4).

The other 32-bit timer (timer 1:2) uses one counter register (TIM12) to form a 32-bit timer counter register and one period register (PRD12) to form a 32-bit timer period register. This timer is clocked by the output clock from the prescaler. The timer counter increments by 1 at every prescaler output clock cycle. When the timer counter matches the timer period, a maskable timer interrupt and a timer EDMA event are generated. When the timer is configured in continuous mode, the timer counter is reset to 0 on the cycle after the timer counter reaches the timer period. The timer can be stopped, restarted, reset, or disabled using the TIM12RS and TIM34RS bits in TGCR. In the chained mode, the upper 16-bits of the timer control register (TCR) are not used.

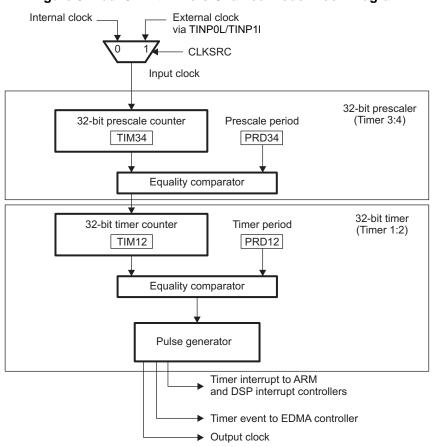
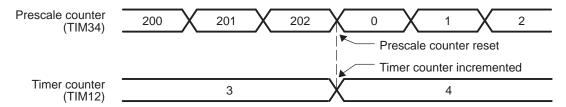


Figure 3. Dual 32-Bit Timers Chained Mode Block Diagram

Figure 4. Dual 32-Bit Timers Chained Mode Example

32-bit prescaler settings: count = TIM34 = 200; period = PRD34 = 202 32-bit timer settings: count = TIM12 = 3; period = PRD12= 4



2.3.2.1.1 Enabling the 32-Bit Timer Chained Mode

The TIM12RS and TIM34RS bits in TGCR control whether the timer is in reset or capable of operating. The TIM12RS bit controls the reset of the timer 1:2 side of the timer and the TIM34RS bits control the reset of the timer 3:4 side of the timer. For the timer to operate, the TIM12RS and TIM34RS bits must be set to 1.

The ENAMODE12 bit in the timer control register (TCR) controls whether the timer is disabled, enabled to run once, or enabled to run continuously; the ENAMODE34 bit has no effect in 32-bit timer chained mode. When the timer is disabled (ENAMODE12 = 0), the timer does not run and maintains its current count value. When the timer is enabled for one time operation (ENAMODE12 = 1), it counts up until the counter value equals the period value and then stops. When the timer is enabled for continuous operation (ENAMODE12 = 2h), the counter counts up until it reaches the period value, then resets itself to zero and begins counting again.

Table 6 shows the bit values in TGCR to configure the 32-bit timer in chained mode.

	TGC	TCR Bit	
32-Bit Timer Configuration	TIM12RS	TIM34RS	ENAMODE12
To place the 32-bit timer chained mode in reset	0	0	0
To disable the 32-bit timer chained mode (out of reset)	1h	1h	0
To enable the 32-bit timer chained mode for one-time operation	1h	1h	1h
To enable the 32-bit timer chained mode for continuous operation	1h	1h	2h

Table 6. 32-Bit Timer Chained Mode Configurations

Once the timer stops, if an external clock is used as the timer clock, the timer must remain disabled for at least one external clock period or the timer will not start counting again. When using the external clock, the count value is synchronized to the internal clock.

Note that when both the timer counter and timer period are cleared to 0, the timer can be enabled but the timer counter does not increment because the timer period is 0.

2.3.2.1.2 32-Bit Timer Chained Mode Configuration Procedure

To configure the GP timer to operate as a dual 32-bit chained mode timer, follow the steps below:

- 1. Select 32-bit chained mode (TIMMODE bit in TGCR).
- 2. Remove the timer from reset (TIM12RS and TIM34RS bits in TGCR).
- 3. Select the desired timer period (PRD12).
- 4. Select the desired timer prescaler value (PRD34).
- 5. Enable the timer (ENAMODE12 bit in TCR).



2.3.2.2 Unchained Mode

The general-purpose timers can each be configured as a dual 32-bit unchained timers by setting the TIMMODE bit in TGCR to 1

In the unchained mode (Figure 5), the timer operates as two independent 32-bit timers. One 32-bit timer (timer 3:4) operates as a 32-bit timer being clocked by a 4-bit prescaler. The other 32-bit timer (timer 1:2) operates as a 32-bit timer with no prescaler.

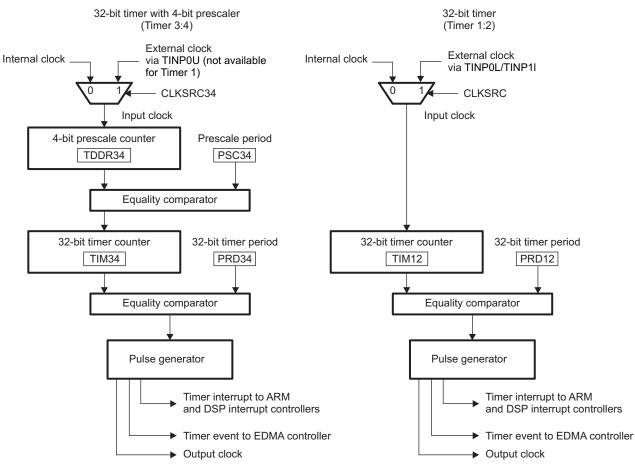


Figure 5. Dual 32-Bit Timers Unchained Mode Block Diagram

2.3.2.2.1 32-Bit Timer With a 4-Bit Prescaler

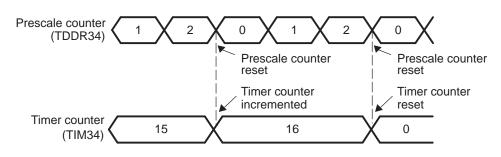
In the unchained mode, the 4-bit prescaler must be clocked by the internal clock; an external clock source cannot be used for timer 3:4. The 4-bit prescaler uses the timer divide-down ratio (TDDR34) bit in TGCR to form a 4-bit prescale counter register and the prescale counter bits (PSC34) to form a 4-bit prescale period register (see Figure 5). When the timer is enabled, the prescale counter starts incrementing by 1 at every timer input clock cycle. One cycle after the prescale counter matches the prescale period, a clock signal is generated for the 32-bit timer.

The 32-bit timer uses TIM34 as a 32-bit timer counter register and PRD34 as a 32-bit timer period register. The 32-bit timer is clocked by the output clock from the 4-bit prescaler (see the example in Figure 6). The timer counter increments by 1 at every prescaler output clock cycle. When the timer counter matches the timer period, a maskable timer interrupt and a timer EDMA event are generated. When the timer is configured in continuous mode, the timer counter is reset to 0 on the cycle after the timer counter reaches the timer period. The timer can be stopped, restarted, reset, or disabled using the TIM34RS bit in TGCR. For timer 3:4, the lower 16 bits of the timer control register (TCR) have no control.



Figure 6. Dual 32-Bit Timers Unchained Mode Example

4-bit prescaler settings: count = TDDR34 = 1; period = PSC34 = 2 32-bit timer settings: count = TIM34 = 15; period = PRD34 = 16



2.3.2.2.2 32-Bit Timer with No Prescaler

The other 32-bit timer (timer 1:2) uses TIM12 as the 32-bit counter register and PRD12 as a 32-bit timer period register (see Figure 5). When the timer is enabled, the timer counter increments by 1 at every timer input clock cycle. When the timer counter matches the timer period, a maskable timer interrupt and a timer EDMA event are generated. When the timer is configured in continuous mode, the timer counter is reset to 0 on the cycle after the timer counter reaches the timer period. The timer can be stopped, restarted, reset, or disabled using the TIM12RS bit in TGCR. For timer 1:2, the upper 16 bit of the timer control register (TCR) have no control.

2.3.2.2.3 Enabling the 32-Bit Unchained Mode Timer

The TIM12RS and TIM34RS bits in TGCR control whether the timer is in reset or capable of operating. The TIM12RS bit controls the reset of the timer 1:2 side of the timer and the TIM34RS bit controls the reset of the timer 3:4 side of the timer. For the timer to operate, the TIM12RS and/or TIM34RS bits must be set to 1.

The ENAMODE*n* bit in the timer control register (TCR) controls whether the timer is disabled, enabled to run once or enabled to run continuously. When the timer is disabled (ENAMODEn = 0), the timer does not run and maintains its current count value. When the timer is enabled for one time operation (ENAMODEn = 1), it counts up until he counter value equals the period value and then stops. When the timer is enabled for continuous operation (ENAMODEn = 2h), the counter counts up until it reaches the period value, then resets itself to zero and begins counting again.

Table 7 shows the bit values in TGCR to configure the 32-bit timer in unchained mode.

Once the timer stops, if an external clock is used as the timer clock, the timer must remain disabled for at least one external clock period or the timer will not start counting again. When using the external clock, the count value is synchronized to the internal clock. External clock is only available on the timer 1:2 side in unchained mode.

Note that when both the timer counter and timer period are cleared to 0, the timer can be enabled but the timer counter does not increment because the timer period is 0.



	TGC	R Bit	TCF	R Bit	
32-Bit Timer Configuration	TIM12RS	TIM34RS	ENAMODE12	ENAMODE34	
To place the 32-bit timer unchained mode with 4-bit prescaler in reset	х	0	х	0	
To disable the 32-bit timer unchained mode with 4-bit prescaler (out of reset)	х	1h	x	0	
To enable the 32-bit timer unchained mode with 4-bit prescaler for one-time operation	х	1h	x	1h	
To enable the 32-bit timer unchained mode with 4-bit prescaler for continuous operation	х	1h	x	2h	
To place the 32-bit timer unchained mode with no prescaler in reset	0	х	0	x	
To disable the 32-bit timer unchained mode with no prescaler (out of reset)	1h	х	0	x	
To enable the 32-bit timer unchained mode with no prescaler for one-time operation	1h	х	1h	x	
To enable the 32-bit timer unchained mode with no prescaler for continuous operation	1h	x	2h	x	

Table 7. 32-Bit Timer Unchained Mode Configurations

2.3.2.2.4 32-Bit Timer Unchained Mode Configuration Procedure

To configure timer 1:2, follow the steps below:

- 1. Select 32-bit unchained mode (TIMMODE bit in TGCR).
- 2. Remove the timer 1:2 from reset (TIM12RS bit in TGCR).
- 3. Select the desired timer period for timer 1:2 (PRD12).
- 4. Select the desired clock source for timer 1:2 (CLKSRC12 bit in TCR).
- 5. Enable timer 1:2 (ENAMODE12 bit in TCR).

To configure timer 3:4, follow the steps below:

- 1. Select 32-bit unchained mode (TIMMODE bit in TGCR).
- 2. Remove the timer 3:4 from reset (TIM34RS bit in TGCR).
- 3. Select the desired timer period for timer 3:4 (PRD34).
- 4. Select the desired prescaler value for timer 3:4 (PSC34 bit in TGCR).
- 5. Enable timer 3:4 (ENAMODE34 bit in TCR).

2.3.3 Counter and Period Registers Used in GP Timer Modes

Table 8 summarizes how the counter registers (TIM*n*) and period registers (PRD*n*) are used in each GP timer mode.

Table 8. Counter and Period Registers Used in GP Timer Modes

Timer Mode	Counter Registers	Period Registers
64-bit general-purpose	TIM34:TIM12	PRD34:PRD12
Dual 32-bit chained		
Prescaler (Timer 3:4)	TIM34	PRD34
Timer (Timer 1:2)	TIM12	PRD12
Dual 32-bit unchained		
Timer (Timer 1:2)	TIM12	PRD12
Timer with prescaler (Timer 3:4)	PSC34 bits and TIM34	TDDR34 bits and PRD34

16 64-Bit Timer/Watchdog Timer



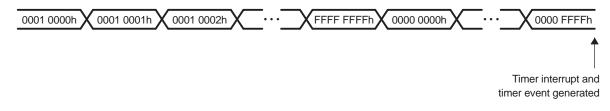
2.3.4 General-Purpose Timer Operation Boundary Conditions

The following boundary conditions affect the timer operation.

2.3.4.1 Timer Counter Overflow

Timer counter overflow can happen when the timer counter register is set to a value greater than the value in the timer period register. The counter reaches its maximum value (FFFF FFFFh or FFFF FFFF FFFFh), rolls over to 0, and continues counting until it reaches the timer period. An example is in Figure 7.

Figure 7. 32-Bit Timer Counter Overflow Example



2.3.4.2 Writing to Registers of an Active Timer

Writes to the timer registers are not allowed when the timer is active, except for stopping or resetting the timers. In the 64-bit and dual 32-bit timer modes, registers that are protected by hardware are:

- TIM12
- TIM34
- PRD12
- PRD34
- TCR (except the ENAMODE bit)
- TGCR (except the TIM12RS and TIM34RS bits)

2.3.5 General-Purpose Timer Power Management

The timer can be placed in an idle mode to conserve power when it is not being used. The timer can be placed in reduced power modes to conserve power during periods of low activity. The power management of the peripheral is controlled by the processor Power and Sleep Controller (PSC). The PSC acts as a master controller for power management for all of the peripherals on the device. For detailed information on power management procedures using the PSC, see the *TMS320DM646x DMSoC ARM Subsystem Reference Guide* (SPRUEP9).

2.4 Watchdog Timer Mode

This section describes the use of Timer2 as a watchdog timer.

2.4.1 Watchdog Timer

Timer2 can be configured only as a 64-bit watchdog timer. As a watchdog timer, it can be used to prevent system lockup when the software becomes trapped in loops with no controlled exit.

After a hardware reset, the watchdog timer is disabled. The timer then can be configured as a watchdog timer using the timer mode (TIMMODE) bit in the timer global control register (TGCR) and the watchdog timer enable (WDEN) bit in the watchdog timer control register (WDTCR). In the watchdog timer mode, the timer requires a special service sequence to be executed periodically. Without this periodic servicing, the timer counter increments until it matches the timer period and causes a watchdog timeout event.

When the timeout event occurs, the watchdog timer resets the entire processor.



Architecture

2.4.2 Watchdog Timer Mode Restrictions

The watchdog timer mode has the following restrictions:

- No external clock source
- No one-time enabling

2.4.3 Watchdog Timer Mode Operation

The watchdog timer mode is selected and enabled when:

- TIMMODE = 2h in TGCR
- WDEN = 1 in WDTCR

Figure 8 shows the timer when it is used in the watchdog timer mode. The counter registers (TIM12 and TIM34) form a 64-bit timer counter register and the period registers (PRD12 and PRD34) form a 64-bit period register. When the timer counter matches the timer period, the timer generates a watchdog timeout event which resets the entire processor.

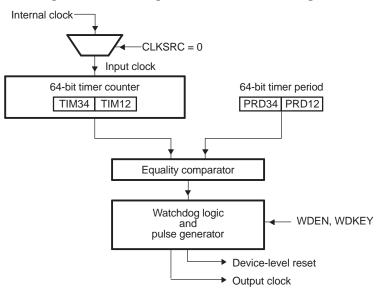


Figure 8. Watchdog Timer Mode Block Diagram

To activate the watchdog timer, a certain sequence of events must be followed, as shown in the state diagram of Figure 9.

Once the watchdog timer is activated, it can be disabled only by a watchdog timeout event or by a hardware reset. A special key sequence is required to prevent the watchdog timer from being accidentally serviced while the software is trapped in a loop or by some other software failure.

To prevent a watchdog timeout event, the timer has to be serviced periodically by writing A5C6h followed by DA7Eh to the watchdog timer service key (WDKEY) bits in WDTCR before the timer finishes counting up. Both A5C6h and DA7Eh are allowed to be written to the WDKEY bits, but only the correct sequence of A5C6h followed by DA7Eh to the WDKEY bits services the watchdog timer. Any other writes to the WDKEY bits triggers the watchdog timeout event immediately.

When the watchdog timer is in the Timeout state, the watchdog timer is disabled, the WDEN bit is cleared to 0, and the timer is reset. After entering the Timeout state, the watchdog timer cannot be enabled again until a hardware reset occurs.



Architecture

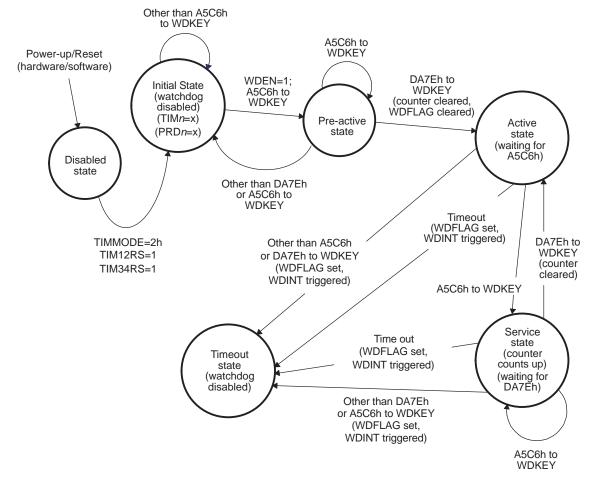


Figure 9. Watchdog Timer Operation State Diagram

After a hardware reset, the watchdog timer is disabled; however, reads or writes to the watchdog timer registers are allowed. Once the WDEN bit is set (enabling the watchdog timer) and A5C6h is written to the WDKEY bits, the watchdog timer enters the Pre-active state. In the Pre-active state:

- A write to WDTCR is allowed only when the write comes with the correct key (A5C6h or DA7Eh) to the WDKEY bits.
- A write of DA7Eh to the WDKEY bits when the WDEN bit is set to 1 resets the counters and activates the watchdog timer.

The watchdog timer must be configured before the watchdog timer enters the Active state. The WDEN bit must be set to 1 before writing DA7Eh to the WDKEY bits in the Pre-active state. Every time the watchdog timer is serviced by the correct WDKEY sequence, the watchdog timer counter is automatically reset.

2.4.4 Watchdog Timer Register Write Protection

Once the watchdog timer enters the Pre-active state (see Figure 9), writes to TIM12, TIM34, PRD12, PRD34, and WDTCR are write protected (except for the WDKEY field). While the watchdog timer is in the Timeout state, writing to the WDEN bit has no effect.

Once the watchdog timer enters its Initial state (see Figure 9), do not write to TGCR.

2.4.5 Watchdog Timer Power Management

The watchdog timer cannot be placed in power-down mode.



2.5 Timer Pulse Generation

Driven by the timer interrupt TINT*n*, the two basic timer output modes are the pulse mode and the clock mode. These modes are selected by the C/Pn bit in the timer control register (TCR). In the pulse mode, the PWID*n* bit in TCR sets the pulse width to 1, 2, 3, or 4 timer clocks, and this pulse is inverted by setting the INVOUTP*n* bit in TCR to 1. In the clock mode, the PWID*n* and INVOUTP*n* bits in TCR are ignored, and the timer output is a 50% duty-cycle signal that toggles high-to-low or low-to-high each time a timer interrupt is generated.

In the 64-bit timer mode and the 32-bit unchained timer mode, the PWID34, INVOUTP34, and C/P34 bits in TCR are ignored.

In the Timer2 watchdog timer mode, the PWID34 bit in TCR must be set to 3h for the watchdog timer to function properly.

2.6 Reset Considerations

The timer has two reset sources: hardware reset and the timer reset (TIM12RS and TIM34RS) bits in the timer global control register (TGCR).

2.6.1 Software Reset Considerations

When the TIM12RS bit in the timer global control register (TGCR) is cleared to 0, the TIM12 register is held with the current value.

When the TIM34RS bit in the timer global control register (TGCR) is cleared to 0, the TIM34 register is held with the current value.

The entire Timer module may also be reset through the Power and Sleep Controller (PSC). Note that from the Timer perspective, this reset appears as a hardware reset to the entire module.

2.6.2 Hardware Reset Considerations

When a device reset is asserted, all Timer registers are set to their default values.

2.7 Interrupt Support

Each of the timers can send either one of two separate interrupt events (TINT*n*) to the ARM and/or the DSP, depending on the operating mode of the timer. The timer interrupts are generated when the count value in the counters register reaches the value specified in the period register.

Table 9 shows the interrupts generated in each mode on each instance of the timer. Table 10 shows the interrupt number for each interrupt event.

For more information on the DSP interrupt controller (INTC) and the ARM interrupt controller (AINTC), see the *TMS320DM646x DMSoC DSP Subsystem Reference Guide* (SPRUEP8) and the *TMS320DM646x DMSoC ARM Subsystem Reference Guide* (SPRUEP9).

	Timer0		Timer1		Timer2	
Timer Mode	ARM	DSP	ARM	DSP	ARM	DSP
64-bit mode	TINTL0	TINTL0	TINTL1	TINTL1	-	-
32-bit chained mode	TINTL0	TINTL0	TINTL1	TINTL1	-	-
32-bit unchained mode without prescaler (timer 1:2)	TINTL0	TINTL0	TINTL1	TINTL1	-	-
32-bit unchained mode with prescaler (timer 3:4)	TINTH0	TINTH0	TINTH1	TINTH1	-	-
Watchdog mode	-	-	-	-	WDINT	-

Table 9. Timer Interrupts Generated

		Interrupt Number		
Acronym	Source	AINTC	INTC	
TINTL0	Timer0 lower (TINT12)	32	4	
TINTH0	Timer0 upper (TINT34)	33	5	
TINTL1	Timer1 lower (TINT12)	34	6	
TINTH1	Timer1 upper (TINT34)	35	7	
WDINT	Watchdog timer (Timer2)	7	-	

Table 10. Timer Interrupts

2.8 EDMA Event Support

Each of the timers can send either one of two separate timer events (TEVT*n*) to the EDMA, depending on the operating mode the timer. The timer events are generated when the count value in the counters register reaches the value specified in the period register.

Table 11 shows the EDMA events generated in each mode on each instance of the timer.

	Time	er0	Timer1		
Timer Mode	Acronym	Event	Acronym	Event	Timer2
64-bit mode	TEVTL0	48	TEVTL1	50	-
32-bit chained mode	TEVTL0	48	TEVTL1	50	-
32-bit unchained mode without prescaler (timer 1:2)	TEVTL0	48	TEVTL1	50	-
32-bit unchained mode with prescaler (timer 3:4)	TEVTH0	49	TEVTH1	51	-
Watchdog mode	-	-	-	-	-

Table 11. Timer EDMA Events Generated

2.9 Emulation Considerations

Each timer has an emulation management register (EMUMGT). As shown in Table 12, the FREE and SOFT bits of EMUMGT determine how the timer responds to an emulation suspend event. An emulation suspend event corresponds to any type of emulator access to either the ARM or the DSP, such as a hardware or software breakpoint or a probe point.

Note that during emulation, the timer count values will increment once every timer peripheral clock (not CPU clock). So when single-steeping though code, the timer values will not update on every CPU clock cycle.

The timer can respond to emulation events from the ARM or the DSP CPU based on the configuration of the emulation suspend source register (SUSPSRC). See the data manual for detailed information on SUSPSRC and how it is configured.

FREE	SOFT	Emulation Mode
0	0	The timer stops immediately.
0	1	The timer stops when the timer counter value increments and reaches the value in the timer period register.
1	x	The timer runs free regardless of SOFT bit status.

Table 12. Timer Emulation Modes Selection

3 Registers

Table 13 lists the memory-mapped registers for the 64-bit timer. See the device-specific data manual for the memory address of these registers. All other register offset addresses not listed in Table 13 should be considered as reserved locations and the register contents should not be modified. The module base address is 01C2 1400h for Timer0, 01C2 1800h for Timer1, and 01C2 1C00h for Timer2.

Offset	Acronym	Register Description	Section
0h	PID12	Peripheral Identification Register 12	Section 3.1
4h	EMUMGT	Emulation Management Register	Section 3.2
10h	TIM12	Timer Counter Register 12	Section 3.3
14h	TIM34	Timer Counter Register 34	Section 3.3
18h	PRD12	Timer Period Register 12	Section 3.4
1Ch	PRD34	Timer Period Register 34	Section 3.4
20h	TCR	Timer Control Register	Section 3.5
24h	TGCR	Timer Global Control Register	Section 3.6
28h	WDTCR	Watchdog Timer Control Register (Timer2 only)	Section 3.7

Table 13. 64-Bit Timer Registers

3.1 Peripheral Identification Register 12 (PID12)

The peripheral ID register 12 (PID12) contains identification data (type, class, and revision) for the peripheral. The PID12 is shown in Figure 10 and described in Table 14.

31	-	•	23	22	· · ·	16
01	Reserved		20		TYPE	10
	R-0				R-1h	
15		8	7			0
CLASS					REVISION	
	R-7h				R-1h	

LEGEND: R = Read only; -n = value after reset

Table 14. Peripheral Identification Register 12 (PID12) Field Descriptions

Bit	Field	Value	Description
31-23	Reserved	0	Reserved
22-16	TYPE		Identifies type of peripheral
		1h	Timer
15-8	CLASS		Identifies class of peripheral
		7h	Timer
7-0	REVISION		Identifies revision of peripheral.
		1h	Current revision of peripheral.

3.2 Emulation Management Register (EMUMGT)

The emulation management register (EMUMGT) is shown in Figure 11 and described in Table 15.

Figure 11. Emulation Management Register (EMUMGT)

31				16
	Reserved			
	R-0			
15		2	1	0
	Reserved		SOFT	FREE
	R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 15. Emulation Management Register (EMUMGT) Field Descriptions

Bit	Field	Value	Description	
31-2	Reserved	0	Reserved	
1	SOFT		etermines emulation mode functionality of the timer. When the FREE bit is cleared to 0, the SOFT bit elects the timer mode.	
		0	The timer stops immediately.	
		1	The timer stops when the counter increments and reaches the value in the timer period register (PRDn).	
0	FREE		Determines emulation mode functionality of the timer. When the FREE bit is cleared to 0, the SOFT bit elects the timer mode.	
		0	The SOFT bit selects the timer mode.	
		1	The timer runs free regardless of the SOFT bit.	



3.3 Timer Counter Registers (TIM12 and TIM34)

The timer counter register is a 64-bit wide register. This 64-bit register is divided into two 32-bit registers, TIM12 and TIM34.

In the dual 32-bit timer mode, the 64-bit register is divided with TIM12 acting as one 32-bit counter and TIM34 acting as another. These two registers can be configured as chained or unchained.

3.3.1 Timer Counter Register 12 (TIM12)

The timer counter register 12 (TIM12) is shown in Figure 12 and described in Table 16

Figure 12. Timer Counter Register 12 (TIM12)

31		16
	TIM12	
	R/W-0	
15		0
	TIM12	
	R/W-0	

LEGEND: R/W = Read/Write; -n = value after reset

Table 16. Timer Counter Register 12 (TIM12) Field Descriptions

Bit Field	Value	Description
31-0 TIM12	0-FFFF FFFFh	TIM12 count bits. This 32-bit value is the current count of the main counter.

3.3.2 Timer Counter Register 34 (TIM34)

The timer counter register 34 (TIM34) is shown in Figure 13 and described in Table 17.

Figure 13. Timer Counter Register 34 (TIM34)

31		16
	TIM34	
	R/W-0	
15		0
	TIM34	

LEGEND: R/W = Read/Write: -n = value after reset

Table 17. Timer Counter Register 34 (TIM34) Field Descriptions

Bit	Field	Value	Description
31-0	TIM34	0-FFFF FFFFh	TIM34 count bits. This 32-bit value is the current count of the main counter.



3.4 Timer Period Registers (PRD12 and PRD34)

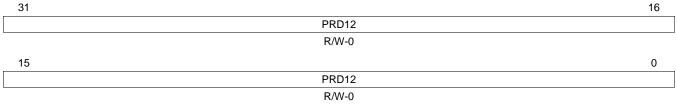
The timer period register is a 64-bit wide register. This 64-bit register is divided into two 32-bit registers, PRD12 and PRD34.

Similar to TIM*n* in the dual 32-bit timer mode, PRD*n* can be divided into 2 registers: for timer 1:2, PRD12 and for timer 3:4, PRD34. These two registers can be used in conjunction with the two timer counter registers TIM12 and TIM34.

3.4.1 Timer Period Register (PRD12)

The timer period register 12 (PRD12) is shown in Figure 14 and described in Table 18.

Figure 14. Timer Period Register 12 (PRD12)



LEGEND: R/W = Read/Write; -*n* = value after reset

Table 18. Timer Period Register (PRD12) Field Descriptions

Bit	Field	Value	Description
31-0	PRD12	0-FFFF FFFFh	PRD12 period bits. This 32-bit value is the number of timer input clock cycles to count.

3.4.2 Timer Period Register 34 (PRD34)

The timer period register 34 (PRD34) is shown in Figure 15 and described in Table 19.

Figure 15. Timer Period Register 34 (PRD34)

31		16
	PRD34	
	R/W-0	
15		0
	PRD34	
	R/W-0	

LEGEND: R/W = Read/Write; -*n* = value after reset

Table 19. Timer Period Register (PRD34) Field Descriptions

Bit	Field	Value	Description
31-0	PRD34	0-FFFF FFFFh	PRD34 period bits. This 32-bit value is the number of timer input clock cycles to count.

3.5 Timer Control Register (TCR)

The timer control register (TCR) is shown in Figure 16 and described in Table 20.

Figure 16. Timer Control Register (TCR)

	J	-			• • • •	- /			
25	24	23	22	21	20	19	18	17	16
d	CLKSRC34	ENAM	ODE34	PW	ID34	C/P34	Rsvd	INVOUTP34	Rsvd
	R/W-0	R/\	N-0	R/\	N-0	R/W-0	R-0	R/W-0	R-0
9	8	7	6	5	4	3	2	1	0
d	CLKSRC12	ENAM	ODE12	PW	ID12	C/P12	Rsvd	INVOUTP12	Rsvd
	R/W-0	R/\	N-0	R/\	N-0	R/W-0	R-0	R/W-0	R-0
	d	25 24 25 24 CLKSRC34 R/W-0 9 8 25 24 R/W-0 9 8 25 24 R/W-0 9 8	25 24 23 26 CLKSRC34 ENAM R/W-0 R/M 9 8 7 26 CLKSRC12 ENAM	25 24 23 22 dd CLKSRC34 ENAMODE34 R/W-0 R/W-0 9 8 7 6 dd CLKSRC12 ENAMODE12	25 24 23 22 21 dd CLKSRC34 ENAMODE34 PW R/W-0 R/W-0 R/A 9 8 7 6 5 dd CLKSRC12 ENAMODE12 PW	25 24 23 22 21 20 dd CLKSRC34 ENAMODE34 PWID34 R/W-0 R/W-0 R/W-0 9 8 7 6 5 4 ed CLKSRC12 ENAMODE12 PWID12	25 24 23 22 21 20 19 dd CLKSRC34 ENAMODE34 PWID34 C/P34 R/W-0 R/W-0 R/W-0 R/W-0 9 8 7 6 5 4 3 dd CLKSRC12 ENAMODE12 PWID12 C/P12	25 24 23 22 21 20 19 18 dd CLKSRC34 ENAMODE34 PWID34 C/P34 Rsvd R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R-0 9 8 7 6 5 4 3 2 dd CLKSRC12 ENAMODE12 PWID12 C/P12 Rsvd	25 24 23 22 21 20 19 18 17 id CLKSRC34 ENAMODE34 PWID34 C/P34 Rsvd INVOUTP34 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 9 8 7 6 5 4 3 2 1 id CLKSRC12 ENAMODE12 PWID12 C/P12 Rsvd INVOUTP12

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. Timer Control Register (TCR) Field Descriptions

Bit	Field	Value	Description
31-25	Reserved	0	Reserved
24	CLKSRC34		CLKSRC34 determines the selected clock source for the timer (Reserved except for Timer0).
		0	Internal clock.
		1	Timer input pin.
23-22	ENAMODE34	0-3h	ENAMODE34 determines the enabling modes of the timer. Note that ENAMODE34 is applicable only when the timer is configured in dual 32-bit unchained timer mode (TIMMODE = 01 in TGCR).
		0	The timer is disabled (not counting) and maintains current value.
		1h	The timer is enabled one time. The timer stops after the counter reaches the period.
		2h	The timer is enabled continuously, TIM <i>n</i> increments until the timer counter matches the period, resets the timer counter to 0 on the cycle after matching and continues.
		3h	Reserved.
21-20	PWID34	0-3h	PWID34 determines the timer output pulse width. Only applicable in pulse mode (C/P34 = 0).
		0	Timer output pulse duration is 1 timer cycle long.
		1h	Timer output pulse duration is 2 timer cycles long.
		2h	Timer output pulse duration is 3 timer cycles long.
		3h	Timer output pulse duration is 4 timer cycles long.
19	C/P34		C/P34 determines the timer output mode.
		0	Timer output in pulse mode.
		1	Timer output in clock mode.
18	Reserved	0	Reserved.
17	INVOUTP34		INVOUTP34 determines the timer output pulse polarity. Only applicable in pulse mode (C/P34 = 0).
		0	Non-inverted timer output.
		1	Inverted timer output.
16-9	Reserved	0	Reserved.
8	CLKSRC12		CLKSRC12 determines the selected clock source for the timer (Reserved except for Timer0 and Timer1).
		0	Internal clock.
		1	Timer input pin.
7-6	ENAMODE12	0-3h	ENAMODE12 determines the enabling modes of the timer.
		0	The timer is disabled (not counting) and maintains current value.
		1h	The timer is enabled one time. The timer stops after the counter reaches the period.
		2h	The timer is enabled continuously, TIM <i>n</i> increments until the timer counter matches the period, resets the timer counter to 0 on the cycle after matching and continues.
		3h	Reserved.



Bit	Field	Value	Description
5-4	PWID12	0-3h	PWID12 determines the timer output pulse width. Only applicable in pulse mode (C/P12 = 0).
		0	Timer output pulse duration is 1 timer cycle long.
		1h	Timer output pulse duration is 2 timer cycles long.
		2h	Timer output pulse duration is 3 timer cycles long.
		3h	Timer output pulse duration is 4 timer cycles long.
3	C/P12		C/P12 determines the timer output mode.
		0	Timer output in pulse mode.
		1	Timer output in clock mode.
2	Reserved	0	Reserved.
1	INVOUTP12		INVOUTP12 determines the timer output pulse polarity. Only applicable in pulse mode (C/P12 = 0).
		0	Non-inverted timer output.
		1	Inverted timer output.
0	Reserved	0	Reserved.

Table 20. Timer Control Register (TCR) Field Descriptions (continued)

3.6 Timer Global Control Register (TGCR)

The timer global control register (TGCR) is shown in Figure 17 and described in Table 21.

						16
		Rese	erved			
		R	-0			
15		12	11			8
	TDDR34			PS	C34	
	R/W-0			R/	W-0	
7		4	3	2	1	0
	Reserved		TIMN	10DE	TIM34RS	TIM12RS
	R-0		RΛ	V-0	R/W-0	R/W-0

Figure 17. Timer Global Control Register (TGCR)

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 21. Timer Global Control Register (TGCR) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Reserved
15-12	TDDR34	0-Fh	Timer linear divide-down ratio specifies the timer divide-down ratio for timer 3:4. When the timer is enabled, TDDR34 increments every timer clock. The TIM34 counter increments on the cycle after TDDR34 matches PSC34. TDDR34 resets to 0 and continues. When TIM34 matches PRD34, timer 3:4 stops, if timer 3:4 is enabled one time; TIM34 resets to 0 on the cycle after matching PRD34 and timer 3:4 continues, if timer 3:4 is enabled continuously.
11-8	PSC34	0-Fh	TIM34 pre-scalar counter specifies the count for timer 3:4.
7-4	Reserved	0	Reserved
3-2	TIMMODE	0-3h	TIMMODE determines the timer mode.
		0	The timer is in 64-bit GP timer mode.
		1h	The timer is in dual 32-bit timer unchained mode.
		2h	The timer is in 64-bit watchdog timer mode.
		3h	The timer is in dual 32-bit timer, chained mode.
1	TIM34RS		Timer 3:4 reset.
		0	Timer 3:4 is in reset.
		1	Timer 3:4 is not in reset. Timer 3:4 can be used as a 32-bit timer. Note that for the timer to function properly in 64-bit timer mode, both TIM34RS and TIM12RS must be set to 1. Changing this bit does not affect the timer, if the timer is in the watchdog active state.
0	TIM12RS		Timer 1:2 reset.
		0	Timer 1:2 is in reset.
		1	Timer 1:2 is not in reset. Timer 1:2 can be used as a 32-bit timer. Note that for the timer to function properly in 64-bit timer mode, both TIM34RS and TIM12RS must be set to 1. Changing this bit does not affect the timer, if the timer is in the watchdog active state.



3.7 Watchdog Timer Control Register (WDTCR)

The watchdog timer control register (WDTCR) is shown in Figure 18 and described in Table 22.

Figure 18. Watchdog Timer Control Register (WDTCR)

31						16
					WDKEY	
					R/W-0	
15	14	13	12	11		0
WDFLAG	WDEN	Rese	erved		Reserved	
R/W-0	R/W-0	R/\	N-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 22. Watchdog Timer Control Register (WDTCR) Field Descriptions

Bit	Field	Value	Description
31-16	WDKEY	0-FFFFh	16-bit watchdog timer service key. Only the sequence of an A5C6h followed by a DA7Eh services the watchdog. Not applicable in regular timer mode.
15	WDFLAG		Watchdog flag bit. WDFLAG can be cleared by enabling the watchdog timer, by device reset, or being written with 1. It is set by a watchdog time-out.
		0	No watchdog time-out occurred.
		1	Watchdog time-out occurred.
14	WDEN		Watchdog timer enable bit.
		0	Watchdog disabled.
		1	Watchdog enabled.
13-12	Reserved	0	Reserved. This bit field must be written as 00b.
11-0	Reserved	0	Reserved

Registers

Appendix A Revision History

Table 23 lists the changes made since the previous version of this document.

Reference	Additions/Modifications/Deletions
Section 1.2	Added last feature.
Figure 1	Added NOTE.
Section 2.5	Added subsection. Subsequent subsections renumbered.
Figure 16	Changed figure.
Table 20	Changed table.

Table 23. Document Revision History

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