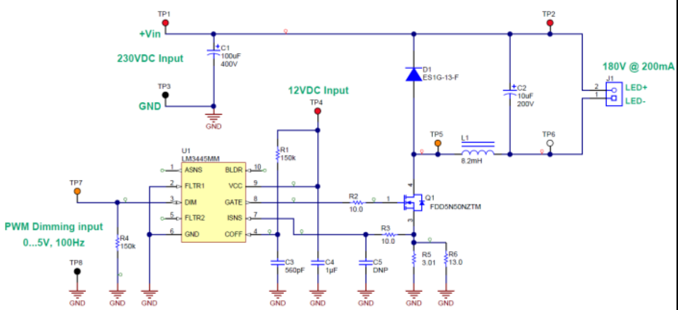
Test Report: PMP30439

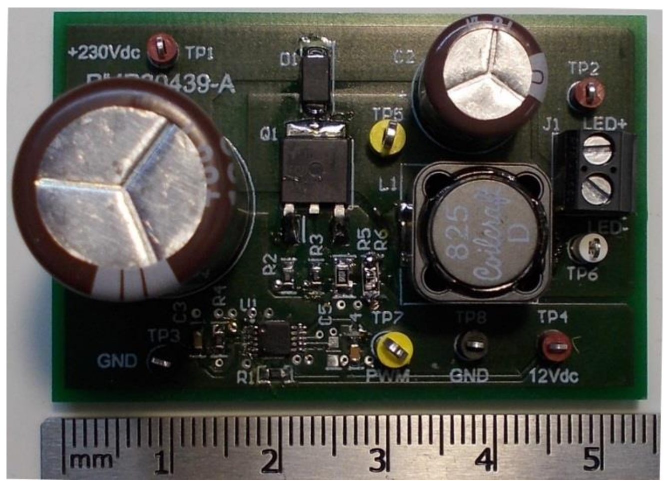
230 V in to 180 V out at 200 mA Constant-Current LED Driver Reference Design

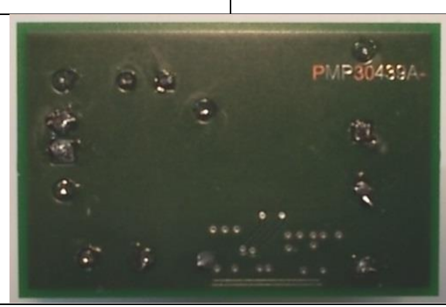
TEXAS INSTRUMENTS

Description

This reference design is a low-side Buck (the output voltage is referenced to the positive DC input (+Vin node), not to the GND node). The controller drives a LED string up to 180V with 200mA constant current. The low-side Buck topology simplifies the schematic thanks to direct-driving of the FET, without the need of high-side driver.
The reference design PMP30439 Rev_B has been built on PMP30439 Rev_A PCB.







1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	SPECIFICATIONS
Input Voltage	230VDC
Output Voltage	180VDC
Output Current	200mA

1.2 Required Equipment

- 0…300VDC, (min. 300mA), constant voltage source (VS1)
- 0…15VDC, (min. 50mA), constant voltage source (VS2)
- LED string, 180V (nominal), 200mA
- Oscilloscope (min. 100 MHz bandwidth)
- Current probe (min. 100 KHz bandwidth)
- Function generator (FG): providing 0.1%...99.9% duty cycle, 0..5Vpk, 100Hz, PWM signal for dimming
- Optional: infrared camera

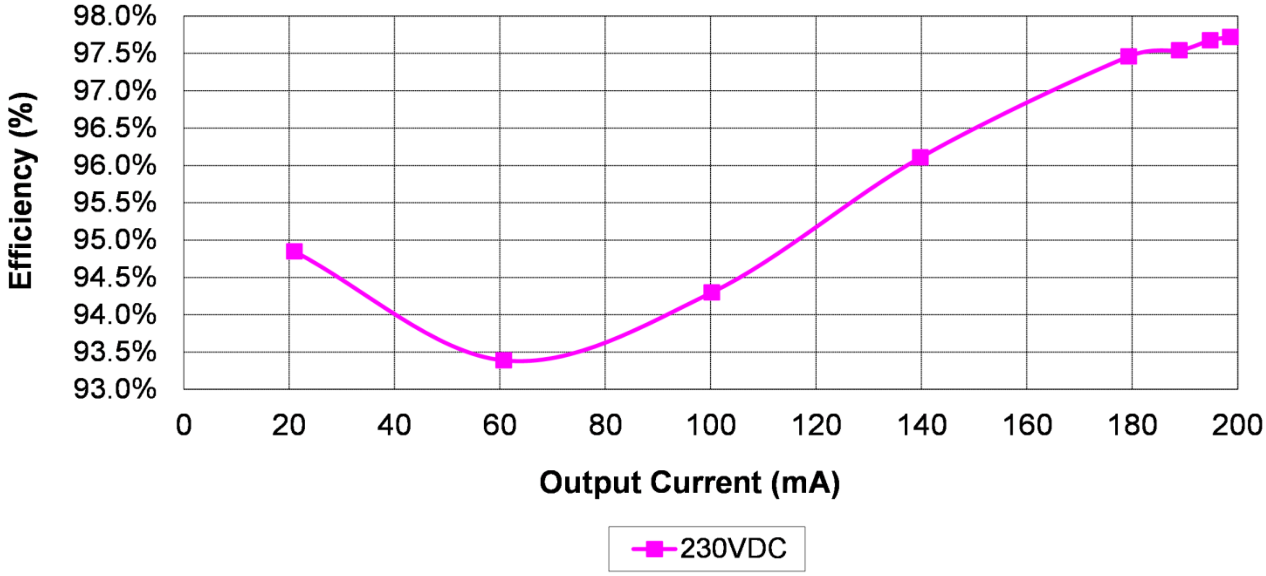
1.3 Considerations

a) Connect the source VS1 to TP1 and TP3.
b) Connect the source VS2 to TP4 and TP3.
c) Connect the function generator FG to TP7 and TP8.
d) Connect the LED string to TP2 and TP6, with the positive to TP2
e) Set the function generator to supply a PWM signal, with low level = 0V and high level = 5V, frequency = 100 Hz, and duty cycle = 0.1%.
f) Turn VS2 on.
g) Enable the FG output.
h) Turn VS1 on.
i) Adjust the duty cycle of FG from 0.1% to 99.9% to vary LED current
j) Turn off the board by reverse sequencing (h-g-f)
k) Wait until both output and input capacitors are completely discharged (warning: HIGH VOLTAGE)

2 Testing and Results

2.1 Efficiency Graphs:

The efficiency graph, versus output LED current, is shown below. The output current has been varied by adjusting the PWM dimming duty cycle, from 99.9% to 0.1%.
The input voltage has been set to 230 VDC, and the bias voltage to 12VDC.



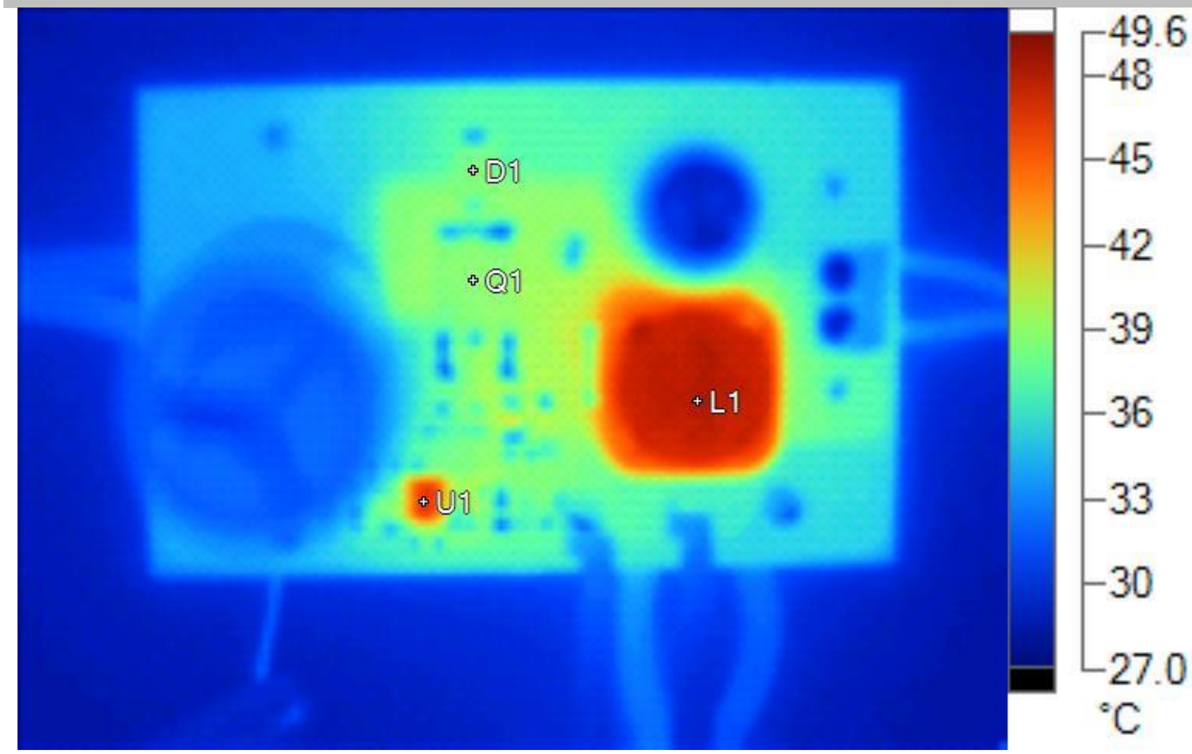
2.2 Efficiency Data:

The efficiency graph reports the data from the table shown below:

Vin(V)	Vbias(V)	Iin(mA)	Ibias(mA)	Pin (W)	Vout (V)	Iout(mA)	Pout (W)	Efficiency (%)	PWM(%)
230	12	0	3.65	0.044	0	0	0	0.0%	99.9
230	12	15.3	4.19	3.569	161.2	21.0	3.39	94.84%	90.0
230	12	46.5	6.83	10.777	165.8	60.7	10.06	93.38%	70.0
230	12	77.9	8.75	18.022	169.6	100.2	16.99	94.30%	50.0
230	12	109.0	9.20	25.180	173.1	139.8	24.20	96.10%	30.0
230	12	140.2	11.21	32.381	176.0	179.3	31.56	97.46%	10.0
230	12	148.0	11.93	34.183	176.5	188.9	33.34	97.54%	5.0
230	12	152.6	11.96	35.242	176.7	194.8	34.42	97.67%	2.0
230	12	155.6	12.15	35.934	176.8	198.6	35.11	97.71%	0.1

2.3 Thermal Image

The graph and table below show the thermal picture of the converter supplied at 230VDC and loaded with a LED string. The output voltage was ~ 180V and the current 200mA. The image has been taken after the board was running for 20 minutes, placed horizontal on the bench, at full load, with ambient temperature of 25C and in still air condition.



Main Image Markers

Name	Temperature	Emissivity	Background
L1	48.5°C	0.95	25.0°C
U1	46.5°C	0.95	25.0°C
Q1	38.7°C	0.95	25.0°C
D1	38.4°C	0.95	25.0°C

2.4 Dimensions

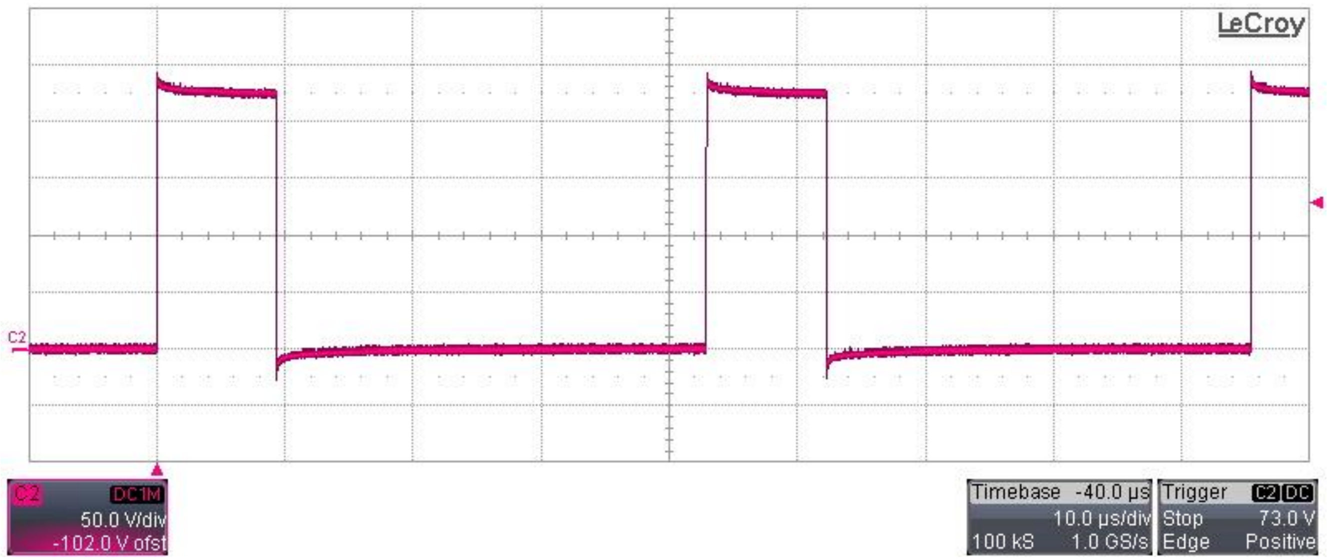
The board dimensions are 54.61 mm x 35.56 mm, height 40 mm.

3 Waveforms

3.1 Switching

The switching waveforms have been measured by supplying the converter at 230VDC in full load condition.

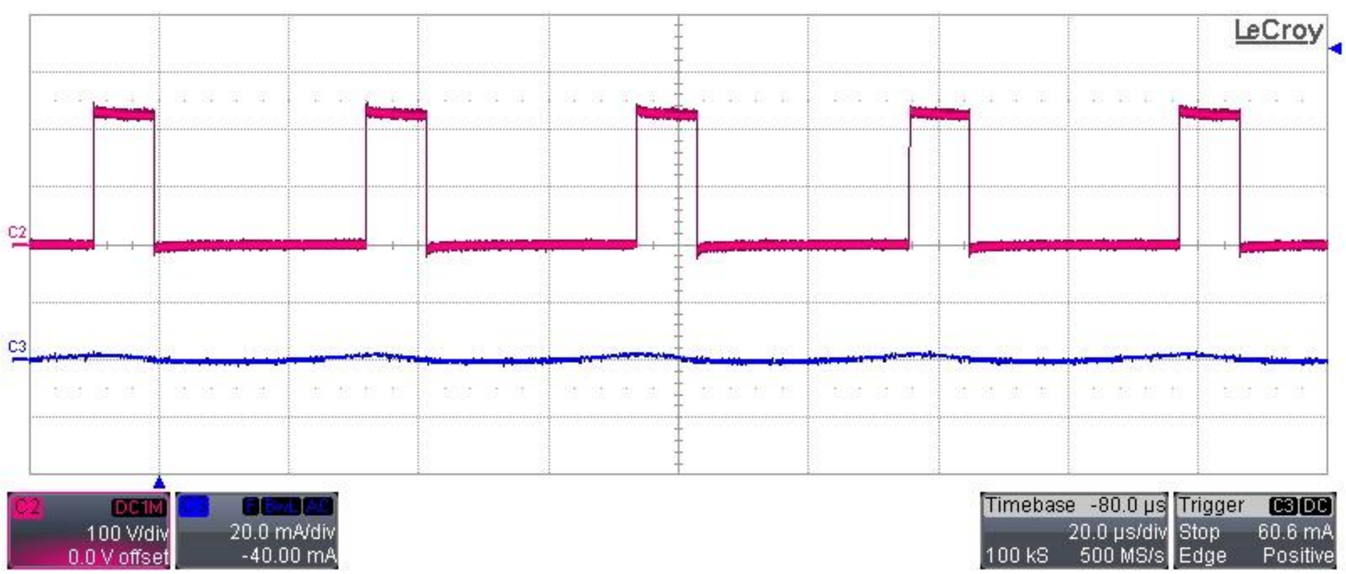
Ch.2: Switch-node (Drain of Q1) (50V/div, 10usec/div, no BWL)



3.2 Output Current Ripple

The output current ripple has been measured by supplying the converter at the same conditions of point 3.1.

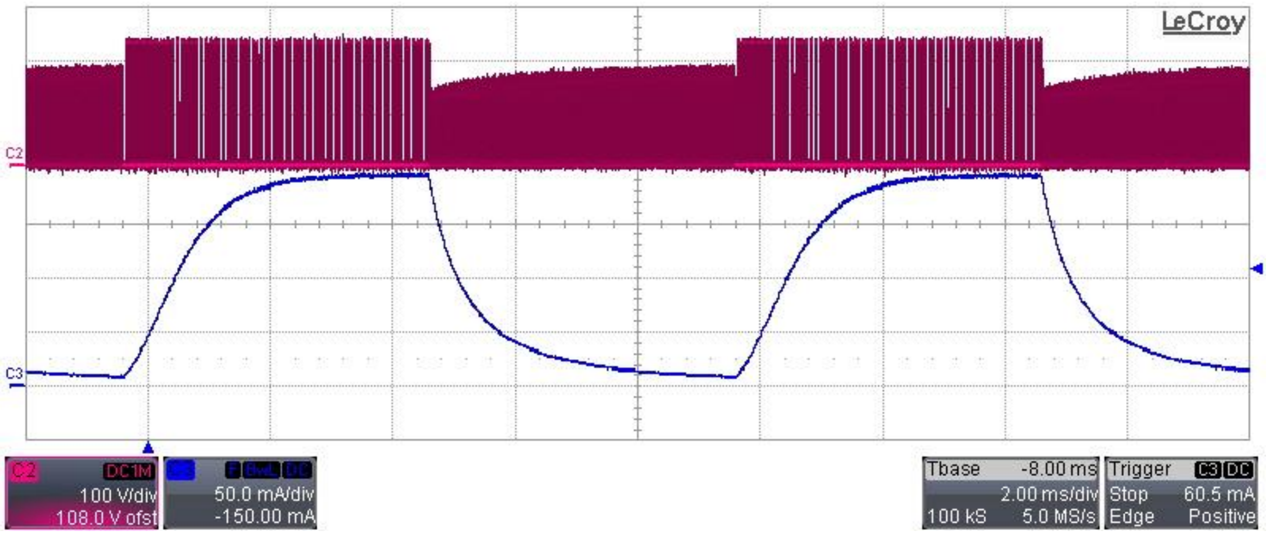
Ch.2: Switch-node (Drain of Q1) (100V/div, 20usec/div, no BWL)
Ch.3: Output current ripple (LED current) (20mA/div, AC coupling, 20 MHz BWL)



3.3 Output Current Variation during PWM Dimming

The output current variation has been measured by supplying the converter at the same conditions of point 3.1 and by applying 50% duty cycle @ 100Hz to dimming input (TP7).

Ch.2: Switch-node (Drain of Q1) (100V/div, 2msec/div, no BWL)
Ch.3: Output current ripple (LED current) (50mA/div, 20 MHz BWL)



3.4 PWM Dimming Linearity

The output current variation versus PWM duty cycle is shown in the table below. Test conditions: same as point 3.1. The PWM dimming duty cycle has been varied between 99.9% (no LED current) to 0.1% (almost full current).