TI Designs

230-V, 900-W Mains Powered BLDC Motor Drive for Vacuum Cleaner

Design Overview

The TIDA-00433 is a discrete IGBT-based three-phase inverter using trapezoidal control for driving high-speed brushless DC (BLDC) motors rated up to 900 W in mains powered vacuum cleaners. The design provides ready implementation of Hall sensor-based BLDC motor trapezoidal control and provision for sensorless trapezoidal control using back-EMF (BEMF) sensing. The inverter stage works with or without an active PFC stage and is tested up to 390-V DC from active PFC.

Design Resources

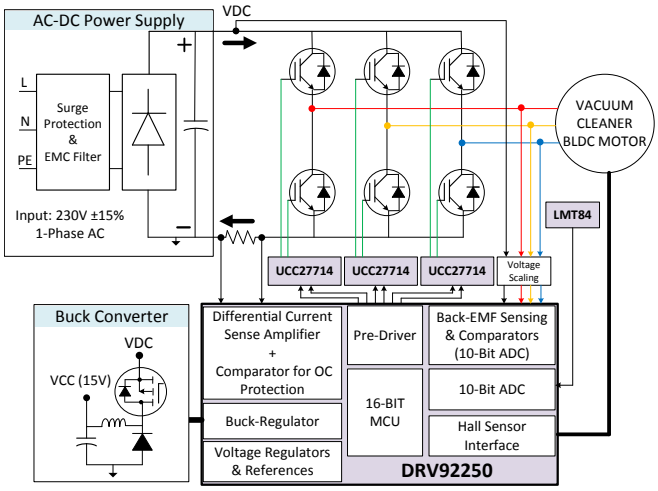
TIDA-00433	Design Folder
DRV92250	Product Folder
UCC27714	Product Folder
LMT84	Product Folder
TL431A	Product Folder

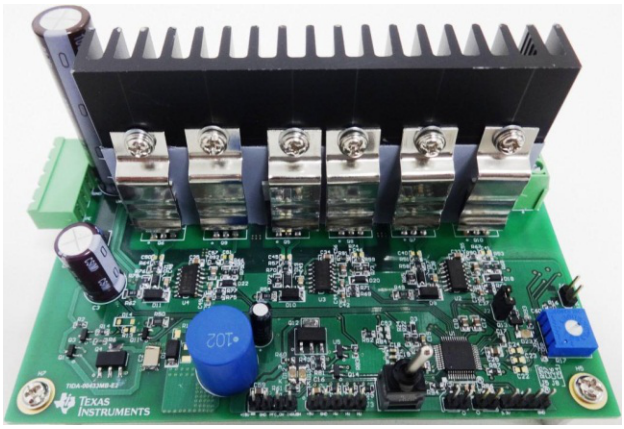
Featured Applications

- Vacuum Cleaner
- Air Conditioner
- Blowers

Design Features

- 900-W, 325-V DC Three-Phase Inverter Board With Discrete IGBT-Based Implementation Capable of Driving High-Speed BLDC Motors
- Uses DRV92250 High-Voltage BLDC Motor Controller, Which Integrates 16-Bit MCU, Low-Side Pre-Driver Circuits, One Differential Current Sense Amplifier, Comparator With a DAC for Overcurrent Protection, Buck Controller and LDOs
- Ready Implementation of Hall Sensor-Based BLDC Motor Trapezoidal Control and Provision for Sensorless Trapezoidal Control Using BEMF Sensing
- Integrated DC-DC Controller and LDOs of DRV92250 Enables Generation of Bias Power Supplies Directly From the High Voltage
- Uses 600-V High-Side Low-Side Gate Driver With 4A/4A Source/Sink Current Capability, for Driving the Three-Phase Inverter
- Cycle-by-Cycle Motor Overcurrent Protection, Over Temperature and Line Undervoltage Protections
- Thermal Design to Enable Operating Ambient up to 55°C
- AC Mains Input Designed to Pass Surge, EFT, and Conducted Emission as per EN55014





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1 Introduction

This reference design is a three-phase inverter using trapezoidal control for driving high-speed BLDC motors rated up to 900 W in mains powered vacuum cleaners. The inverter stage is preceded by an AC-DC converter that comprises of EMI filter, full-bridge rectifier, and DC bus electrolytic capacitor. This stage rectifies the input single phase AC supply of 195- to 265 V, 50 or 60 Hz to generate DC bus voltage of 275- to 375 V. The inverter stage can also optionally operate from a front end active power factor correction stage with DC bus voltage of up to 390-V DC. The design uses six discrete IGBTs and three high-voltage half-bridge gate driver ICs for the power stage, which enable flexible form-factor and cost competitive designs as compared to IPM module. The design uses DRV92250 a high-voltage BLDC motor controller that integrates a 16-bit RISC microcontroller (MCU), a low-side pre-driver circuit, one differential current sense amplifier, comparator with programmable DAC for overcurrent protection, DC-DC buck controller, LDOs of 5.35 V, 5.0 V, 3.3 V, and 1.9 V, and BEMF detection comparators for sensorless controller. The design uses the UCC27714 gate driver, a 600-V high-side low-side gate driver with 4 A/4 A source/sink current capability.

The integrated buck controller of the DRV92250 along with an external MOSFET-based circuit generates a 15-V bias power supply directly from the high-voltage DC bus of the inverter. This DC-DC buck controller works without any intervention of the MCU except few register settings. The design provides cycle-by-cycle motor overcurrent protection, over temperature, and line undervoltage protections. The board is designed to pass conducted emission, surge, and EFT as per EN55014.

A vacuum cleaner is a common household and industrial appliance that works with a suction motor to create suction pressure and airflow for the removal of dust and dirt. Generally, vacuum cleaners come with variety of motor power levels typically ranging from 500 to 2200 W. There are small handheld vacuum cleaners that operate on a low-voltage battery and have a power rating below 100 W.

One of the main requirements of a vacuum cleaner motor is that, it should be able to spin at very high RPM. Although a universal series motor is commonly used in this application due to its simplicity of control, it poses challenges for high speed operation due to the commutator and brushes and lower efficiency. The brushless construction of BLDC enables very high speed operation, and they can be more efficient as well.

The Directive 2009/125/EC of the European Parliament and of the Council with regard to the eco-design requirements for vacuum cleaners laid out the limit on the annual energy consumptions and input power of vacuum cleaners. As per the EU regulation, the rated input power for vacuum cleaners must be less than 900 W starting September 2017. This would require the use of high efficiency brushless motors.

This reference design provides a ready platform for the 900-W inverter for BLDC motor-based vacuum cleaners. The design has a three-phase discrete IGBT-based inverter with the necessary protections implemented in hardware and software.

2 Key System Specifications

Table 1. Key System Specifications of Power Stage

PARAMETER	SPECIFICATION
AC input voltage	230 V ±15%
Rated output power	900 W
Inverter switching frequency	10 kHz
Operating ambient temperature	–20°C to 55°C
Inverter efficiency	≥ 97% at rated load
Power supply specification for gate driver	15 V ±5%
Feedbacks	Three motor winding voltages, input DC voltage, Low side DC bus current
Protections	Overcurrent (cycle-by-cycle/latch), over temperature, input under voltage
Conducted emission	EN55014

3 System Description

Permanent magnet BLDC motors are gaining importance because of their high efficiency, low maintenance, high reliability, low rotor inertia and low noise compared to their brushed motor counterpart. A permanent magnet BLDC motor has a wound stator and a permanent magnet rotor assembly. These motors generally use internal or external devices to sense rotor position. The sensing devices provide logic signals for electronically switching the stator windings in the proper sequence to maintain rotation of the magnet assembly.

An electronic drive is required to control the stator currents in a brushless permanent magnet motor. The electronic drive consists of:

- Power stage with three-phase inverter with the required power capability
- MCU to implement the motor control algorithm
- Motor voltage and current sensing for sensorless control and closed loop speed or torque control
- Gate driver for driving the three-phase inverter
- Bias power supply to power up the gate driver and MCU

3.1 BLDC Motor — Trapezoidal Control

The BLDC motor or the trapezoidal BEMF motor has the ampere conductor distribution of the stator that ideally remains constant and fixed in space for a fixed interval known as the commutation interval. For a three-phase winding, the commutation interval is 60° electrical. At the end of each commutation interval, the ampere conductors are commutated to the next position. These motors use a two-phase ON control, where two phases of the motor will be energized at a time and the third winding will be open. The principle of the BLDC motor is to energize the phase pair at all times, which can produce the highest torque. The combination of a 120° electrical square wave current in synchronism with the 120° electrical flat top of the trapezoidal BEMF makes it theoretically possible to produce a constant torque. In practice, the current cannot be established instantaneously in a motor phase; as a consequence, the torque ripple is present at each 60° phase commutation. Figure 1 describes the electrical wave forms in the BLDC motor in the two phases ON operation.

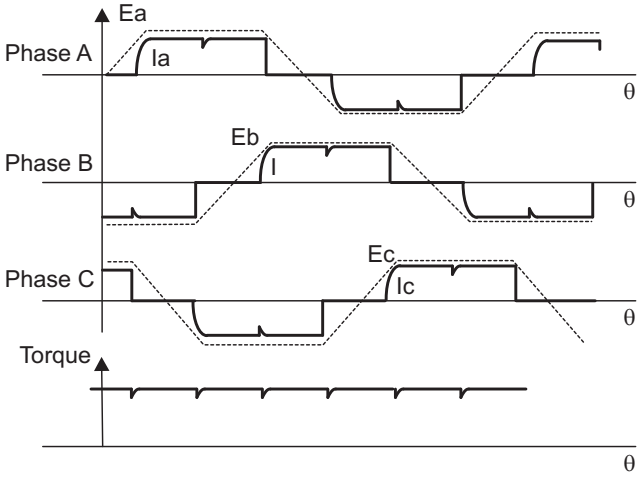

Figure 1. Electrical Waveforms in Two-Phase ON Control of BLDC Motor and Torque Ripple

Trapezoidal control has the following advantages:

- Only one current at a time needs to be controlled.
- Only one current sensor is necessary (or none in case of speed loop only).
- The positioning of the current sensor allows the use of low cost sensors as a shunt.

For more details about trapezoidal control, see the application report *Sensorless Trapezoidal Control of BLDC Motors* (SPRABQ7).

3.2 Power Stage for the BLDC Motor Drive

This reference design provides a 900-W inverter along with the AC-DC power stage working at 230 V ±15%, for brushless motor control in vacuum cleaners. The reference design uses Hall sensor-based trapezoidal control using the DRV92250 as the controller. The three-phase inverter is designed using IGBT with the UCC27714 as the gate driver. Figure 2 shows the assembled inverter board and the AC-DC power supply board.

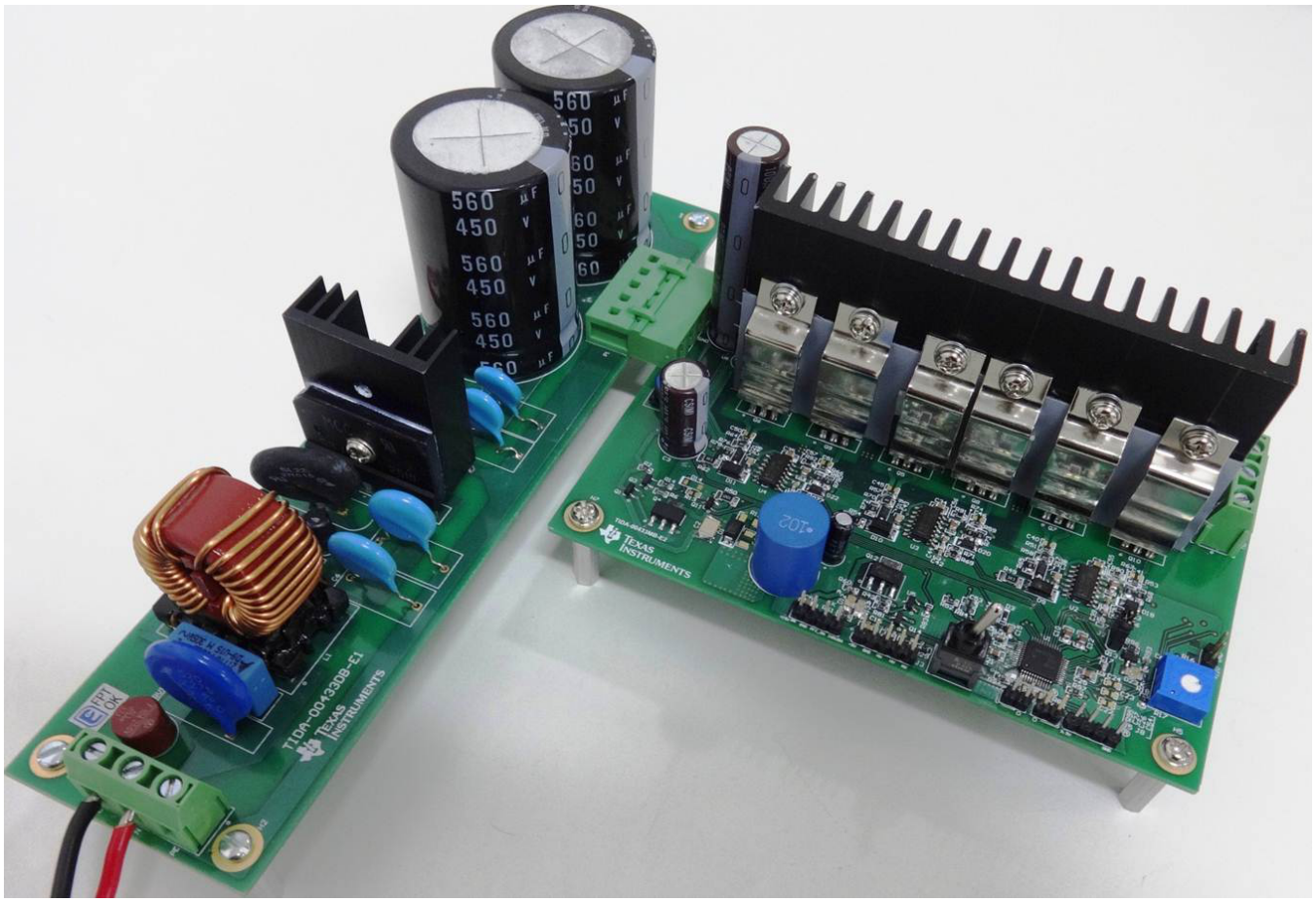

Figure 2. Assembled Inverter Board and AC-DC Converter

The inverter is designed to operate from the DC voltage obtained by rectifying the input 230-V AC ±15%. The maximum input AC voltage is 265 V and corresponding peak DC bus voltage is 375 V. However, if an active power factor correction (PFC) is required, the DC voltage will be more than the peak input voltage. With the active PFC, typically the maximum DC bus voltage is 390 V at an input AC voltage of 265 V. In the reference design, the three-phase inverter is designed for a maximum DC bus voltage of 390 V.

4 Block Diagram

Figure 3 depicts the block diagram of the inverter system with the power stage. The main parts of the system consists of the AC-DC power supply stage, three-phase IGBT Inverter bridge, the gate driver UCC27714, the controller DRV92250, the 15-V buck regulator, the temperature sensor, and the input DC voltage, motor voltage, and winding current sense feedback circuits.

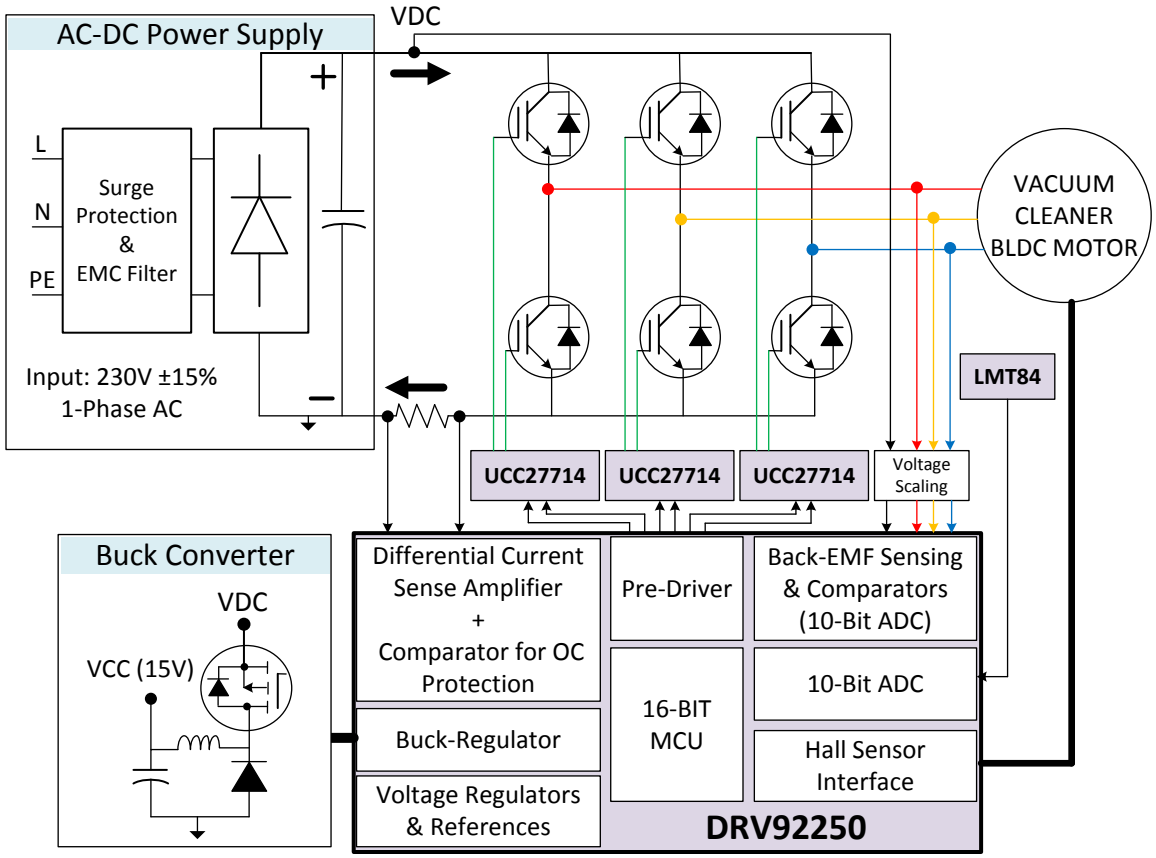

Figure 3. Block Diagram of 900-W Inverter System

This reference design shows a discrete implementation for the three-phase BLDC inverter. The inverter uses six IGBTs. The UCC27714 is used as the gate driver for the IGBTs. The UCC27714 is a 600-V high-side low-side gate driver with 4 A/4 A source/sink current capability, capable of driving power MOSFETs or IGBTs. The device comprises of one ground-referenced channel (LO) and one floating channel (HO), which is designed for operating with bootstrap supplies. It has the VDD bias supply range of 10 to 20 V, which allows designing the IGBT gate drive with the maximum allowed gate voltage.

The trapezoidal control is implemented using the controller DRV92250. It provides six PWM outputs to drive the three-phase inverter. It can support both sensored and sensorless operation with the internal comparators. The DRV92250 has an internal buck regulator, which helps in generating the 15-V bias power supply for the gate driver. The DRV92250 generates 1.9 V, 3.3 V and 5 V internally using internal LDOs for the operation of the internal MCU and the analog peripherals of the controller.

The speed of the motor can be controlled easily using the potentiometer. More features can be added or the performance can be optimized by programming the DRV92250.

5 Highlighted Products

The following are the highlighted products used in the reference design.

5.1 DRV92250

DRV92250 is a high-voltage BLDC motor controller which integrates a 16-bit RISC MCU and pre-driver circuits in a 48-pin LQFP with PowerPAD heat sink. 32KB of single-cycle (40 ns) Flash memory is embedded with the digital MCU sub-system. The 16-bit MCU is instruction set compatible with TI's MSP430F5438 family. The DRV92250 has low-side pre-driver circuits, one differential current sense amplifier, a comparator with programmable DAC for overcurrent protection, a DC-DC buck controller, LDOs of 5.35 V, 5.0 V, 3.3 V, and 1.9 V, and BEMF detection comparators for sensorless controller.

5.2 UCC27714

The UCC27714 is a 600-V high-side low-side gate driver with 4 A/4 A source/sink current capability, targeted to drive power MOSFETs or IGBTs. The device comprises of one ground-referenced channel (LO) and one floating channel (HO), which is designed for operating with bootstrap supplies. The device features an excellent robustness and noise immunity with the capability to maintain operational logic at negative voltages of up to –8-V DC on the HS pin (at VDD = 12 V).The device features the industry best-in-class input propagation delays and delay matching between both channels aimed at minimizing pulse distortion in high-frequency switching applications. Each channel is controlled by its respective input pins (HI and LI), allowing full and independent flexibility to control the on/off state of the output. The UCC27714 includes protection features wherein the outputs are held LOW when inputs are floating or when the minimum pulse width specification of the input is not met. The driver inputs are CMOS/TTL compatible for easy interface to digital power controllers and analog controllers alike. An Enable/Disable function is included in the UCC27714 to enable the output gate signals. The device accepts a wide range bias supply input from 10 to 20 V and offers UVLO protection for both the VCC and HB bias supply pins. The UCC27714 is available in SOIC-14 package and rated to operate from –40°C to 125°C.

5.3 LMT84

The LMT84 is precision CMOS integrated-circuit temperature sensors with an analog output voltage that is linearly and inversely proportional to temperature. It can operate down to 1.5-V supply with 5.4-µA power consumption, making it ideal for battery powered devices. Multiple package options including through-hole TO-92 and TO-126 packages also allow the LMT84 to be mounted on-board, off-board, to a heat sink, or on multiple unique locations in the same application. Class-AB output structures gives the LMT84 strong output source and sink current capability that can directly drive up to 1.1-nF capacitive loads. This means it is well suited to drive an analog-to-digital converter sample-and-hold input with its transient load requirements. It has accuracy capability specified in the operating range of −50°C to 150°C.

5.4 TL431A

The TL431 is a three-terminal adjustable shunt regulator with specified thermal stability over applicable automotive, commercial, and military temperature ranges. The output voltage can be set to any value between V_{REF} (approximately 2.5 V) and 36 V with two external resistors. The TL431 has a typical output impedance of 0.2 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for Zener diodes in many applications such as onboard regulation, adjustable power supplies, and switching power supplies. The TL431 has a low-output drift versus temperature ensures good stability over the entire temperature range.

6 System Design Theory

The complete system is designed in two boards, as shown in Figure 4. The boards TIDA-00433DB is the power supply board with DC bus capacitors, which rectifies the 230-V AC input supply. The other board TIDA-00433MB consists of the three-phase inverter with the onboard 15-V bias power supply.

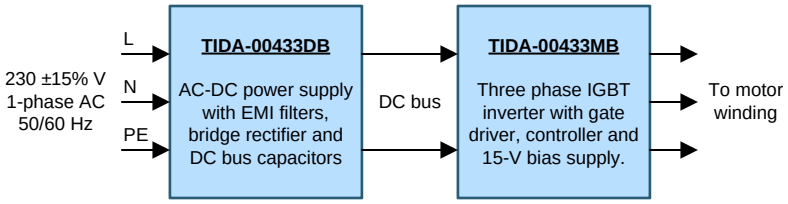

Figure 4. Power Supply — Inverter Board Split Up

6.1 AC-DC Power Supply Board (TIDA-00433DB)

The AC-DC power supply board schematic is shown in Figure 5. The power supply board is designed using the diode bridge rectifier and bulk electrolytic capacitor at the DC bus, with provision for necessary filters for conducted emission, surge, and EFT protection as per the standard EN55014.

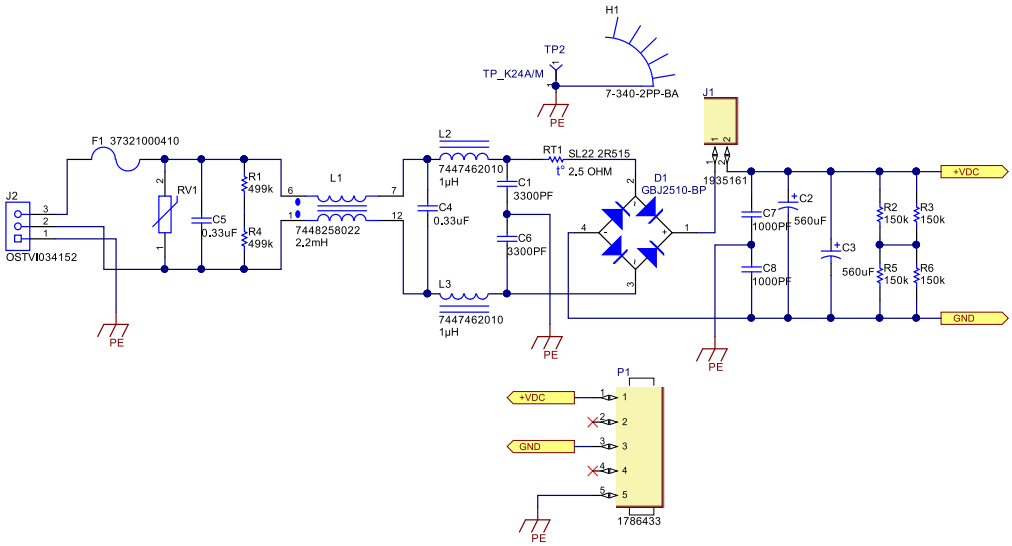

Figure 5. AC-DC Power Supply (TIDA-00433DB)

In the schematic, J2 is the three-pin connector for the single-phase AC input. In the schematic, F1 is the protection fuse followed by the Metal Oxide Varistor (MOV) for surge protection. A 20-mm diameter MOV with 275-V AC rating is selected for this application. R1 and R4 forms discharge resistor for the X2 capacitor C4 and C5. The filter network consists of C5, C4, L1, L2, L3 C1, C6, C7, and C8 form the conducted emission filter. C5 and C4 are X2 rated capacitors, C1, C6, C7, and C8 are Y2 rated capacitors. L1 is a common mode filter and L2 and L3 are differential mode filters. To limit the inrush current of the bulk DC capacitors, an inrush current limiter RT1 is provided. D1 is the full bridge rectifier.

J1 is the connector for connecting external DC choke. The external chock can be connected to meet the harmonic standards.

C2 and C3 are the electrolytic capacitors at the DC bus. The capacitors are designed for 10% voltage ripple at a power of 900 W. R2, R3, R5, and R6 forms the bleeder resistor for the bulk capacitors.

NOTE: The bleeder resistors can be eliminated on integration of the inverter board and AC-DC power supply into single board. The differential mode inductors L2 and L3 were not used in the conduction emission test because the test is giving satisfactory performance without L2 and L3 and hence can be eliminated.

6.1.1 Design of DC Bus Capacitor

The DC bus capacitor is important while designing the inverter-fed motor drives operating from the AC mains. The DC bus capacitor serves the following purposes.

1. Reduces the voltage ripple in the DC link and provide a stable DC link voltage for the inverter. A high DC voltage ripple may cause motor torque ripple and cause inferior performance of the motor drive.
2. In PWM inverter drives, there could be huge current ripple in the DC bus. The DC bus capacitor act as local storage for handling the ripple current.
3. The DC bus capacitor act as a storage for regenerative energy from the motor. If diode bridge rectifiers are used, the regenerative energy could not be fed back to the source and hence absence of a proper DC bus capacitor may cause high voltage build up in the DC link during regeneration and cause voltage breakdown of the semiconductors.

In this reference design, the capacitor is designed to limit the DC bus voltage ripple to less than 10% of the peak value at rated DC bus power of 900 W.

If the AC input supply is 230 V, 50 Hz, the discharge time of the capacitor, $t_{discharge}$ = 10 ms (approximate, to make the calculations simple). If the average DC link current is at 900 W, $I_{DC} \approx 3$ A. Therefore, required capacitance value is found with

$$C \geq I_{DC} \times \frac{\Delta t}{\Delta V_{DC}}$$

where

- $\Delta t = t_{discharge} = 10$ ms
- ΔV = 10% of 325 = 32.5 V (1)

Substituting in Equation 1, C ≥ 924 µF.

The ripple current capacity of the capacitor also needs to be decided. The application is a BLDC motor driven by the three-phase inverter using trapezoidal control. In trapezoidal control, the DC link current would have huge current ripple during commutation in motor. The DC bus ripple current could be as high as two times the DC bus average current. The DC bus capacitors should be able to handle this ripple current. A high ESR capacitor will increase the losses in the capacitor, which leads to capacitor heating and hence reduced capacitor life.

This reference design uses two 560-µF capacitors with a 2-A ripple current capacity, which are connected in parallel to share the ripple current.

6.1.2 Selection of Bridge Rectifier

The diode bridge rectifier should withstand the peak inverse voltage at 265-V AC. If a DC link choke is not used, the peak current drawn by the bulk electrolytic capacitors could be as high as 20 A at rated input power of 900 W. This reference design uses a 1000-V, 25-A full bridge rectifier.

Thermal design is done to select the appropriate heat sink for the bridge rectifier by calculating the losses in the bridge rectifier.

Rated power = 900 W
The DC bus capacitor is designed for 10% voltage ripple.
Therefore the average DC bus voltage, V_{DCavg} = 310 V

At 900 W, average DC bus current, $I_{DCavg} \approx 3$ A
Therefore, the average forward current through the bridge rectifier, I_{Favg} = 3 A

During the charging, the bulk capacitors draws very high peak current from the supply of the order of 20 A. Therefore, the RMS current flowing through the diode will be more compared to the average current.

The simulation results with the designed capacitor value shows that at 900-W DC bus power, the RMS DC bus current ≈ 7.5 A

For the thermal design calculations, the following values are used:

- Diode forward average current, I_{Favg} = 3 A
- Diode forward RMS current, I_{Frms} = 7.5 A

Conduction loss in the diode can be calculated using Equation 2:

$$P_{DIODE} = \frac{1}{T}\int_0^T V_{F(T_j, I_F)} I_F \, dt$$

where

- $V_{F(Tj,If)}$ is the forward voltage of the diode at a junction temperature T_j and forward current I_F (2)

The user can express the forward voltage V_F at a forward current I_F as in Equation 3.

$$V_F = V_{F0} + \left(r_D \times I_F\right) \quad (3)$$

Where V_{F0} is the zero current forward voltage drop, which is obtained by drawing a tangent to the forward characteristics of diode over the operating current range, extend it to the voltage axis, and take the voltage axis intercept. r_D is the dynamic resistance of the diode, which is the slope of the tangent line.

Using Equation 3, the power dissipation in the diode can be expressed as in Equation 4.

$$P_{DIODE} = V_{F0} I_{Favg} + r_D I_{Frms}^2 \quad (4)$$

Normally V_{F0} and r_D are specified in the datasheet. In this reference design, the full-bridge rectifier is used and at any time two diodes are ON. Therefore, the total loss in the bridge rectifier can be found with

$$P_{RECT} = 2 \times \left(V_{F0} I_{Favg} + r_D I_{Frms}^2\right) \quad (5)$$

From the datasheet, approximate values of V_{F0} and r_D are V_{F0}= 0.75 V and r_D= 24 mΩ.

Therefore, P_{RECT} = 2 × [(0.75 × 3) + (0.024 × 7.5^2)] = 7.2 W.

From the rectifier datasheet, the junction to case thermal resistance of the rectifier, $R_{\theta JC}$ = 0.6°C/W.

The maximum operating ambient temperature, $T_{amb(max)}$ = 55°C

To limit the junction temperature of the diode rectifier to 115°C (maximum operating temperature of the bridge rectifier is 150°C), connect a heat sink to the rectifier. The heat sink can be directly mounted on the bridge rectifier without any interface material (the rectifier case is isolated).

If $R_{\theta HA}$ is the thermal resistance of the heat sink to the ambient, the thermal equation can be written as

$$T_j - T_{amb(max)} = P_{RECT} \times \left(R_{\theta JC} + R_{\theta HA}\right) \quad (6)$$

Substituting T_j = 115°C in Equation 6 leads to $R_{\theta HA}$ = 7.7°C/W. Therefore, select a heat sink with a thermal resistance less than 7.7°C/W.

6.2 Inverter Board (TIDA-00433MB)

6.2.1 Three-Phase Inverter

The three-phase inverter is designed to operate from the rectified 230-V AC mains. However, with an active power factor correction front end the maximum DC bus voltage could be up to 390 V. Figure 6 shows the input connector J1 in the inverter board. A three-terminal connector is used, which interfaces the DC supply terminals, and the earth connection.

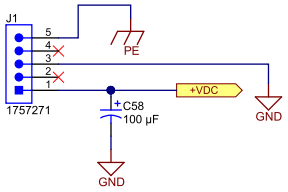

Figure 6. DC Power Supply Connector to Inverter Board

NOTE: The capacitor C58, rated 100 µF, 400 V, is used as a DC capacitor near the inverter bridge to supply the ripple current locally in the inverter board. However, on integration of the AC-DC power supply and the three-phase inverter in a single board, the DC capacitors used in the rectifier board (in this reference design 560 µF × 2, in the AC-DC board) is sufficient and the capacitor C58 can be removed.

Figure 7 shows the schematic of the three-phase inverter . The decoupling capacitors C30, C31, and C32 are provided for each leg of the inverter to limit the switching voltage spikes. These capacitors must be placed very close to each leg of the inverter. The resistor R55 is used to sense the DC bus return current. The filter network consists of C17, R25, and R26 is used as a high frequency differential filter. The terminal block J7 is used to connect the three-phase motor terminals.

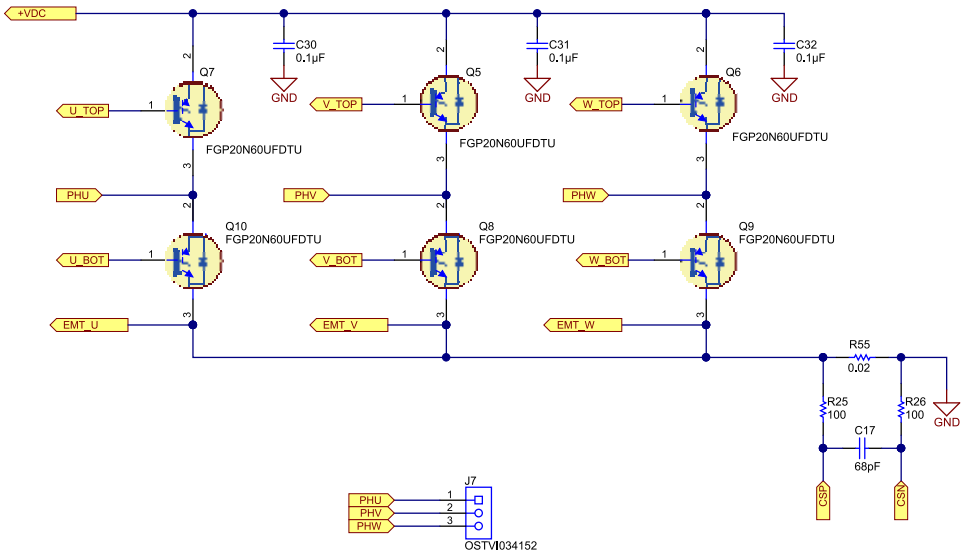

Figure 7. Three-Phase Inverter

6.2.2 Selection of Switching Device

The three-phase inverter is designed to operate from the rectified 230-V AC main. However, with an active power factor correction front end the maximum DC bus voltage could be up to 390 V. Considering the safety factor and switching spikes, the switching device with voltage rating of 1.25 to 1.5 times the maximum input voltage can be selected.

Voltage rating of the switching device, $V_{SW} \geq 1.25 \times 390 \approx 500$ V.

The current rating of the switching device depends on the peak winding current. The rated power is 900 W. Considering average DC bus voltage of 310-V DC, at 230-V AC input, average current at the DC bus:

$$I_{AVG} \approx \frac{900\ W}{310\ V} \approx 3\ A$$

The peak current in the motor winding depends on the motor parameters. Normally in trapezoidal control, the peak winding current could be as high as two times the average DC current. Therefore, the peak current in the switches could be more than 6 A. In the reference design, the peak current limit is kept at 7 A. Keeping the current limit to a lower value will limit the torque capability of the drive. Considering a factor of safety, a switching device with current rating 1.5 to 2 times the calculated peak current can be selected. The device should be rated for this current at the maximum operating junction temperature (T_j). Therefore, the current rating of the switching device, $I_{SW} \geq 1.5 \times 7 \approx 11$ A, at $T_j = 125°C$.

Another aspect for selecting the switching device is the switching frequency. This reference design uses a switching frequency of 10 kHz. IGBTs are selected for the application because of lower switching frequency (10 kHz), high voltage (400-V DC) and reasonable high power (≈ 1 kW).

The reference design uses a 600-V, 20-A IGBT.

6.2.3 Selection of Sense Resistor

The sense resistor is used at the DC link return path to measure the inverter or motor current. In trapezoidal control of BLDC motors, only two phases are ON at a time, thus the DC link current is the same as the winding current. Therefore, different current or torque control strategies can be implemented by sensing only the DC bus current. The DRV92250 has an internal differential amplifier to sense the bottom DC link current. If the designer is implementing any current control algorithm, consider the differential amplifier parameters when selecting the sense resistor.

The power dissipation is another factor to be considered in the selection. A high resistance value that leads to a high power loss in the resistor and a very low value may cause noise problems in sensing and control.

This reference design uses the sense resistor to implement peak winding current control using the internal comparator of the DRV92250. The inverting input of the comparator is used as the current threshold reference and is fed from a digital-to-analog converter (DAC), whose maximum output voltage is 1.2 V. In this reference design, the peak current limit is designed to be 7 A. Selecting a 20-mΩ sense resistor, The sense voltage, $V_{SENSE} = I_{SENSE} \times R_{SENSE}$. At 7 A, $V_{SENSE} = 0.14$ V.

The nominal RMS current of the motor winding current is less than 5 A for this application. Therefore, the power loss in the resistor at 5 $A_{(RMS)}$ is given by Equation 7.

$$\text{Power loss in the resistor} = I_{RMS}^2 \times R_{SENSE} = 5^2 \times 0.02 = 0.5\,W \quad (7)$$

In case of a blocked rotor or any other over current situation, the peak current will be limited to 7 A. The power loss in the resistor at a 7-A continuous current = 0.98 W. Therefore, a standard 2-W, 2512-package resistor can be used.

6.2.4 IGBT Loss Calculation

The trapezoidal BLDC motor control is used in this reference design. In trapezoidal control, any switch will conduct for 120° in an electrical cycle, and in any case two switches are ON, one from the high side and the other from the low side.

With a stable 230-V AC input system; the diode rectified average DC bus voltage is a constant. Therefore, in order to control the average voltage applied to the motor, a PWM technique can be used. This can be achieved by inserting the PWM to the 120° conduction period of either top side or bottom side switch or both.

Here, only the top side is switched to control the voltage applied to the motor winding and the bottom side switch is continuously ON for the entire 120° period. This leads to saving in switching loss from the bottom switch.

The inverter losses are calculated at 900-W output power from the inverter. The specifications given in Table 2 are used in calculating the inverter losses.

Table 2. Parameters Used for Inverter Loss Calculation

PARAMETER	VALUE
Rated voltage of the motor	300 V
Nominal motor current (RMS)	4.5 A
Average DC current	3 A
Rated RPM	18000
No of poles of the motor	4
Motor electrical frequency at rated RPM	600 Hz

6.2.4.1 Power Loss in Low-Side IGBT

Conduction Loss

IGBT conduction losses can be calculated using an approximate equivalent circuit consists of a series connection of a voltage source (V_{CE0}) representing the ON state zero current collector-emitter drop and the dynamic collector-emitter ON state resistance (r_C).

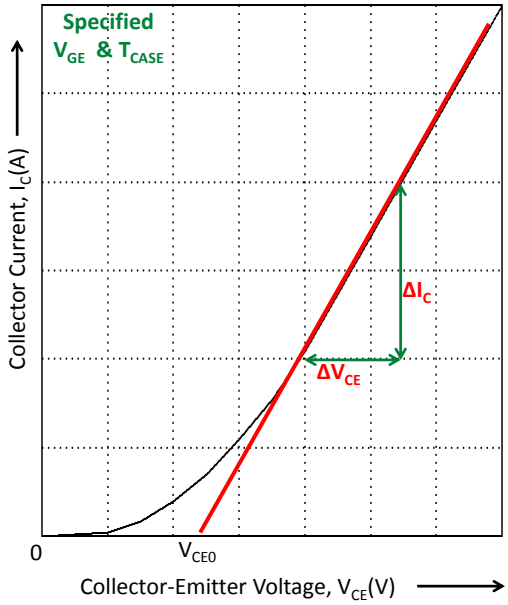

Figure 8. Modeling of IGBT for Loss Calculation

Figure 8 shows typical output characteristics of an IGBT at a particular gate-to-emitter voltage (V_{GE}) and case temperature. A linear interpolation is done on the output characteristics to derive the equivalent circuit equation given in Equation 8.

$$V_{CE} = V_{CE0} + r_C \times I_{C,RMS} \tag{8}$$

Where r_C is the equivalent dynamic resistance of the IGBT, which is the slope of the output characteristics. $I_{C,RMS}$ is the RMS value of the switch current and $I_{C,AVG}$ is the average switch current.

Based on the assumption above, the conduction loss (P_C) of an IGBT can be expressed as in Equation 9.

$$P_C = \left(V_{CE0} \times I_{C,AVG}\right) + \left(r_C \times I^2_{C,RMS}\right) \tag{9}$$

In BLDC trapezoidal control, one switch is conducting for 120°, or one third of the total electrical cycle.

Therefore, the conduction loss in one lower IGBT is

$$P_{CL} = \frac{1}{3} \times \left(\left(V_{CE0} \times I_{C,AVG}\right) + \left(r_C \times I^2_{C,RMS}\right)\right) \tag{10}$$

From the output characteristics of the IGBT at the case temperature of 125°C, the approximate values of the loss modeling parameters are $V_{CE0} \approx 1.2$ V and $r_C \approx 50$ mΩ.

Therefore, the conduction loss in one lower IGBT is $P_{CL} = (1/3) \times [(1.2 \times 3) + (0.005 \times 4.5^2)] \approx 1.55$ W.

Switching Loss

There is no PWM switching in low-side switches and is continuously ON for the 120° interval. However, the low-side switch is commutating at the motor electrical frequency.

The motor electrical frequency at rated RPM is

$$f_{ele} = \frac{\text{No of pole pairs} \times \text{RPM}}{60} = \frac{2 \times 18000}{60} = 600 \text{ Hz}$$

$$P_{SWL} = f_{ele} \times \left(E_{ON} + E_{OFF}\right) \tag{11}$$

From the datasheet of the IGBT,
Turn ON switching loss, E_{ON} = 0.41 mJ, when tested at V_{CC} = 400 V, I_C = 20 A, R_G = 10 Ω, V_{GE} = 15 V
Turn OFF switching loss, E_{OFF} = 0.36 mJ, when tested at V_{CC} = 400 V, I_C = 20 A, R_G = 10 Ω, V_{GE} = 15 V

In the reference design, V_{GE} = 15 V, and the peak winding current I_{PK} = 7 A.

Low side IGBT switching loss,

$$P_{SWL} = \left(E_{ON} + E_{OFF}\right) \times \left(\frac{V_{NOM} \times I_{PK}}{V_{CC(test)} \times I_{C(test)}}\right) \times f_{ele} \tag{12}$$

$$P_{SWL} = (0.41 + 0.36) \times \left(\frac{325 \times 7}{400 \times 20}\right) \times 600 = 0.13 \text{ W}$$

Total loss on a single low-side IGBT,

$$P_L = P_{CL} + P_{SWL} \tag{13}$$

$$P_L = 1.55 + 0.13 \approx 1.7 \text{ W}$$

6.2.4.2 High-Side IGBT Loss

The PWM is applied to high-side switches; therefore, the only difference in estimating the conduction loss in the high-side IGBT and low-side IGBT is that the user needs to consider the duty cycle of the PWM.

- Average DC bus voltage = 310 V
- Average motor winding voltage at rated load = 300 V (Rated voltage of the motor)
- At rated load, PWM Duty Cycle, D = 300/310 = 0.968

Therefore, the conduction loss in one high-side IGBT,

$$P_{CH} = \frac{1}{3} \times \left(\left(D \times V_{CE0} \times I_{C,AVG} \right) + \left(r_C \times I_{C,RMS}^2 \right) \right) \tag{14}$$

$$P_{CH} = \frac{1}{3} \times \left((0.968 \times 1.2 \times 3) + (0.05 \times 4.5^2) \right) \approx 1.5 \text{ W}$$

In the reference design, the high-side IGBT is switching at 10 kHz. Therefore, the switching loss is

$$P_{SWH} = \frac{1}{3} \times \left(E_{ON} + E_{OFF} \right) \times \left(\frac{V_{NOM} \times I_{PK}}{V_{CC(test)} \times I_{C(test)}} \right) \times f_{SW} \tag{15}$$

$$P_{SWH} = \frac{1}{3} \times (0.41 + 0.36) \times \left(\frac{325 \times 7}{400 \times 20} \right) \times 10 \text{ k} = 0.73 \text{ W}$$

Total loss on a single high-side IGBT, $P_H = P_{CH} + P_{SWH}$

$P_H = 1.5 + 0.73 = 2.23$ W

6.2.4.3 Diode Losses

Losses Due to PWM Switching

When the top IGBT is turned off during PWM switching, the motor current gets transferred to the antiparallel diode of the lower IGBT. Therefore, the lower diode losses can be calculated using Equation 16.

$$P_{DIODE,SW} = \left(\frac{1}{3} \times (1-D) \times V_F \times I_{F,AVG}\right) + \left(f_{SW} \times E_{DIODE}\right) \quad (16)$$

Where E_{DIODE} is the reverse recovery switching losses in the diode. Excluding the reverse recovery switching loss in the diode,

$$P_{DIODE,SW} = \frac{1}{3} \times (1-D) \times V_F \times I_{F,AVG}$$

where

- V_F is the forward loss in the diode
- $I_{F,AVG}$ is the average diode forward current (17)

$$P_{DIODE,SW} = \frac{1}{3} \times (1 - 0.968) \times 1.7 \times 3 = 0.0544 \text{ W}$$

The diode losses calculated above are for the low side. The high-side diodes are conducted during the commutation period only and hence calculated separately.

Losses Due to Phase Commutation

During commutation, the motor winding current will freewheel through the antiparallel diode of the complimentary IGBT. For example, if the top IGBT is commutating, then the winding current which was flowing through the top IGBT will get transferred to the antiparallel diode of the lower IGBT. There are six commutations in one electrical cycle of the motor current waveform. The commutation period can be defined as the duration of time in which the winding current of the commutation phase reduces to zero. The commutation period depends on the motor inductance and the peak winding current, hence the commutation period varies from motor to motor.

The reference design uses a vacuum cleaner motor for testing and the approximate commutation time is observed as less than 100 µs. The commutation time, $T_{commutation}$ = 100 µs.

For a 4-pole motor running at 18000 RPM, the electrical frequency of motor winding current is

$$f_{elec} = 600 \text{ Hz} \quad (18)$$

Since there are six commutations in one electrical cycle, the total diode loss due to phase commutation can be calculated as

$$P_{DIODE,COMM} \approx 6 \times V_F \times I_{F,avg} \times T_{commutation} \times f_{ele}$$

where

- $V_{F,avg}$ is the diode forward voltage drop
- $I_{F,avg}$ is the average forward current of the diode during commutation (19)

The multiplication factor of 6 in Equation 19 is because there are six commutations in an electrical cycle. During commutation, the current in the commutating phase reduces from the peak value to zero. In the application design, the peak winding current is 7 A. Therefore, $I_{F,avg}$ = 7/2 = 3.5 A.

From the device datasheet, $V_{F,avg} \approx$ 1.5 V, at diode junction temperature of 125°C at a forward current of 7 A.

Substituting the values in Equation 19,

$$P_{DIODE,COMM} \approx 6 \times 1.5 \times 3.5 \times 100 \text{ µs} \times 600 \text{ Hz} = 1.89 \text{ W}$$

Therefore, the total diode loss, $P_{DIODE} = (3 \times P_{DIODE,SW}) + P_{DIODE,COMM}$ = 2.1 W.

Total Loss in Three-Phase Inverter

The total losses in the IGBTs of the three-phase inverter are:

$$P_{LOSS} = 3 \times \left(P_L + P_H\right) + P_{DIODE} \tag{20}$$

$$P_{LOSS} = 3 \times \left(1.7 + 2.23\right) + 2.1 \approx 14\ W$$

6.2.5 Thermal Design for Three-Phase Inverter

Proper thermal design is crucial for the safe and reliable operation of semiconductors. Operating the semiconductor at higher operating temperature reduces the safe operating area and may lead to failure or reduce the life of the device.

The whole aim of the thermal design is to limit the junction temperature of the IGBTs with in the safe values at full load. The datasheet specifies that the IGBT has a maximum junction temperature rating of 150°C. The user need to design a heat sink or any cooling method needs to have the junction temperature within safe limits.

However, the user has access to the case of the IGBT and hence should limit the case temperature in such a way that at that particular case temperature the junction temperature is in safe limit. The difference between the case and junction temperature depends on the junction to case thermal resistance.

The datasheet of the IGBT specifies the thermal resistance of the IGBT and antiparallel diode separately.

From the datasheet:

- The junction to case thermal resistance of the IGBT, $R_{\theta JC\_IGBT}$ = 0.76°C/W
- The junction to case thermal resistance of the Diode, $R_{\theta JC\_DIODE}$ = 2.51°C/W

The case of the IGBT is generally connected to the collector terminal. Therefore, an electrically insulated and thermally conducting filler or interface material is required between the IGBT case and the heat sink. The thermal interface material has to be selected such that it has sufficient electrical insulation voltage rating compared to the system operating voltage. The material should have a very low thermal resistance as well.

The thermal equivalent circuit of a single IGBT with the independent heat sink is as shown in Figure 9.

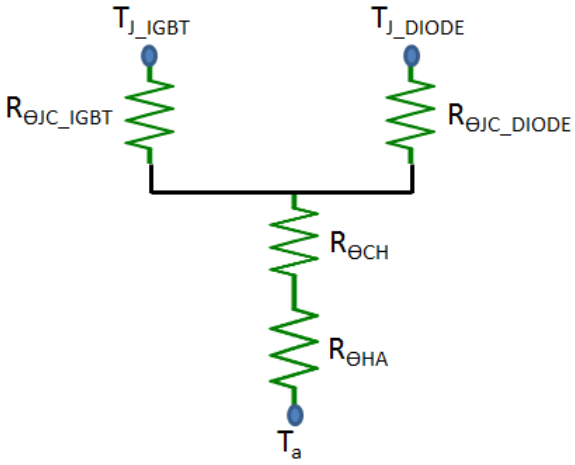

Figure 9. Thermal Equivalent Circuit of Single IGBT to Ambient

NOTE: $R_{\theta CH}$ = Thermal resistance from IGBT case to heat sink or the thermal resistance of the thermal interface material (°C/W)
$R_{\theta HA}$ = Thermal resistance from heat sink to the ambient (°C/W)

In the reference design, a single heat sink is used for all six IGBTs of the three-phase inverter. The thermal equivalent circuit of the system becomes as shown in Figure 10.

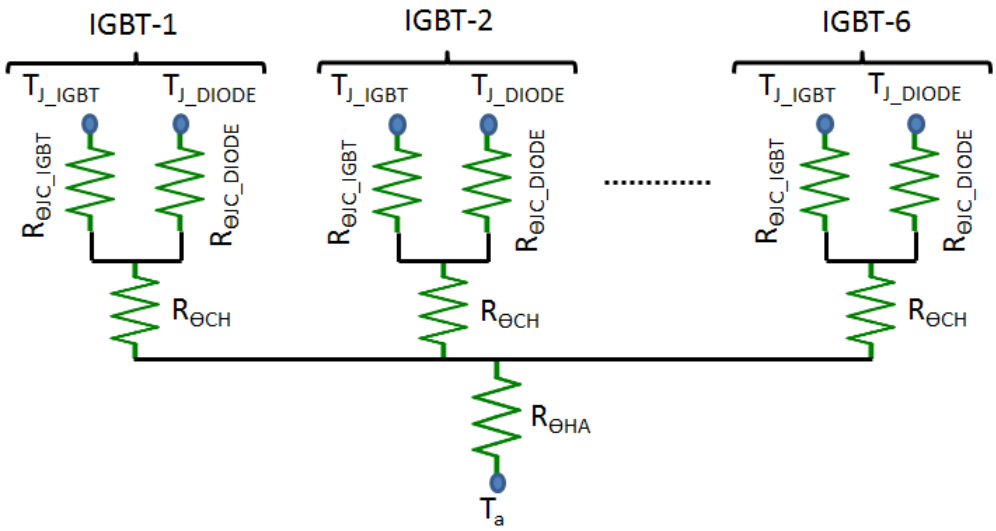

Figure 10. Thermal Equivalent Circuit of Inverter With Heat Sink

For analysis simplicity, It is assumed that all the IGBT losses are same. The diode thermal resistance ($R_{\theta JC\_DIODE}$) is excluded in the mathematical equation.

From the equivalent circuit, the mathematical relation for temperature rise can be written as in Equation 21.

$$T_j - T_a = \left(\frac{R_{\theta JC(IGBT)} + R_{\theta CH}}{6} + R_{\theta HA} \right) \times P_{LOSS} \tag{21}$$

The maximum operating ambient temperature, T_a = 55°C

Considering a safety margin, let the maximum junction temperature at rated load be 110°C, the temperature rise, $T_j - T_a$ = 55°C.

A typical thermal interface material has a thermal resistance less than 0.5°C/W. The calculated IGBT power loss at a rated inverter output power $P_{LOSS} \approx$ 14 W. Considering a design margin of 2 W, the IGBT losses can be approximated to 16 W. Substituting these values in Equation 21 gives $R_{\theta HA}$ = 3.2°C/W.

An extrusion heat sink with thermal resistance less than 3.2°C/W and having length sufficient to mount six IGBTs is a good choice.

6.2.6 Buck Regulator Using DRV92250

The bias power supply of 15 V required for DRV92250 and UCC27714 is derived using the external high voltage P-channel FET and discrete gate drive controlled by the buck regulator inside the DRV92250. The buck converter circuit is shown in Figure 11.

The DC/DC buck converter controller on the DRV92250 has special protection features designed in to prevent any damage to external components in case of a floating VCC pin (15-V power supply pin). In addition, to protect the off chip switching transistor/FET, duty cycle control is also provided through serial register bits DCDeGlitch and DcDcWidth[1;0]. Minimum duty cycle is controlled by setting the DCDeGlitch control bit to a 1. This enables pulse extension circuitry on chip which guarantees a minimum switcher pulse width of at least 1 µs. Similarly, maximum switcher duty cycle is controlled by programming DcDcWidth[1:0] control bits. For duty-cycle greater than what is set by control bits DcDcWidth[1:0], the SWDR output waveform is modulated by a 125-kHz clock signal to protect the switching power transistor and inductor.

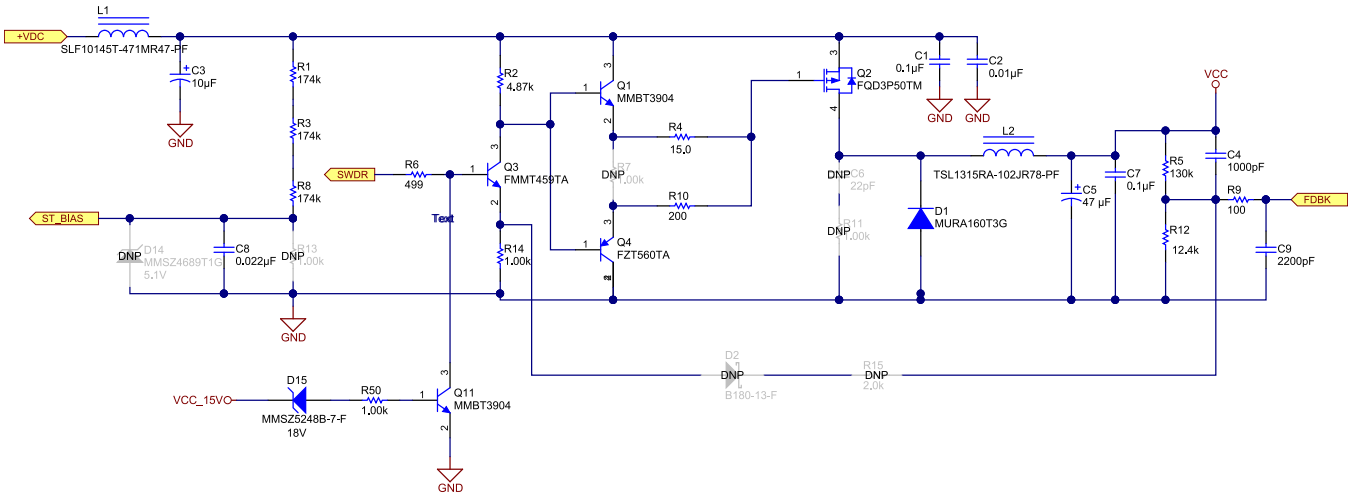

Figure 11. Buck Converter Circuit

FDBK is the feedback control input for the DC/DC converter. The output voltage of the buck converter is fed back to the FDBK pin using a feedback resistive network. An on-chip hysteresis comparator closes the control loop by comparing the voltage on pin FDBK against reference voltage derived from the band gap. The nominal value of the band gap voltage is 1.3 V. The comparator switching output drives the external switch through pin SWDR. The comparator hysteresis voltage is programmable and provides four options of 10 mV, 20 mV, 30 mV, and 40 mV using the control bit HYSDCDC[1:0].

The DRV92250 derives the start-up bias supply through the pin ST_BIAS. The resistive divider network connected between ST_BIAS and the high voltage DC bus is used for this purpose.

6.2.6.1 Discrete Gate Drive for High-Side Buck Converter

Figure 11 shows the buck converter using the DRV92250 controller. The external switch for the buck converter is a P-channel MOSFET Q2. The transistors Q1, Q3, and Q4 form the gate driver circuit. D1 is the freewheeling diode of the buck converter. R11 and C6 form the snubber for D1. The inductor L2 and capacitor C5 forms the output filter. The resistors R5 and R12 are the voltage divider to feed back the output voltage to the DRV92250 through the FDBK pin. The starting bias for the DC/DC converter is derived from the mains voltage using the resistor network R1, R3, and R8. Three resistors are used to reduce the voltage stress on each resistor.

Working of Gate Driver

The transistors Q1, Q3 and Q4 are operating in the linear region. The leg consist of R2, R14, and Q3 forms a voltage regulator (when Q3 is ON), which regulates the voltage across R2, when input voltage V_{DC} varies over a wide range. This can be explained as follows.

The SWDR is the PWM signal from DRV92250 with PWM high level voltage of 3.3 V and low level of 0 V.

When SWDR is high, the KVL equation for the loop consists of SWDR, R6, the base emitter junction of Q3, and R14 can be written as in Equation 22.

$$3.3 = \left(i_{b(Q3)} \times R6\right) + V_{BE(Q3)} + \left(i_{e(Q3)} \times R14\right)$$

where

- $i_{e(Q3)}$ is the emitter current of Q3
- $i_{b(Q3)}$ is the base current of Q3 (22)

Typically, $V_{BE(Q3)}$ = 0.7 V. Neglecting the base current, Equation 22 can be re-written as

$$i_{e(Q3)} = \frac{3.3 - 0.7}{R14} = \frac{2.6}{R14} \quad (23)$$

The design uses R14 = 1 kΩ. Therefore, $i_{e(Q3)}$ = 2.6 mA.

This means the resistor R14 fixes the emitter current of the transistor Q3. The collector current of Q3 can be approximated to emitter current (neglecting the base current).
$i_{c(Q3)} \approx i_{e(Q3)}$ = 2.6 mA

Then the voltage drop across R2 is determined by the emitter current. Therefore, the voltage drop across R2:

$$V_{R2} = i_{c(Q3)} \times R2 \quad (24)$$

This clearly shows that the voltage across R2 is regulated (when Q3 is ON) independent of the DC bus voltage.

Because of the totem pole network consisting of Q1 and Q4, the voltage at the collector of Q3, will be reflected at the emitters of Q1 and Q4 with a difference of 0.7 V. In short, the voltage across R2 will appear as the gate-to-source voltage (V_{GS}) of the P-channel FET Q2, with a difference of V_{BE} of the totem pole transistor Q4.

Therefore,

$$V_{GS(Q2)} = -\left(V_{R2} + V_{BE(Q4)}\right) \quad (25)$$

Assuming $V_{BE\ (Q4)}$ = −0.7 V,

$$V_{GS(Q2)} = -\left(V_{R2} - 0.7\ V\right)$$

This reference design uses the high voltage P-channel FET FQD3P50TM. Typical gate to source voltage of –12 to –15 V is a good choice.

Considering –12 V as the required gate voltage, substituting in Equation 25,

$$V_{R2} = -(V_{GS(Q2)} - 0.7) = 12.7\ V \quad (26)$$

Therefore, the required resistor,

$$R2 = \frac{V_{R2}}{i_{c(Q3)}} = \frac{12.7\ V}{2.6\ mA} = 4.88\ k\Omega$$

.

When Q3 is ON, the voltage drop across R2 makes Q4 to turn ON. The gate drive provides the required gate charge to Q2 by means of the gate current flowing through the gate-to-source capacitance of Q2, R10, and Q4. Therefore, the negative voltage across the gate-to-source capacitance of Q2 will build up slowly and causes turn ON of Q2. Similarly when Q3 is OFF, Q4 will turn OFF, and Q1 will turn ON. This removes the gate charge from Q2 through Q1 and R4. That means R10 forms the turn on resistance and R4 forms turn off resistance of Q2.

The maximum voltage across Q3 is equal to the maximum DC bus voltage. The maximum DC bus voltage could be 400 V in this application. Therefore, the transistor Q3 should have a minimum collector to emitter breakdown voltage of 450 V. The voltage across the transistor Q1 is clamped to less than 15 V by the resistor R2. Therefore, a low-voltage (typically 40-V rated) transistor is good enough.

The maximum voltage across the transistor Q4 is equal to the DC bus voltage. The resistor R10 controls the gate current of Q2 during its turn ON. A low value of R10 increases the losses in Q4, and a high value of R10 slows down the turn on of Q2 and hence the turn on losses of Q2. The reference design uses a 200-Ω resistor R10, which is selected based on simulation results to limit the power loss in Q4 (the reference design uses a 500-V, 150-mA PNP transistor having a maximum power capacity of 2 W).

6.2.6.2 Design of Power Components in Buck Converter

The buck converter is designed to generate the bias power supply required in the board. The bias supply voltage of 15 V is generated in the reference design, which optimizes the gate drive for the IGBT. The total power required from the bias supply is approximately 3 W.

The bias power supply is required mainly for the gate drivers, the DRV92250, and the PFC board. The design specification of the buck converter is summarized as in Table 3.

Table 3. Specifications for 15-V Bias Power Supply

PARAMETER	VALUE
Input voltage	90-V to 400-V DC
Output voltage	15 V, 200 mA (approximately 3-W output)
Average output current (I_{OUT})	200 mA
Efficiency	> 70%
Protections	Output overvoltage protection
Isolation	Non-isolated (Buck)

The buck regulator of the DRV92250 is operating in hysteresis control with programmable minimum ON time. At lower input voltages, the buck converter is operating in continuous conduction mode (CCM) to deliver the rated output current. However, as the voltage increases the buck regulator starts operating in discontinuous conduction mode (DCM). The switching frequency is not constant as this controller is based on hysteresis control. Therefore, for a constant output load, as the input voltage increases, the switching frequency decreases. The switching frequency also depends on the hysteresis band provided. The minimum on time of the switching pulse is limited to 1 µs. Therefore, for a constant output load, as the input voltage increases, the on time of the switching pulse reduces and when the pulse width is less than 1 µs, the pulse is extended to 1 µs and the switching frequency is reduced.

6.2.6.3 Output Inductor Selection

In DCM, the inductor current increases the peak current (I_{PK}) and reduces to zero before the next switching cycle.

The voltage across the output inductor can be expressed as in Equation 27.

$$V_L = L \times \frac{di_L}{dt} \tag{27}$$

On linearizing Equation 27,

$$\Delta I_L = \frac{V_L}{L} \times \Delta t \tag{28}$$

In DCM, the inductor current increases during the ON state to the peak current (I_{PK}). Therefore,

$$I_{PK} = \Delta I_{L(ON)} = \frac{V_{IN} - V_{OUT}}{L} \times T_{ON} \tag{29}$$

The maximum DC input voltage, $V_{DC(MAX)}$ = 400 V

The minimum turn ON period of the switching pulse from the buck regulator in the DRV92250 is 1 µs. Considering the non-linearities in the gate driver and the hysteresis controller, the minimum on period of T_{ON_MIN} = 2 µs is considered in this reference design.

At 400-V DC, using Equation 29,

$$_{PK} = \frac{400 - 15}{L} \times T_{ON\_MIN}$$

$$I_{PK} = \frac{385}{L} \times 2\ \mu s \tag{30}$$

The peak value of the current is dependent on the output inductor value. Selecting a lower inductor value increases the peak current in the switch and the freewheeling diode. The DC-DC converter switch current rating should be greater than the peak current rating with a sufficient safety margin. To limit the peak current to less than 1 A, the minimum required value of inductor is

$$L_{MIN} = \frac{385}{I_{PK}} \times T_{ON\_MIN}$$

$$L_{MIN} = \frac{385}{1} \times 2\ \mu s = 0.77\ mH \tag{31}$$

Selecting a standard 1-mH inductor, the peak current is I_{PK} = 0.77 mA.

The current rating of the selected inductor is 780 mA and the saturation current is 1.2 A.

6.2.6.4 MOSFET Selection

The P-channel MOSFET Q2 is selected to handle 0.77-A peak current safely. The voltage rating of the FET should be greater than 1.25 times the maximum input DC bus voltage (considering 25% safety margin due to voltage spike):

- Voltage rating > 1.25 × 400 V = 500 V

The current rating should be greater than 1.5 times the peak current. (50% safety margin):

- Current rating > 1.5 × 0.77 = 1.2 A

The selected device FQD3P50TM is rated for a voltage of 500 V and 2.1-A current capability.

6.2.6.5 Freewheeling Diode Selection

In the reference design, D1 is the freewheeling diode. A fast rectifier diode can be selected with

- Peak Inverse Voltage > 1.25 × $V_{IN(max)}$ = 1.25 × 400 = 500 V
- Forward current I_F > 1.5 × I_{OUT} = 1.5 × 0.2 A = 0.3 A

So 2-A, 600-V diode MURA160T3G is chosen for the application.

6.2.6.6 Selection of Output Voltage Feedback Network

The resistors R5 and R12 are used to take the output voltage feedback signal to the DRV92250. An on-chip hysteresis comparator closes the control loop by comparing the voltage on pin FDBK against a reference voltage derived from the bandgap.

- Required output voltage, V_{OUT} = 15 V
- Typical bandgap voltage of the DRV92250, V_{bg} = 1.3 V

Therefore,

$$V_{bg} = V_{OUT} \frac{R12}{R12 + R5} \tag{32}$$

Substituting V_{OUT} = 15 V and V_{bg} = 1.3 in Equation 32 gets $\frac{R12}{R5} = \frac{1.3}{13.7}$

The sum of these resistors should be selected to be high to limit the standby power. This reference design uses R5 = 130 kΩ and R12 = 12.4 kΩ, which satisfies Equation 32.

6.2.6.7 Output Voltage Ripple

The buck regulator of the DRV92250 is operating in hysteresis control. The different hysteresis voltage thresholds are 10 mV, 20 mV, 30 mV, and 40 mV. The reference design uses a 30-mV hysteresis voltage threshold (V_{HYS}).

Therefore, the minimum output peak-to-peak voltage ripple is

$$\Delta V_{OUT} = V_{HYS} \times \frac{R12 + R5}{R12}$$

where

- V_{HYS} = 30 mV
- ΔV_{OUT} = 344 mV (33)

This is approximately 2.5 % of the rated output voltage of 15 V. Operating frequency is not constant and depends on the input voltage, output voltage, inductor value, V_{HYS}, equivalent series resistance (ESR) of output capacitor, and the delay in the feedback network and hysteresis controller.

6.2.6.8 Output Capacitor Selection

The ESR of the output capacitor affects the ripple of the regulator. However, the V_{HYS} sets the first order value of this ripple. As ESR is increased with a given inductance, the operating frequency also increases. If ESR is reduced, then the operating frequency reduces. The recommended ESR is

$$ESR \leq \frac{\Delta V_{OUT}}{I_{PK}} = \frac{0.344}{0.77} = 0.446\ \Omega \quad (34)$$

The reference design uses a 47-µF, 25-V capacitor with an ESR of 0.4 Ω.

6.2.6.9 Overvoltage Protection

In the circuit shown in Figure 11, the 18-V Zener D15 and transistor Q11, are provided to protect the bias supply going more than 18 V, by pulling the PWM pulses of the DRV92250 to zero.

NOTE: The filter L1 and C3 is used as the input filter for the buck converter. On integration of the AC-DC power supply and buck converter circuit in a single board, these filters can be eliminated or the filter component value can be reduced depending on the closeness of the buck converter circuit and the DC bus bulk capacitor. Placing a small value of L1 and C3 helps to reduce the voltage ramp rate at the buck converter input.

6.2.7 Gate Driver Using UCC27714

The features of the gate driver UCC27714 are

- High-side low-side configuration with independent Inputs
- Fully operational up to 600 V (HS pin)
- Floating channel designed for bootstrap operation
- Peak output current capability of 4A/4A sink/source at VDD = 15 V
- Best-in-class propagation delay (90 ns typ, 125 ns max)
- Best-in-class delay matching (20 ns max)
- TTL and CMOS compatible logic input thresholds independent of supply voltage with hysteresis
- VDD bias supply range of 10 to 20 V
- Undervoltage lockout (UVLO) protection feature on the supply circuit blocks between VDD and VSS pins, as well as between HB and HS pins
- Rail-to-rail drive with outputs held low when inputs are floating
- Robust operation under negative voltage transients (logic operational up to –8 V on HS pin for VDD = 12 V). The parasitic inductance in the circuit can cause negative voltage at HS respect to COM, which can makes logic error of HO if the driver cannot handle negative voltage of HS
- Separated grounds for logic (VSS) and driver (COM) with capability to sustain voltage difference
- Option enable/disable function, pin internally pulled high to enable outputs by default

The circuit diagram for a half-bridge gate drive using UCC27714 is shown in Figure 12.

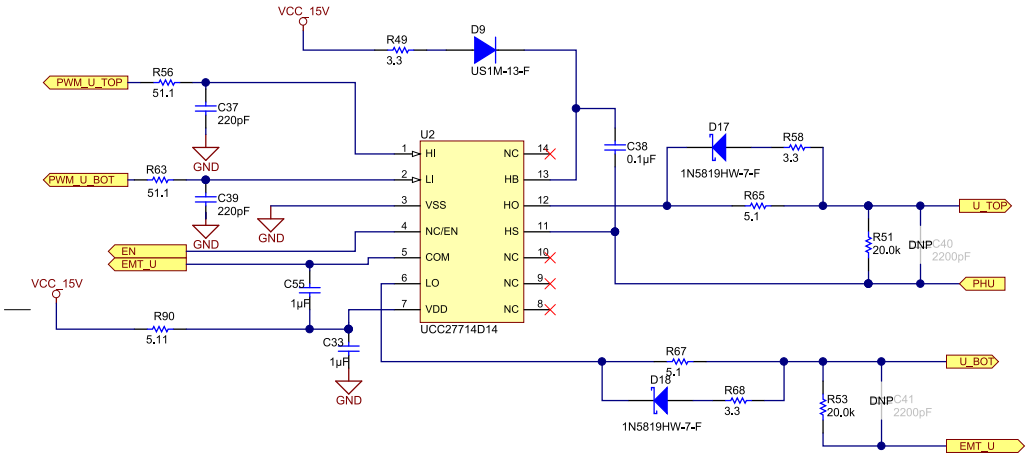

Figure 12. Gate Driver Circuit Using UCC27714

6.2.7.1 Selecting HI and LI Low-Pass Filter Components

An RC filter should be added between PWM controller and input pin of the UCC27714 to filter the high frequency noise. The recommended value of the RC filter is

- $R_{HI} = R_{LI} = 51\ \Omega$
- $C_{HI} = C_{LI} = 220$ pF

In the reference design, R56 and C37 form R_{HI} and C_{HI}, for the phase U. Similarly, R63 and C39 form R_{LI} and C_{LI}.

6.2.7.2 Selecting Boost Capacitor (C_{BOOT})

The boost capacitor should be sized to have more than enough energy to drive the gate of IGBT high, without depleting the boot capacitor more than 10%. A good rule of thumb is size C_{BOOT} to be at least 10 times — as large as the equivalent IGBT gate capacitance (C_g).

C_g will have to be calculated based on the voltage driving the high side IGBT's gate (V_{GE}) and knowing the IGBT's gate charge (Q_g). V_{GE} is approximately the bias voltage supplied to VDD less the forward voltage drop of the boost diode D9 (V_{DBOOT}). In this design example, the estimated V_{GE} was approximately 14.4 V.

$$V_{GE} \approx V_{DD} - V_{DBOOT} = 15\ V - 0.6\ V = 14.4\ V \tag{35}$$

The IGBT used in this example had a specified Q_g of 63 nC.

$$C_g = \frac{Q_g}{V_{GE}} = \frac{63\ nC}{14.4} \approx 4.4\ nF \tag{36}$$

Once C_g is estimated C_{BOOST} should be sized to be at least 10 times larger than C_g.

$$C_{BOOST} \geq 10 \times C_g = 44\ nF \tag{37}$$

For this design example, a 100-nF capacitor was chosen for the boost capacitor.

$$C_{BOOST} = C_{38} = 100\ nF$$

6.2.7.3 Selecting VDD Bypass and Holdup Capacitor (C_{BOOT}) and R_{bias}

The VDD capacitor (C_{VDD}) should be chosen to be at least 10 times larger than C_{BOOST}. For this design example, a 1-µF capacitor was selected. C33 is the VDD capacitor.

$$C_{VDD} \geq 10 \times C_{BOOST} = 1\ uF \tag{38}$$

Under the condition when the output of UCC27714 has not any load and VDD/HB-HS ramp up very fast, the HO/LO has error logic spike even HI/LI is low condition. If the VDD/HB-HS ramp up time from 0 to 15 V less than 50 µs, in another word, if the ramp up slew rate of VDD/HB-HS larger than 300 V/ms, there is risk to hit this phenomenon. A 5-Ω resistor R_{bias} series with bias supply and VDD pin is recommended to make the VDD ramp up time larger than 50 µs. In Figure 12, the resistor R90 is used as the R_{bias} resistor.

6.2.7.4 Estimate Boost Diode Power Dissipation (P_{DBOOT})

Estimate the boost diode power dissipation (P_{DBOOT}) based on the switching frequency, diode forward voltage drop, and gate driver switching frequency (f_{SW}). For this example, the switching frequency was set to 10 kHz. The estimated power loss for the boost diode is given in Equation 39:

$$P_{DBOOST} = \frac{1}{2} \times Q_g \times f_{SW} \times V_{DBOOT} = \frac{1}{2} \times 63\ nC \times 10\ kHz \times 0.6\ V \approx 0.2\ mW \tag{39}$$

6.2.7.5 Selecting Boost Diode Current Limiting Resistor (R_{BOOT})

The resistor R_{BOOT} is selected to limit the current in D_{BOOT} and limit the ramp up slew rate of voltage of HB-HS. It is recommended when using the UCC27714 that R_{BOOT} is between 2 and 10 Ω. For this design, a current limiting resistor of 3.3 Ω is used. The peak boost diode current ($I_{DBOOTpk}$) was limited to roughly 4.4 A.

R_{BOOT} = R49 = 3.3 Ω

$$I_{DBOOT_{PK}} = \frac{VDD - V_{DBOOT}}{R_{BOOT}} = \frac{15\ V - 0.6\ V}{3.3\Omega} \approx 4.36\ A \quad (40)$$

6.2.7.6 Selection of Bootstrap Diode

The voltage seen by the bootstrap diode will be same as the full DC bus voltage (in this case, 325-V DC). The bootstrap diode voltage rating must be greater than the DC bus rail voltage. It must be a fast recovery diode to minimize the recovery charge and hence charge fed from the bootstrap capacitor to the 15-V VDD supply. The diode should be able to carry a pulsed peak current of 4.36 A. However, the average current is much smaller and is dependent on the switching frequency and the gate charge requirement of the high side IGBT. This reference design uses a 1000-V, 1-A, fast recovery diode.

6.2.7.7 Selecting Gate Resistor R_{HO}/R_{LO}

The gate resistors are sized to reduce ringing caused by parasitic inductances and capacitances and also to limit the source/sink current of the gate driver.

From the UCC27714 datasheet,

- LO, HO output pull-down resistance, $R_{HOL} = R_{LOL}$ = 1.45 Ω
- LO, HO output pull-up resistance, $R_{HOH} = R_{LOH}$ = 3.75 Ω

The reference design uses different gate resistors for turn and turn off of the IGBT. The external gate resistors used are

- The high side turn ON gate resistance, R_{HO_ON} = R65 = 5.1 Ω

The parallel combination of the resistors R58 and R65 form the turn OFF equivalent resistance.

- The high side turn OFF gate resistance, R_{HO_OFF} = 2 Ω (5.1 Ω and 3.3 Ω in parallel)
- The low side turn ON gate resistance, R_{LO_ON} = R67 = 5.1 Ω
- The low side turn OFF gate resistance, R_{LO_OFF} = 2 Ω (R67 and R68 in parallel)

Maximum HO drive current (I_{HO_DR}):

$$I_{HO\_DR} = \frac{V_{DD} - V_{DBOOT}}{R_{HO\_ON} - R_{HOH}} = \frac{15\ V - 0.6\ V}{5.1\ \Omega + 3.75\ \Omega} \approx 1.63\ A \quad (41)$$

Maximum HO sink current (I_{HO_SK}):

$$I_{HO\_SK} = \frac{V_{DD} - V_{DBOOT}}{R_{HO\_OFF} - R_{HOL}} = \frac{15\ V - 0.6\ V}{2\ \Omega + 1.45\ \Omega} \approx 4\ A \quad (42)$$

Maximum LO drive current (I_{LO_DR}):

$$I_{LO\_DR} = \frac{V_{DD}}{R_{LO\_ON} - R_{LOH}} = \frac{15\ V}{3\ \Omega + 3.75\ \Omega} \approx 1.63\ A \quad (43)$$

Maximum LO sink current (I_{LO_SK}):

$$I_{LO\_SK} = \frac{V_{DD}}{R_{LO\_OFF} - R_{LOL}} = \frac{15\ V}{3\ \Omega + 1.45\ \Omega} \approx 4\ A \quad (44)$$

6.2.7.8 Estimation of UCC27714 Power Losses ($P_{UCC27714}$)

The power dissipation of the gate driver has two portions as shown in Equation 45:

$$P = P_{DC} + P_{SW} \quad (45)$$

The DC portion of the power dissipation is:

$$P_{DC} = I_Q \times V_{DD}$$

where

- I_Q is the quiescent current for the driver (46)

The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and so on, and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through). The UCC27714 features very low quiescent currents (less than 1.1 mA). In practice, this is the power consumed by driver when its output is disconnected from the gate of power switch.

The power dissipated in the gate driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_{GE}, which is very close to input bias supply voltage V_{DD} due to low V_{OH} drop-out)
- Switching frequency
- Use of external gate resistors

To turn on an IGBT the sufficient gate charge must be provided by the gate driver.

The energy required to supply the gate charge,

$$E_G = Q_G \times V_{GE}$$

where

- V_{GE} is the gate voltage supplied by the gate driver across the gate and emitter of the IGBT (47)

If the IGBT is switching at a frequency f_{SW}, then the gate power supplied by the gate driving during the turn ON of the IGBT,

$$P_{G\_ON} = \frac{1}{2} \times Q_G \times V_{GE} \times f_{SW} \quad (48)$$

The same energy is dissipated when the IGBT turns off also. Therefore, the total gate power required to turn ON and OFF one IGBT is

$$P_G = Q_G \times V_{GE} \times f_{SW} \quad (49)$$

In BLDC trapezoidal control, only upper IGBT is switched using PWM, and lower IGBT is continuously ON for 120° electrical. Both upper and lower IGBTs are ON only for one third of the electrical cycle.

Therefore, the gate power required for the upper IGBT is

$$P_{GH} = \frac{1}{3} \times Q_G \times V_{GE} \times f_{SW} \quad (50)$$

The gate power required for the lower IGBT can be calculated based on the electrical frequency of the inverter output voltage and current. The lower IGBT is switched ON and OFF once in every electrical frequency. The electrical frequency of the motor winding voltage at 18000 RPM for a 4-pole motor is 600 Hz.

$$P_{GL} = Q_G \times V_{GE} \times f_{ele} \quad (51)$$

The total power loss in a single UCC27714 is:

$$P_{UCC27714} \approx \left(V_{DD} \times I_{QDD}\right) + \left(\frac{1}{3} \times Q_G \times V_{GE} \times f_{SW}\right) + \left(Q_G \times V_{GE} \times f_{ele}\right) \quad (52)$$

$$P_{UCC27714} \approx \left(15\ V \times 1.1\ mA\right) + \left(\frac{1}{3} \times 63\ nC \times 15\ V \times 10000\ Hz\right) + \left(63\ nC \times 15\ V \times 600\ Hz\right) = 20.217\ mW$$

There are three gate drivers. Therefore, the total gate drive power loss = 61 mW.

NOTE: In the application example schematic, there are 20-kΩ resistors across the gate and emitter terminals of IGBTs. These resistors are a safety precaution and are placed across these nodes to ensure the IGBTs are not turned on if the UCC27714 is not in place or not properly soldered to the circuit board.

The VDD power terminal for the device requires the placement of electrolytic capacitor as energy storage capacitor, because the UCC27714 is a 4-A peak current driver. And requires the placement of low-ESR noise decoupling capacitance as directly as possible from the VDD terminal to the VSS terminal, ceramic capacitors with stable dielectric characteristics over temperature are recommended, such as X7R or better. The recommended electrolytic capacitor is a 22-µF/50-V capacitor. The recommended decoupling capacitors are a 1-µF 0805-sized 50-V X7R capacitor, ideally with (but not essential) a second smaller parallel 100-nF 0603- sized 50-V X7R capacitor. If a shunt resistor used between COM and VSS, then also bypass this pin to COM with a 1-uF SMD capacitor. The reference design uses a 47-µF capacitor at the output of the 15-V bias supply buck converter and this capacitor is placed near the gate driver.

6.2.8 DRV92250 Controller

The DRV92250 provides all the necessary control features for implementing a three-phase BLDC motor controller and driver. It supports both the Hall sensor BLDC motor control scheme and sensorless BLDC control scheme. A full complement of protective features, such as overcurrent protection, thermal protection and power supply monitoring, makes for a robust system. The CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand. The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock. Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers. Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

6.2.8.1 Voltage Regulators and Power-on Sequence in DRV92250

The DRV92250 has a number of on-chip voltage regulators. The DC-to-DC switcher generates the 15-V VCC supply voltage on the board. This 15-V supply voltage is designated as VCC and in turn powers up the on-chip bandgap reference circuit and the internal and external 5-V linear regulators. The rest of the linear regulators for generating 3.3-V and 1.90-V supply voltages are fed by the internal 5-V regulator. All regulator voltages are listed in Table 4:

Table 4. Internal Power Supplies of DRV92250

SUPPLY VOLTAGE	DESCRIPTION	NOMINAL OUTPUT VOLTAGE (V)
V5P	External analog supply voltage	5.35
V5R	Internal analog supply voltage	5.00
V3P3A	Internal analog supply voltage	3.30
V3P3D	Internal digital supply voltage	3.30
VDD	MCU digital core supply voltage	1.90

The 5-V regulator — used to generate the supply voltage (V5P) for external PCB use — is equipped with output short-circuit detection and protection circuitry. The maximum short-circuit current is controlled by programming the serial register bit REG5V90. When REG5V90 = 0, the maximum short-circuit output current is limited to 180 mA. When REG5V90 = 1, the maximum short-circuit output current is limited to 90 mA. This feature helps protect the on-chip circuitry from any damage in the event of a short to ground at the regulator output.

In addition, in the event of output short-circuit, a status bit (REG5V_SHORT) in the serial register can be set high and an interrupt can be triggered. This behavior is controlled by bit REG5V_INT. When REG5V_INT is set to a 0, output short-circuit detection is disabled and status bit REG5V_SHORT is always set to 0. However, when REG5V_INT = 1, a short-circuit condition at the regulator output will set REG5V_SHORT to a 1 and an interrupt will also be generated for the MCU.

A power-on sequence is initiated when VCC starts to rise. It consists of a coarse and a fine control phase. During the coarse power-up phase, the internal bandgap, the internal 5-V regulator, and both 3.3-V regulators are energized. These blocks do not depend on a specific power-on-reset or power-on-enable signal - they begin to power up as VCC rises. The internal bandgap voltage is the first to stabilize followed by the internal 5-V regulator and the two 3.3-V regulators. A coarse monitoring circuit raises an internal control line to indicate when both of the 3.3-V regulators are above a 3-V threshold. This, in turn, enables the 2-MHz oscillator and an on-board state machine which controls the rest of the power sequencing.

During the fine power-up phase, VCC, V3P3D, and VDD are compared to pre-set threshold voltages or trip points to verify that they have powered-up completely and correctly. These trip points have hysteresis built-in for noise rejection during power-up and power-down transients. As a typical example, when VCC is rising, it must get to a voltage of 7 V or higher before it is qualified as good. Similarly, when VCC is falling, it must fall below a voltage level of 6 V before a VCC fault is flagged. Once all of the monitored supply voltages have been qualified as good, the digital state machine generates a power-on-reset (PORZ) signal approximately 1 ms later. This marks the completion of the entire power-up sequence and the start of normal operation.

6.2.8.2 Digital-to-Analog Converter (DAC)

The DRV92250 has an integrated 8-bit DAC with an output swing from 0 to 1.2 V. The DAC is used to set the current-limit threshold for the overcurrent comparator. The DAC digital input can be set directly by programming the serial port register DACB.

6.2.8.3 Analog-to-Digital Converter (ADC)

The DRV92250 includes an integrated 10-bit ADC with a full scale input range from 0 to 2.4 V. It uses an internal 2.4-V reference voltage.

Figure 13 shows the schematic of the DRV92250 used in the reference design. J4 is the programming connector. The capacitors C10, C11, C12, C13, C21, C25, C26, and C27 are the recommended decoupling resistors. The header J2 is used as the provision for external 12-V supply for programming the DRV92250.

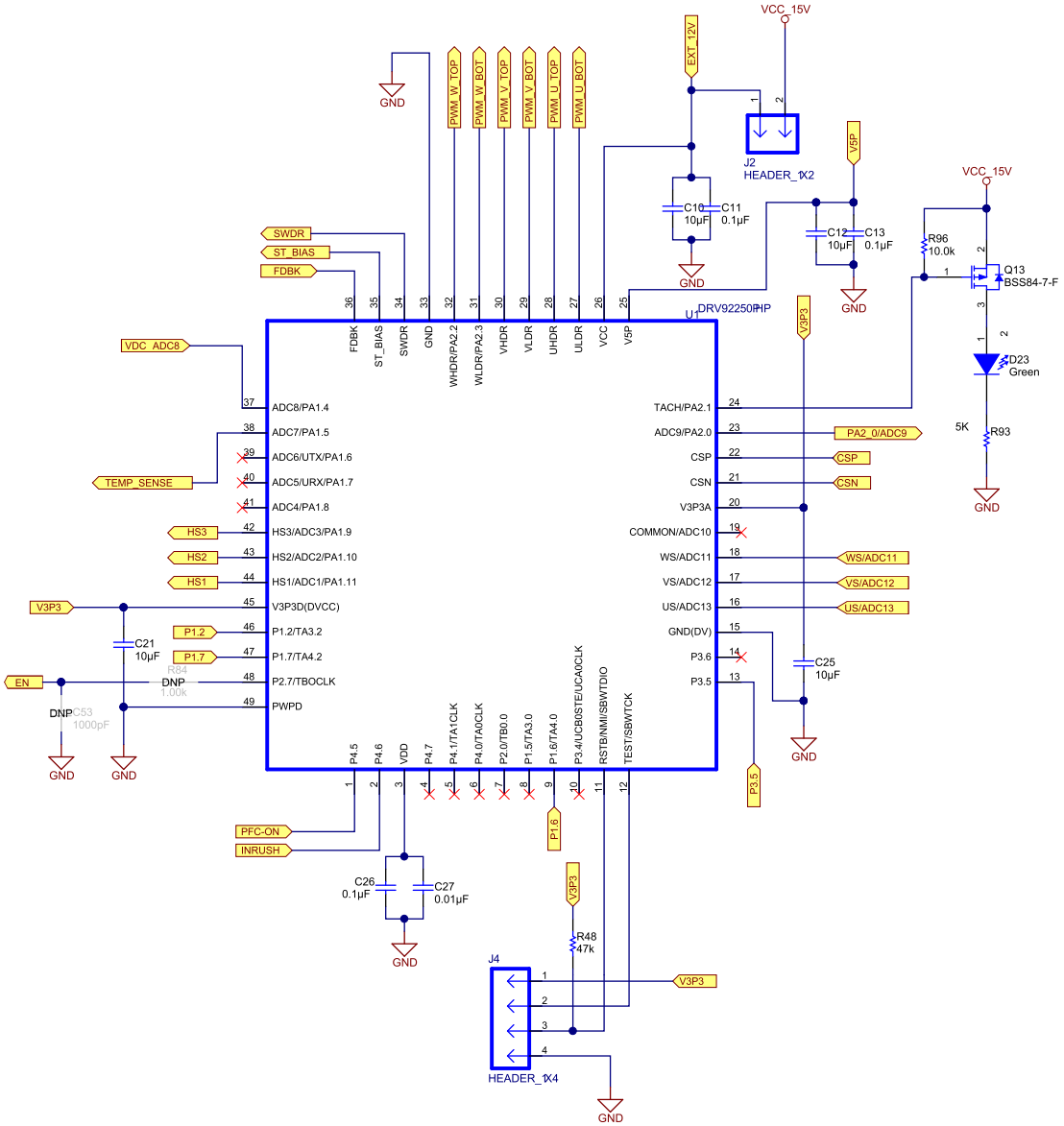

Figure 13. DRV92250 Schematic

6.2.9 Programming of DRV92250

Programmer kit: MSP-FET430UIF (MSP430 USB debugging interface)
Platform: CCStudio™ 5.5

The programmer tool has a 14-pin JTAG connector. The programming of the DRV92250 is done by means of 2-wire Spy-Bi-Wire. The four-pin connector between the programmer and the DRV92250 can be formed as shown in Figure 14.

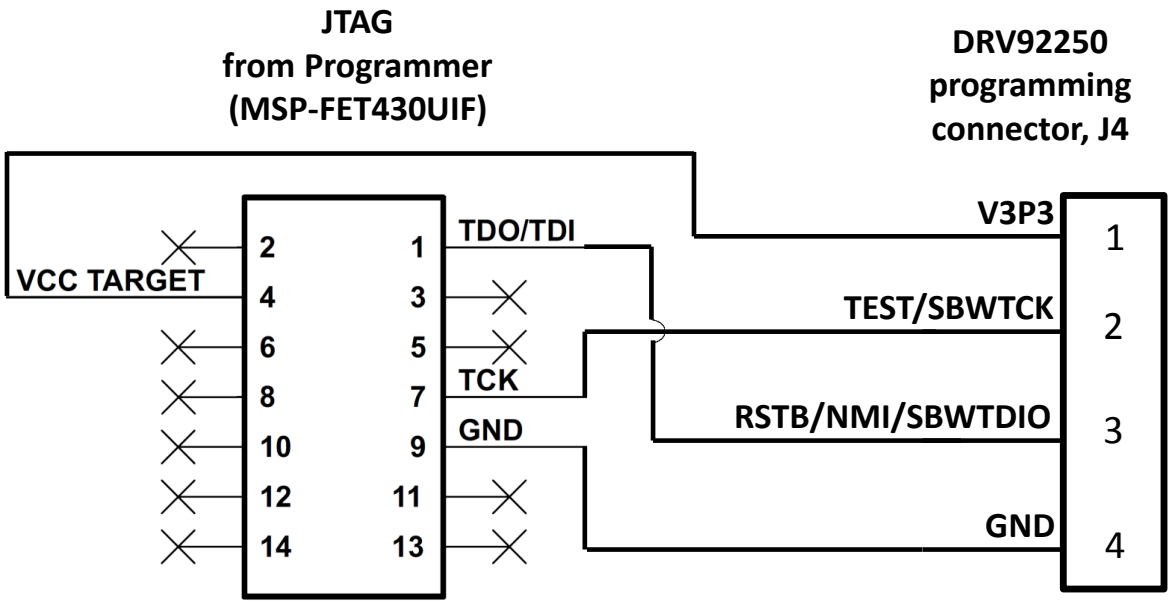

Figure 14. Programming Connector

J4 is the programming connector. The header J6 is used as the provision for external 12-V supply for programming the DRV92250. By default the external 12 V is connected to the board. If the jumper J2 is closed, the 15 V generated in the board will be connected to the DRV92250. Figure 15 shows the terminal connector J6 for external 12-V programming supply. Figure 16 shows the image of board during programming.

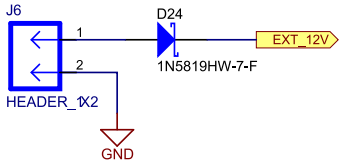

Figure 15. External Power Supply for Programming

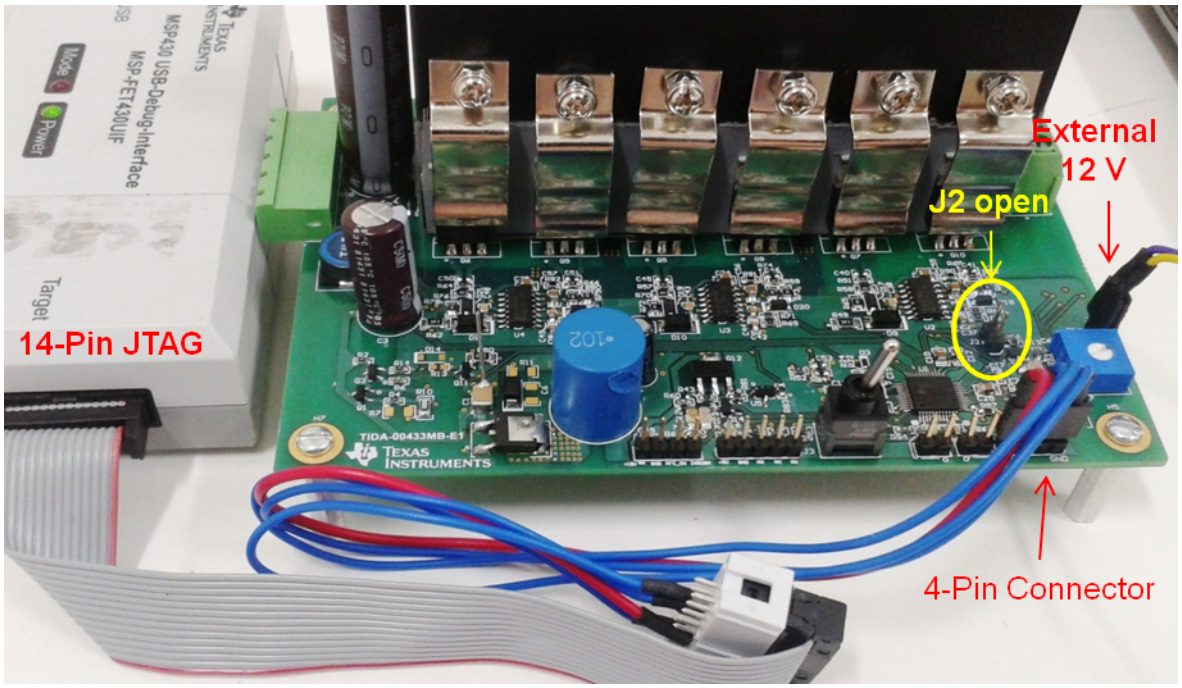

Figure 16. Programming of DRV92250

Follow these steps to program the DRV92250:

1. Switch off the board. Wait for the DC bus voltage to ramp down to zero.
2. Remove or open the J2 connection.
3. Give an external 12 V to J6 with the correct polarity, and turn on the 12-V supply.
4. Connect the 4-pin programming connector.
5. Open Code Composer Studio. Build and debug the program to burn the code.

6.2.10 External Hall Sensor Interface

Figure 17 shows the connector J3 used to interface the Hall sensors from the motor to the board. The 5.35 V generated by the DRV92250 is used as the power supply for the Hall sensor. Usually, the Hall sensors have an open drain or open collector configuration. R27, R28, and R29 are used as the pull up resistors. R87, R88, and R89 are used as voltage divider so that the voltage to pins HS1, HS2, and HS3 can be properly scaled. Here, the scaling is done to make the logic high voltage to 3.3 V. R30, R31, and R35 along with C18, C19, and C20 form noise filtering at the Hall sensor input.

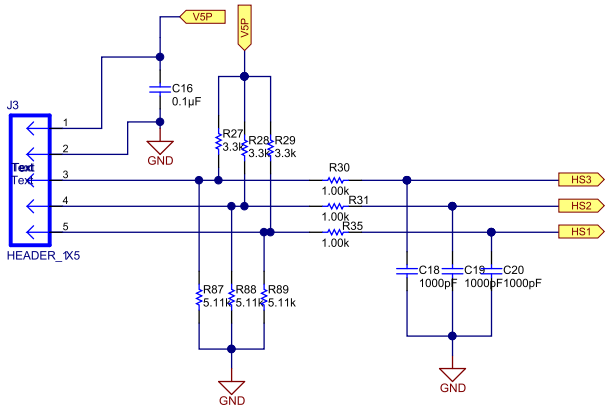

Figure 17. Hall Sensor Connector

NOTE: The Hall sensor connection should match with the winding for proper operation of the BLDC motor. The winding phases U, V, and W are named as MU, MV, and MW and the Hall sensors as HU, HV, and HW in the inverter board. The Hall sensors inside the motor are placed such that the connection matches as per Table 5. To change the direction of rotation, two phase winding and the corresponding Hall sensors should be interchanged.

Table 5. Hall Sensor and Motor Winding Connection Matching

HALL SENSOR SIGNAL	HALL SENSOR	MATCHING WINDING PHASE	COMMENTS
HS1	HU	MU	Hall sensor HU placed at the start of the U phase winding
HS2	HV	MV	Hall sensor HV placed at the start of the V phase winding
HS3	HW	MW	Hall sensor HW placed at the start of the W phase winding

6.2.11 Motor Winding Voltage Feedback

The motor winding voltages are fed back to the controller for sensorless control implementation. The winding voltages are switching at a maximum voltage equal to the DC bus voltage. Therefore, proper scaling network is required before feeding to the controller as shown in Figure 18.

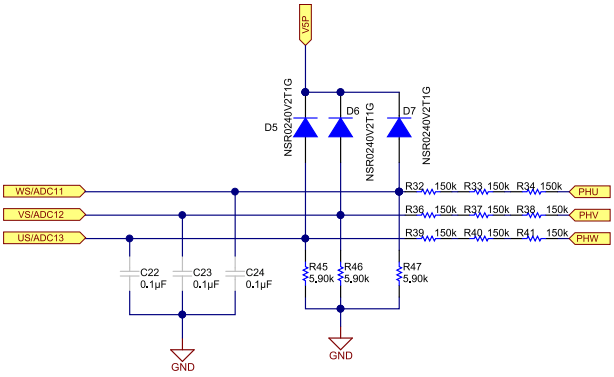

Figure 18. Motor Winding Voltage Sensing

The maximum voltages that can be fed to the US, VS, and WS terminals of the DRV92250 are 5.35 V. The maximum voltage at the DC bus could be approximately 390 V when fed from an active power factor correction front end.

Therefore, considering a one-phase voltage sensing network,

$$V_{ADC} = V_M \times \frac{R47}{R32 + R33 + R34 + R47} \tag{53}$$

$$V_M = V_{ADC} \times \frac{R32 + R33 + R34 + R47}{R47}$$

$$V_M = 5.35 \times \frac{150 + 150 + 150 + 5.9}{5.9} = 413 \text{ V}$$

Therefore, the resistive divider ensure that with the maximum motor winding voltage that can be sensed is more than the required 390 V with a small margin.

These ADC terminals have internal voltage divider comprising of 100k resistor and 150k resistor to further scale it down to the ADC measurable voltage of less than 2.4 V. The terminals US, VS, and WS have internal programmable pull-down resistors of 20k and 5k. Therefore, the user can utilize these resistors also instead of R45, R46, and R47.

6.2.12 DC Bus Voltage Feedback

Figure 19 shows the DC bus voltage sensing circuit. The resistors R19, R20, R21, and R24 are selected to a high value to reduce the stand by current of the board. D3 is used as a protection clamp diode.

The resistors R19, R20, and R21 are designed to bring down the voltage across R24 to a maximum of 5.35 V when the DC bus voltage is approximately 390 V. The 150k and 100k network further reduce the voltage to less than 2.4 V, which is the maximum measurable voltage of the ADC.

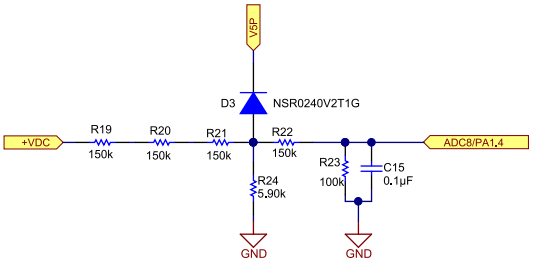

Figure 19. DC Bus Voltage Sensing

6.2.13 Current Sense Amplifier and Overcurrent Protection Using DRV92250

The DRV92250 includes robust motor current sensing and overcurrent detection capability. Current to voltage conversion is achieved on the PCB using a current-sense resistor connected to ground. A fully differential current sense amplifier on-chip is directly connected across the current-sense resistor at pins CSP and CSN. Excellent common-mode and ground bounce rejection is achieved due to the fully differential configuration. The amplifier has register programmable voltage gains of 4V/V and 10V/V controlled by register bit ISnsHiGain. In addition to amplifying the incoming signal, the differential current-sense amplifier also converts it to single-ended. This single-ended signal is directly applied to the on-board analog-to-digital converter (ADC) and the digital output is fed to the microcontroller for accurate motor current control.

Overcurrent detection can be performed using either the internal voltage comparator or an external discrete voltage comparator. This is controlled by register bit OCFromGPIO. When OCFromGPIO=0 (default state), an internal overcurrent comparator is used. When OCFromGPIO=1, an external overcurrent comparator can be used. This reference design uses the internal voltage comparator.

When overcurrent detection is implemented internally (OCFromGPIO=0), the on-chip voltage comparator is connected directly to the positive terminal of the external current-sense resistor. The reference comparison threshold voltage for the overcurrent comparator is supplied by the integrated 8-bit DAC. Whenever the comparator threshold is exceeded, an overcurrent event is flagged if the leading edge blanking interval is exceeded. The leading-edge blanking interval provides protection against false detection due to current over-shoot or ringing. It can be programmed using serial register control bits CURLIM[1:0].

When overcurrent detection is implemented externally, the output of the external signal must be routed to multi-function pin ADC8/PA1.4 and this pin must be configured as a digital input (G1p4[WR,RD]=01). The expected swing out of the external comparator is 0 to 5 V. For external OC detection, the on-chip leading edge blanking circuitry is bypassed as well.

When an overcurrent event is detected, it sets the hardware overcurrent limit (HOC) bit in the serial register and asserts an interrupt for the MCU. At the same time, pre-drivers are disabled. The number of pre-drivers disabled depends on the state of a few serial register control bits. Specifically, when control bit TRKHSPWM=0 (the default state), all six pre-drivers are disabled when an overcurrent is detected. However, if TRKHSPWM=1, only the three high side pre-drivers are disabled if control bit HSDPWM is also equal to a 1. If TRKHSPWM=1and HSDPWM=0, only the three low-side pre-drivers are disabled in the event of an overcurrent.

Once disabled, the pre-drivers resume normal operation as soon as the motor current falls below the overcurrent threshold if the control bit PreDrvHLD=0 (a feature known as pulse-skipping). Conversely, when PreDrvHLD=1, the pre-drivers remain powered down until PreDrvHLD is reset to 0. However, in either case, once the control bit HOC is set, it can only be reset by the MCU reading back the state of register Misc1.

The overcurrent comparator provides programmable hysteresis for excellent performance even in noisy environments. The amount of hysteresis is controlled by the register bits IcompHys[1:0] bits. Additional protection against false comparator trips is provided by the programmable leading edge blanking feature for the current sense signal.

6.2.13.1 Setting Current Limit in Software

The DRV92250 has an integrated 8-bit DAC with an output swing from 0 to 1.2 V. The DAC is used to set the current-limit threshold for the overcurrent comparator. The DAC digital input can be set directly by programming the serial port register DACB:

drv922xxSpiWrite(ASSI_DACB_WRITE, 0x1E);

The calculation is shown as follows:

- R_{SENSE} = The sense resistor value
- I_{OC} = Required overcurrent limit

For the 8-bit DAC the maximum hex value is 0xFF (255 Decimal) and the corresponding DAC output voltage is 1.2 V.

Therefore, the equivalent decimal value to be stored in the DACB registers,

$$DACB_{dec} = \left(\frac{I_{OC} \times R_{SENSE}}{1.2} \right) \times 255 \tag{54}$$

Approximate $DACB_{dec}$ to the nearest integer value, convert into the equivalent hex, and write in the DACB register. For example: In the reference design, R_{SENSE} = 20 mΩ

To set the current limit at 7 A, I_{OC} = 7 A, substituting in Equation 54:

$$DACB_{dec} = \left(\frac{7 \times 0.02}{1.2} \right) \times 255 = 29.75 \tag{55}$$

The nearest integer value is 30. The equivalent hex value of 30_D is $1E_H$. Therefore, the value to be stored in DACB register is 0x1E.

6.2.14 Heat Sink Temperature Sensor

Figure 20 shows the temperature sensor circuit used to measure the heat sink temperature. The LMT84 is an analog output temperature sensor. The temperature sensing element is comprised of a simple base emitter junction that is forward biased by a current source. The temperature sensing element is then buffered by an amplifier and provided to the OUT pin. The amplifier has a simple push-pull output stage, thus providing a low-impedance output source. The average output sensor gain is –5.5 mV/0C.

Although the LMT84 is very linear, its response does have a slight umbrella parabolic shape. The output voltages at different temperatures are given in the datasheet of LMT84 in tabular form. For an even less accurate linear approximation, a line can easily be calculated over the desired temperature range using the two-point equation of a line. Using this method of linear approximation, the transfer function can be approximated for one or more temperature ranges of interest.

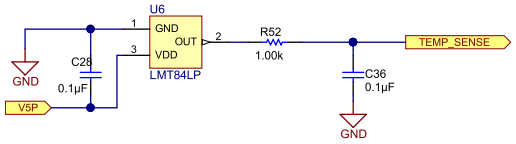

Figure 20. Heat Sink Temperature Sensor

6.2.15 Features and Controls Available in Board

6.2.15.1 Safe Turn-Off Circuit for DRV92250

To enable the DRV92250 to turn off with the proper power sequence, a safe turn off circuit as shown in Figure 21 is implemented.

The shunt regulator TL431 is used in this reference design, to implement this feature. The reference voltage, V_{REF} = 2.5 V

When the voltage across R83 reaches 2.5 V, Q12 will turn on and the generated power supply voltage 15 V (VCC) will be fed to the DRV92250 (VCC_15V).

From Figure 21,

$$V_{REF} = V_{DC} \times \left(\frac{R83}{R42 + R44 + R82 + R83} \right) \quad (56)$$

The DC bus voltage at which the transistor Q2 will turn ON can be found out using Equation 57:

$$V_{DC} = V_{REF} \times \left(\frac{R42 + R44 + R82 + R83}{R83} \right) \quad (57)$$

Substituting the values, V_{DC} = 60 V

Therefore, when the DC voltage goes down to less than 60 V, this circuit will turn off the 15-V supply going to the DRV92250 immediately, which enables proper power down sequence of the DRV92250.

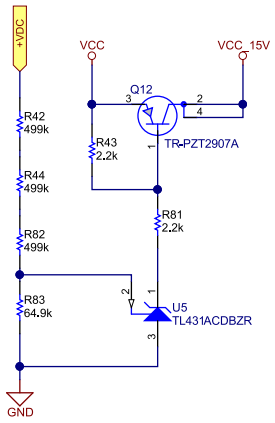

Figure 21. Safe Turn-Off Circuit for DRV92250

6.2.15.2 Speed Control of Motor

The speed control is done using a potentiometer (POT) and the POT voltage is fed to ADC9 of the DRV92250. The circuit is shown in Figure 22. The POT is supplied from the 5.35 V generated by the DRV92250. A 20k POT is used in the reference design. The resistor R16 is used to limit the maximum voltage across the POT to 2.4 V, which is the maximum measurable voltage of the ADC.

The maximum POT voltage is

$$V_{POT,MAX} = 5.35 \times \frac{R17}{R16 + R17} \tag{58}$$

$$V_{POT,MAX} = 5.35 \times \frac{20}{24.9 + 20} = 2.38 \text{ V}$$

The resistor R18 is used to ensure that the speed control reference is zero if the POT terminal is open.

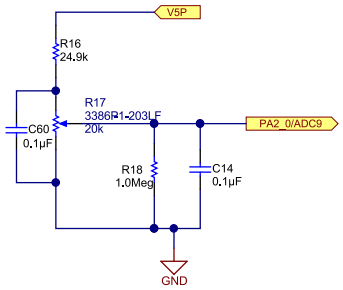

Figure 22. Potentiometer Connection for Speed Control

6.2.15.3 Digital Inputs

The reference design has the provision for two digital inputs, fed to P1.6 and P1.7, which the user can configure based on the application requirement. The user can configure these inputs for different features like direction control, maximum speed options, and so on.

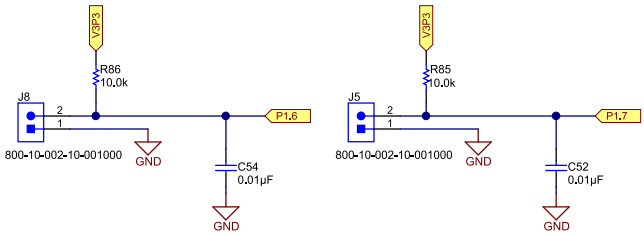

Figure 23. Digital Inputs to DRV92250

6.2.15.4 Software Start Control

The reference design uses a software start control feature using the toggle switch S1 as shown in Figure 24. This switch acts as the software trigger and thus starts the inverter operation.

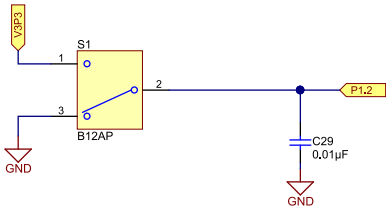

Figure 24. Digital Inputs to Start DRV92250 Execution

6.2.15.5 Control of PFC Board

Figure 25 shows the connector J9 for interfacing the active power factor correction (PFC) front end to the inverter board. The inverter board provides a 15-V supply to the PFC board. PFC_ON is the digital output from the DRV92250 to trigger ON the PFC. The digital output named INRUSH is also fed to the PFC board.

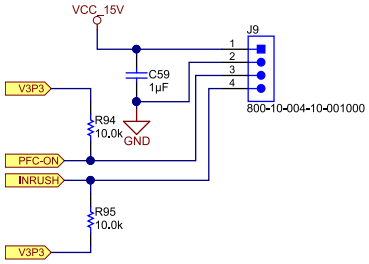

Figure 25. Interfacing Active PFC Front End to Inverter Board

7 Getting Started Firmware

Refer to the document *Hall Sensor-Based Trapezoidal Control of 230-V, 900-W Mains Powered BLDC Motor Drive Using DRV92250* (TIDCAI3).

8 Test Results

Figure 26 and Figure 27 show the top view of the power supply board and the three-phase inverter board.

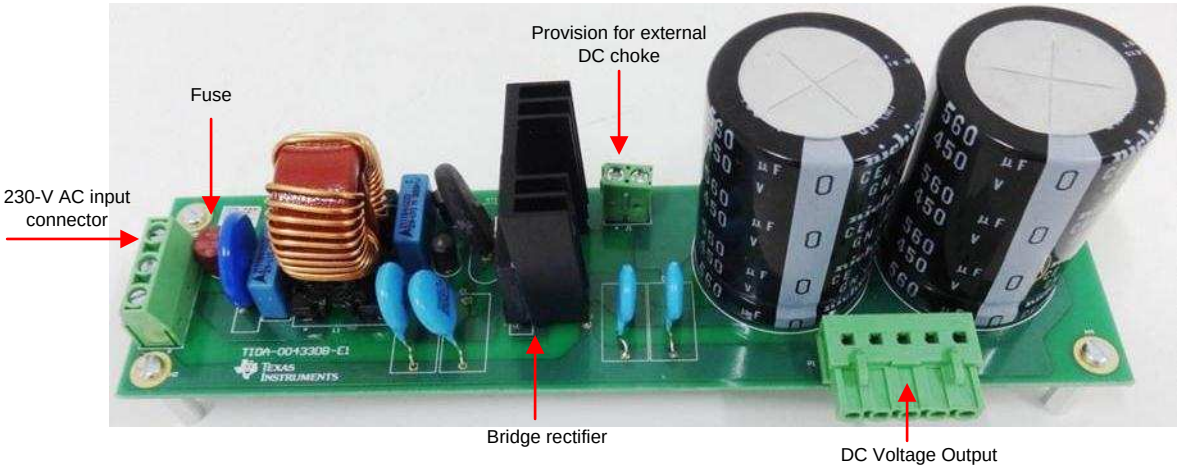

Figure 26. Assembled AC-DC Power Supply

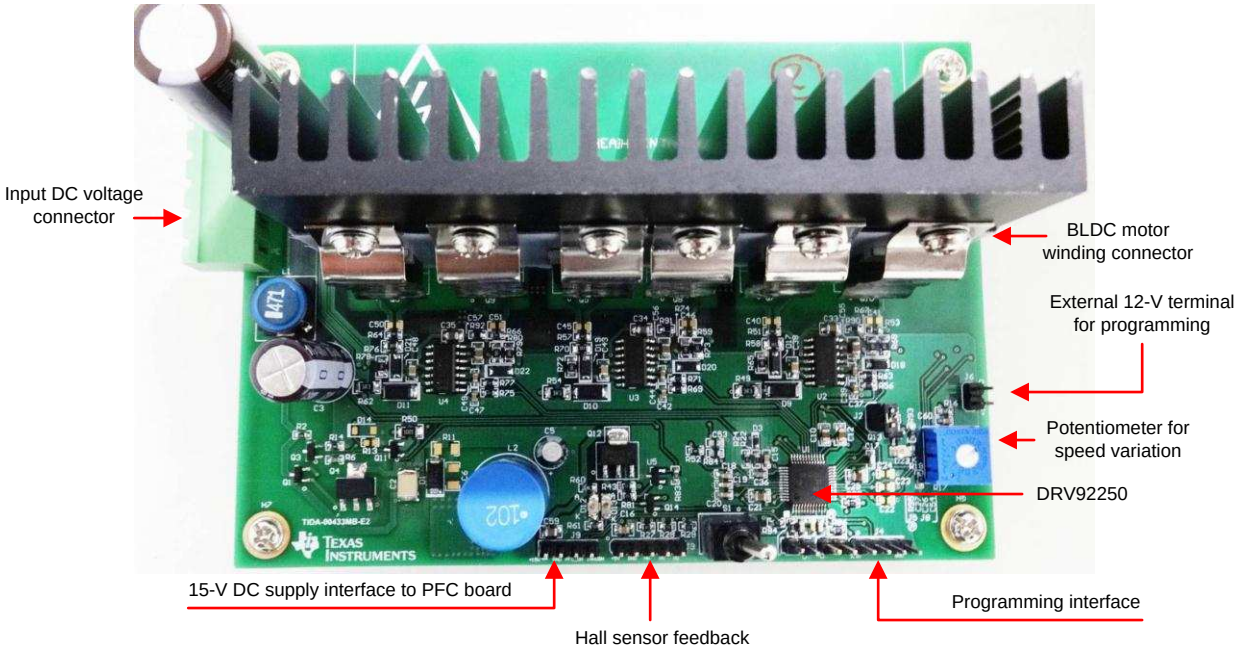

Figure 27. Assembled Inverter Board

8.1 Functional Tests of Buck Regulator Using DRV92250

The operating voltage range of the buck converter depends on the bias resistor connected from the positive DC bus to the ST_BIAS pin of the DRV92250. With a 524-kΩ resistor, when the input voltage is more than approximately 75 V, the buck converter will start building up and regulate the output voltage. The buck converter is tested up to 400 V. The buck regulator inside the DRV92250 has a hysteresis controller and hence the switching frequency is not constant with the input DC variation or the output load variation. The buck regulator performance can be optimized using the configuration registers inside the DRV92250. The reference design uses the configuration as per Table 6 for the testing of buck regulator. Figure 28 shows the buck converter output waveforms when tested at an input DC voltage of 100 V.

Table 6. Buck Controller Register Configuration in DRV92250

REGISTER BIT	SET BINARY VALUE	REMARKS
DcDeGlitch	1	Minimum pulse width = 1 µs
HYSDCDC	10	Hysteresis band = 30 mV
DcDcWidth	00	Maximum duty cycle = 42%

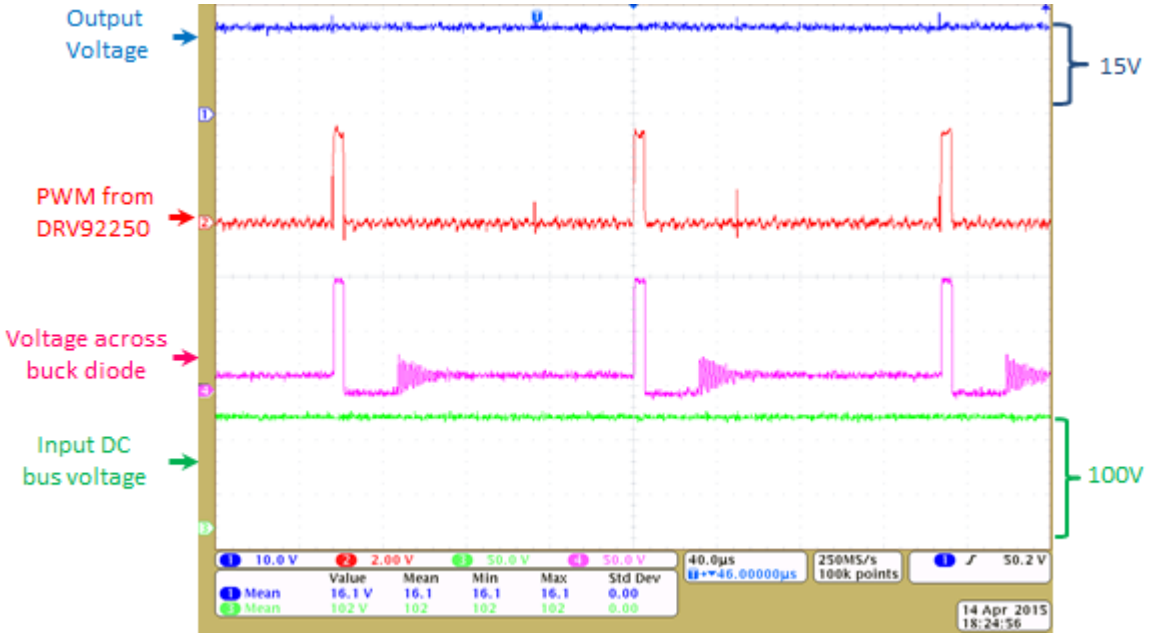

Figure 28. Test Results of Buck Converter at 100-V DC

From Figure 28:

- Time period of the switching pulse (SWDR), T = 117 µs
- ON time of SWDR, T_{ON} = 5.2 µs
- Switching frequency of buck regulator, f_{SW} = 8.5 kHz
- Operating duty cycle = 0.044

The buck regulator is tested up to an input DC voltage of 390 V and the test results are shown in Figure 29.

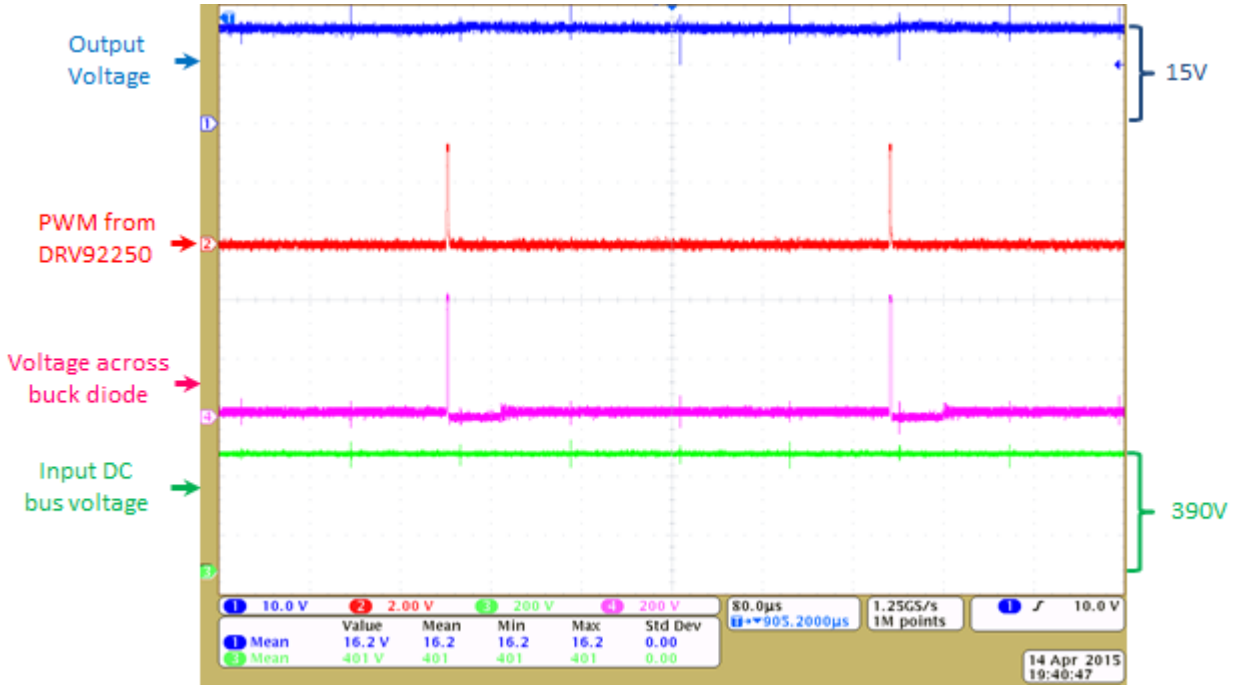

Figure 29. Test Results at 390-V DC

From Figure 29:

- Time period, T = 387 µs
- T_{ON} = 2 µs
- f_{SW} = 2.58 kHz
- Duty cycle = 0.005

Figure 30 shows the start-up of the buck regulator. The test result shows that when the input DC voltage (V_{IN}) is more than 75 V (approximately), the DRV92250 starts generating the PWM pulses at SWDR pin.

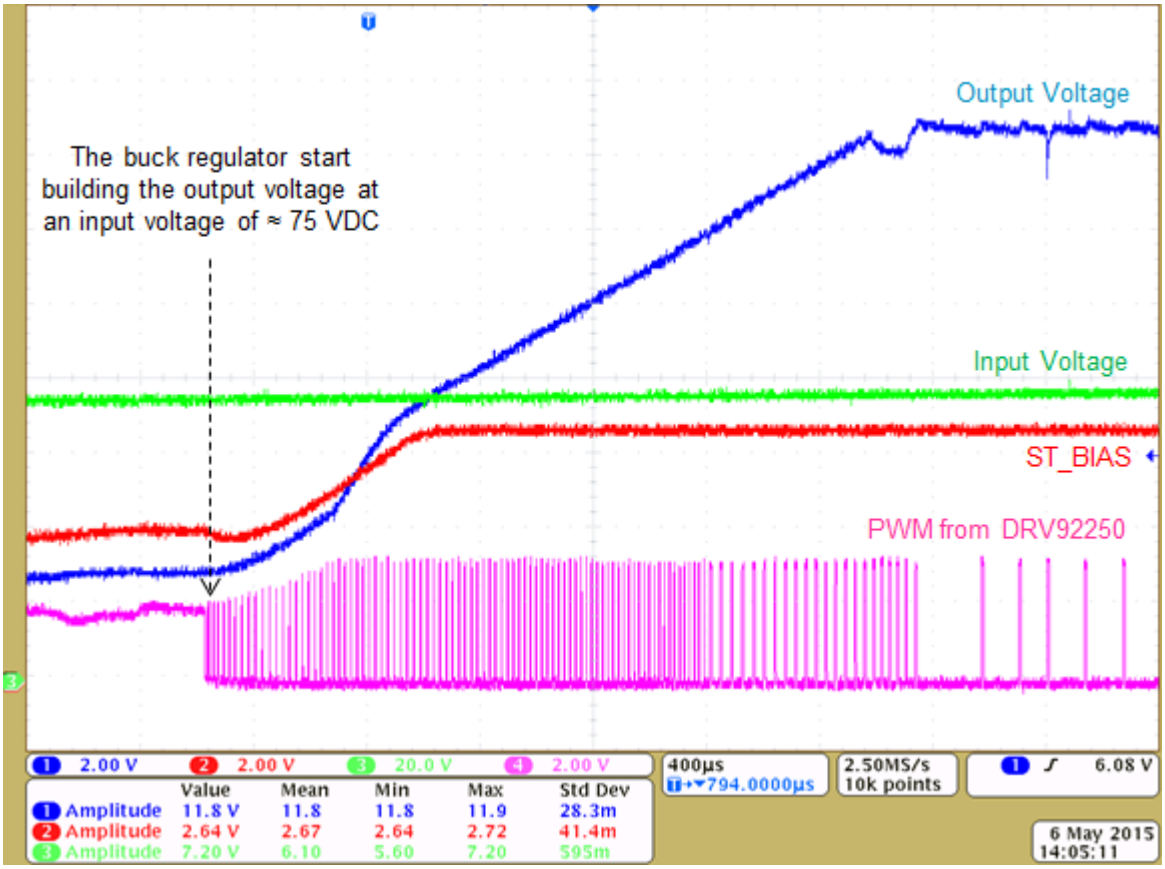

Figure 30. Start-up of Buck Converter and Voltage Build-up

Figure 31 shows the voltage ripple in the 15-V output at 325-V DC input. The peak-to-peak ripple voltage present at the 15-V output is approximately 388 mV (for 30-mV hysteresis control).

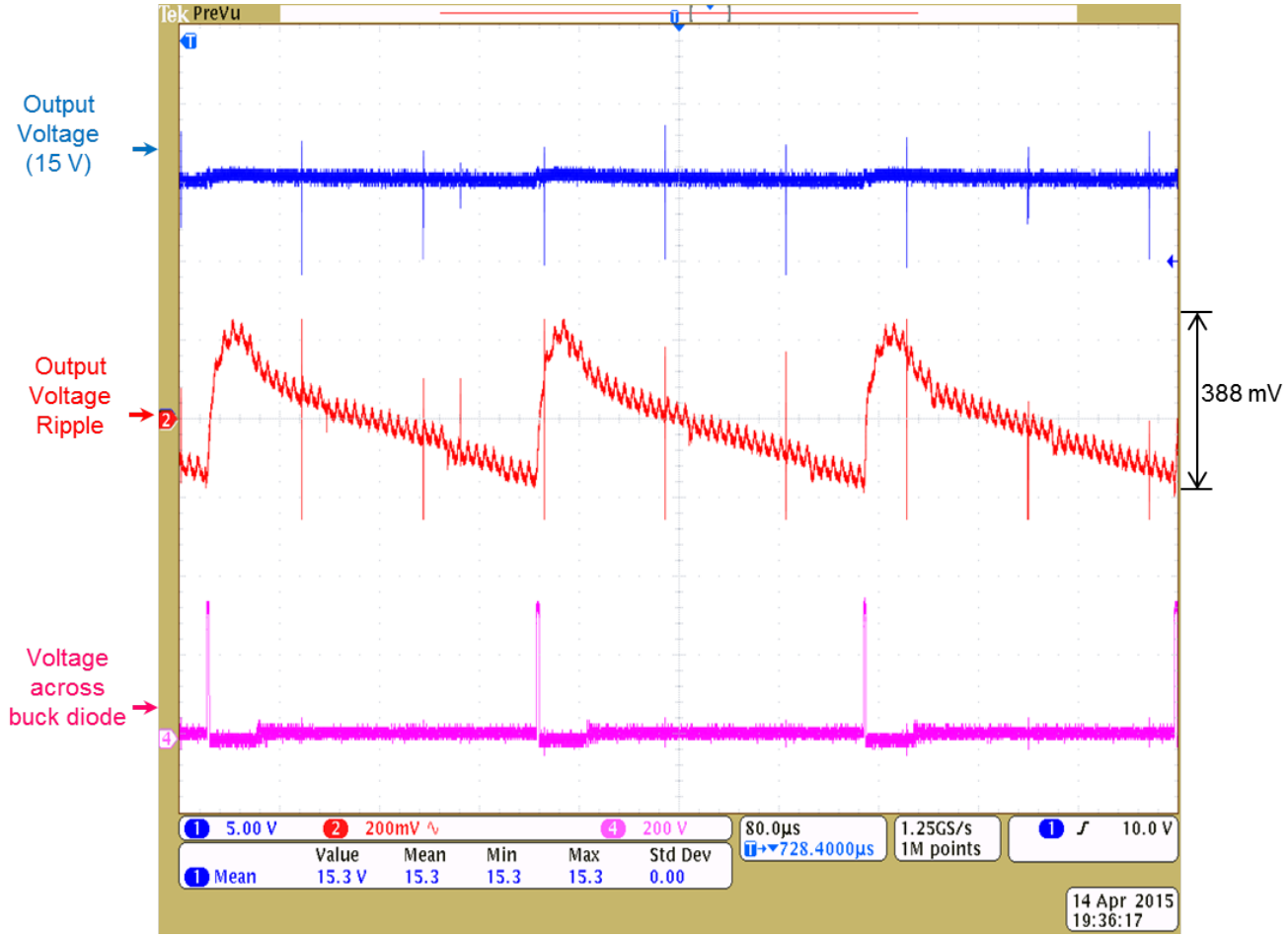

Figure 31. Ripple Voltage at 15-V Supply

8.2 Functional Tests of the DRV92250 Internal Voltage Regulator

The VCC of the DRV92250 in this reference design is 15 V. The on-chip voltage regulators of the DRV92250 generates internal analog supply voltage 5 V, external analog supply voltage 5.35 V from the 15 V. The internal linear regulators also generate 3.3 V and 1.9 V.

Figure 32 shows the reference voltage outputs of DRV92250. The regulated 5.35 V and the ripple are shown in Figure 33.

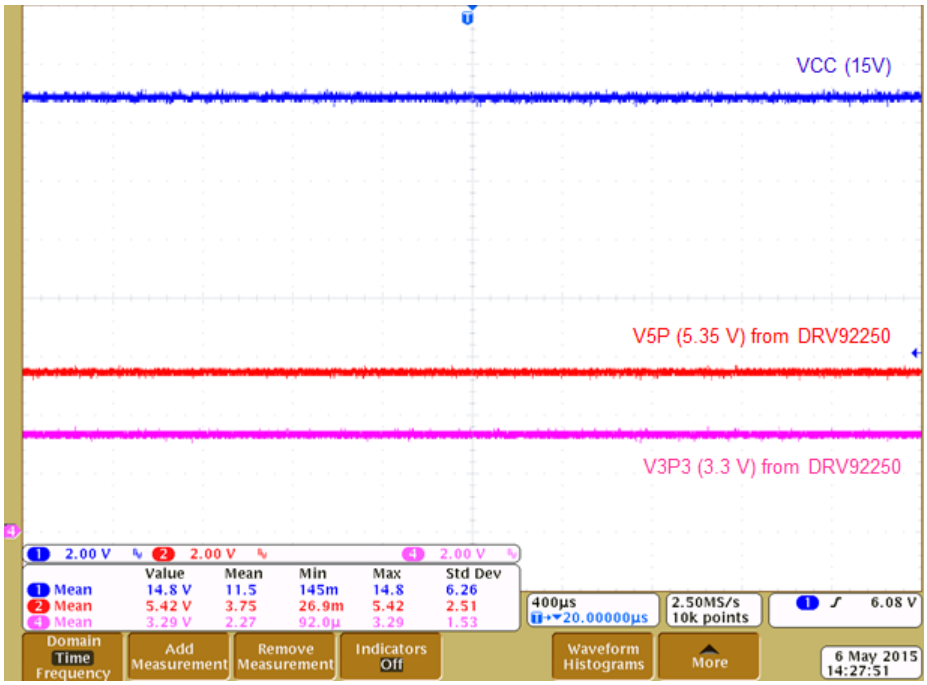

Figure 32. DRV92250 Voltage Regulator Output

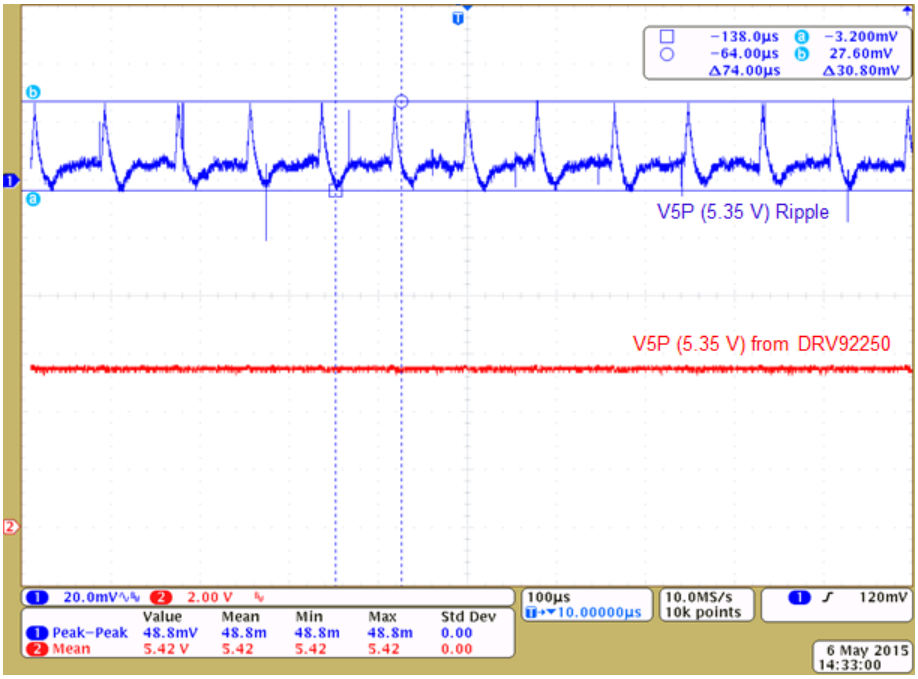

Figure 33. Voltage Ripple at Regulated 5.35 V From DRV92250

8.3 Functional Tests of IGBT Gate Driver UCC27714

Figure 34 shows the PMM input to the UCC27714, which is fed from the DRV92250. In BLDC unipolar trapezoidal control, only the high-side is modulated at the PWM frequency (10 kHz in this design) in the 120° ON period. The low side is continuously ON for 120°.

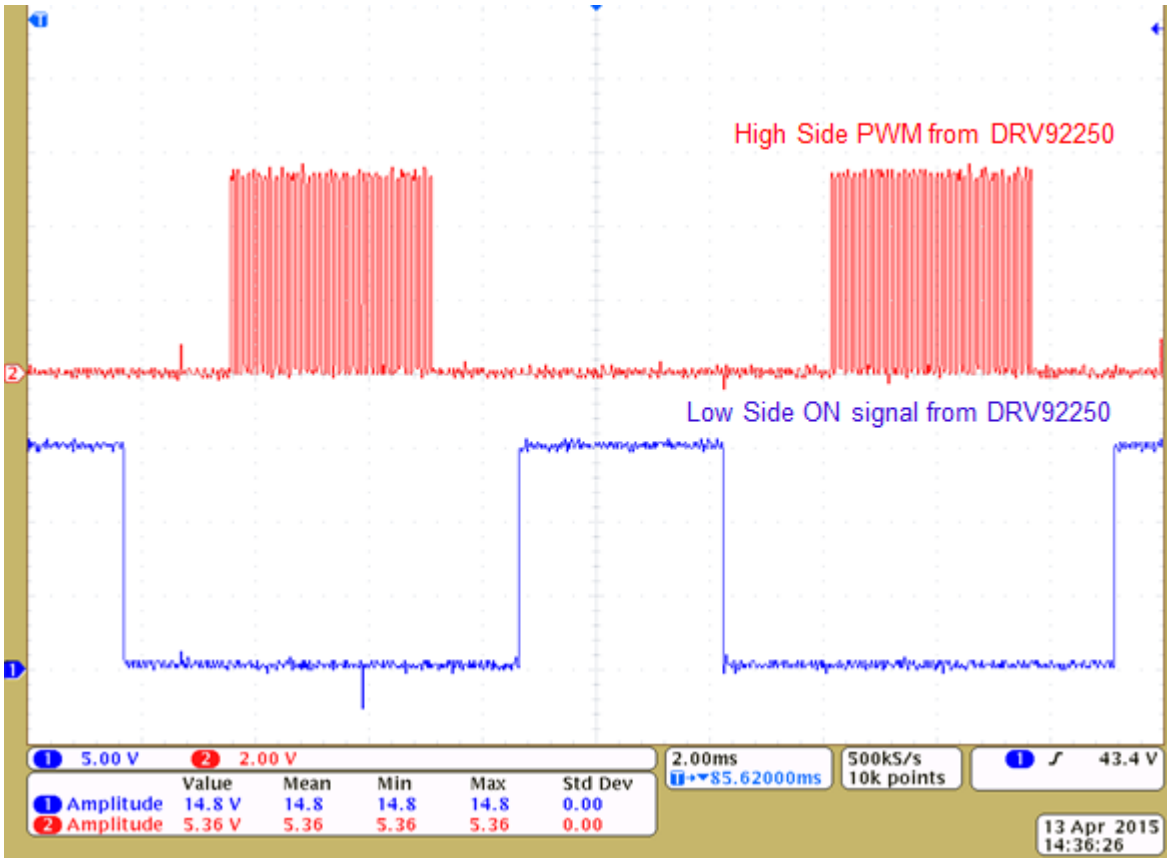

Figure 34. High-Side and Low-Side 120° Unipolar PWM Input to UCC27714 From DRV92250

Figure 35 shows the low-side signal input and the corresponding low-side output of one UCC27714. The supply voltage for the low-side pre-driver of the DRV92250 is VCC, which is 15 V. That means the low-side PWM output from the DRV92250 will swing between ground and 15 V. The low-side gate output from the UCC27714 swings between ground and VCC of the UCC27714.

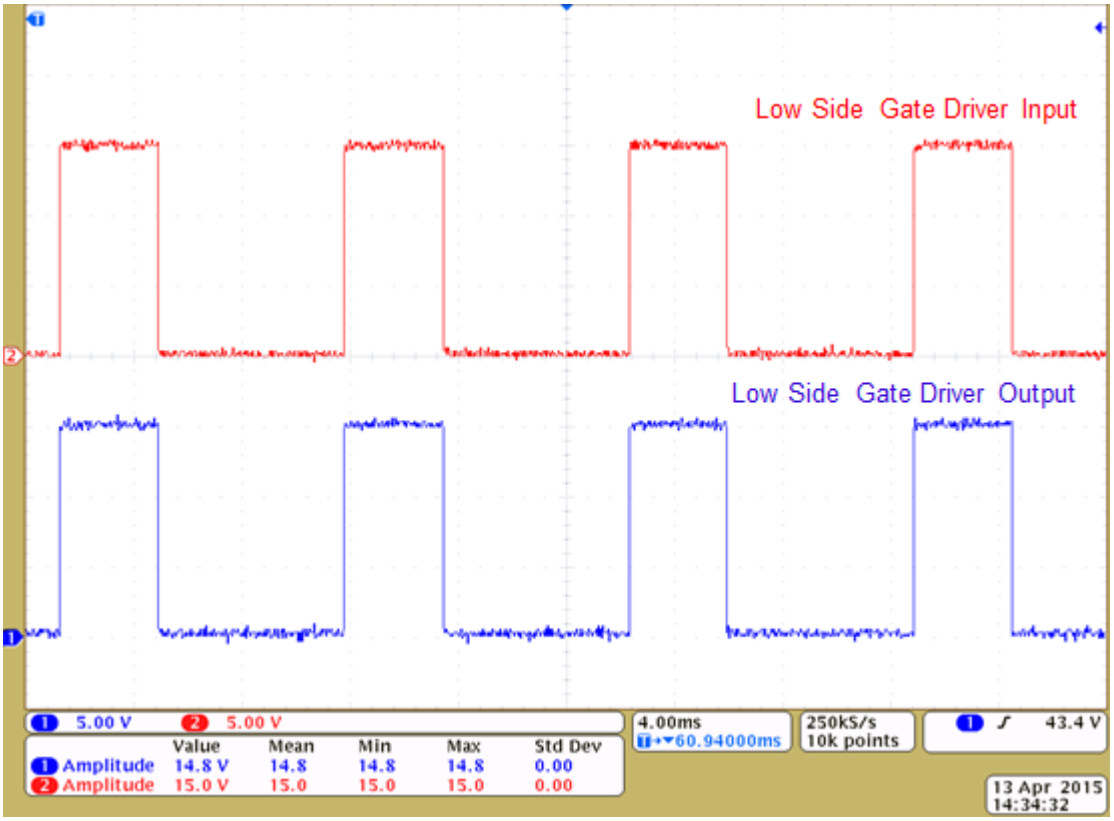

Figure 35. Low-Side PWM Input and Output of UCC27714

Figure 36 shows the high-side signal input to UCC27714, the corresponding high-side output of UCC27714 measured across the gate to emitter (V_{GE}) of the IGBT and the corresponding phase voltage measured with respect to the board ground (DC minus). The supply voltage for the high-side pre-driver of the DRV92250 is V5P, which is 5.35 V. That means the high-side PWM output from the DRV92250 will swing between ground and 5.35 V. The gate-to-emitter voltage is equal to VDD of the UCC27714 minus the voltage drop across the bootstrap diode of the high side driver in the UCC27714. The waveforms reveal that the V_{GE} is approximately 14.4 V

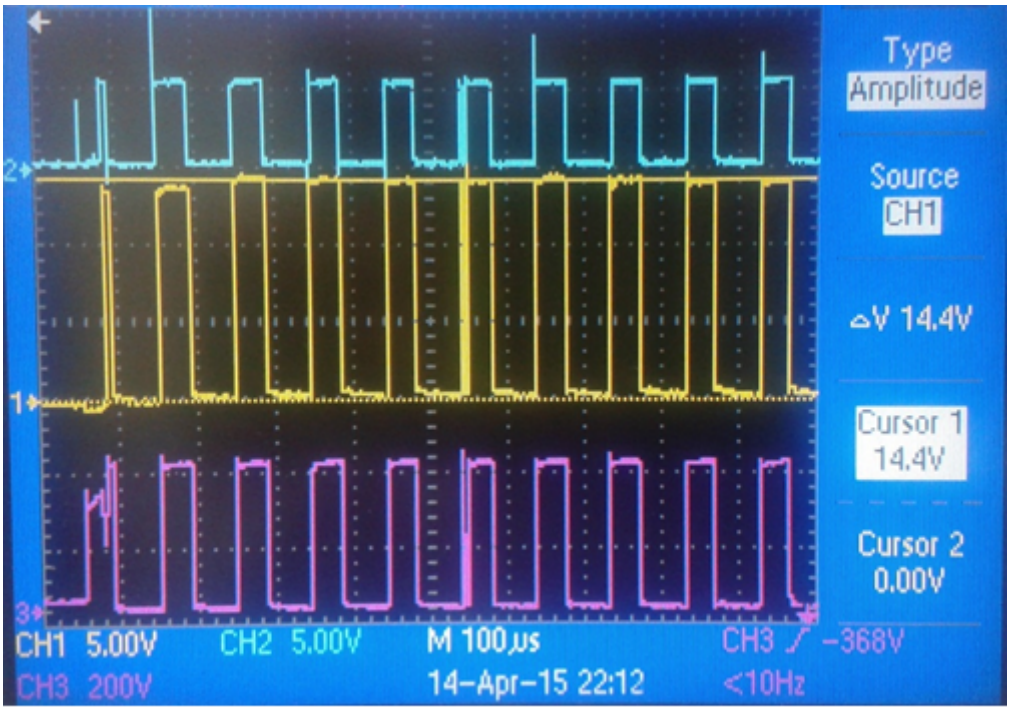

Figure 36. High-Side PWM Input and Output of UCC27714

8.4 Load Tests

The load test evaluates the performance of the three-phase inverter with load variation, load capacity, and thermal characteristics of the board. The inverter board is tested with a vacuum cleaner motor with the specification as given in Table 7.

Table 7. Specification of Motor Used for Load Test

RATED VOLTAGE (V)	RATED SPEED (RPM)	RATED POWER (W)	NOMINAL CURRENT (A)
300-V DC	18000	900	3.75

Figure 37. Load Test Setup

Figure 37 shows the load setup. The winding terminals of the motor are connected to the phase connections terminals MU, MV, and MW of the inverter board. The Hall sensor 5-pin connector is connected to the terminal J3 of the inverter board. Then, the inverter board and the AC-DC power supply boards are connected using the interface connector J1. The system is tested with DC input supply up to 390 V and also with AC supply from 195-V to 265-V AC with and without the PFC front end. The test results are covered in the subsequent sections.

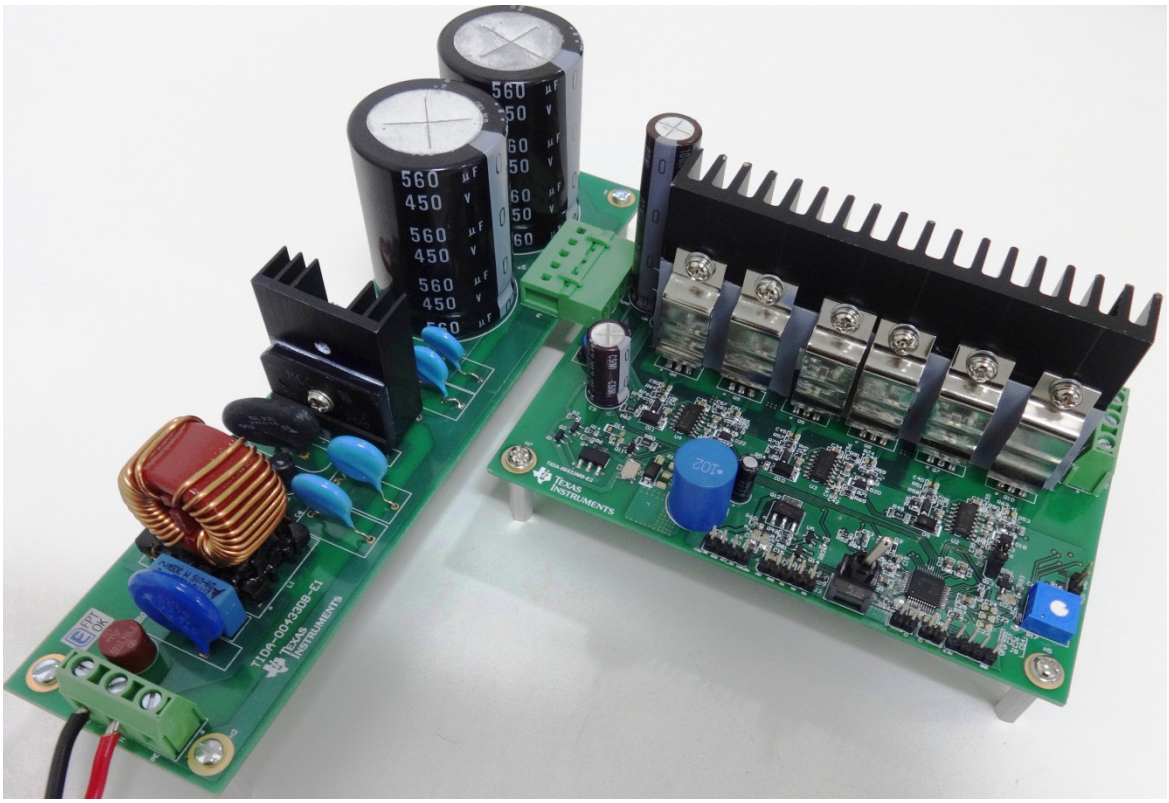

Figure 38. Assembled Power Stage With Power Connections

The load test is done at the rated power of 900 W. Table 8 list the test results at 900-W power.

Table 8. Load Test Results at 900 W

DC VOLTAGE (V)	DC CURRENT (A)	RMS WINDING CURRENT (A)	PEAK-TO-PEAK WINDING CURRENT (A)	MOTOR SPEED (RPM)	DC INPUT POWER (W)
324.4	2.76	3.76	15.4	15789	895.34

Figure 39 shows the motor winding current and winding voltage measured with respect to DC minus. The winding voltage is switching at 10 kHz. Figure 40 shows the thermal image of the inverter board at 900 W when operated from 325-V DC, with a heat sink having thermal resistance of 3°C/W. The heat sink temperature at this power level is 72.4°C and the DRV92250 temperature is 53.6°C.

NOTE: All the temperature mentioned in the test results are absolute temperature. All the tests are done at an ambient temperature of 25°C.

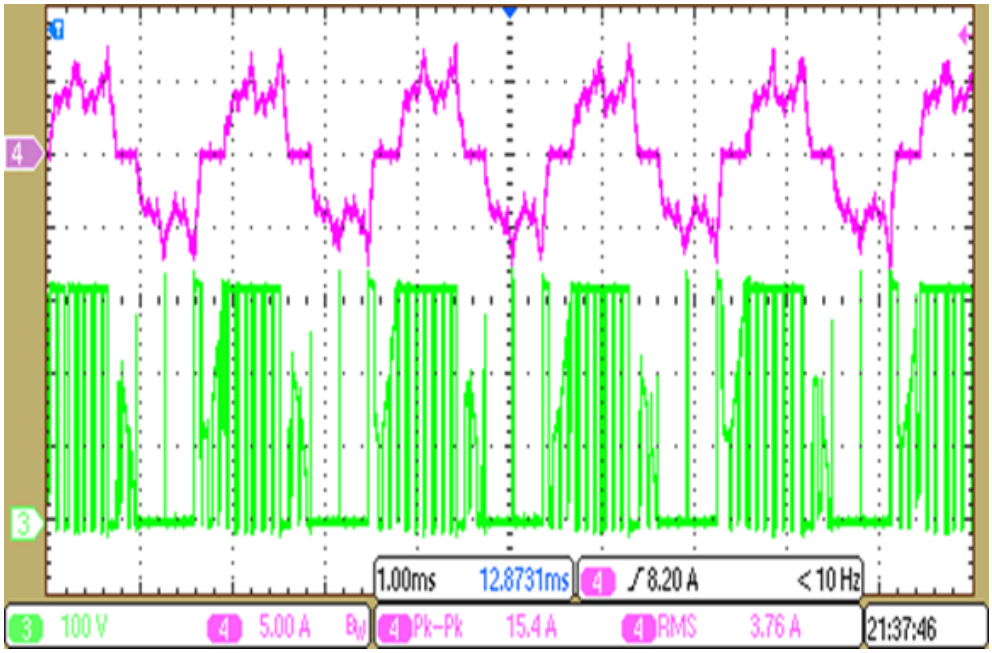

Figure 39. Load Test at 325-V DC, 900-W Input Power
Motor Winding Current and Winding Voltage Measured With Respect to DC Minus

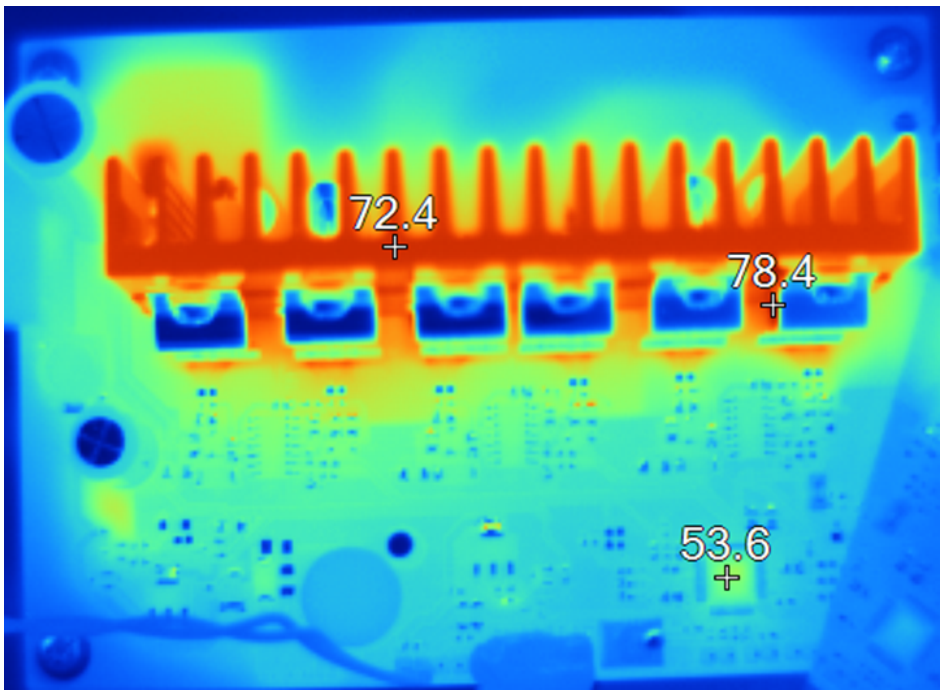

Figure 40. Thermal Image of Load Test at 325-V DC, 900-W Input Power

The load test is done with PFC front end as well. With PFC, the DC bus voltage is kept at 390 V and the load test is done up to 950-W input power. The test results are tabulated in Table 9.

Table 9. Load Test Results at 120% Overload

DC VOLTAGE (V)	DC CURRENT (A)	RMS WINDING CURRENT (A)	PEAK-TO-PEAK WINDING CURRENT (A)	MOTOR SPEED (RPM)	DC INPUT POWER (W)
390	2.435	3.92	15	16484	950

Figure 41 shows the motor winding current and winding voltage measured with respect to DC minus at the above test condition. Figure 42 shows the thermal image of the inverter board at 950 W when operated from 390-V DC. The heat sink temperature at this power level is 76.3°C and the DRV92250 temperature is 53.9°C.

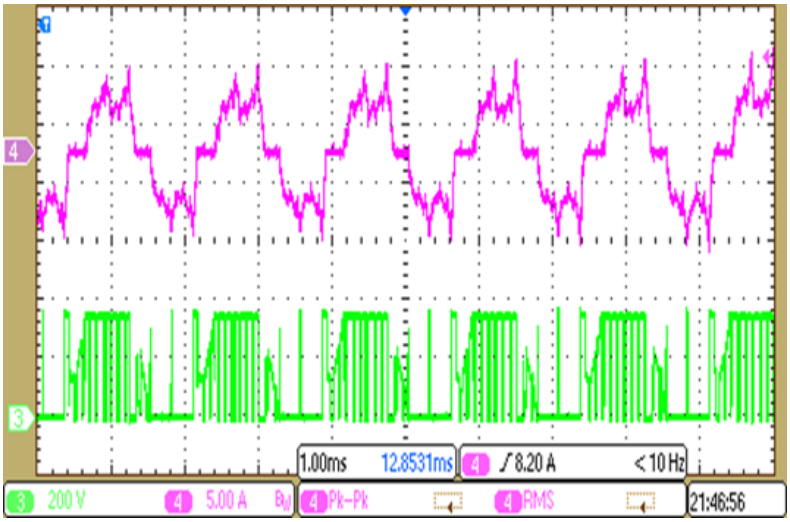

Figure 41. Load Test at 390-V DC, 950-W Input Power
Motor Winding Current and Winding Voltage Measured With Respect to DC Minus

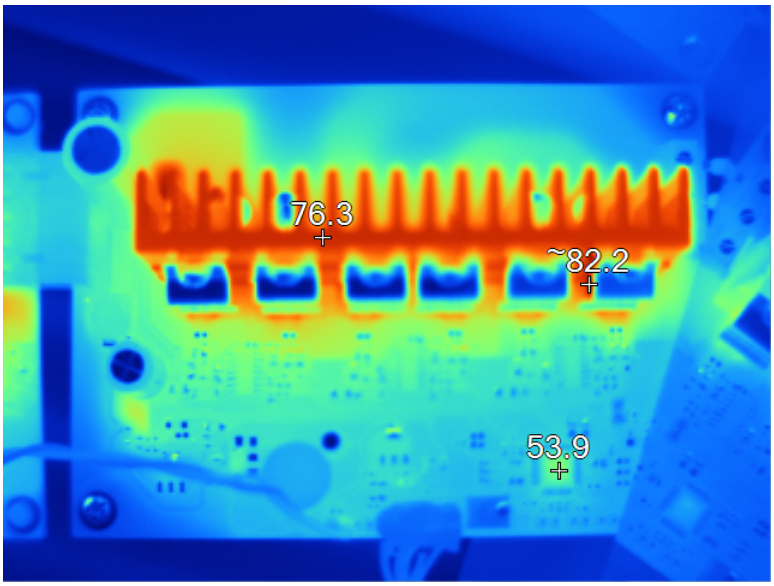

Figure 42. Thermal Image of Load Test at 390-V DC, 950-W Input Power

8.5 Test Results of the AC-DC Power Stage

The testing of the complete system is done at AC input voltage from 195-V to 265-V AC. When energized using trapezoidal control, the BLDC motor will draw a high ripple current from the DC bus capacitor. The DC bus ripple current could be as high as two times the average DC bus current because of the commutation in BLDC motor. The peak winding current of the motor will get reflected at the DC bus. Figure 39 shows that the peak winding current is above 7 A.

Figure 43 shows the ripple current after the bulk capacitor present in the power supply board. The current is measured at the interface connector. The waveform shows the ripple current at 870-W input power when tested with a 230-V AC input supply. The peak ripple current is 3.52 A and the average DC bus current is 2.67 A. The reduction in ripple current (compared to 7 A), is due to the filtering of the decoupling capacitors present in each of the inverter leg and the 100-µF capacitor present at the input of the inverter board.

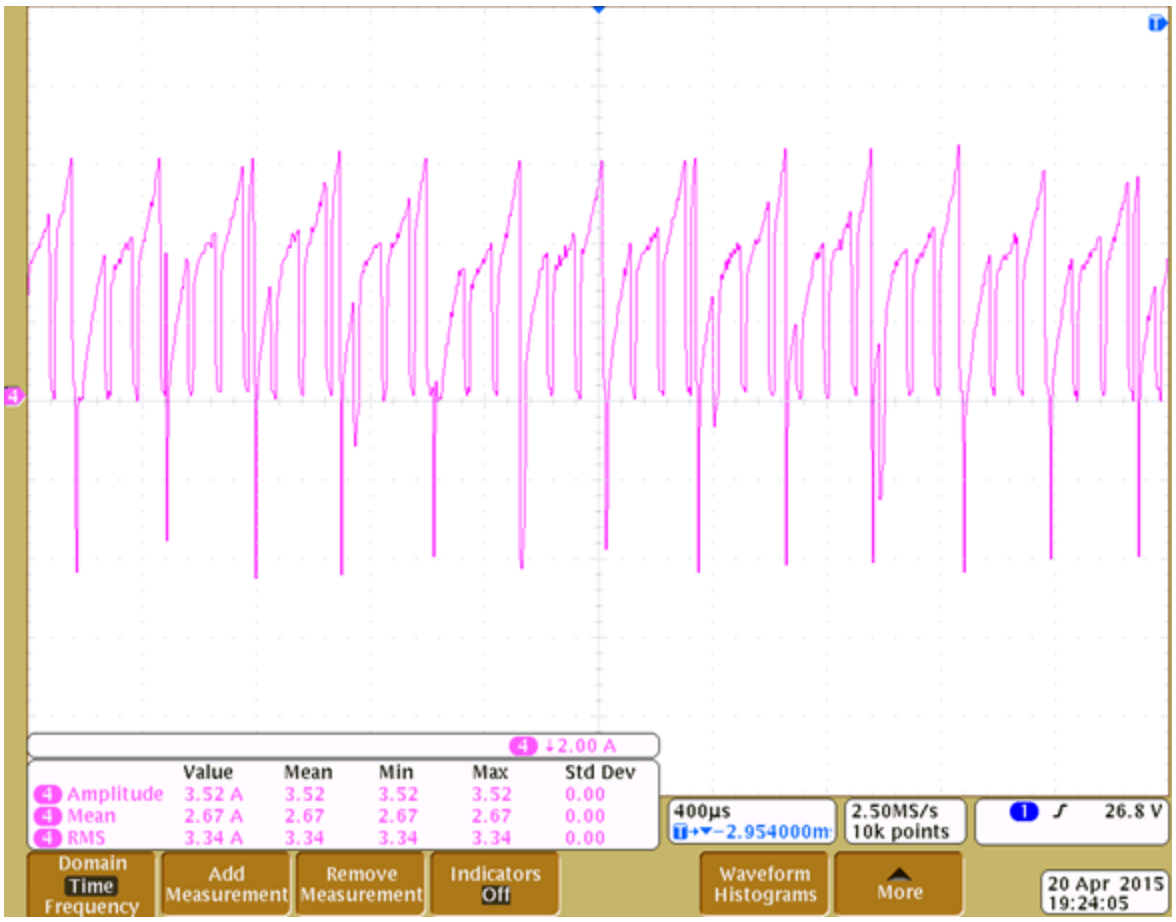

Figure 43. DC Link Ripple Current After Bulk Capacitor at 870 W

Figure 44 shows the current waveform at the output of the bridge rectifier that is before the DC bus bulk capacitors. The testing is done at 870-W input power and 230-V AC, without using any DC chokes. The bulk capacitor draws peak charging current. The peak current is 17 A and the average current is 2.65 A.

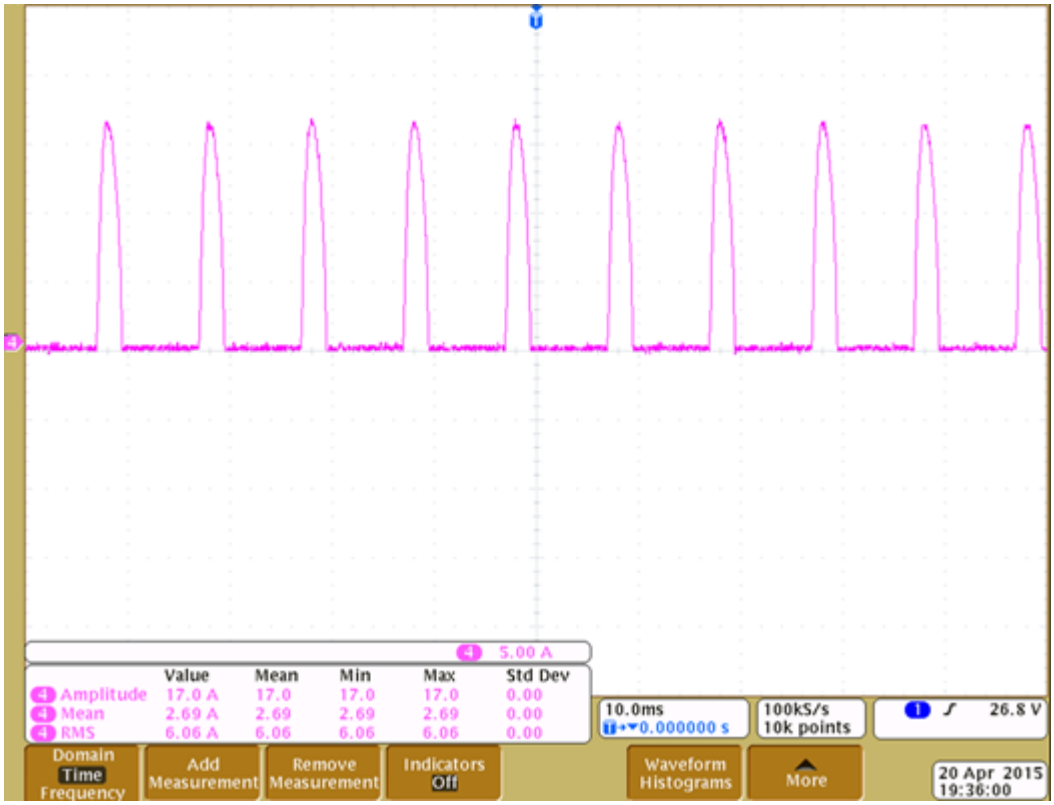

Figure 44. DC Link Ripple Current Before Bulk Capacitor at 870 W

Figure 45 shows the ripple voltage present at the DC bus capacitors at 900-W input power. The testing is done with a 230-V AC input. The peak-to-peak ripple voltage at the DC bus is 21.6 V.

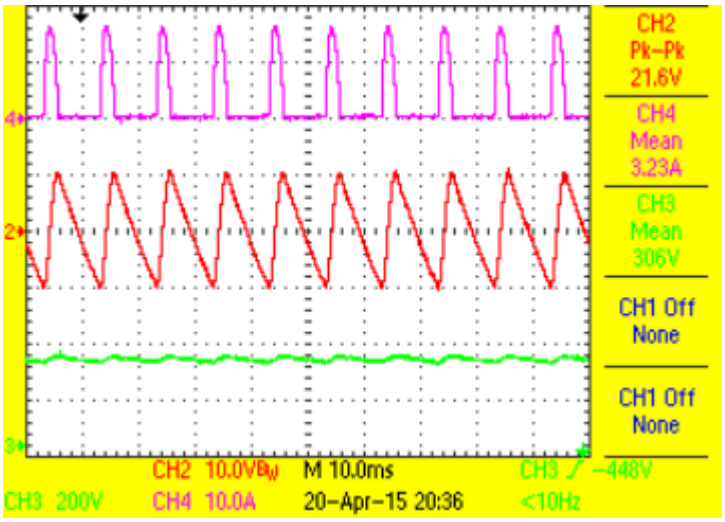

Figure 45. DC Bus Voltage Ripple at 900 W

Figure 46 shows the thermal image of the AC-DC converter board. The testing is done at 230-V AC input and 900-W input power. The heat sink temperature of the diode bridge rectifier is 73.7°C. The hottest component is the inrush current limiting resistor. The continuous heating of the inrush current limiter (ICL) can be eliminated by using a relay circuit across the ICL, such that the ICL will be bypassed by the relay after limiting the starting inrush.

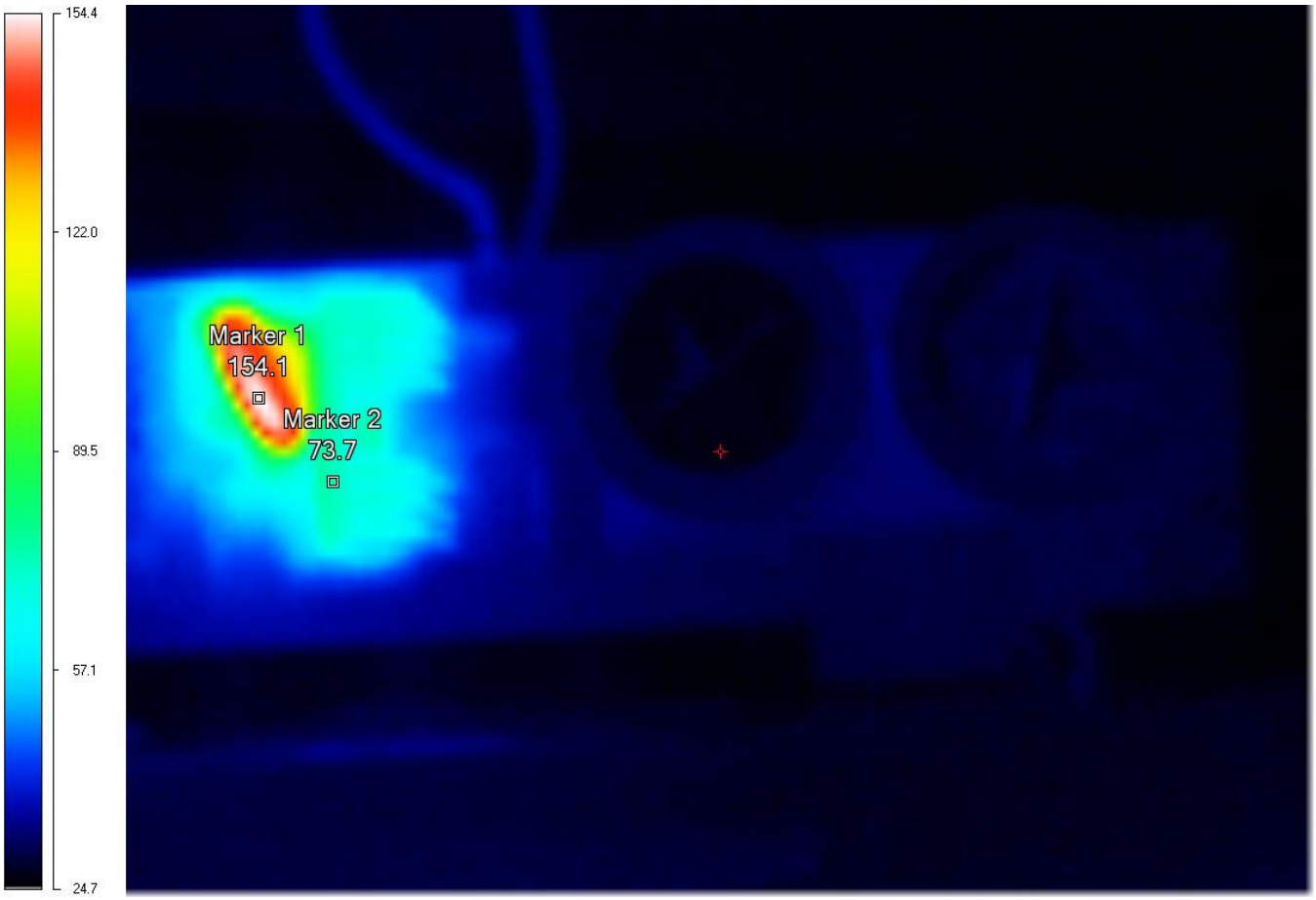

Figure 46. Thermal Image of AC-DC Converter Board at 230-V AC Input and 900-W Input Power

8.6 Overcurrent Protection of DRV92250

The overcurrent protection feature of the DRV92250 is tested at different current references. The parameters as per Table 10 are set for current limit operation setting.

Table 10. Settings of DRV92250 for Current Limit Protection

REGISTER BIT	BINARY SETTING	REMARKS
OCFromGPIO	0	On-chip voltage comparator for OC detection
TRKHSPWM	1	Number of pre-drivers disabled depends on HSDPWM
HSDPWM	1	Only the three high-side pre-drivers are disabled
PreDrvHLD	0	Pulse skipping control
CURLIM [1:0]	0	Leading-edge current limit blanking interval = 800 ns
IcompHys [1:0]	1	0-mV hysteresis control for OC comparator
DACB [7:0]	0x0D	8-bit reference for the current limit

A 20-mΩ sense resistor is used to detect the DC bus current. Figure 47 and Figure 48 show the current limit operation when the overcurrent reference is set at 3 A. Figure 48 shows a zoomed view of the overcurrent protection operation showing the PWM signals shut down when the current peak to the set current reference. The PWM duty cycle was 75% and testing is done at 325 V. The high side PWM is immediately pulled down whenever the current reaches the reference threshold. It can be seen that the overcurrent protection acts at around 3.5 A.

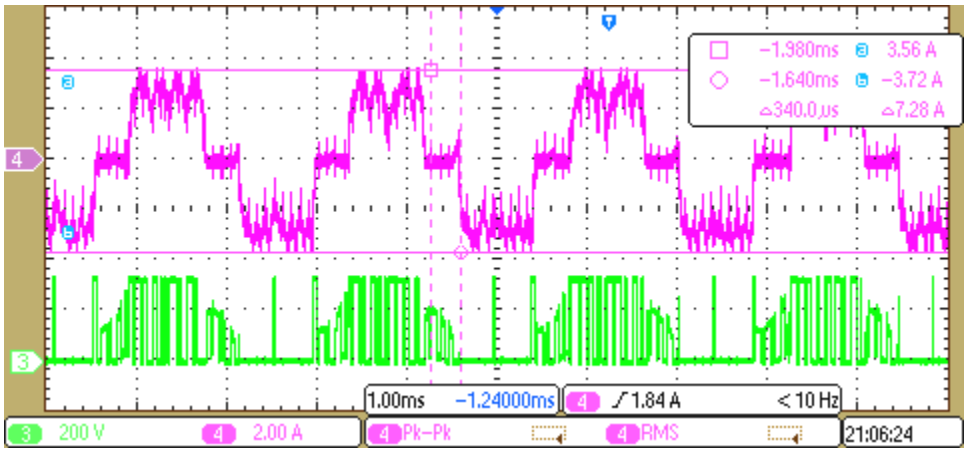

Figure 47. Overcurrent Protection at 3-A Peak Current

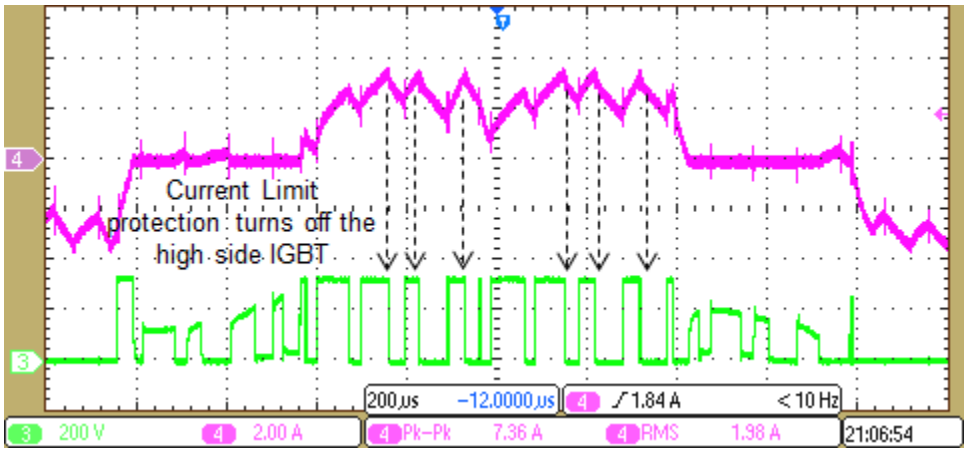

Figure 48. High-Side PWM Shut Down During Overcurrent Protection at 3-A Peak Current

Figure 49 and Figure 50 show the current limit operation when the overcurrent reference is set at 7 A. Figure 50 shows a zoomed view of the overcurrent protection operation showing the PWM signals shut down when the current peak to the set current reference. The PWM duty cycle was 75% and testing is done at 325 V. The high-side PWM is immediately pulled down whenever the current reaches the reference threshold. It can be seen that the overcurrent protection acts at around 7.2 A

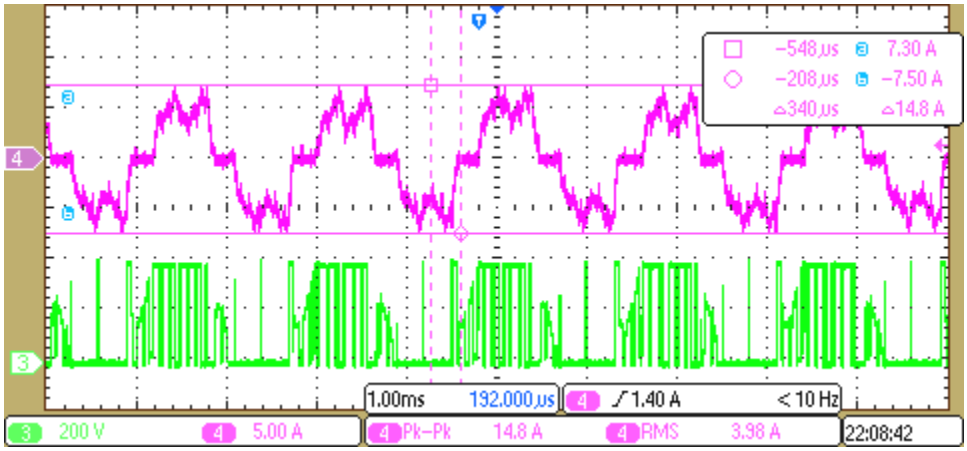

Figure 49. Overcurrent Protection at 7-A Peak Current

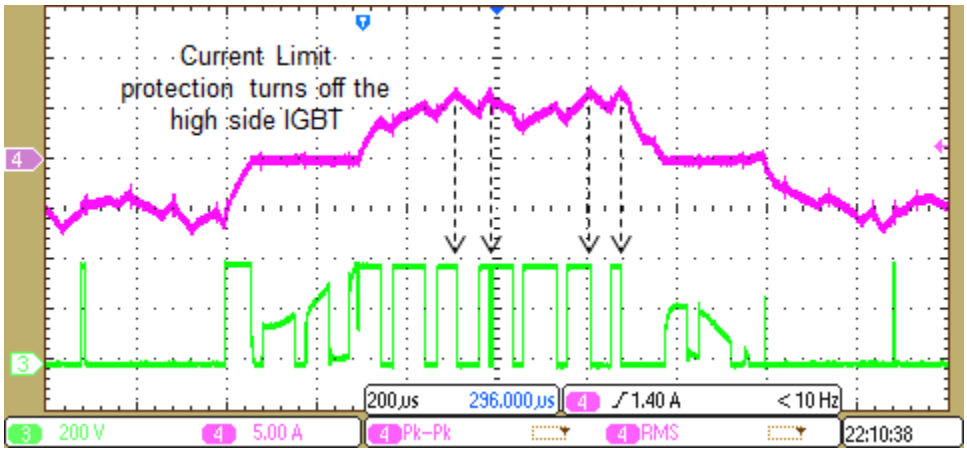

Figure 50. High-Side PWM Shut Down During Overcurrent Protection at 7-A Peak Current

8.7 Conducted Emission Test

This reference design has been tested for conducted emission as per EN55022 class B (EN55014) limits. During the test, the common mode choke L1 is replaced by the part 7448041104 from Wurth Electronics, which is a 4-mH, 11-A common mode filter and the gate resistors of the IGBTs are made to 20 Ω. Test results are shown in Figure 52 and the board passes the result with a 5-dB margin.

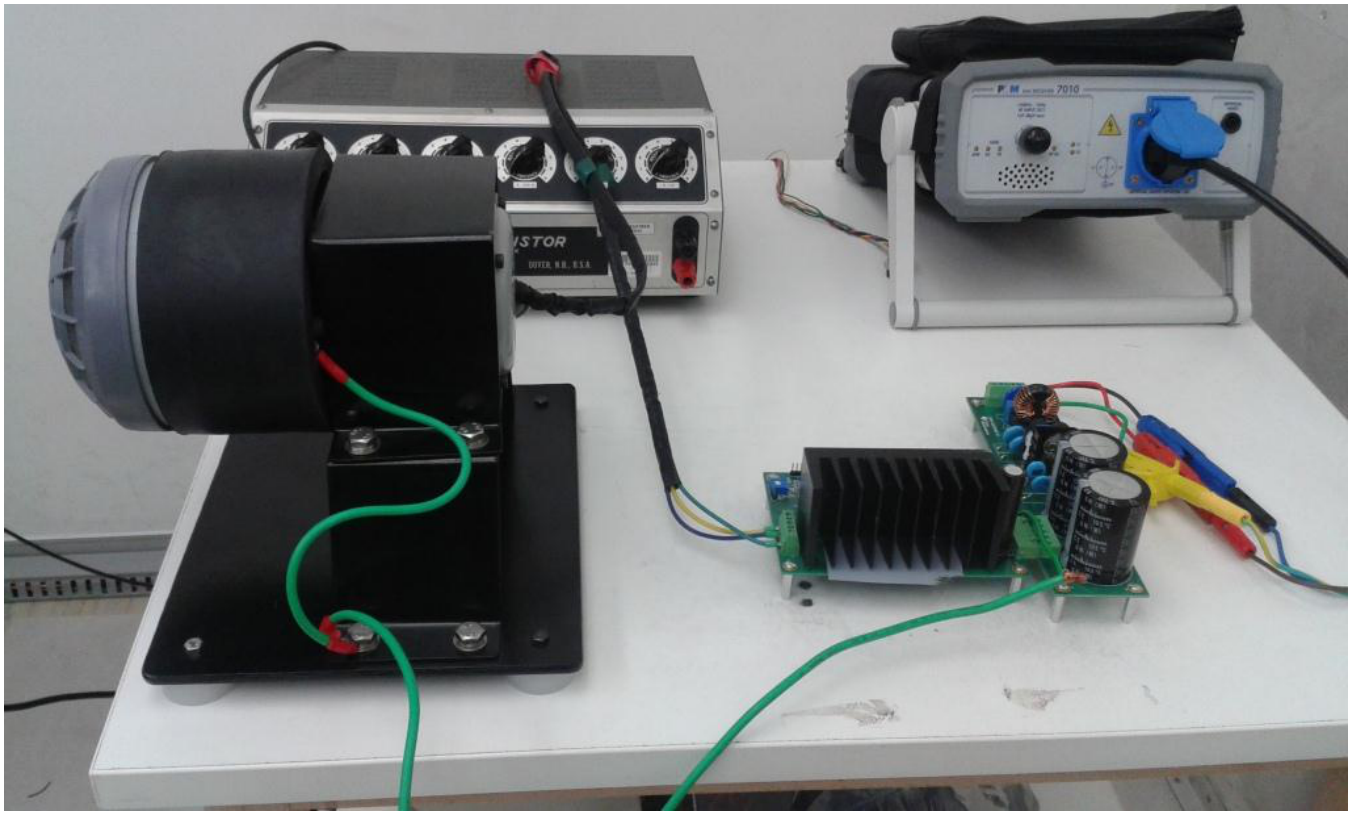

Figure 51. Conducted Emission Test Setup

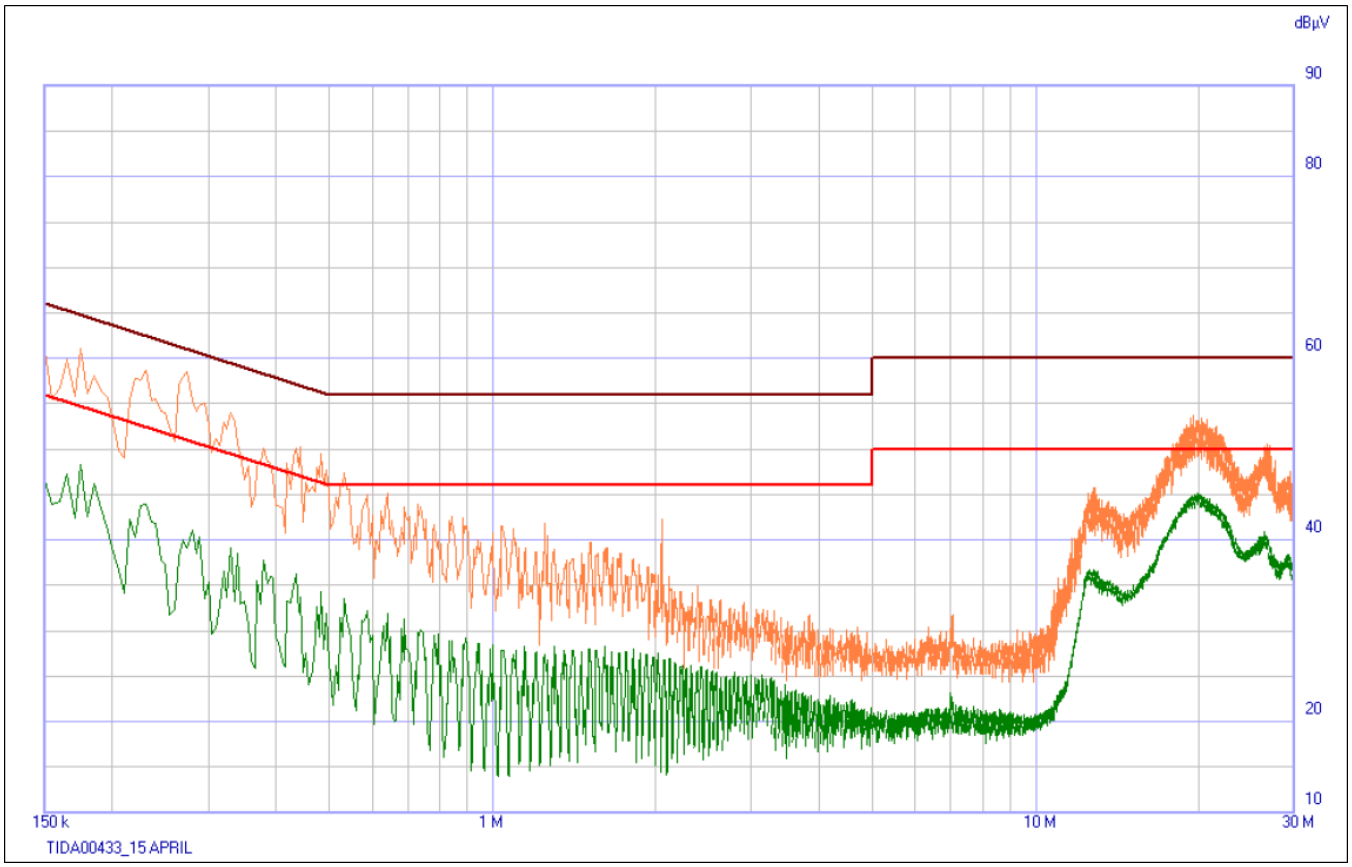

Figure 52. Conducted Emission Results as per EN55022 Class B Average and Peak Detector Output

8.8 Surge and EFT Test

Surge and EFT testing is done on the boards as per EN55014. The test condition and test results are tabulated in Table 11.

Table 11. Surge and EFT Test Result

BASIC STANDARD	PORT	REQUIREMENTS FOR RESIDENTIAL, COMMERCIAL AND LIGHT-INDUSTRIAL ENVIRONMENTS	PERFORMANCE CRITERION	TEST RESULT
IEC/EN 61000-4-4: Fast transients (burst)	AC input	±1 kV, 5 kHz	B	Passed (Meeting performance criterion A)
IEC/EN 61000-4-5: Surge	AC input	±2-kV line to earth, ±1-kV line to line	B	Passed (Meeting performance criterion A)

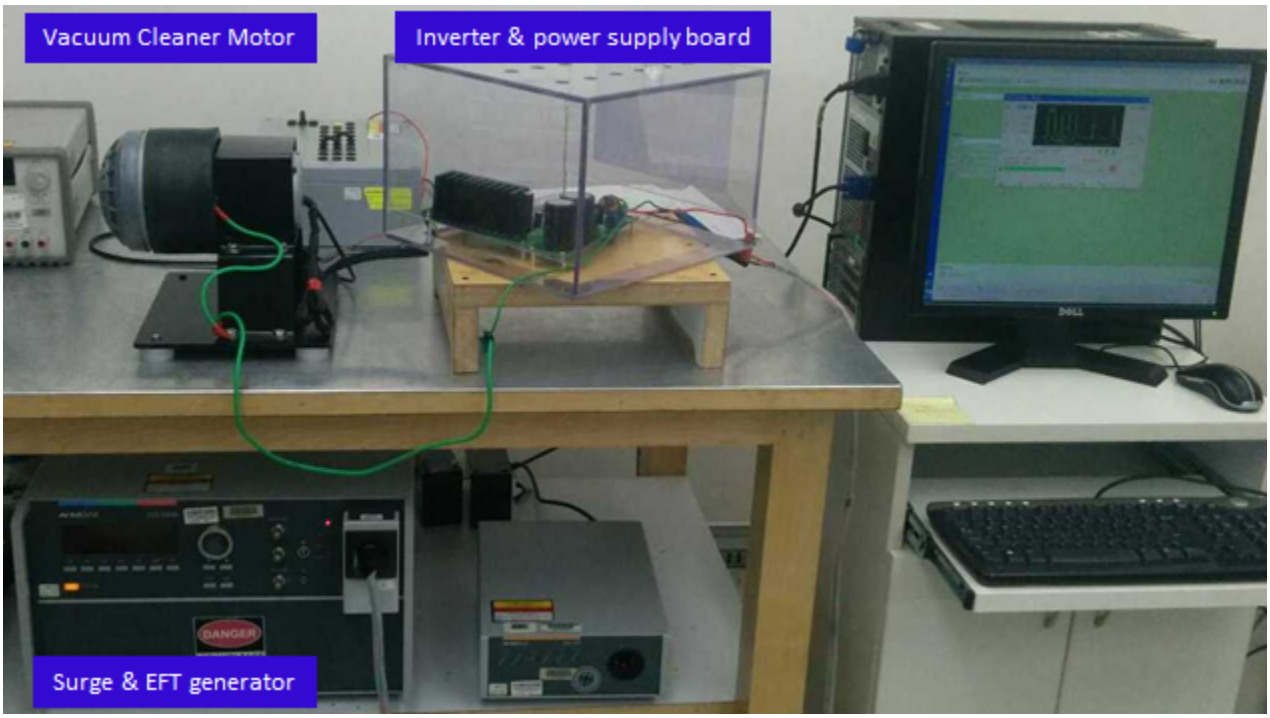

Figure 53. Surge and EFT Test Setup

9 Design Files

9.1 Schematics

To download the schematics, see the design files at TIDA-00433.

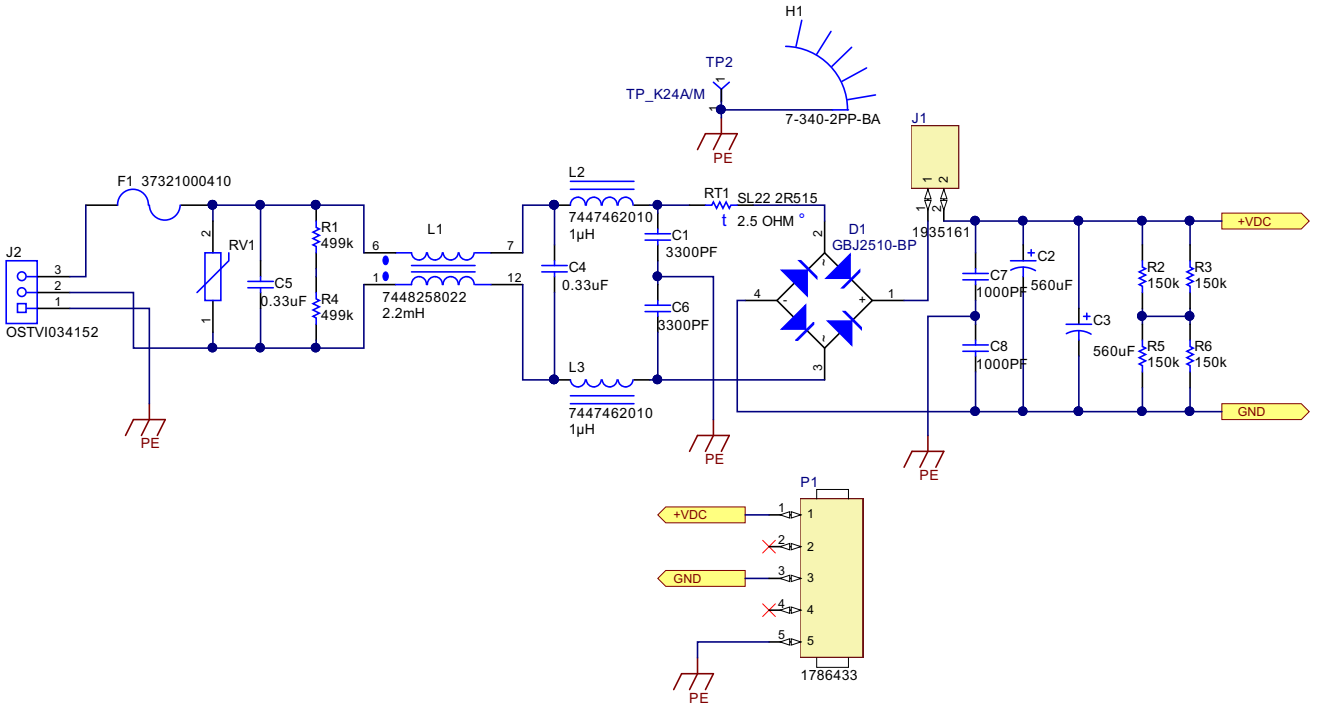

Figure 54. AC-DC Power Supply (TIDA-00433DB)

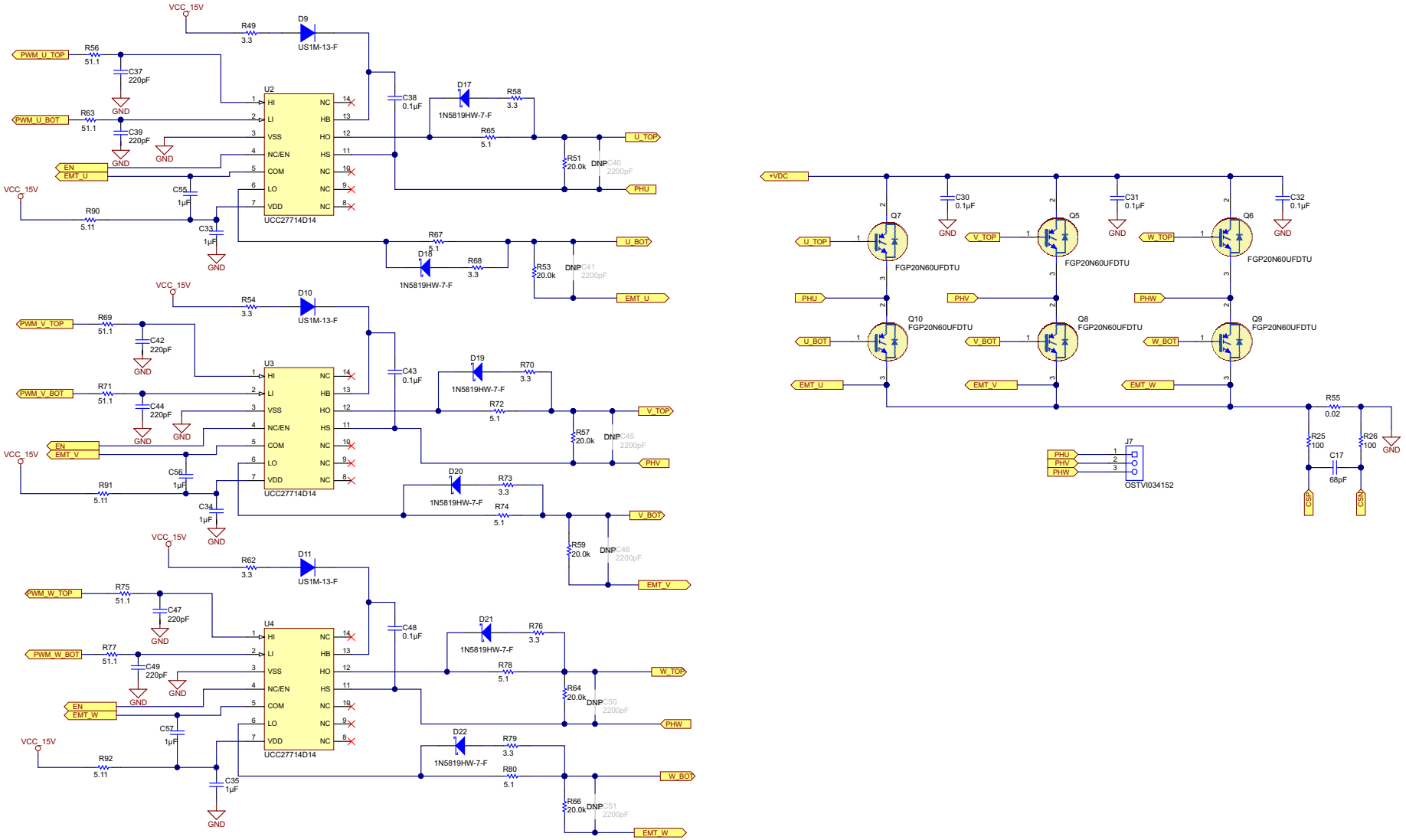

Figure 55. Gate Driver and Three Phase Inverter (TIDA-00433MB)

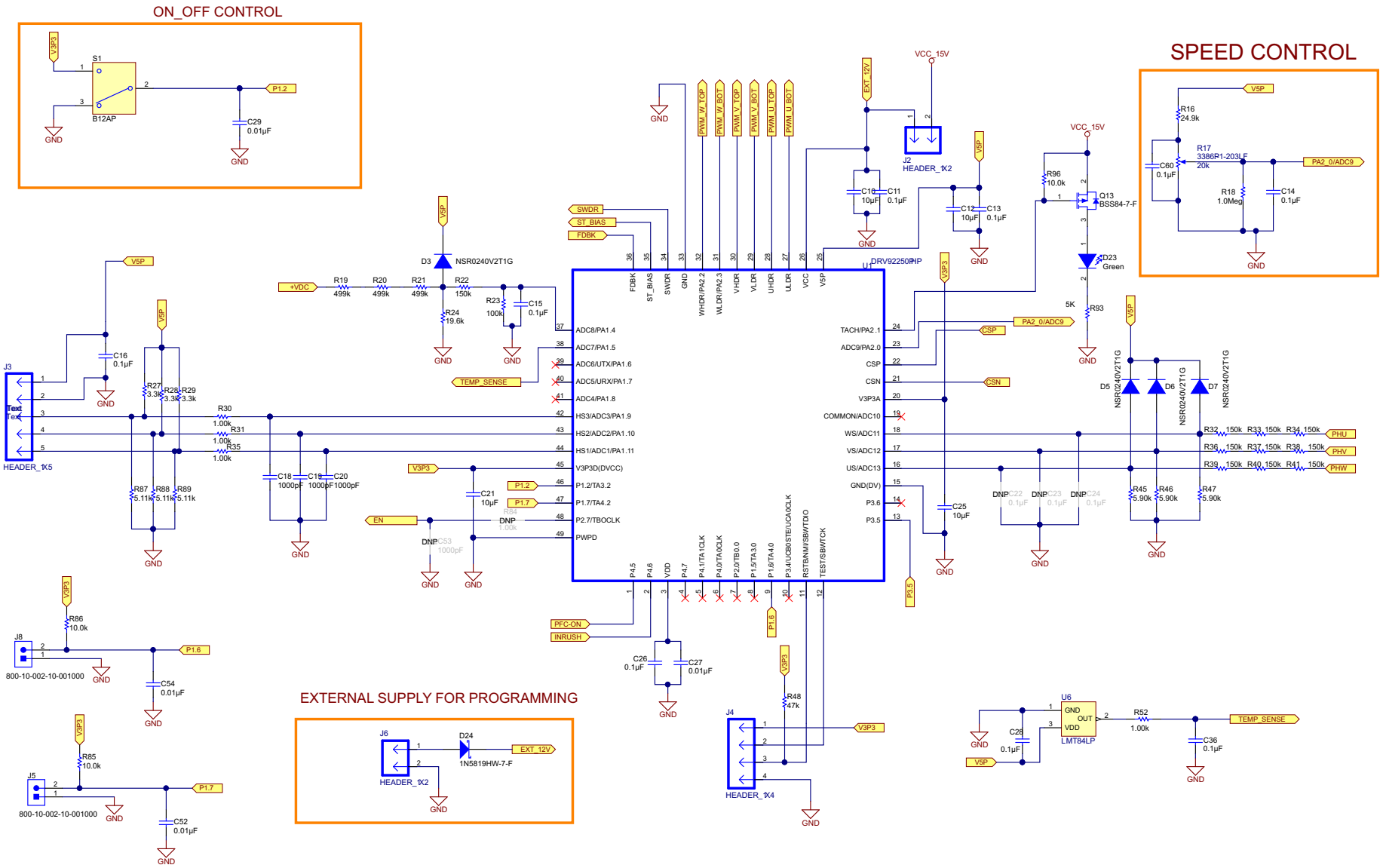

Figure 56. DRV92250 Controller and Feedbacks (TIDA-00433MB)

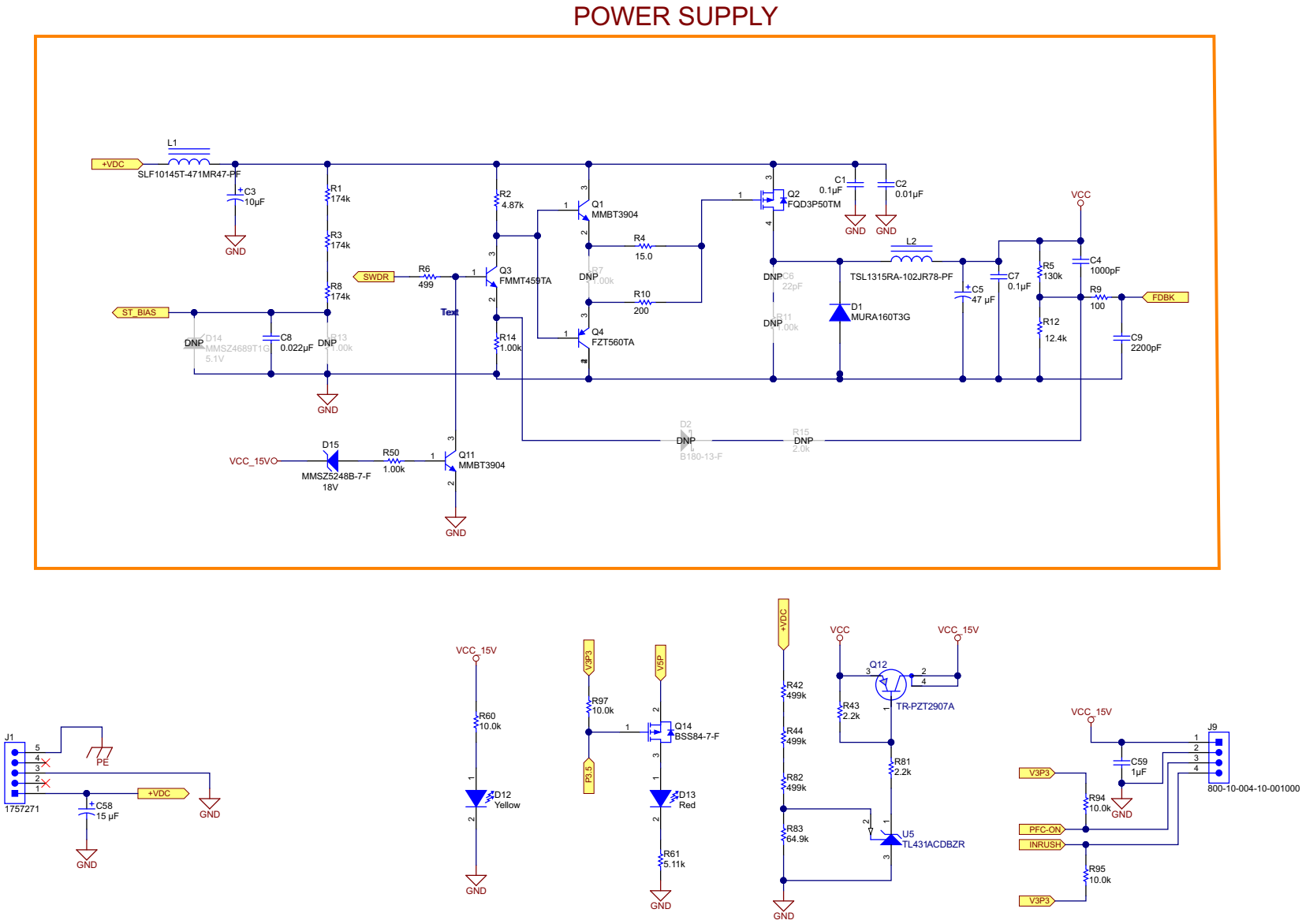

Figure 57. Bias Power Supply (15-V) (TIDA-00433MB)

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00433.

9.2.1 TIDA-00433DB

Table 12. TIDA-00433DB BOM

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT	NOTE
1	!PCB1	Printed Circuit Board	Any	TIDA-00433DB-E2		Fitted
2	C1, C6	CAP CER 3300PF 300VAC 20% RADIAL	Kemet	C947U332MZWDBA7317		Fitted
2	C2, C3	CAP, ALUMINUM, 560 uF, 450V, 20%, TH	NICHICON	LGN2W561MELC50		Fitted
2	C4, C5	CAP FILM 0.33UF 630VDC RADIAL	EPCOS(TDK)	B32922C3334M189		Fitted
2	C7, C8	CAP CER 1000PF 300VAC 20% RADIAL	Kemet	C907U102MZVDBA7317		Fitted
1	D1	RECT BRIDGE GPP 25A 1000V GBJ	MICRO COMMERCIAL COMPONENTS	GBJ2510-BP		Fitted
1	F1	FUSE BOARD MNT 10A 250VAC RADIAL	Littelfuse Inc	37321000410	Radial, Can, Vertical	Fitted
1	H1	HEATSINK PWR DUAL BLACK TO-220	CTS Thermal Management Products	7-340-2PP-BA	TO-220 Heat Sink	Fitted
4	H2, H3, H4, H5	MACHINE SCREW PAN SLOTTED M3	Keystone Electronics	29344	Screw	Fitted
1	J1	TERM BLOCK PCB, 2POS, 5.0MM, TH	PHOENIX CONTACT	1935161		Fitted
1	J2	TERMINAL BLOCK 7.50MM 3POS PCB, TH	On-Shore Technology	OSTVI034152		Fitted
1	L1	FILTER, WE-CMB COMMON MODE POWER LINE CHOKE, 2.2mH, 8A, VERTICAL	Wurth Elektronics	7448258022		Fitted
2	L2, L3	Inductor, Unshielded Drum Core, Ferrite, 1uH, 8A, 0.006 ohm, TH	Wurth Elektronik eiSos	7447462010	D6 x 8.5mm	Fitted
1	P1	TERM BLOCK HDR 5POS R/A 5.08MM	PHOENIX CONTACT	1786433		Fitted
2	R1, R4	RES, 499k ohm, 1%, 0.25W, 1206	Vishay-Dale	CRCW1206499KFKEA	1206	Fitted
4	R2, R3, R5, R6	RES, 150k ohm, 1%, 0.25W, 1206	Vishay-Dale	CRCW1206150KFKEA	1206	Fitted
1	RT1	CURRENT LIMITR INRSH 2.5 OHM 15A	AMETHERM	SL22 2R515		Fitted

Table 12. TIDA-00433DB BOM (continued)

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT	NOTE
1	RV1	VARISTOR, 387V, 8KA, DISC 20MM	EPCOS Inc	B72220S271K151		Fitted
1	TP2	Pin, Thru Hole, Tin Plate, for 0.062 PCB's	Vector	K24A/M	0.039 inch	Fitted
4	HEX STAND	HEX STANDOFF M3 ALUMINUM 20MM	Keystone Electronics	24437	HEX STAND	Fitted
1	HEX NUT	HEX NUT 0.217" STEEL M3	Keystone Electronics	4708	HEX NUT	Fitted

9.2.2 TIDA-00433MB

Table 13. TIDA-00433MB

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT	NOTE
1	!PCB1	Printed Circuit Board	Any	TIDA-00433MB-E2		Fitted
4	C1, C30, C31, C32	CAP, CERM, 0.1 µF, 630 V, +/- 10%, X7R, 1812	MuRata	GRM43DR72J104KW01L	1812	Fitted
4	C10, C12, C21, C25	CAP, CERM, 10uF, 16V, +/-20%, X5R, 0805	TDK Corporation	C2012X5R1C106M085AC	0805	Fitted
3	C11, C13, C28	CAP, CERM, 0.1 µF, 25 V, +/- 10%, X7R, 0603	AVX	06033C104KAT2A	0603	Fitted
4	C14, C15, C36, C60	CAP, CERM, 0.1uF, 16V, +/-5%, X7R, 0603	AVX	0603YC104JAT2A	0603	Fitted
1	C16	CAP, CERM, 0.1uF, 25V, +/-10%, X7R, 0805	AVX	08053C104KAT2A	0805	Fitted
1	C17	CAP, CERM, 68pF, 50V, +/-5%, C0G/NP0, 0603	AVX	06035A680JAT2A	0603	Fitted
3	C18, C19, C20	CAP, CERM, 1000 pF, 50 V, +/- 10%, X7R, 0603	TDK	C1608X7R1H102K080AE	0603	Fitted
1	C2	CAP, CERM, 0.01uF, 500V, +/-10%, X7R, 1812	Vishay-Vitramon	VJ1812Y103KXEAT	1812	Fitted
1	C26	CAP, CERM, 0.1 µF, 25 V, +/- 10%, X7R, 0603	Kemet	C0603C104K3RACTU	0603	Fitted
4	C27, C29, C52, C54	CAP, CERM, 0.01uF, 100V, +/-10%, X7R, 0603	AVX	06031C103KAT2A	0603	Fitted
1	C3	CAP, AL, 10 µF, 400 V, +/- 20%, TH	Nichicon	UCS2G100MPD1TD	RCAP, TH, 10 x 20mm	Fitted
6	C33, C34, C35, C55, C56, C57	CAP, CERM, 1uF, 25V, +/-10%, X7R, 0805	MuRata	GRM21BR71E105KA99L	0805	Fitted

Table 13. TIDA-00433MB (continued)

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT	NOTE
6	C37, C39, C42, C44, C47, C49	CAP, CERM, 220 pF, 50 V, +/- 1%, C0G/NP0, 0603	TDK	C1608C0G1H221J080AA	0603	Fitted
3	C38, C43, C48	CAP, CERM, 0.1 µF, 25 V, +/- 10%, X7R, 0805	MuRata	GRM21BR71E104KA01L	0805	Fitted
1	C4	CAP, CERM, 1000pF, 25V, +/-10%, X7R, 0603	MuRata	GRM188R71E102KA01D	0603	Fitted
1	C5	CAP ALUM 47UF 25V 20% RADIAL	Kemet	ESY476M025AC3EA	5.0x9.0mm	Fitted
1	C58	CAP ALUM 100UF 400V 20% RADIAL	Nichicon	UPZ2G101MNY9	12.5x20	Fitted
1	C59	CAP, CERM, 1uF, 50V, +/-10%, X7R, 0805	Taiyo Yuden	UMK212F105ZG-T	0805	Fitted
1	C7	CAP, CERM, 0.1uF, 25V, +/-5%, X7R, 0603	AVX	06033C104JAT2A	0603	Fitted
1	C8	CAP, CERM, 0.022 µF, 25 V, +/- 10%, X7R, 0603	Kemet	C0603C223K3RACTU	0603	Fitted
1	C9	CAP, CERM, 2200pF, 100V, +/- 10%, X7R, 0603	TDK	C1608X7R2A222K	0603	Fitted
1	D1	Diode, Ultrafast, 600V, 1A, SMA	ON Semiconductor	MURA160T3G	SMA	Fitted
1	D12	LED YELLOW CLEAR 1206 SMD	Stanley Electric Co., LTD	HAY1105W-TR	1.6x1.85x3.2	Fitted
1	D13	LED, Red, SMD	Stanley Electric Co., LTD	HBR1105W-TR	1.6x1.85x3.2	Fitted
1	D15	Diode, Zener, 18V, 500 mW, SOD-123	Diodes Inc.	MMSZ5248B-7-F	SOD-123	Fitted
7	D17, D18, D19, D20, D21, D22, D24	Diode, Schottky, 40V, 1A, SOD-123	Diodes Inc.	1N5819HW-7-F	SOD-123	Fitted
1	D23	LED GREEN CLEAR 1206 SMD	Stanley Electric Co., LTD	HPG1105W-TR	1.6x1.85x3.2	Fitted
4	D3, D5, D6, D7	DIODE SCHOTTKY 40V 250MA SOD523	ON Semiconductor	NSR0240V2T1G	SOD-523	Fitted
3	D9, D10, D11	Diode, Ultrafast, 1000V, 1A, SMA	Diodes Inc.	US1M-13-F	SMA	Fitted
1	J1	TERM BLOCK HDR 5POS R/A 5.08MM	Phoenix Contact	1757271	17.24x8.6x12mm	Fitted
4	J2,J5,J6, J8	Header, Male 2-pin, 100mil spacing,	Wurth Electronics Inc	61300211121	0.100 inch x 2	Fitted
1	J3	Header, Male 5-pin, 100mil spacing,	Wurth Electronics Inc	61300511121	0.100 inch x 5	Fitted
2	J4,J9	Header, Male 4-pin, 100mil spacing,	Wurth Electronics Inc	61300411121	0.100 inch x 4	Fitted
1	J7	TERMINAL BLOCK 7.50MM 3POS PCB, TH	On-Shore Technology	OSTVI034152		Fitted
1	L1	Inductor, Shielded Drum Core, Ferrite, 470uH, 0.47A, 1.03 ohm, SMD	TDK	SLF10145T-471MR47-PF	SLF10145	Fitted

Table 13. TIDA-00433MB (continued)

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT	NOTE
1	L2	FIXED IND 1MH 780MA 1 OHM TH	TDK	TSL1315RA-102JR78-PF	14x17mm	Fitted
2	Q1, Q11	Transistor, NPN, 40V, 0.2A, SOT-23	Fairchild Semiconductor	MMBT3904	SOT-23	Fitted
1	Q12	Transistor, PNP, 60-V, 800-mA, 1000-mW	Fairchild	PZT2907A	SOT-223	Fitted
2	Q13, Q14	MOSFET, P-CH, -50V, -0.13A, SOT-23	Diodes Inc.	BSS84-7-F	SOT-23	Fitted
1	Q2	MOSFET P-CH 500V 2.1A DPAK	Fairchild Semiconductor	FQD3P50TM	DPAK	Fitted
1	Q3	TRANSISTOE, NPN, 450V, 0.15A, SOT23-3	DIODES INCORPORATED	FMMT459TA		Fitted
1	Q4	TRANSISTOR, PNP, 500V, 0.15A, SOT223	DIODES INCORPORATED	FZT560TA		Fitted
6	Q5, Q6, Q7, Q8, Q9, Q10	IGBT Transistors 600V, 20A Field Stop	Fairchild Semiconductor	FGP20N60UFDTU		Fitted
3	R1, R3, R8	RES, 174 k, 1%, 0.25 W, 1206	Yageo America	RC1206FR-07174KL	1206	Fitted
1	R10	RES, 200 ohm, 1%, 0.25W, 1206	Panasonic	ERJ-8ENF2000V	1206	Fitted
1	R12	RES, 12.4 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060312K4FKEA	0603	Fitted
5	R14, R30, R31, R35, R52	RES, 1.00 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031K00FKEA	0603	Fitted
1	R16	RES, 24.9k ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-0724K9L	0603	Fitted
1	R17	TRIMMER, 20k ohm, 0.5W, TH	Bourns	3386P-1-203LF	375x190x375mil	Fitted
1	R18	RES, 1.0Meg ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031M00JNEA	0603	Fitted
12	R19, R20, R21, R32, R33, R34, R36, R37, R38, R39, R40, R41	RES, 150k ohm, 1%, 0.25W, 1206	Vishay-Dale	CRCW1206150KFKEA	1206	Fitted
1	R2	RES, 4.87 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06034K87FKEA	0603	Fitted
1	R22	RES, 150k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603150KJNEA	0603	Fitted
1	R23	RES, 100k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603100KFKEA	0603	Fitted
4	R24, R45, R46, R47	RES, 5.90 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06035K90FKEA	0603	Fitted
2	R25, R26	RES, 100, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603100RFKEA	0603	Fitted
3	R27, R28, R29	RES, 3.3 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06033K30JNEA	0603	Fitted
1	R4	RES, 15.0, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060315R0FKEA	0603	Fitted
3	R42, R44, R82	RES, 499 k, 1%, 0.25 W, 1206	Panasonic	ERJ-8ENF4993V	1206	Fitted
2	R43, R81	RES, 2.2 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06032K20JNEA	0603	Fitted
1	R48	RES, 47k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060347K0JNEA	0603	Fitted
3	R49, R54, R62	RES, 3.3 ohm, 5%, 0.25W, 1206	Vishay-Dale	CRCW12063R30JNEA	1206	Fitted
1	R5	RES, 130 k, 1%, 0.1 W, 0603	Yageo America	AC0603FR-07130KL	0603	Fitted

Table 13. TIDA-00433MB (continued)

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT	NOTE
1	R50	RES, 1.00 k, 1%, 0.25 W, 1206	Vishay-Dale	CRCW12061K00FKEA	1206	Fitted
6	R51, R53, R57, R59, R64, R66	RES, 20.0k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060320K0FKEA	0603	Fitted
1	R55	RES, 0.02, 1%, 3 W, 2512	Bourns	CRA2512-FZ-R020ELF	2512	Fitted
6	R56, R63, R69, R71, R75, R77	RES, 51.1, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060351R1FKEA	0603	Fitted
6	R58, R68, R70, R73, R76, R79	RES, 3.3 ohm, 5%, 0.125W, 0805	Vishay-Dale	CRCW08053R30JNEA	0805	Fitted
1	R6	RES, 499, 1%, 0.1 W, 0603	Yageo America	RC0603FR-07499RL	0603	Fitted
8	R60, R85, R86, R93, R94, R95, R96, R97	RES, 10.0k ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-0710KL	0603	Fitted
4	R61, R87, R88, R89	RES, 5.11 k, 0.5%, 0.1 W, 0603	Yageo America	RC0603FR-075K11L	0603	Fitted
6	R65, R67, R72, R74, R78, R80	RES, 5.1 ohm, 5%, 0.125W, 0805	Vishay-Dale	CRCW08055R10JNEA	0805	Fitted
1	R83	RES, 64.9 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060364K9FKEA	0603	Fitted
1	R9	RES, 100 ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-07100RL	0603	Fitted
3	R90, R91, R92	RES, 5.11, 1%, 0.1 W, 0603	Yageo America	RC0603FR-075R11L	0603	Fitted
1	S1	SWITCH TOGGLE SPDT 0.4VA 28V	NKK Switches	B12AP	6.8x23.1x8.8mm	Fitted
1	U1	IC, Voltage Brushless DC (BLDC) Motor Controller	Texas Instruments	DRV92250PHP	HTQFP-48	Fitted
3	U2, U3, U4	High-Speed Low-side Gate Driver Device, D0014A	Texas Instruments	UCC27714D14	D0014A	Fitted
1	U5	Adjustable Precision Shunt Regulator, 34 ppm / degC, 100 mA, 0 to 70 degC, 3-pin SOT-23 (DBZ), Green (RoHS & no Sb/Br)	Texas Instruments	TL431ACDBZR	DBZ0003A	Fitted
1	U6	IC, TEMP SENSOR PREC ANLG, TO-92, ROHS	Texas Instruments	LMT84LP	LP	Fitted
0	C22, C23, C24	CAP, CERM, 0.1 µF, 25 V, +/- 10%, X7R, 0603	AVX	06033C104KAT2A	0603	Not Fitted
0	C40, C41, C45, C46, C50, C51	CAP, CERM, 2200 pF, 25 V, +/- 10%, X7R, 0603	MuRata	GRM188R71E222KA01D	0603	Not Fitted
0	C53	CAP, CERM, 1000 pF, 50 V, +/- 10%, X7R, 0603	TDK	C1608X7R1H102K	0603	Not Fitted
0	C6	CAP, CERM, 22pF, 100V, +/-5%, C0G/NP0, 1206	AVX	12061A220JAT2A	1206	Not Fitted

Table 13. TIDA-00433MB (continued)

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	PCB FOOTPRINT	NOTE
0	D14	Diode, Zener, 5.1V, 500 mW, SOD-123	ON Semiconductor	MMSZ4689T1G	SOD-123	Not Fitted
0	D2	Diode, Schottky, 80V, 1A, SMA	Diodes Inc.	B180-13-F	SMA	Not Fitted
0	R13, R84	RES, 1.00 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031K00FKEA	0603	Not Fitted
0	R15	RES, 2.0 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06032K00JNEA	0603	Not Fitted
0	R7, R11	RES, 1.00k ohm, 1%, 0.25W, 1206	Vishay-Dale	CRCW12061K00FKEA	1206	Not Fitted
1	HEAT SINK	FISCHER ELEKTRONIK SK 81/ 50 SA HEAT SINK, EXTRUDED	FISCHER ELEKTRONIK	SK 81/ 50 SA	HEAT SINK	Fitted
4	H4, H5, H6, H7	MACHINE SCREW PAN SLOTTED M3	Keystone Electronics	29316	Screw	Fitted
4	HEX STAND	HEX STANDOFF M3 ALUMINUM 20MM	Keystone Electronics	24437	HEX STAND	Fitted
6	CLIP-TO220	MAX CLIP TO-220/MAX220 SCREW-MNT	Aavid Thermalloy	MAX07NG	CLIP-TO220	Fitted
6	MACHINE SCREW	MACHINE SCREW PAN SLOTTED M3	Keystone Electronics	29316	Screw	Fitted

9.3 Layer Plots

To download the layer plots, see the design files at TIDA-00433.

9.4 Altium Project

To download the Altium project files, see the design files at TIDA-00433.

9.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00433.

9.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00433.

10 References

1. Texas Instruments, *Highly Integrated High Voltage Brushless DC (BLDC) Motor Controller*, DRV92250 Datasheet
2. Texas Instruments, *UCC27714 High-Speed, 600-V High-Side Low-Side Gate Driver with 4A Peak Output*, Datasheet (SLUSBY6)
3. Texas Instruments, *Sensorless Trapezoidal Control of BLDC Motors*, Application Report (SPRABQ7)

11 Terminology

SPI— Serial Peripheral Interface

PWM— Pulse Width Modulation

BLDC— Brushless DC motor

MCU— Microcontroller unit

FETs, MOSFETs—Metal–oxide–semiconductor field-effect transistor

IGBT— Insulated Gate Bipolar Transistor

ESD— Electrostatic Discharge

RPM— Rotation per Minute

RMS— Root Mean Square

12 About the Author

MANU BALAKRISHNAN is a systems engineer at Texas Instruments where he is responsible for developing subsystem design solutions for the Industrial Motor Drive segment. Manu brings to this role his experience in power electronics, analog and mixed signal designs. He has system level product design experience in permanent magnet motor drives. Manu earned his bachelor of technology in electrical and electronics engineering from the University of Kerala and his master of technology in power electronics from National Institute of Technology Calicut, India.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265