Design Guide: TIDA-010966

Bidirectional Isolated Dual-Bridge Series Resonant DC/DC Converter Reference Design for Pack Balance

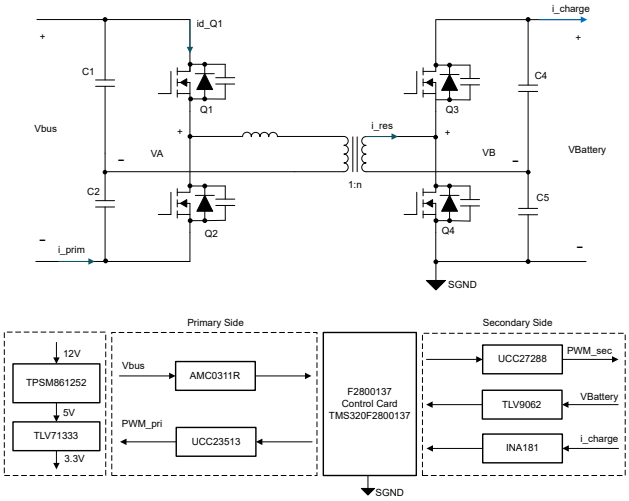
Description

This reference design is a bidirectional isolated dual-bridge series resonant DC/DC converter used to achieve pack balance in a residential energy storage system. This reference design can achieve constant current mode and constant voltage mode with 95% peak efficiency. This reference design is for 40V to 60V residential energy storage systems.

Resources

TIDA-010966	Design Folder
UCC27288, UCC23513	Product Folder
TMS320F2800137, TLV9062	Product Folder
INA181, TPSM861252	Product Folder

Ask the TI E2E™ support experts

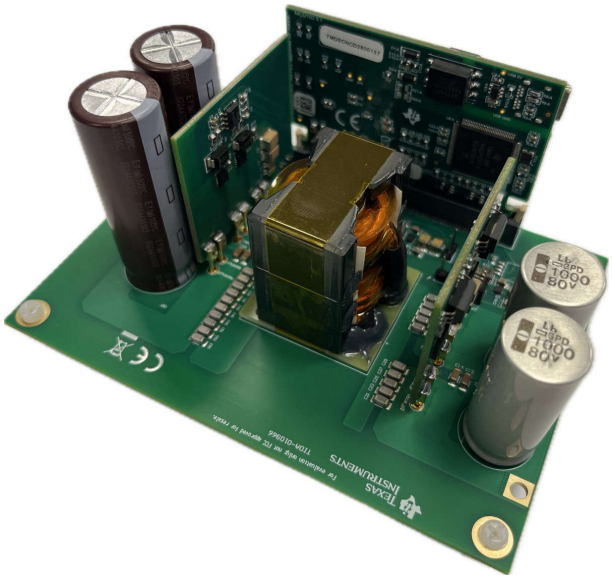


Features

- Bidirectional dual-active-bridge with Single-Phase-Shift (SPS) plus Varying-Frequency (VF) control
- Bidirectional power control with constant current (CC) and constant voltage (CV) loop control
- TMS320F2800137 controller for implementation of digital control
- Maximum charge and discharge current of 5A
- Without isolated voltage and current sensing for low cost requirements
- Peak efficiency – 95%, full-load efficiency – 93.7%
- Switching frequency of 80kHz to 300kHz to provide full range zero-voltage switching (ZVS)
- Input voltage 24V, output voltage of 40V–58V, full input range can realize soft-switching

Applications

- ESS – Battery management system (BMS)



1 System Description

Energy storage system (ESS) play an important role in renewable energy applications. Depending on the system voltage, capacity and usage, ESS can be divided into three different categories: residential ESS, commercial and industrial ESS, and grid ESS. Commercial and industrial, and grid ESS contain several racks that each contain packs in stack. Residential ESS only contains packs. Residential ESS is divided into high-voltage residential ESS and low-voltage residential ESS. Among them, the high-voltage system is composed of packs connected in series with each other to form high voltage, and then inverted to the grid through PCS (bidirectional DC/DC + bidirectional DC/AC). Figure 1-1 shows the system architecture for a high-voltage residential ESS.

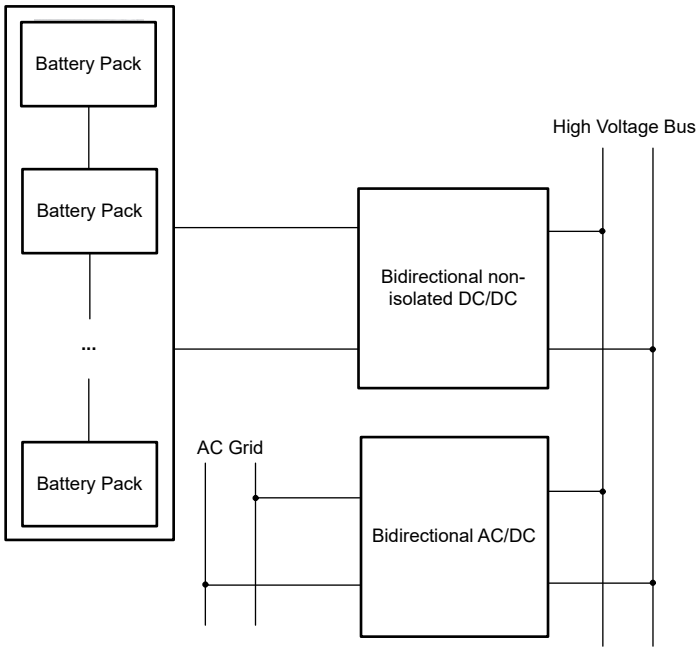


Figure 1-1. Architecture of High-Voltage Residential ESS

Battery packs connected in series produce identical charge and discharge current profiles. Pack voltage imbalances result from degree of aging differences between packs. Inconsistent voltage levels affect system utilization and lifespan. Weaker packs develop higher voltages under same charging energy, further exacerbating imbalance.

There are several reasons why the aging degree of a pack is not the same:

- With the increase of the service life of the energy storage system, the heat of different packs is different, which gradually causes inconsistencies between packs.
- There is a mix of old and new packs in residential ESS which causes capacity inconsistencies between packs.

Therefore, to optimize the imbalance between packs, active pack balance is required to balance the voltages between different packs, Figure 1-2 shows several bidirectional isolated DC/DC converters are used here as active pack balance.

These bidirectional DC/DC converters are terminated with a battery pack on one end and an auxiliary power rail on the board on the other.

When high-voltage conditions prevail, discharge the pack directly from the battery connector. Conversely, recharge the pack when low-voltage conditions exist. Using this approach maintains voltage balance between packs.

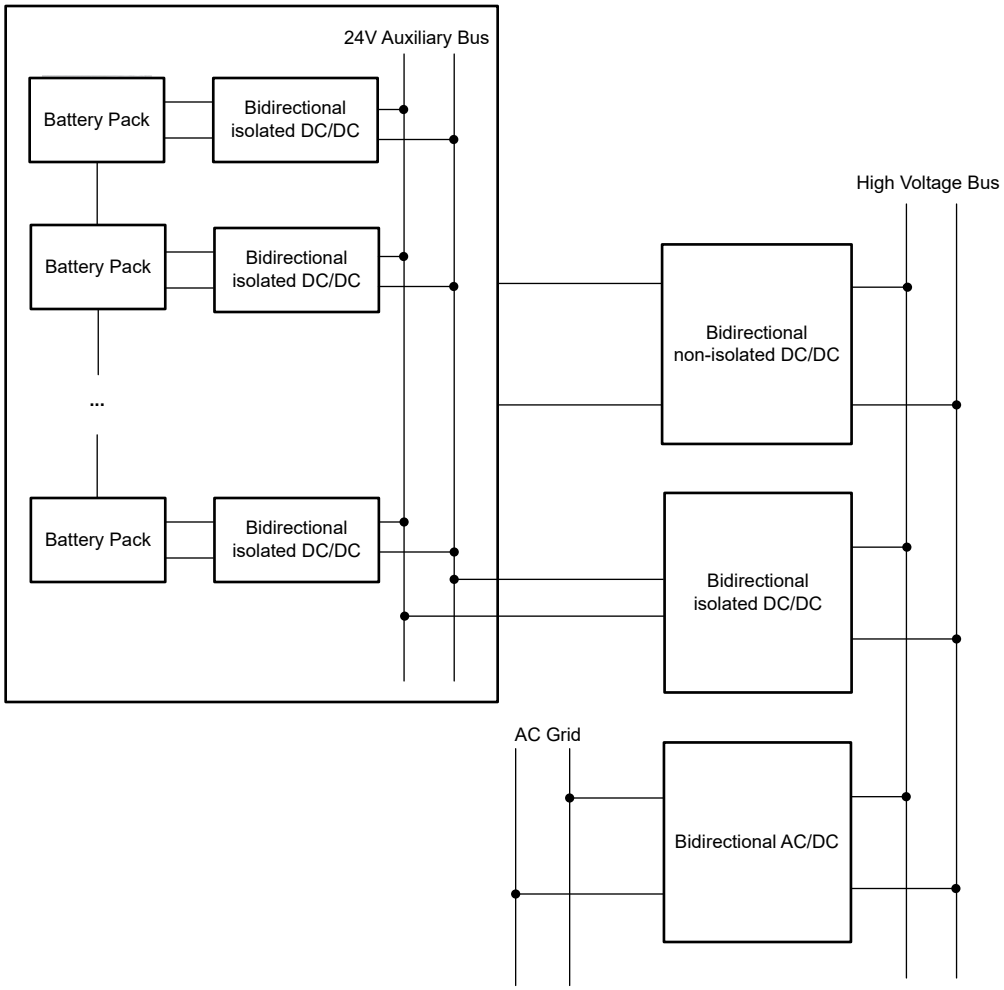


Figure 1-2. Active Pack Balance in High-Voltage Residential ESS

Power density, system cost, and system efficiency are important requirements of a converter used in this system. A bidirectional isolated dual-bridge series resonant DC/DC converter only has two half bridges that can achieve isolated bidirectional power transmission. Less switches can help improve power density and system cost. This topology also can help release Zero Voltage Switching (ZVS), which also can help improve system efficiency.

This reference design proposes a brand-new architecture for active pack balance in residential ESS, and uses bidirectional isolated dual-bridge series resonant DC/DC converter to achieve power transmission. For this topology, this reference design proposes new varying frequency plus phase-shift control methods to provide full-range ZVS.

2 System Overview

2.1 Block Diagram

Figure 2-1 shows the block diagram of this bidirectional isolated DC/DC design. The primary side needs voltage and current sensing. The TLV9062 device senses the input voltage for the voltage loop and the INA185 is used to sense the input current to perform the current loop.

A TMDSCNCD2800137 control card supports the digital control and the UCC27288 and UCC23513 devices are used as gate drivers on both sides. The architecture has two half bridges with four Si MOSFETs, resonant capacitors, resonant inductors, and one transformer.

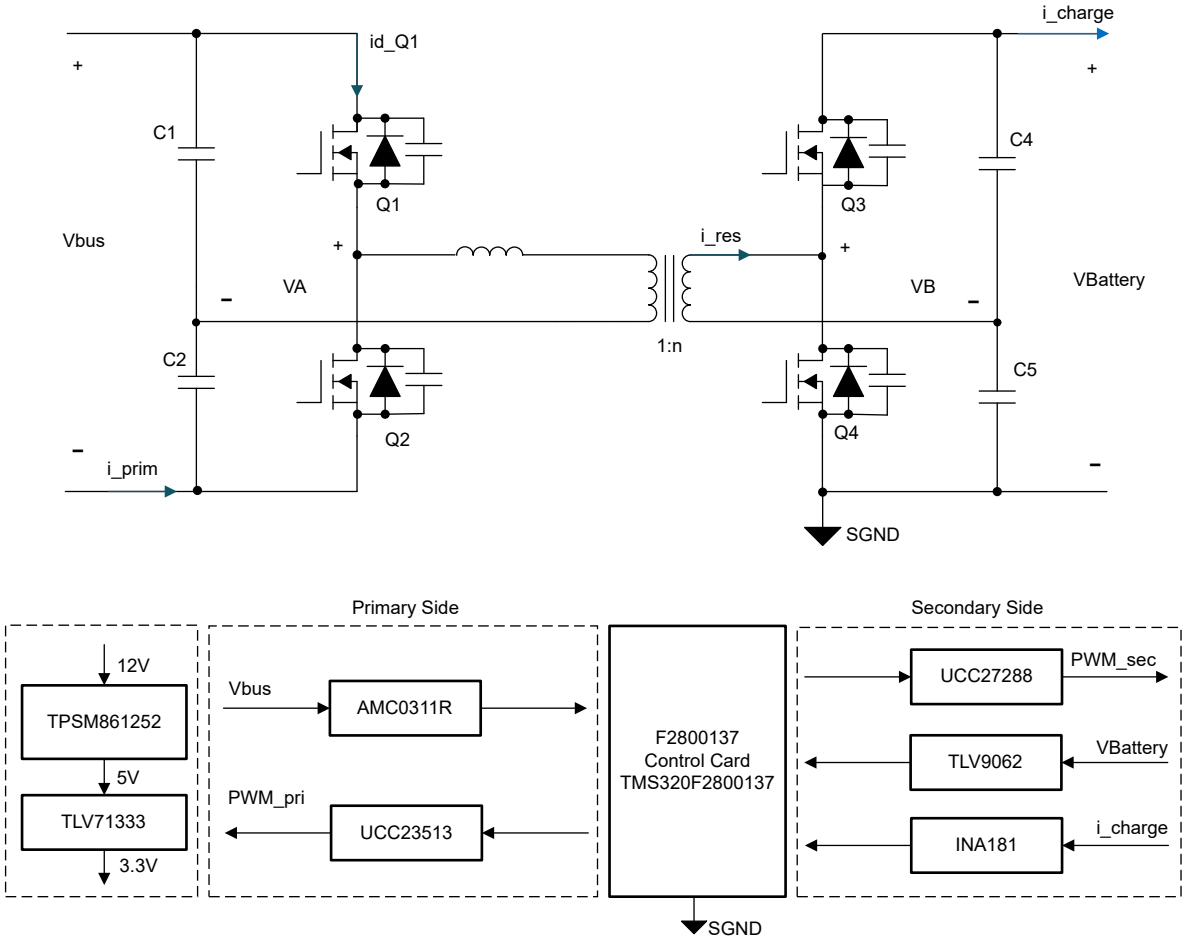


Figure 2-1. TIDA-010966 Block Diagram

2.2 Design Considerations

The following sections give an extensive overview of the dual-bridge series-resonant DC/DC converter.

2.2.1 Introduction

Dual-bridge series-resonant DC/DC converters (DBSRC) are an excellent choice for applications in which a bidirectional power flow is required, such as the battery-to-bus or battery-to-battery interfaces in ESS. The key features of DBSRCs include symmetrical structure, soft-switching, and step-up or step-down operation. Also, the resonant capacitor can filter the DC current and limit fault currents under abnormal operation.

For high power density and high-efficiency applications, soft switching of all active power devices is mandatory to provide a high efficiency, because hard switching causes additional switching losses. Furthermore, soft-switching reduces the electromagnetic interference by suppressing the rate of the voltage change (dv/dt) and enhances the converter reliability to avoid high-voltage ringing on power transistors.

Soft-switching implementation of DBSRC is especially challenging in the presence of wide I/O voltage variations and load ranges. With the traditional constant frequency phase-shift modulation (PSM), DBSRC are known to experience severe hard switching at light-to-intermediate load, even though optimized design methods are employed. To overcome this problem, advanced techniques, either hardware- or software-based, have been proposed to extend the soft-switching operation range. Hardware-based designs modify the resonant tank to provide the extended zero-voltage switching (ZVS) commutation current by adding extra passive or active auxiliary circuits. These designs require additional components and even gate drive circuitry, leading to an overall increase in the system cost and complexity.

This design proposed varying frequency modulation (VFM) plus phase-shift modulation (PSM) to provide full input range and full load range ZVS.

2.2.2 Basic Operation Principles and ZVS Requirements

Figure 2-2 shows the topology circuit of dual-bridge series-resonant DC/DC converter. Q1 and Q2 are complementary-turn-on with a 50% duty cycle, and Q3 and Q4 are the same. Changing the phase angles of Q1 and Q3, control the transmitting power. By doing this, the voltage measured by the primary and secondary bridge arms becomes a two-square wave, where the primary side is $\pm 1/2V_{bus}$ and the secondary side is $\pm 1/2V_{Battery}$ (without considering transformer ratio).

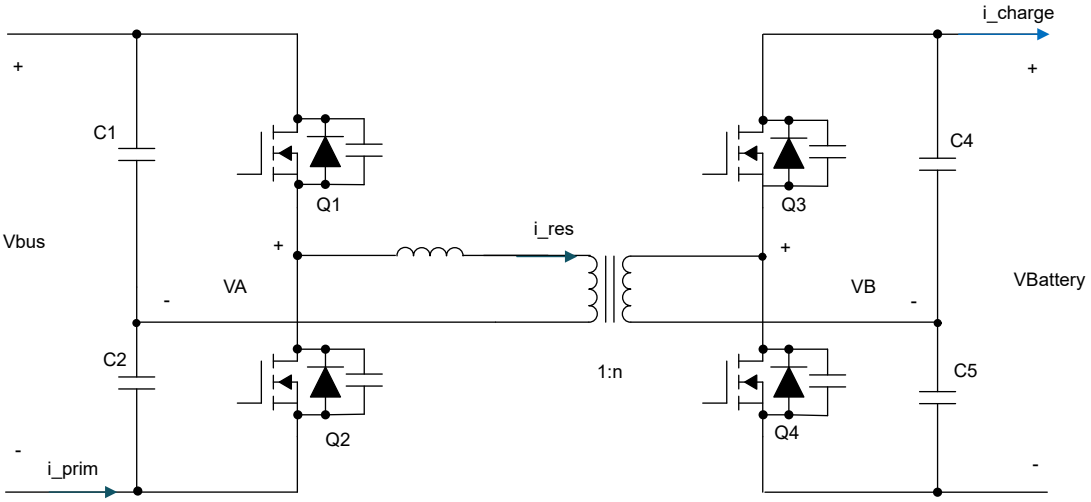


Figure 2-2. Topology Circuit of Dual-Bridge Series-Resonant DC/DC Converter

Figure 2-3 shows the equivalent circuit diagram where the voltage VA of the primary arm is ahead of the voltage VB of the secondary arm, and the power is transferred from the primary side to the secondary side. Figure 2-4 shows the opposite, where VA lags behind VB, so power is transferred from the secondary side to the primary side.

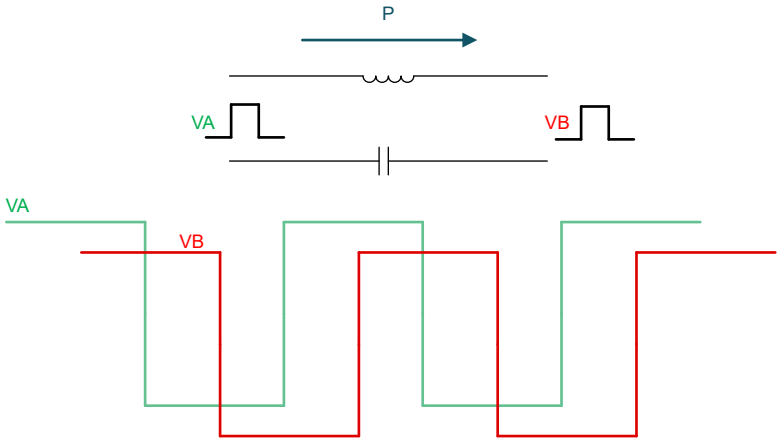


Figure 2-3. Equivalent Circuit Diagram

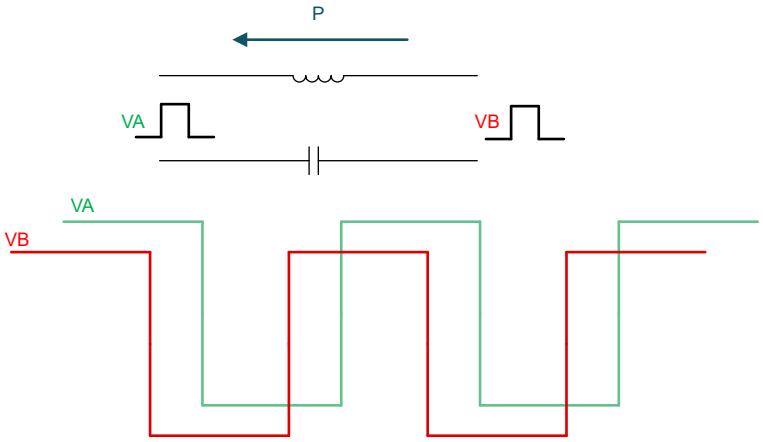


Figure 2-4. Power Secondary to Primary

Figure 2-5 shows the related waveforms for the DBSRC, primary bridge voltage VA, secondary bridge voltage VB and resonant current i_{res}. As shown in the figure, when Q1 is on, VA is positive. In Figure 2-5, t_0 is the moment when Q2 is turned off, and if Q1 wants to achieve ZVS, there needs to be a current to draw away the energy of the junction capacitors on Q1, and make the current flow through the body diode of Q1, as Figure 2-6 shows. That means that the current at time t_0 needs to be negative.

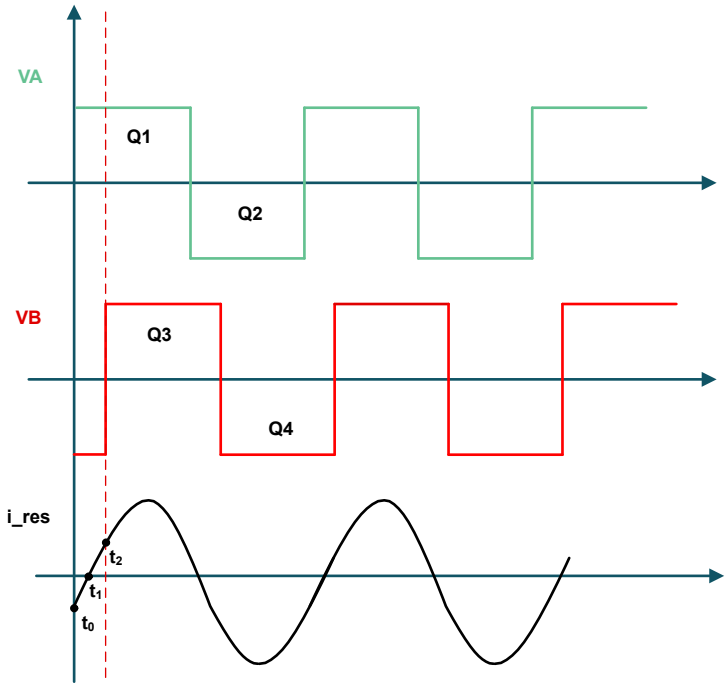


Figure 2-5. Bridge Waveforms

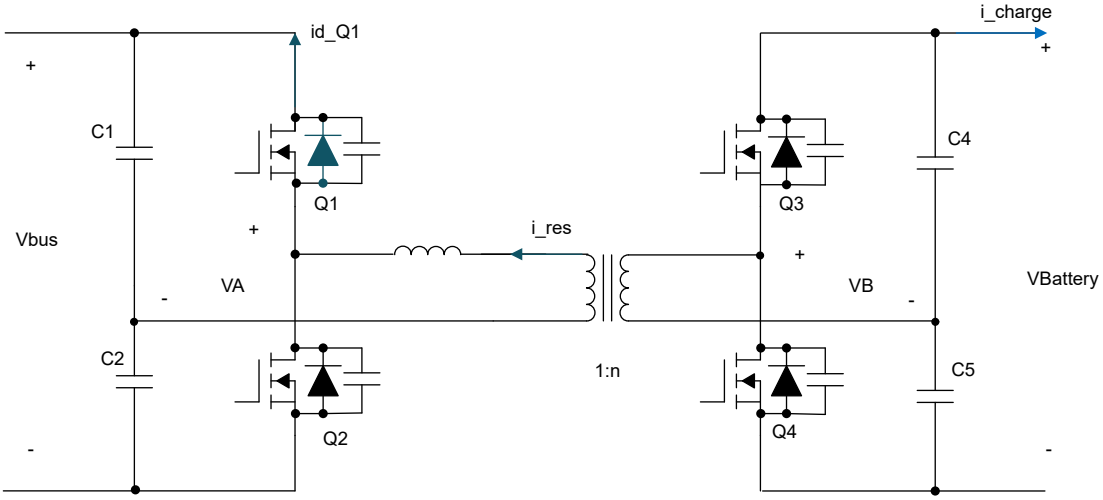


Figure 2-6. Current Flow Through Q1

In the same way, to realize the zero-voltage opening of the secondary side switch Q3, the current needs to be positive at t_2.

2.3 Highlighted Products

This section highlights the critical components of the design which include the gate driver, F2800137 controller, amplifiers for current and voltage sensing, and voltage references.

2.3.1 UCC27288

The UCC27288 is a robust N-channel MOSFET driver with a maximum switch node voltage rating of 100V. The device allows for two N-channel MOSFETs to be controlled in half-bridge or synchronous buck configuration based topologies. The 3A peak source and sink current along with low pullup and pulldown resistance allows the UCC27288 to drive large power MOSFETs with minimum switching losses during the transition of the MOSFET Miller plateau. Since the inputs are independent of the supply voltage, UCC27288 can be used in conjunction with both analog and digital controllers. Two inputs are completely independent of each other; therefore, added control design flexibility is provided.

The input pins as well as the HS pin are able to tolerate significant negative voltage, which improves system robustness. The inputs are completely independent of each other. This allows for control flexibility where two outputs can be overlapped by overlapping inputs, if needed. Small propagation delay and delay matching specifications minimize the dead-time requirement which improves system efficiency.

Undervoltage lockout (UVLO) is provided for both the high-side and low-side driver stages forcing the outputs low if the VDD voltage is below the specified threshold. No integrated bootstrap diode allows the designer to use application-appropriate external bootstrap diode. UCC27288 is offered in an SOIC8 package to improve system robustness in harsh environments.

2.3.2 UCC23513

The UCC23513 drivers are opto-compatible, single-channel, isolated gate drivers for IGBTs, MOSFETs, and SiC MOSFETs, with 4.5A source and 5.3A sink peak output current and 5.7kV_{RMS} reinforced isolation rating. The high supply-voltage range of 33V allows the use of bipolar supplies to effectively drive IGBTs and SiC power FETs. UCC23513 can drive both low-side and high-side power FETs. Key features and characteristics bring significant performance and reliability upgrades over standard optocoupler-based gate drivers while maintaining pin-to-pin compatibility in both schematic and layout design. Performance highlights include high common-mode transient immunity (CMTI), low propagation delay, and small pulse width distortion. Tight process control results in small part-to-part skew. The input stage is an emulated diode (e-diode) which means long-term reliability and excellent aging characteristics compared to traditional light-emitting diodes (LEDs). The device is offered in a stretched SO6 package with >8.5mm creepage and clearance, and a mold compound from material group I which has a comparative tracking index (CTI) >600V. The high performance and reliability of the UCC23513 makes this device an excellent choice for use in all types of motor drives, solar inverters, industrial power supplies, and appliances. The higher operating temperature opens up opportunities for applications not previously able to be supported by traditional optocouplers.

2.3.3 TMS320F2800137

The TMS320F280013x (F280013x) is a member of the C2000™ real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics.

The real-time control subsystem is based on TI's 32-bit C28x DSP core, which provides 120MHz of signal-processing performance for floating- or fixed-point code running from either on-chip flash or Static Random Access Memory (SRAM). The C28x CPU is further boosted by the Trigonometric Math Unit (TMU), speeding up common algorithms key to real-time control systems. The F280013x supports up to 256KB (128KW) of flash memory. Up to 36KB (18KW) of on-chip SRAM is also available to supplement the flash memory.

High-performance analog blocks are integrated into the F280013x real-time microcontroller (MCU) and are closely coupled with the processing and pulse width modulation (PWM) units to provide best-in-class real-time signal chain performance.

Fourteen PWM channels enable control of various power stages from a three-phase inverter to power-factor correction and other advanced multilevel power topologies. The voltage and current of the panel and string lines are used to calculate and track the maximum power point (MPP) and the TMS320F2800137 enables quick data acquisition from the various analog signals using the internal analog-to-digital converter (ADC), set to read from the ADC channels once every 40µs. Operating at 120MHz allows for fast conversion and calculation to efficiently

perform Maximum Power Point Tracking (MPPT) and adjust the duty cycle of the converter accordingly. The comparator subsystem (CMPSS) is also utilized to fast protect the converter from overvoltage, overcurrent, or overtemperature.

An enhanced pulse width modulator (ePWM) is used to generate the PWM for four switches. The high-resolution pulse width modulator (HRPWM) can be used to generate a three-level signal for AFE031, which can be used for Programmable Logic Controller (PLC) transmission function. The internal ADC is used to sample the RX signal at 300kHz to receive the PLC signals. An FSK decoding library (part of the C2000 ware) is used to decode the sampled signal.

Status indicators, controlled by the MCU, are also included in the design to provide feedback to the user.

2.3.4 TLV9062

The TLV9061 (single), TLV9062 (dual), and TLV9064 (quad) devices are single-, dual-, and quad low-voltage (1.8V to 5.5V) operational amplifiers (op amps) with rail-to-rail input and output swing capabilities.

These devices are highly cost-effective options for applications where low-voltage operation, a small footprint, and high capacitive load drive are required.

Although the capacitive load drive of the TLV906x is 100pF, the resistive open-loop output impedance makes stabilizing with higher capacitive loads simpler. These op amps are designed specifically for low-voltage operation (1.8V to 5.5V), with performance specifications similar to the OPAx316 and TLVx316 devices.

The TLV906xS devices include a shutdown mode that allow the amplifiers to switch into standby mode with typical current consumption less than 1µA.

The TLV906xS family helps simplify system design, because the family is unity-gain stable, integrates the RFI and EMI rejection filter, and provides no phase reversal in overdrive condition.

Micro-size packages, such as X2SON and X2QFN, are offered for all the channel variants (single, dual, and quad), along with industry-standard packages, such as SOIC, MSOP, SOT-23, and TSSOP.

2.3.5 INA181

The INA181, INA2181, and INA4181 (INAx181) current sense amplifiers are designed for cost-optimized applications. These devices are part of a family of bidirectional, current-sense amplifiers (also called current-shunt monitors) that sense voltage drops across current-sense resistors at common-mode voltages from –0.2V to +26V, independent of the supply voltage. The INAx181 family integrates a matched resistor gain network in four, fixed-gain device options: 20V/V, 50V/V, 100V/V, or 200V/V. This matched gain resistor network minimizes gain error and reduces the temperature drift.

These devices operate from a single 2.7V to 5.5V power supply. The single-channel INA181 draws a maximum supply current of 260µA; whereas, the dual-channel INA2181 draws a maximum supply current of 500µA, and the quad-channel INA4181 draws a maximum supply current of 900µA.

The INA181 is available in both the 6-pin, SOT-23 and SC70 packages. The INA2181 is available in 10-pin, VSSOP and WSON packages. The INA4181 is available in a 20-pin, TSSOP package. All device options are specified over the extended operating temperature range of –40°C to +125°C.

2.3.6 TPSM861252

The TPSM86125x is a simple, easy-to-use, high-efficiency, high-power density, synchronous buck module with an input voltage ranging from 3V to 17V, supporting up to 1A continuous current.

The TPSM86125x employs D-CAP3™ control mode to provide a fast transient response and to support low-ESR output capacitors with no requirement for external compensation. The device can support up to 95% duty-cycle operation.

The TPSM861252 operates in Eco-mode, which maintains high efficiency during light load. The TPSM861257 operates in forced continuous conduction mode (FCCM), which keeps the same frequency and lower output ripple during all load conditions. TPSM861253 is a fixed 3.3V output voltage part with FCCM mode. The device also integrates the divider resistors and a feedforward capacitor inside the module. The TPSM86125x integrates complete protection including OVP, OCP, UVLO, OTP, and UVP with hiccup.

The device is available in a QFN package. The junction temperature is specified from –40°C to 125°C.

2.3.7 AMC0311R

The AMC0x11R-Q1 is a precision, galvanically isolated amplifier with a 2.25V, high-impedance input and differential output. The high-impedance input is optimized for connection to high-impedance resistive dividers or other voltage signal sources with high output resistance.

The isolation barrier separates parts of the system that operate on different common-mode voltage levels. The isolation barrier is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation up to $5kV_{RMS}$ (DWV package) and basic isolation up to $3kV_{RMS}$ (D package) (60s).

The AMC0x11R-Q1 outputs a single-ended signal that is proportional to the input voltage. The full-scale output is set by the voltage applied to the REFIN pin. The output of the AMC0x11R-Q1 is designed to connect directly to the input of an ADC. Connect REFIN to the same reference voltage as the ADC to match the dynamic input voltage range of the ADC.

The AMC0x11R-Q1 devices come in 8-pin, wide- and narrow-body SOIC packages, and are fully specified over the temperature range from –40°C to +125°C

3 System Design Theory

3.1 Design Theory

3.1.1 Resonant Tank Design

The design of the DBSRC resonant tank is one of the most critical parts of the resonant converter. When designing the resonator, the first thing to consider is the design of the resonant frequency, which determines the approximate range of the switching frequency.

Since the switching frequency affects the volume of the passive components in one respect, and the switching loss of the system from another perspective, the resonant frequency f_r is selected as 80kHz after considering these two factors.

For the effective value of the resonator current, different resonant frequency and different combinations of resonant inductors and resonant capacitors do not affect the effective value of the resonator current under a certain load, which is analyzed in the following sections.

The smaller the resonant capacitor, the greater the voltage on the capacitor. The cost of the capacitor increases, and then after comprehensive consideration, the resonant inductance 2.1μH is selected, and the resonant capacitance is 1600nF. In the topological circuit diagram in Figure 3-1, the resonant capacitance (C_r) is composed of the primary side C_1, C_2 and the secondary side C_3 and C_4, as in Equation 1.

$$C_r = \frac{1}{\frac{1}{C_1 + C_2} + \frac{1}{n^2 \times (C_3 + C_4)}} \quad (1)$$

where

- $C_1 = C_2 = C_3 = C_4 = 1000nF$
- n is transformer ratio = 2

At this point, the peak-to-peak voltage on the capacitor is less than 100V.

3.1.2 Full-Range ZVS Realization

This section discusses how to achieve a full-range of ZVS under this DBSRC, related content is now filed for a U.S. patent.

Figure 3-1 and Figure 3-2 provide separate topology schematics and waveforms. In Figure 3-2, θ is the phase angle between Q1 and Q3. According to the analysis in the previous section, to achieve the zero voltage opening of the four switches on the primary and secondary side, t1 must be in the range of 0,θ.

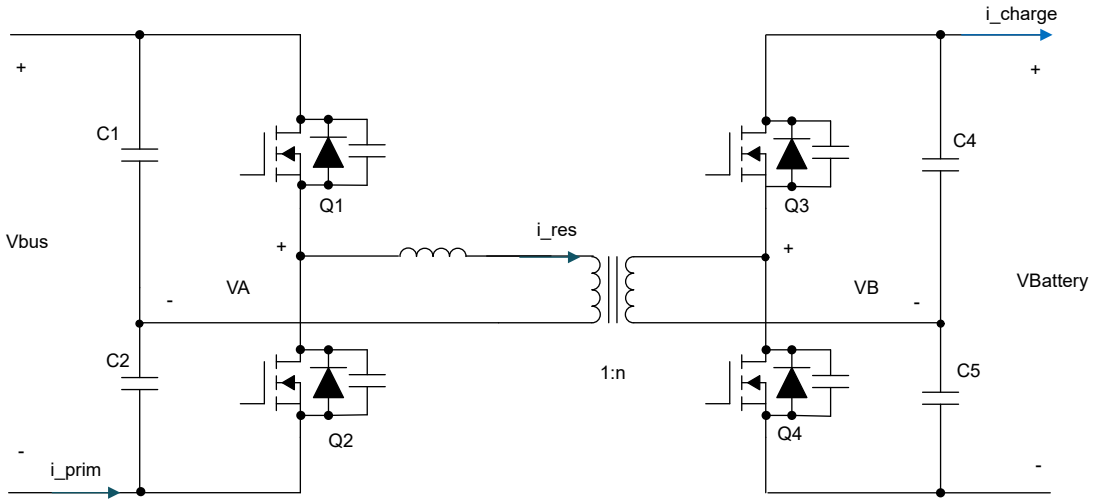


Figure 3-1. Topology Schematics

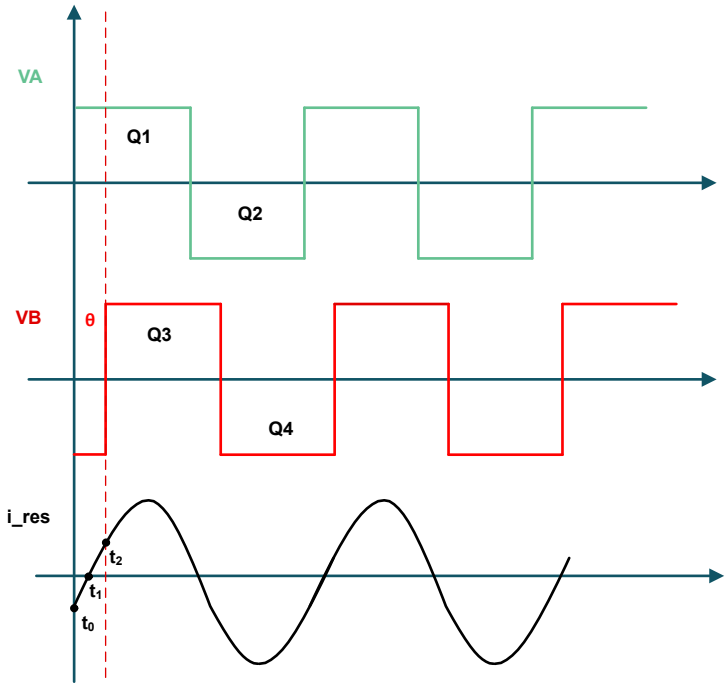


Figure 3-2. Topology Waveforms

Conventional single-phase-shift (SPS) control, as a single-degree-of-freedom control, θ is often used to control power transmission, so this is difficult to make sure that the soft-switching implementation conditions can be met in the full range. Based on this, another degree of freedom, switching frequency, is introduced into this design to provide the realization of a full range of soft switching, which is analyzed in detail in the rest of this topic.

Figure 3-2 shows the bridge voltage VA, VB and resonant current i_res, which is analyzed using the fundamental harmonic analysis (FHA) method, that is, only the fundamental waves of VA and VB are analyzed and normalized. After normalization, the expressions for VA and VB are respectively:

$$v_{\mathrm{A\_pu}}(\mathrm{t}) = \frac{4}{\pi}\sin(\omega \mathrm{t}) \tag{2}$$

$$v_{\mathrm{B\_pu}}(\mathrm{t}) = \frac{4\mathrm{M}}{\pi}\sin(\omega \mathrm{t} - \theta) \tag{3}$$

where

- M = $V_{Battery}$ / nV_{bus} = voltage gain
- Resonant current = Equation 4

$$\mathrm{i}_{\mathrm{res\_pu}}\left(\mathrm{t}\right) = \frac{v_{\mathrm{A\_pu}}(\mathrm{t}) - v_{\mathrm{B\_pu}}(\mathrm{t})}{\mathrm{X}_{\mathrm{res}}} \tag{4}$$

where *X*res represents the total impedance of the resonant network. The resonant tank consists of a series resonant inductor Lr and a resonant capacitor Cr. Since the current loop operates the system above the resonant frequency (fs > fr) to maintain an inductive tank for zero-voltage switching, the net fundamental inductive reactance Xres at any given switching frequency is defined as:

$$Xres = \omega Lr - \frac{1}{\omega Cr} > 0 \tag{5}$$

Using phasor analysis $v_{\mathrm{A\_pu}}(\mathrm{t})$ with as the reference phasor, the net voltage phasor driving the resonant tank is $\dot{V_A} - \dot{V_B}$. Solving the system equation $\dot{I_{res}} = (\dot{V_A} - \dot{V_B}) / jXres$ yields the rigorous time-domain fundamental resonant current $i_{\mathrm{res}}(\mathrm{t})$:

$$i_{\mathrm{res}}(\mathrm{t}) = \frac{2Vbus}{\pi \cdot Xres} \cdot \left[M \cdot \sin\theta \cdot \cos(\omega t) + (1 - M \cdot \cos\theta) \cdot \sin(\omega t)\right] \quad (6)$$

To solve for the precise moment the inductor current crosses zero $i_{\mathrm{res}}(\mathrm{t}) = 0$, we set the inner bracket of the time-domain current equation to zero:

$$M \cdot \sin\theta \cdot \cos(\omega t_{zero}) = -(1 - M \cdot \cos\theta) \cdot \sin(\omega t_{zero}) \quad (7)$$

Dividing both sides by $\cos(\omega t_{zero})$ yields the tangent relationship:

$$\tan(\omega t_{zero}) = \frac{-M\sin\theta}{1 - M\cos\theta} \quad (8)$$

Thus, the exact electrical angle at which the fundamental current crosses zero during the half-cycle is:

$$\omega t_{\mathrm{zero}} = \arctan\left(\frac{-M\sin\theta}{1 - M\cos\theta}\right) \quad (9)$$

To verify symmetrical switching current amplitudes and eliminate high circulating reactive currents when $M \neq 1$, your physical target is to position this zero-crossing point exactly at the midpoint between the primary turn-on instance t_0 ($\omega t_0 = 0$) and the secondary turn-on instance t_2 ($\omega t_2 = 0$) :

$$\omega t_{\mathrm{zero}} = \frac{0 + \theta}{2} = \frac{\theta}{2} \quad (10)$$

Substituting this target into the tangent relationship:

$$\frac{\sin\left(\frac{\theta}{2}\right)}{\cos\left(\frac{\theta}{2}\right)} = \frac{1 - M + 2M\sin^2\left(\frac{\theta}{2}\right)}{2M\sin\left(\frac{\theta}{2}\right)\cos\left(\frac{\theta}{2}\right)} \Rightarrow 0 = 1 - M \Rightarrow M = 1 \quad (11)$$

This mathematical proof reveals a critical hardware constraint of the Half-Bridge SPS architecture: **it is mathematically impossible to force the current zero-crossing point exactly to the midpoint** $(\theta/2)$ **when** $M \neq 1$ **.** Because a half-bridge cannot utilize an inner-phase shift angle to match the voltage amplitudes, the current waveform is naturally skewed. Forcing the system to stay at the absolute ZVS boundary creates massive reactive current stress on one side. Therefore, a dynamic tracking function must be established.

To resolve this conflict, we introduce a dynamic tracking factor $\lambda(M)$ that dictates the zero-crossing position relative to θ as a function of the real-time voltage gain M:

$$\omega_s t_{\mathrm{zero}} = \lambda(M) \cdot \theta \quad (12)$$

Where $\lambda(M) = \frac{1}{1 + M}$

- When **M = 1**, $\lambda(1) = 0.5$, forcing the zero-crossing to converge perfectly at the midpoint ($\omega_s t_{\mathrm{zero}} = 0.5\theta$).
- When **M > 1** (Boost mode), $\lambda < 0.5$, the zero-crossing smoothly shifts toward t_0 , securing primary ZVS while clamping down on excessive secondary peak currents.
- When **M < 1** (Buck mode), $\lambda > 0.5$, the zero-crossing smoothly shifts toward t_2 , securing secondary ZVS while preventing primary current spikes.

Substituting $\lambda(M)$ into our zero-crossing equation yields:

$$\tan\left(\frac{1}{1 + M}\theta\right) = \frac{1 - M\cos\theta}{M\sin\theta} \quad (13)$$

Since this expression is a transcendental equation, it cannot be solved analytically for θ .

To run this on a microcontroller (like the TI C2000 F28P55) with minimal computational latency, we perform a multi-point least-squares error minimization fitting against the strict mathematical bounds ($\theta_{\mathrm{strict}} = \arccos[\min(M, 1/M)]$) over the operational range $M \in [0.5, 2.0]$.

The optimized trajectory-tracking phase shift angle can be accurately generalized by a first-order absolute error envelope polynomial:

$$\theta_{\text{track}} = \arccos\left[\min\left(M, \frac{1}{M}\right)\right] \cdot (1 - 0.25 \cdot |M - 1|) \quad (14)$$

Considering the margin for deadtime and Coss of switches,

$$\theta_{\text{track}} = \arccos\left[0.8 \cdot \min\left(M, \frac{1}{M}\right)\right] \cdot (1 - 0.25 \cdot |M - 1|) \quad (15)$$

3.1.3 Total Control Algorithm

The previous section analyzed that to make sure all switches implement ZVS, let θ = $\arccos\left[0.8 \cdot \min\left(M, \frac{1}{M}\right)\right] \cdot (1 - 0.25 \cdot |M - 1|)$; however, for this topology, this is not only necessary to provide soft switching to optimize efficiency, but also to control the charge and discharge current, that is, control power. This reflects the limitations of traditional single-phase-shift, single-degree-of-freedom control, which makes this impossible to control the current if the phase-shift angle is fixed.

This design has a second degree of freedom that can be controlled – the switching frequency – when the phase-shift angle is taken as a ZVS constraint. That is, the switching frequency can be introduced into the current closed loop to control the charge and discharge current. Figure 3-3 shows the total control block diagram.

The two degrees of freedom are calculated separately, the first is the phase-shift angle θ, which is calculated by sensing the input voltage and the output voltage to calculate the voltage gain M. The phase-shift angle is calculated by the formula derived above, which is used to achieve ZVS.

Then is the switching frequency fs, fs is used to control the transferred power, which is generated by current loop. The charge/discharge current is sensed, and then the difference with the current reference value is made to generate an error signal, and then through a PI link, the PI output is used to calculate the switching frequency fs, which is used to control the power.

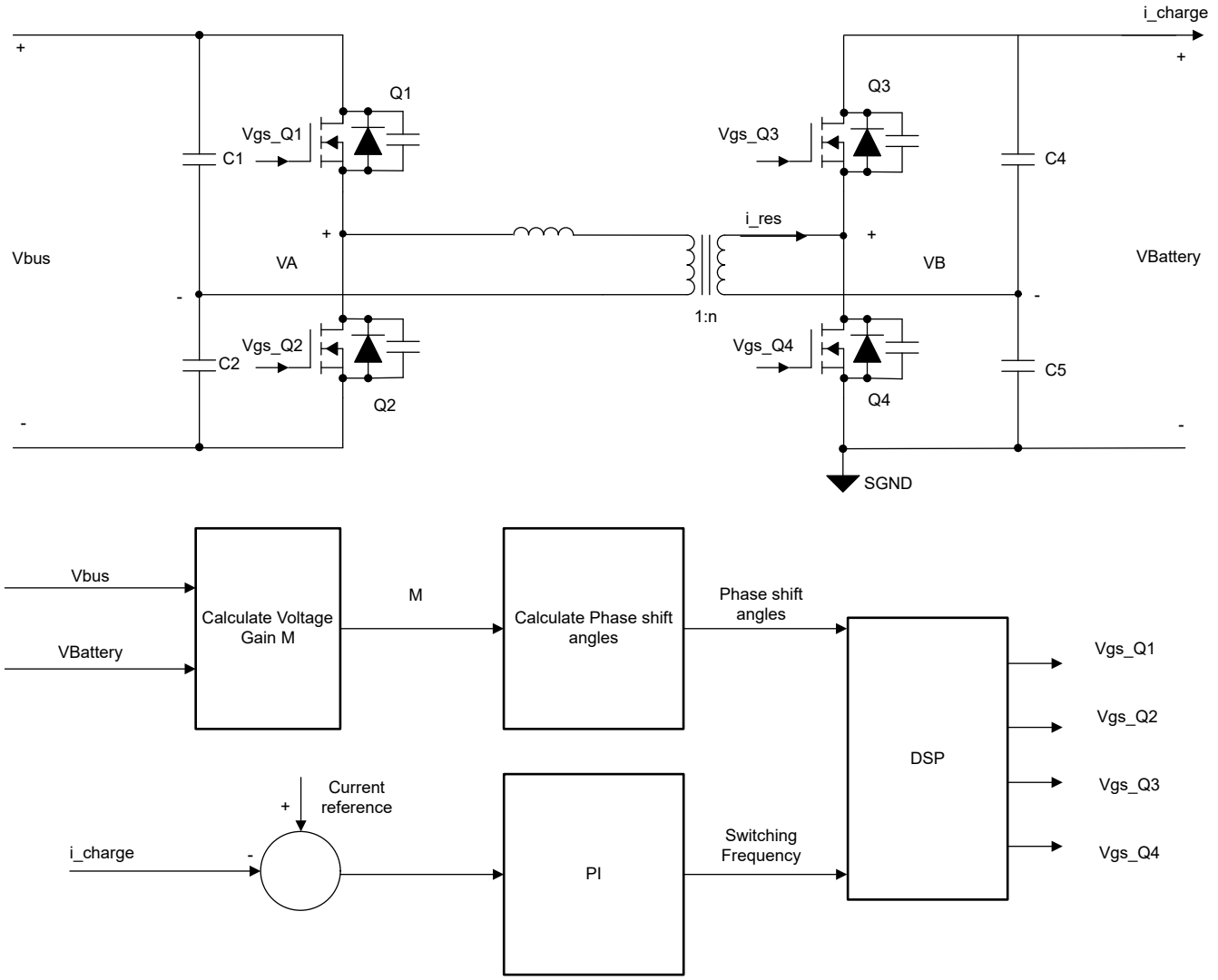


Figure 3-3. Total Control Block Diagram

3.1.4 Resonant Tank RMS Current Analysis

As Section 3.1.3 describes, the design of the resonator does not affect the RMS value of the resonator current. The resonator current is carefully analyzed in this section.

The normalized expression of the resonant current, $i_{res\_pu}(t)$, is obtained in Equation 4, so the expression of the effective value of the resonant current $i_{res\_rms\_pu}(t)$ can be calculated based on Equation 16.

$$i_{res\_rms\_pu}\left(t\right) = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}\left[i_{res\_pu}\left(t\right)\right]^2 \, d\,\omega t} = \frac{2\sqrt{2}}{\pi X_{res}}\sqrt{M^2 - 2M\cos\theta + 1} \tag{16}$$

This expression shows that the current RMS value of the resonant tank is related to resonant impedance X_{res}, phase shift angle θ, and voltage gain M, and the resonant impedance X_{res} is related to the switching frequency and resonant design. At this time, this can be seen that the effective current value of the resonant tank is related to a variety of factors, and this seems that this is inconsistent with the previously provided analysis.

The average output power P_{o_pu} and output current I_{o_pu} of the converter can be calculated using the primary-side or secondary-side bridge voltage (that is, $v_{A\_pu}(t)$ or $v_{B\_pu}(t)$) and tank current $i_{res\_pu}(t)$.

$$P_{o\_pu}\left(t\right) = \frac{1}{2\pi}\int_0^{2\pi} V_{A\_pu}\left(t\right) i_{res\_pu}\left(t\right) \, d\,t = \frac{8M}{\pi^2 X_{res}}\sin\theta \tag{17}$$

$$I_{o\_pu}\left(t\right) = \frac{8}{\pi^2 X_{res}}\sin\theta \tag{18}$$

The resonant tank impedance X_{res} can be obtained from the output current I_{o_pu} expression Equation 19.

$$X_{res} = \frac{8}{\pi^2 I_{o\_pu}\left(t\right)}\sin\theta \tag{19}$$

Bring this into the expression of the effective value of the resonant current $i_{res\_rms\_pu}(t)$, and can get Equation 20.

$$i_{res\_rms\_pu}\left(t\right) = \frac{2\sqrt{2}}{\pi X_{res}}\sqrt{M^2 - 2M\cos\theta + 1} = \frac{\pi I_{o\_pu}\left(t\right)}{2\sqrt{2}\sin\theta}\sqrt{M^2 - 2M\cos\theta + 1} \tag{20}$$

The latest expression shows that the effective current value of the resonant tank $i_{res\_rms\_pu}(t)$ is only related to the output current I_{o_pu}, voltage gain M, and phase shift angle θ at this time. Because the phase shift angle θ is determined, the RMS current value at this time is only related to the input and output voltage and the output current at this time. This can be understood that under a certain input and output, the power level is determined, and the current RMS value is also determined.

3.2 Hardware Design Theory

This section discuss hardware-related selection, and schematic PCB design, as well as the design of input and output capacitors, for example.

3.2.1 Resonant Capacitors

Resonant capacitors need to operate at a high switching frequency. Conventional resonant capacitors typically use film capacitors because of good high-frequency characteristics, withstand voltage characteristics, and excellent reliability.

Multilayer Ceramic Capacitors (MLCC) can also be used as resonant capacitors, and the advantage of using MLCC is that these are small in size and relatively small in loss, but MLCC are not very reliable and are easily damaged. Also MLCC are more expensive than film capacitors.

This design uses MLCC for high efficiency and high power density requirements.

3.2.2 Power Stage

Figure 3-4 shows the power stage of the bidirectional isolated dual-bridge series resonant DC/DC converter. The primary side consists of a 80V, 4.1mΩ, N-channel, NexFET™ power MOSFET CSD19502Q5B to block a DC voltage of 24V, and the secondary side consists of a 100V, 14.5mΩ, N-channel NexFET™ power MOSFET CSD19537Q3 to block DC voltage of 60V. There are two switches on each side of the primary and secondary sides to form a half-bridge, and the other set of bridge arms is composed of resonant capacitors.

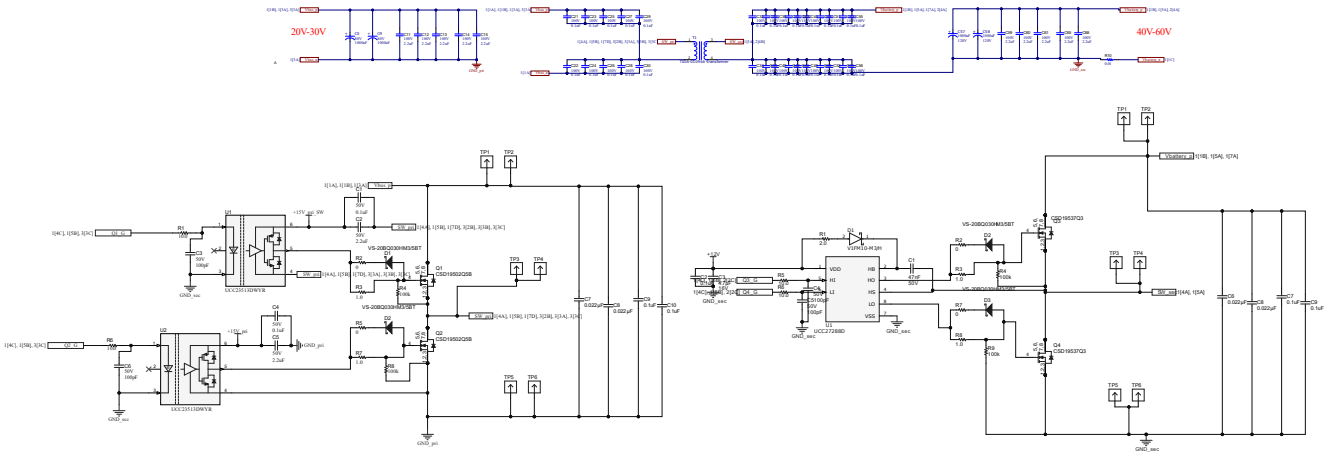


Figure 3-4. Power Stage of Bidirectional Isolated Dual-Bridge Series Resonant DC/DC Converter

The full bridges are connected with a high-frequency transformer with integrated leakage inductance (T1).

3.2.3 Voltage Sensing

This design needs to sense input voltage to perform a constant voltage loop when in reverse mode. The primary DC voltage needs to be sensed.

Figure 3-5 shows the primary voltage sensing circuit. The maximum primary bus voltage to be sensed is 30V, and MCU is put on secondary side. Therefore, choose AMC0311R to sense the primary side DC voltage.

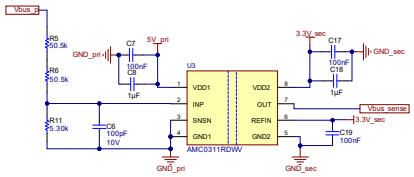


Figure 3-5. Primary Voltage Sensing Circuit

Figure 3-6 shows the secondary voltage sensing circuit. The maximum secondary battery voltage to be sensed is 60V and is scaled down by a resistor divider network to 2.07V, which is compatible to the 3.3V input of the TLV9062.

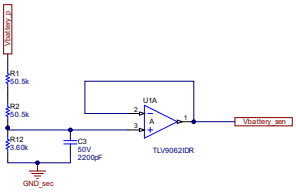


Figure 3-6. Secondary Voltage Sensing Circuit

3.2.4 Current Sensing

Regardless of whether running the design in the forward or reverse mode, this design needs to sense the input current to do constant current loop. The primary-side current must be sensed. Due to the need for the system to operate in both directions, there are two directions in the direction of the input current.

Figure 3-7 shows the primary current sensing circuit. INA181 is used to sense bidirectional current. Select a 1mΩ sampling resistor placed at the low side, the current is less than 20A, so that means the limit of the common-mode voltage is –0.2V to 26V.

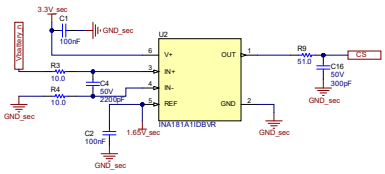


Figure 3-7. Primary Current Sensing Circuit

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Hardware Requirements

The following hardware is required for this reference design:

- One TIDA-010966 power board
- One TMDSCNCD2800137 control card
- USB Type-C® cable
- Laptop

The following test equipment is needed to power and evaluate the DUT:

- DC source capable of delivering voltage between 0V–100V at required current
- Electronic loads, which can support CV and CC modes
- Power analyzer
- Auxiliary power supply
- Oscilloscope
- Isolated voltage probes and current probes

4.2 Software Requirements

4.2.1 Simulation

To support evaluation of this reference design, a PLECS simulation deck is provided in the TIDA-010966 tool folder. This simulation can be used to evaluate the 2-D control method. The simulation is available for PLECS standalone.

4.3 Test Setup

To test the efficiency of this reference design, use the setup shown in Figure 4-1.

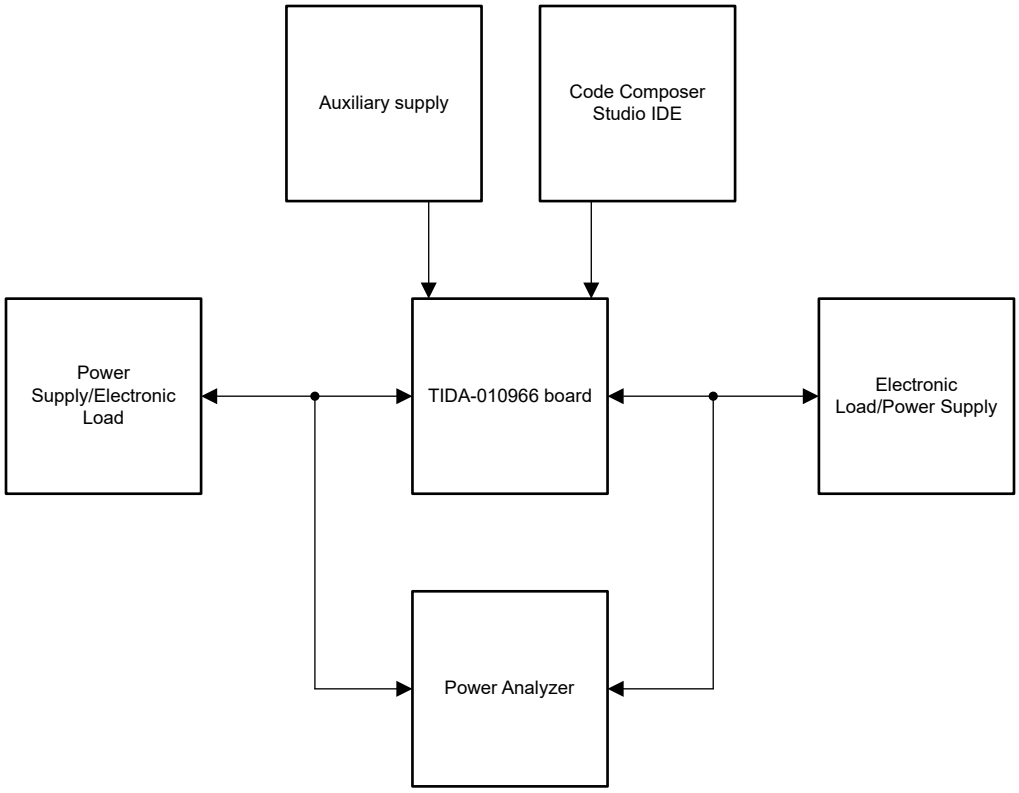


Figure 4-1. Test Setup

- As a bidirectional converter, both the input and output need to connect to a source and a load, where the voltage source and load need to support 300W (24V|40V to 60V).
- Auxiliary power supply to provide one channel for 12V, 1A and two channels for 15V, 1A
- One TMDSCNCD2800137 control card
- Power analyzer
- Oscilloscope with isolated probes for voltage and current

Figure 4-2 shows the board image.

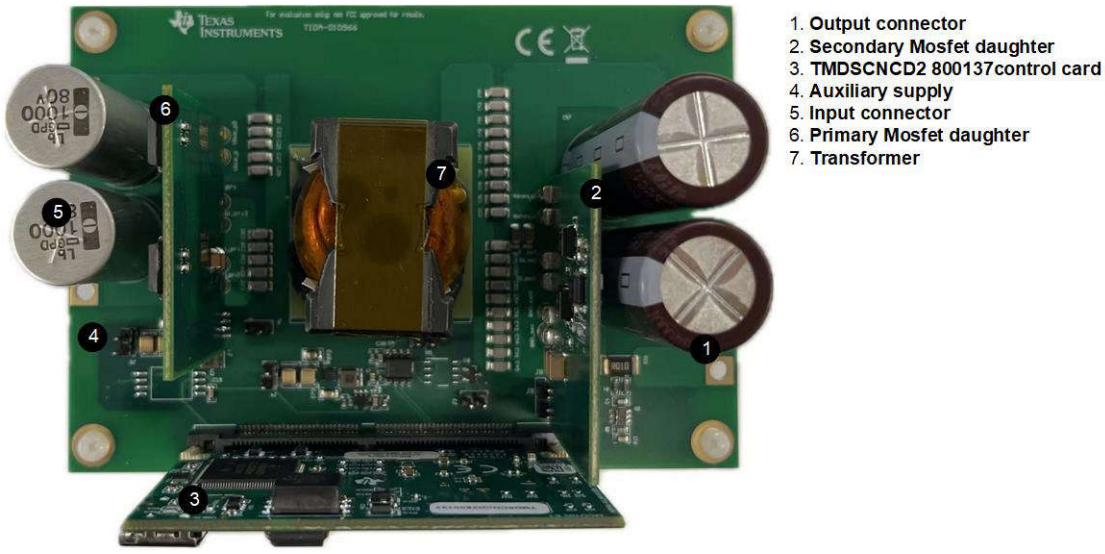


Figure 4-2. TIDA-010966 Board

4.4 Test Results

Figure 4-3 shows the typical waveforms for the SR-DAB, green is the primary bridge voltage VA, and the blue is the resonant current ires.

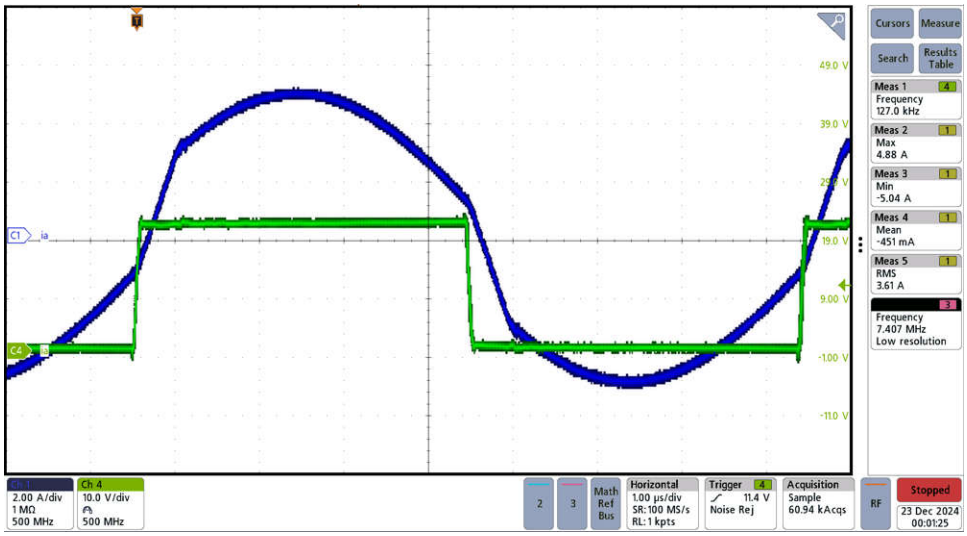


Figure 4-3. Typical Waveforms for SR-DAB

Figure 4-4 and Figure 4-5 show the efficiency curves for different inputs and outputs in forward and reverse working modes.

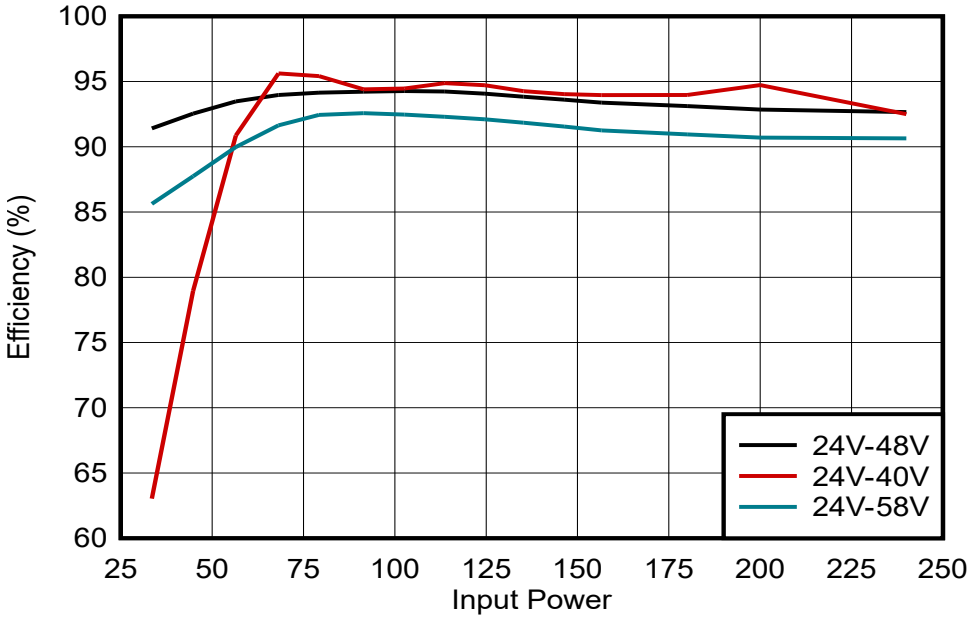


Figure 4-4. Efficiency Curves in Forward Mode

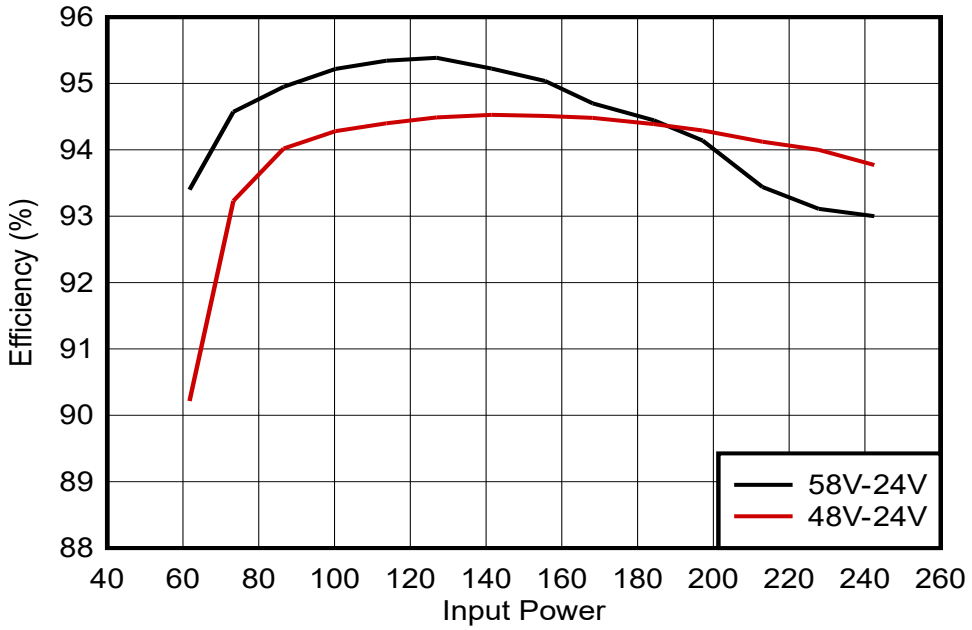


Figure 4-5. Efficiency Curves in Reverse Mode

5 Design and Documentation Support

5.1 Design Files

5.1.1 Schematics

To download the schematics, see the design files at TIDA-010966.

5.1.2 BOM

To download the bill of materials (BOM), see the design files at TIDA-010966.

5.1.3 PCB Layout Recommendations

5.1.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010966.

5.2 Tools

C2000WARE Software Development Kit (SDK)	C2000Ware for C2000 MCUs. C2000Ware is a cohesive set of software and documentation created to minimize development time. It includes device-specific drivers, libraries, and peripheral examples.

5.3 Documentation Support

1. Texas Instruments, *UCC27288 3A 120V Half-Bridge Driver With 8V UVLO and External Bootstrap Diode Data Sheet*
2. Texas Instruments, *UCC23513, 4A Source, 5A Sink, 5.7kV$_{RMS}$ Opto-Compatible Single-Channel Isolated Gate Driver Data Sheet*
3. Texas Instruments, *TMS320F280013x Real-Time Microcontrollers Data Sheet*
4. Texas Instruments, *TLV906xS 10MHz, RRIO, CMOS Operational Amplifiers for Cost-Sensitive Systems Data Sheet*
5. Texas Instruments, *INAx181 Bidirectional, Low- and High-Side Voltage Output, Current-Sense Amplifiers Data Sheet*
6. Texas Instruments, *TPSM86125x 3V to 17V Input, 1A, Synchronous Buck Module in QFN Package Data Sheet*
7. IEEE.org, *A Four-Degrees-of-Freedom Modulation Strategy for Dual-Active-Bridge Series-Resonant Converter Designed for Total Loss Minimization*

5.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

5.5 Trademarks

E2E™, D-CAP3™, and TI E2E™ are trademarks of Texas Instruments.
USB Type-C® is a registered trademark of USB Implementers Forum.
All trademarks are the property of their respective owners.

6 About the Author

WILL TAI is working as systems engineer focusing on Energy Storage System in Grid Infrastructure, where he is responsible for power conversion system and cell balance and pack balance designs. Before joining TI, he received his master's degree in electrical engineering at the University for Nanjing University of Aeronautics and Astronautics.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (July 2025) to Revision A (June 2026)	Page
• Made changes to the control algorithm	19

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025