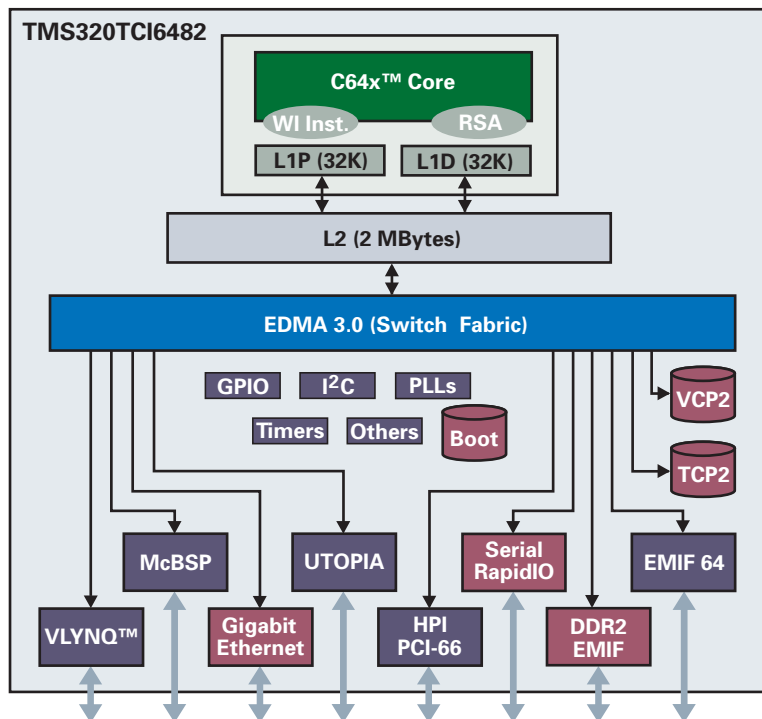*Product Bulletin – Wireless Infrastructure*

TMS320TCI6482 High Performance, Low Power, Programmable DSP for Wireless Base Stations

Optimized Baseband Architecture for Base Stations

The TMS320TCI6482 (TCI6482) Digital Signal Processor (DSP) for wireless infrastructure applications provides a power-efficient platform for multi-standard, soft digital baseband solutions in wireless base stations. The TCI6482 has the latest TMS320C64x™ DSP core based on TI's advanced very long instruction word (VLIW) architecture, which can perform up to eight 32-bit instructions during every cycle (cycle time is 1ns). On top of the 1 Gigahertz (GHz) performance of the basic architecture, the TCI6482 has added new extensions that facilitate code size reduction and the processing of complex arithmetic and bit manipulation functions across wireless standards. Among these enhancements are:

Key Features
- Leverages industry-leading 90nm process technology
- Leading power efficiency:
  ○ Approximately 3 watts or less
- 28 new instructions improve baseband performance
- Industry's first DSP with serial RapidIO™
- Unprecedented integration:
  ○ 3GPP/3GPP2 compliant Turbo and Viterbi co-processors
  ○ Four 1x serial RapidIO interfaces (12.5 Gbps maximum performance throughput)
  ○ 10/100/1000 Ethernet MAC, UTOPIA
- New Rake, RACH, Search and Spread Assist instruction set extension for complex correlation functions required in CDMA base standards
- High-performance memory sub-system:
  ○ 2 MB of L2 memory
  ○ DDR2 external memory interface

TMS320TCI6482

C64x™ Core
WI Inst.   RSA
L1P (32K)   L1D (32K)
L2 (2 MBytes)
EDMA 3.0 (Switch Fabric)
GPIO   I²C   PLLs   VCP2
Timers   Others   Boot   TCP2
McBSP   UTOPIA   Serial RapidIO   EMIF 64
VLYNQ™   Gigabit Ethernet   HPI PCI-66   DDR2 EMIF

The TMS320TCI6482 DSP offers the best combination of power efficiency and high performance for soft digital baseband processing in wireless infrastructure equipment.

- A dedicated software pipelined loop buffer (SPLOOP) instruction that reduces VLIW code size and allows fully optimized code to be interrupted
- Compact 32- and 16-bit instructions that reduce code size
- New wireless infrastructure DSP instructions such as packing, sorting, bit manipulation and Galois field multiplications:
  ○ New Complex Multiply (CMPY) instruction to improve Chip and Symbol rate performance
- Instruction set extension for correlation functions required for CDMA base standards

TCI6482 Improves Performance in Wireless Applications

Included in the core architecture is a new feature for Rake, RACH, Search and Spread Assist (RSA) which helps applications primarily using CDMA standards. CDMA standards are among the most difficult to implement on a DSP and traditionally have been based on an ASIC or FPGA. The TCI6482, seamlessly performs complex multiply accumulate functions found in CDMA resulting in higher channel density while maintaining an all soft implementation. As a result, the TCI6482 addresses the requirements of CDMA systems more successfully than any previous DSP solution.

Twenty-eight new instructions have been added to the TCI6482 to improve performance in wireless infrastructure applications. These instructions improve performance for Symbol Rate and Chip Rate processing found in 3rd Generation (3G) wireless standards, matrix operations found in TD-SCDMA and GSM-EDGE equalizer applications, and FFT/IFFT operations found in OFDM applications such as 802.16. These instructions show as much as a 30 percent improvement over the current C64x™ core in key wireless infrastructure benchmarks. Because the TCI6482 is a member of TI's C64x DSP family, the leading architecture used in 3G wireless base station systems, OEMs can re-use their existing software code base and evolve their system architectures, resulting in a time-to-market advantage.

High Performance and Low Power for an Efficient, High-Density Platform

Operating at 1 GHz and performing up to 8000 million instructions per second (MIPS) with a 1ns instruction cycle, the TCI6482 consumes approximately 3 Watts when operating at full speed. It is capable of 8- x 16-bit complex MACs (4 real, 4 imaginary) per cycle for a total of 8000 MMACs. These figures represent nearly twice the performance and less than half the power consumed versus other DSPs aimed at soft baseband implementations.

This outstanding performance/power consumption ratio makes it practical to use the DSP soft baseband approach out of the laboratory and in real-world applications. Equipment manufacturers can design more devices on a single board without causing thermal problems and pack more features and channels into the same cabinet. The combination enables service providers to lower their operating costs and offer additional services to their customers.

As an example, the TCI6482 can easily support three full TD-SCDMA carriers on a single channel card, leading to the lowest cost and lowest power TD-SCDMA solution.

Greater Connectivity for Board Level Efficiency

The TCI6482 wireless infrastructure processor is the industry's first DSP to feature a serial RapidIO™ interface, designed to add scalable connectivity and control among processing components in embedded systems. This high-speed, peer-to-peer interconnection fabric helps to lower system cost by providing a low pin count standard-based serial interface that eliminates the need for glue logic. Low latency and reduced overhead for packet processing improves system performance by simplifying the distribution of tasks across serial RapidIO enabled processing elements.
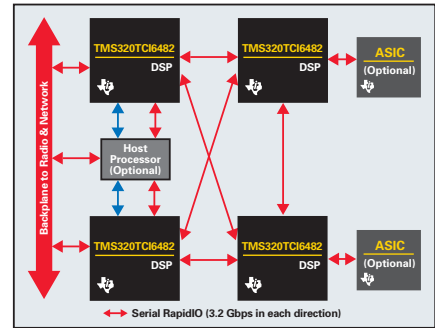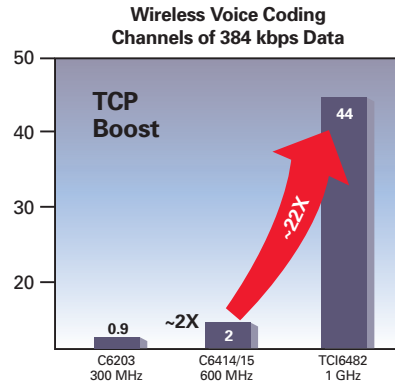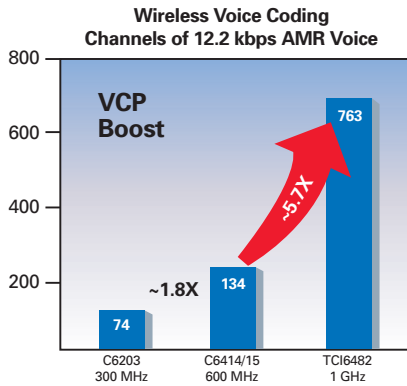

Serial RapidIO enables efficient BTS communication.

The Gigabit Ethernet Media Access Control (MAC) enables the TCI6482 to communicate directly with the network in order to support TCP/IP stacks, User Datagram Protocol (UDP) termination and other network control applications. The Ethernet MAC supports MII, RMII, GMII and RGMII physical interfaces, allowing a wide variety of connectivity choices.

Other interfaces that provide flexibility for wireless infrastructure includes Universal Test and Operations Interface for Asynchronous Transfer Mode (UTOPIA), Peripheral Control Interface (PCI), Host Peripheral Interface (HPI) and general purpose I/O (GPIO). An Enhanced Direct Memory Access (EDMA) controller, more advanced than any other C64x DSP, functions as a low-latency crossbar connecting all modules with seamless arbitration. It features a high-speed, 64-channel read/write transfer controller synchronized to system events.

Integrated Coprocessors

In addition, the highly integrated TCI6482 DSP provides many advanced features for greater flexibility in designing wireless system hardware and software. Included on chip is an enhanced Viterbi decoder coprocessor (VCP2) and an enhanced Turbo

Wireless Voice Coding Channels of 12.2 kbps AMR Voice

VCP Boost

- C6203 300 MHz: 74
- C6414/15 600 MHz: 134 (~1.8X)
- TCI6482 1 GHz: 763 (~5.7X)

Wireless Voice Coding Channels of 384 kbps Data

TCP Boost

- C6203 300 MHz: 0.9
- C6414/15 600 MHz: 2 (~2X)
- TCI6482 1 GHz: 44 (~22X)

TI's industry specific enablers maximize 3G wireless performance and services.

decoder coprocessor (TCP2), both of which significantly speed up channel decoding operations. The VCP2 can decode more than 763 adaptive multi-rate (AMR) voice channels at 12.2 Kbps; and the TCP2 can decode up to 44 turbo encoded 384 kbps data channels or eight 2 Mbps turbo encoded channels. The VCP2 and TCP2 are designed to support most cellular standards including GSM-EDGE, UMTS (3GPP), TD-SCDMA and CDMA2000 (3GPP2).

Generous Memory Subsystem
The TCI6482 memory sub-system has 2 MBs of on chip memory to support the high performance of the DSP core. It also has Layer1 program (L1P) and Layer1 data (L1D) scalable cache memory with sizes of 4, 8, 16 and 32 K for added flexibility. The Internal Direct Memory Access (IDMA) supports dynamic pre-loading of critical code mapped to L1 from L2, freeing the CPU from the data movement task which increases density and lower cost per channel. The TCI6482 also has memory protection to prevent rogue processes from overwriting user selected areas of memory. This feature allows for a more stable system during software development, contributes to shortened time spent in debug and helps to improve time-to-market.

Standards and Applications
With designs based on the TCI6482 DSP, wireless infrastructure equipment manufacturers can use a single hardware platform for many different applications, saving development time and costs in new designs, as well as allowing existing products to be upgraded quickly and efficiently. Among the many standards, features and applications supported by the TCI6482 DSP are:

Wireless Standards
- TD-SCDMA
- UMTS (3GPP)
- CDMA2K (EV-DO, EV-DV)
- GSM-EDGE
- 802.16

Applications
- Macro and micro base stations
- Pico and other small form factor base stations
- HSPDA
- MAC-HS
- OFDM based applications
- TCP/IP

Worldwide Support and Manufacturing
Tools and application software from TI and the industry's largest DSP third-party network provide in-depth support that helps to speed up development and reduce time-to-market. TI's Code Composer Studio™ Integrated

Development Environment (IDE), the most advanced DSP IDE available, provides proven tools and a familiar look and feel for programmers. A range of application software optimized for C6000™ family DSPs is available and rapidly increasing.

Developers in all regions can rely on TI's long-term expertise with many wireless network standards. And TI's leadership in 90nm process technology and manufacturing presence throughout the world assures quality and steady supply when it comes to a volume production.

For More Information
To learn more about the TMS320TCI6482 DSP—or other wireless solutions from TI—visit **www.ti.com/wi** Find out how the TCI6482 software baseband processor can add flexibility and performance to your next wireless infrastructure design.

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