

TMS320TCI6487

1.2 GHz DSP Platform



Product Bulletin

The TMS320TCI6487 (TCI6487) 1.2 GHz device is a very high-performance DSP designed specifically for wireless infrastructure baseband applications. With a high level of functional integration and a high channel density supported on a single device, the TCI6487 DSP offers a modular and scalable design with a small footprint. The TCI6487 DSP is therefore an ideal solution for pico, micro and macro base transceiver stations and enables an SOC baseband solution for UMTS, TD-SCDMA, WiMAX, GSM/EDGE and cdma2000 applications. OEMs can accelerate their channel card development with the use of the TCI6487 DSP, since it offers a software-programmable solution and allows for the reuse of existing C64x™ and C64x+™ DSP code. Advanced features such as MIMO, beamforming and Parallel Interface Cancellation (PIC) can be easily supported without the need for any hardware redesign.

Key Benefits

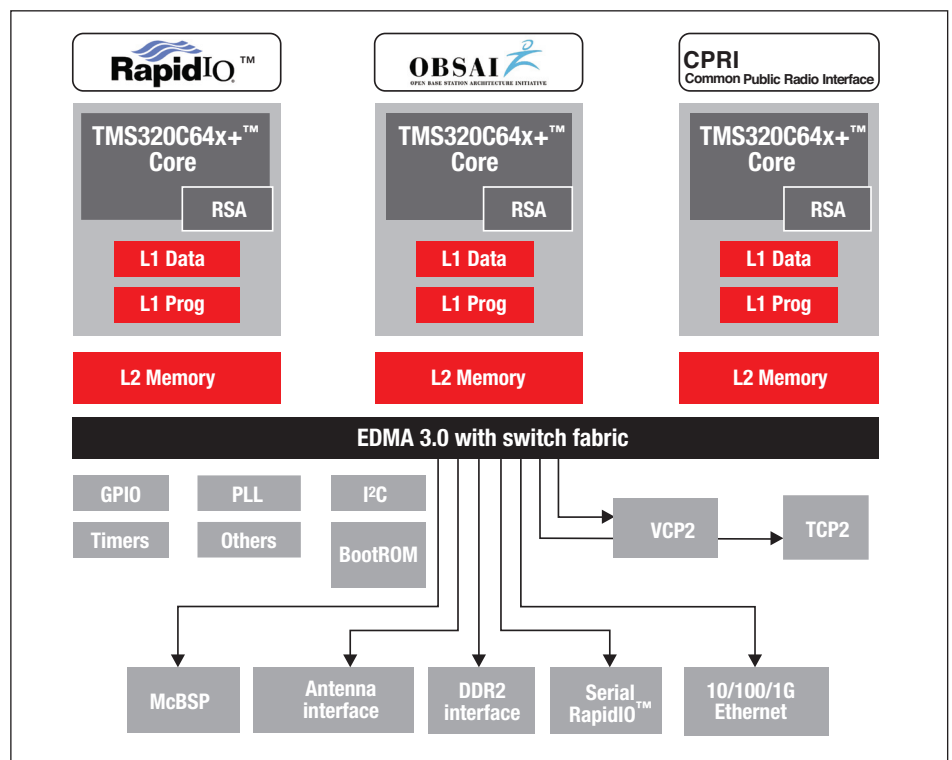
- Multi-standard SOC platform
- SOC baseband solution for LTE, TD-SCDMA, WiMAX, GSM/EDGE cdma2000 and UMTS Tx
- Scalable platform
- Modular design is ideal for pico, micro and macro BTS
- Quick time to market
- Software-programmable solutions with the reuse of existing software leads to a shorter development cycle
- Cost optimization
- Functional integration leads to lower system cost and eliminates the need for accelerator ASICs

TCI6487 DSP Architecture

The TCI6487 high-performance DSP has three independent DSP subsystems. At the heart of each subsystem is a 1.2-GHz C64x+ DSP core. The DSP includes 3 Mbytes of L2 SRAM/cache which are configured among the three cores either as 1/1/1 Mbytes or 1.5/1/0.5 Mbytes. To support wireless applications, the DSP contains a number of specialized coprocessors:

- Viterbi Decoder Coprocessor (VCP2)
- Turbo Code Decoder Coprocessor (TCP2)
- Rake Search/Spread Accelerator (RSA)

The TCP2 coprocessor can decode up to 20 Mbps for all wireless standards including LTE. This helps enable cost efficient systems that are completely software programmable and allows the TCI6487 to serve as the main engine for multi-standard baseband implementations.



▲ Figure1: 1.2 GHz TCI6487 block diagram

The RSA is a tightly coupled coprocessor that can be used to accelerate CDMA chip-rate processing. It can also be used in some 3G and 4G control channel decoding applications. Another important feature of the device is its support of standard interfaces such as Serial

Key Features

- Three integrated C64x+ cores running at 1.2 GHz on a single die
- 3.6 GHz of raw DSP processing power
- 28.8 GMACS (16-bit) in measured performance
- 3 Mbytes of on-chip L2 SRAM/cache
- 100% code compatible with other TI C64x and C64x+ based devices
- Rake Search Accelerator on all three DSP cores
 - Enables high-performance transmit chip-rate processing
 - Enables high-performance RACH preamble detection solution
 - Enables high-performance Reed-Muller decoding
- Industry-leading 65-nm silicon technology
 - Enables a high level of functional integration on a single device
 - Enables a high-channel-density solution
- Software-programmable resources
 - Enables the reuse of MIPS and memory resources on the DSP for various types of functionality
- Standard interfaces
 - SGMII Gigabit Ethernet, DDR2, two serial RapidIO (SRIO) links, McBSP, I²C, GPIO
- Debug interface
 - EMU/trace
- C64+ code compliance
- Antenna interfaces: OBSAI and CPRI standards compliant antenna interface

Advanced features supported/enabled

- MIMO
- Fixed and adaptive beamforming (on both uplink and downlink)
- Parallel interference cancellation

Interfaces

TCI6487 supports standard antenna, network, device and inter-device communication interfaces as well as a high-speed interface to communicate with external memory.

Antenna Interface

Six configurable (full-duplex) links in either OBSAI or CPRI modes that can support a variety of data rates. Supports OBSAI/CPRI daisy chaining between DSPs.

The EDMA 3.0 switch-fabric engine supports high-bandwidth, low-latency internal communications. The EDMA manages communications between peripherals, memories, accelerators and DSP cores.

- OBSAI—614.4-Mbps, 1.2288-Gbps, 2.4576-Gbps link rates supported
- CPRI—768-Mbps, 1.536-Gbps, 3.072-Gbps link rates supported

Network Interface

- 10/100/1000 Ethernet (SGMII) Inter-device Communication
- SRIO – 2 1x lanes at a rate of 1.25, 2.5 or 3.125 Gbps each
- SRIO daisy chain capability between TCI6487 DSPs
- Hardware packet-forwarding mechanism supports passing data through an RIO daisy chain to a specific TCI6487 DSP
- McBSP—Two McBSP links, each at 100 Mbps
- McBSP can be used for multi-channel clocked serial communications
- I²C—One I²C link at 400 kbps
- I²C can be used for communication links between integrated circuits or for peripheral devices on an embedded system

Memory Interface

- DDR2-400 to DDR2-667 support

TCI6487 DSP Applications

The TCI6487 DSP offers a very high density “all-DSP” SOC baseband solution that is easily scalable for pico, micro and macro BTS applications for multiple standards.

General Characteristics

- Supports pico to macro via the TCI6487 scalable architecture
- Supports various radio topologies including:
 - TD-SCDMA, WiMAX, cdma2000, GSM/EDGE and UMTS Tx
 - ASIC-plus-DSP implementations for UMTS
- Code compatible with C64x and C64x+ platforms

LTE Solution

- Supports implementation of software-based (Tx/Rx) modems

- 3 sectors (10 MHz) supported with four devices

TD-SCDMA Solution

- Support for TD-SCDMA chip rate and symbol rate (baseband on chip)
- Up to 3 carriers/69 users with SCJD per device
- Up to 2 carriers with MCJD per device

WiMAX (802.16e) Solution

- Supports implementation of software-based (Tx/Rx) modems
- 3 sectors (5 MHz) or 1 sector (10 MHz) per device

GSM/EDGE Solution

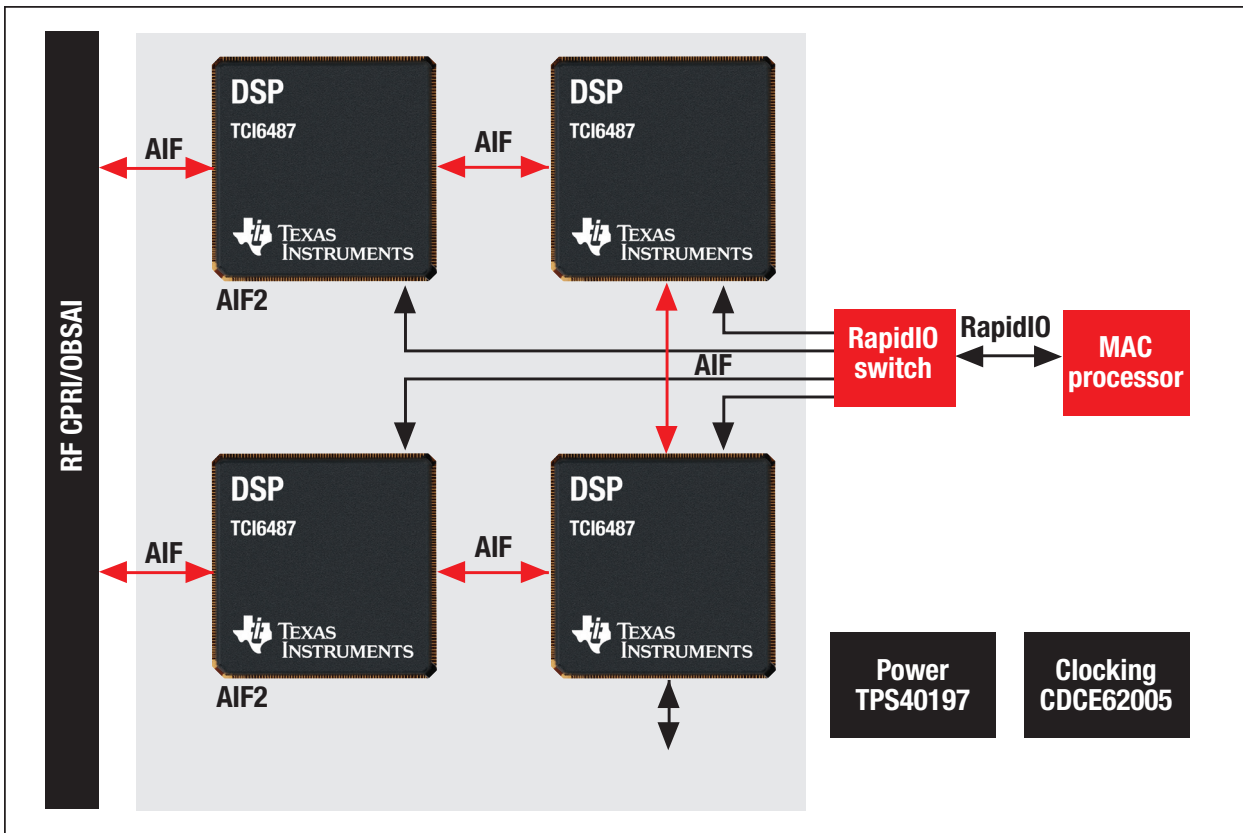
- High-density BTS baseband on a chip
- 10 EDGE-enabled carriers (all soft)
- Complete baseband on a chip

UMTS Solution

- Transmit processing for 144 Rel99 users (voice, UMTS Macro BTS)
- Transmit processing for 92 Rel99 users (voice), including softer handover

Other UMTS Capabilities

- High-density RACH solution
 - Detection of RACH preambles on 3 sectors with 2 antennas over 20 km
 - Detection of RACH preambles on 6 sectors with 2 antennas over 10 km
- HSUPA (E-DCH)
 - 1 Rel6. HSUPA carrier
 - Symbol rate processing and Mac-e
- HSDPA
 - 3 Rel5 HSDPA sectors
 - Symbol rate processing and MAC-HS



▲ Figure 2: LTE channel card design utilizing TIC16487 1.2 GHz DSPs for a 3 sector, 10 MHz, 2 antenna deployment

LTE Application

The 1.2 GHz TIC16487 is an ideal solution for LTE platforms and is a natural extension of TI's leadership portfolio of wireless infrastructure products. The TIC16487 DSP plus LTE optimized baseband software provides a compelling solution for customers. In addition, TI can provide a complete digital and analog solution for OEMs to develop products for the LTE infrastructure market.

10-MHz, 2-antenna, 3-sector LTE solution can be implemented with four 1.2 GHz TIC16487 DSPs. The antenna data is daisy-chained through the system using the CPRI/OBSAI compliant AIF and the higher layer processing is connected via either RapidIO or Ethernet.

SmartReflex™ Technology

The increased processing demands of today's advanced wireless networks have also increased power consumption. To solve this problem, TI has implemented a new power and performance management technology called SmartReflex™ in the TIC16487 DSP.

This technology closely monitors circuit speed and dynamically adjusts voltages to meet exact performance requirements. As a result, minimum power is used for each operating frequency, thereby reducing the amount of heat produced by the device. This provides the flexibility to add multiple TIC16487 devices on a single card while still meeting the designer's power budget. For additional information on the power management

implementation of SmartReflex, please visit www.ti.com/processorpower.

Advanced 65-nm Platform

The TIC16487 is built on the latest cutting-edge technology, the new 65-nm process node. This process technology doubles the transistor density of the previous 90-nm process, shrinking equivalent designs and boosting transistor performance. This allows the TIC16487 to perform at a level that is an order of magnitude higher than the previous process node at a fraction of the power consumption.

For More Information

To learn more about the TMS320TIC16487 DSP—or other wireless solutions from TI—visit www.ti.com/wi

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