TMS320C5517 DSP

Ultra low-power DSP for Audio and Vision Analytics

Texas Instruments

The Texas Instruments' TMS320C5517 ultra-low-power Digital Signal Processor (DSP) is a perfect companion for audio and vision analytics, enabling small form factor and battery-powered systems through the high-performance, low-power TMS320C55x core, tightly coupled FFT hardware accelerator and flexible multi-channel peripherals.

TMS320C55x Core

The C55x DSP architecture achieves high performance and low power through increased parallelism and complete focus on power savings. The CPU supports an internal bus structure that is composed of one program bus, one 32-bit data read bus and two 16-bit data read buses, two 16-bit data write buses and additional buses dedicated to peripheral and DMA activity. These buses provide the ability to perform up to four 16-bit data reads and two 16-bit data writes in a single cycle. The device also includes four DMA controllers, each with four channels, providing data movement for 16 independent channel contexts without CPU intervention. Each DMA controller can perform one 32-bit data transfer per cycle, in parallel and independent of the CPU activity.

FFT Hardware Accelerator

The Fast Fourier Transform (FFT) is an efficient means for computing the Discrete Fourier Transform (DFT). It is one of the most widely used computational elements in DSP applications. This DSP is ideally suited for such applications. It includes an FFT hardware accelerator (HWAFFT) that is tightly coupled with the CPU, allowing high FFT processing performance at very low power. The HWAFFT in the DSP is a software-controlled coprocessor designed to perform FFT and inverse FFT (IFFT) computations on complex data vectors ranging in length from 8 to 1024 points (powers of 2).

Flexible Peripherals

The TMS320C5517 ultra-low-power DSP provides a flexible portfolio of peripherals to fit various requirements and applications. The general-purpose inputs and outputs coupled with a 10-bit SAR ADC provide a multitude of pins for status, interrupts and other media interfaces. Serial media is supported through various combinations of Secure Digital (SD) interface, Inter-IC (I^2S Bus) modules, Serial-Port Interfaces (SPI) and Universal Asynchronous Receiver/Transmitter (UART) interfaces. Advanced peripherals include USB 2.0, McSPI, McBSP and UHPI. McSPI is a synchronous serial bus with up to three master channels, or single channel in slave mode, with DMA support. It is extremely useful in enabling sensor interfaces and codec control. McBSP is a multichanneled buffered protocol that enables continuous full-duplex communication with up to 128 channels in TDM mode. The UHPI enables an external processor to easily communicate with the C5517 DSP by directly accessing on-chip memories.

For more information please visit **www.ti.com/c5517**.

Key Features

- **Core and memory**
  - 1 TMS320C55x DSP at 200 MHz
  - 400 MMACs
  - 320KB on-chip memory
- **Peripherals**
  - External Memory Interface (EMIF)
    - Asynchronous SRAM
    - Flash (NOR/NAND)
    - SDRAM and mSDRAM
  - 4 DMA with 4 channels each
  - McSPI (with slave mode support)
  - SPI with 4 chip selects
  - McBSP with up to 128 channels
  - eMMC/MMC/SD interfaces
  - 3 configurable timers
  - Inter-IC modules
  - UART interfaces
- **Connectivity**
  - USB 2.0 PHY (device mode only)
  - Universal Host Processor Interface
- **Power and cost optimized**
  - Standby: ~0.45 mW @ 25°C (typical)
  - Active: ~108 mW @ 25°C (typical)
  - Integrated on-chip LDOs
    - DSP
    - ANA
    - USB_LDO
  - Multiple I/O voltage support
- **Package and temperature**
  - 10mm × 10mm, 196-pin BGA
  - –40°C to 85°C extended temperature

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