EVM User's Guide: DLPM980E2EVM

DLPM980E2 PLM Evaluation Module (EVM)

Description

The DLP® DLPM980E2EVM Evaluation Module (EVM) offers a reference design to enable faster development of the DLPM980E PLM with the DLPC641 PLM controller. The controller receives high-speed bit-plane data from an external source via the AMD Aurora 64B/66B interface and formats the bit-plane data prior to loading into a DLPM980E2EVM for display on the DLPM980E PLM.

Get Started

1. To order the DLPM980E2EVM, visit the DLPM980E2EVM Product Page.
2. Refer to the TI E2E DLP products forum for help or assistance.

Features

- DLPM980E Phase Light Modulator (PLM) for advanced light steering applications
- Includes a DLPC641 PLM Controller board that utilizes 32 HSSI output data lanes with up to 3.2Gb/s per data lane

Applications

- PLM pre-modulator high dynamic range (HDR) system
- Augmented Reality (AR) and virtual reality (VR)
- 3D printing and additive manufacturing
- Dynamic grayscale marking and coding
- Industrial printing
- High-speed imaging and display

1 Evaluation Module Overview

1.1 Introduction

This guide details the hardware and software features of the DLP DLPM980E2EVM system. The EVM architecture and connectors are described along with a quick start guide on how to assemble the PLM EVM with a DLPC641 PLM Controller board. This guide explains how to operate the PLM system using a graphical user interface (GUI). A separate Virtex® 7 field programmable gate array (FPGA) can also be used to display test patterns with more detailed information in the DLPC964 Apps FPGA User's Guide. Specific details for each DLP component can be found in Reference Documentation.

1.2 Kit Contents

The DLPM980E2EVM kit is a flexible, ready-to-use evaluation module and includes the following hardware components:

- DLPM980E PLM board
- Mechanical mounting hardware for PLM board
- Flex/Interconnect cables
- DLPC641 PLM controller board

Note

Front-end electronics, optics, illumination source, and power supply are not included with the DLPM980E2EVM kit and will need to be purchased separately.

1.3 Specification

The DLPM980E2EVM contains the electronics capable of controlling supported DLPM980E PLM. The DLPM980E2EVM offers several interface options including USB, I^2C, HPC FMC connectors, and Flex Cables connectors. Figure 1-1 shows the EVM Hardware Block diagram of the DLPM980E2EVM.

The major components of the DLPM980E2EVM are:

- DLPC641 PLM Controller
- Power Management Unit to support the DLPC641 subsystem
- DLPC641 configuration Flash memory
- USB 2.0 interface
- Flex Cables—Four are needed to support the DLPM980E PLM board
- HPC FMC Connectors—Two for an attached Apps FPGA or other front-end board

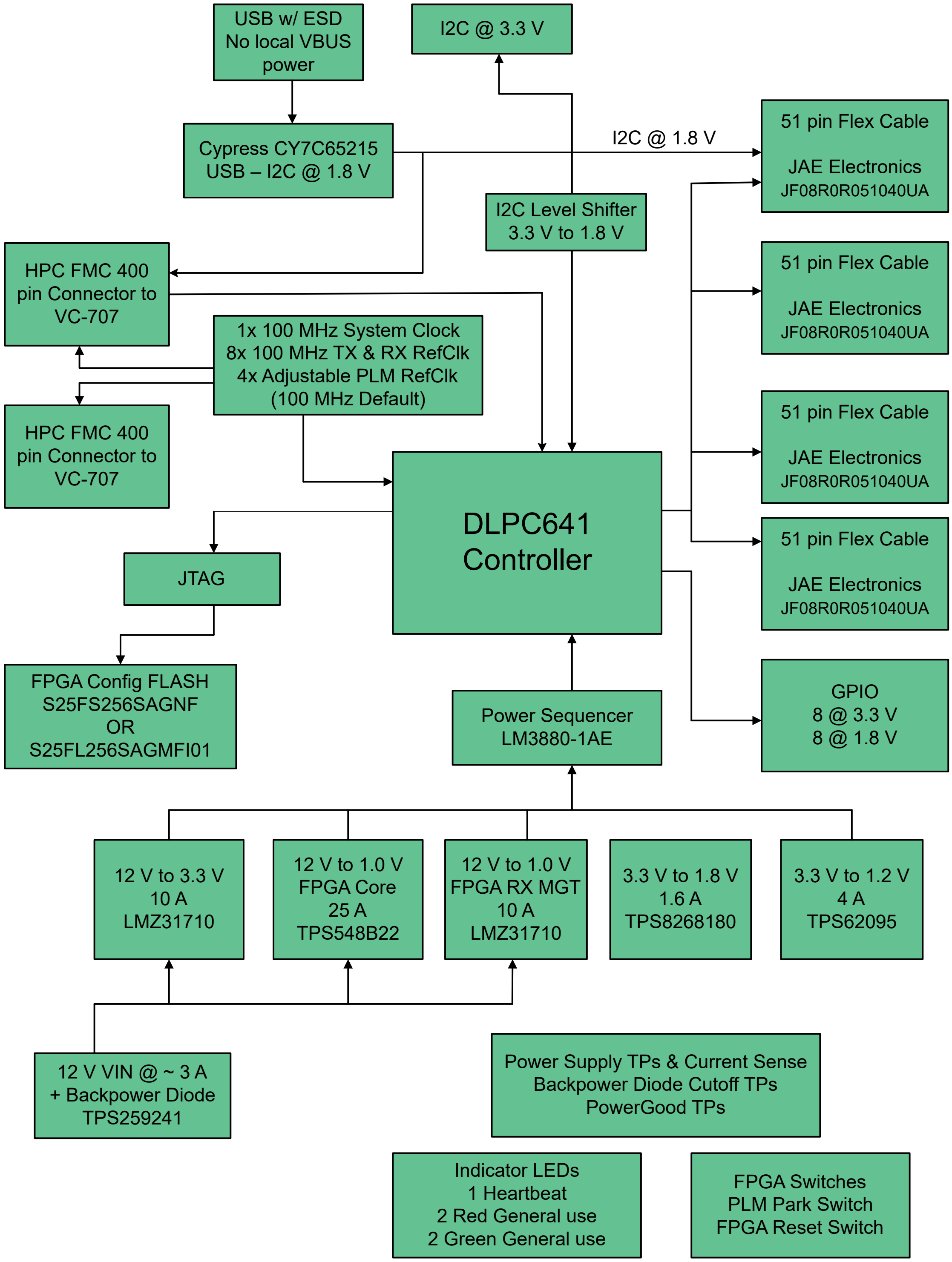

Figure 1-1. DLPC641 PLM Controller Block Diagram

1.4 Device Information

The DLPM980E2EVM consists of the DLPM980E PLM board, mounting hardware, and a DLPC641 PLM controller board.

The DLPC641 PLM controller board, which includes a DLPC641 Digital Controller, USB interface, power management circuits, and supported digital logic can be paired with the DLPM980E PLM board for use as a standalone system. A customer front-end board can also be attached to the DLPM980E2EVM to send external patterns to the DLPM980E2EVM.

Figure 1-2 outlines the major hardware components of the DLPM980E2EVM system with an additional customer front end.

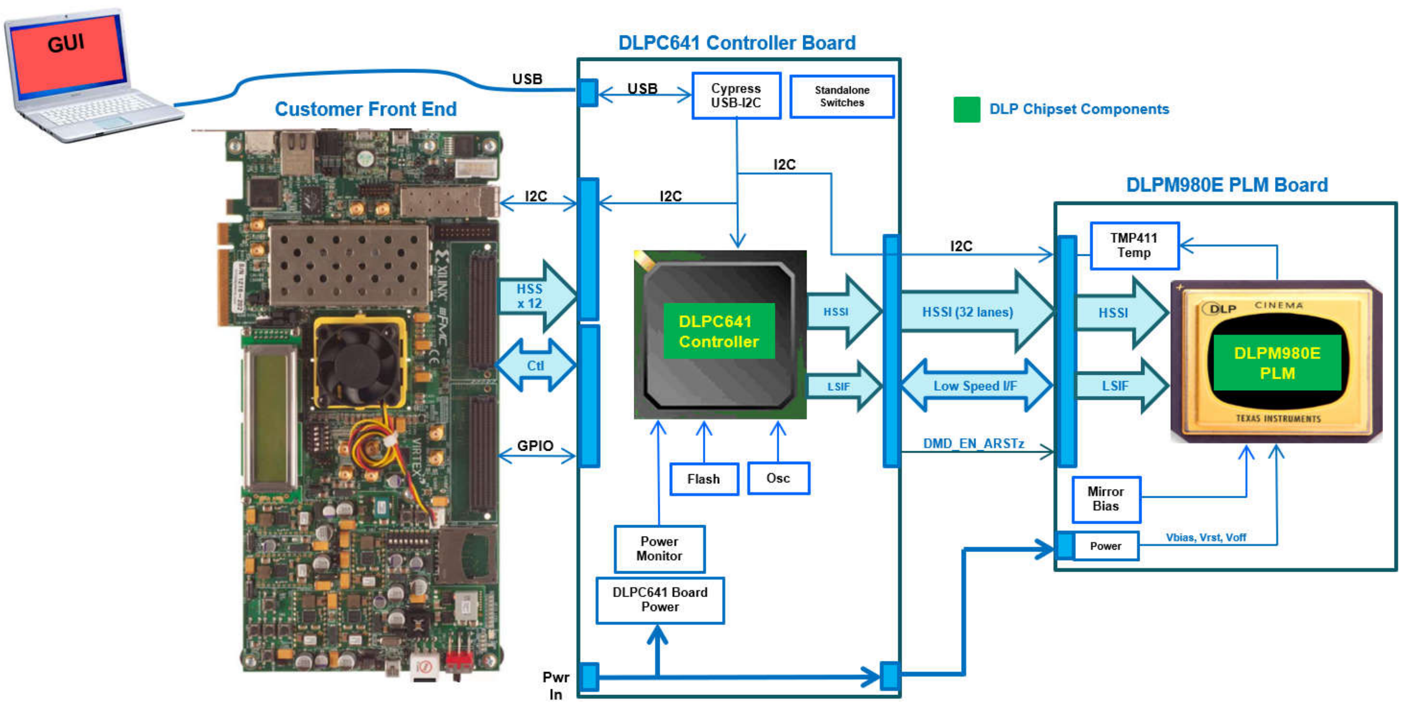

Figure 1-2. DLPM980E2EVM Hardware Components

DLPC641 Controller Board:

- Receives customer front-end board pattern data
- Sends data to the PLM board
- Controlled by DLPC964 Graphical User Interface (GUI) via USB
- Works as a standalone system with select internal patterns when paired with the DLPM980E PLM board

DLPC964 GUI (compatible for DLPC641 controller board):

- Controls DLPM980E2EVM
- Variety of test pattern selections
- Variety of block mode selections
- Continuous monitoring of system performance and status
- Data location on PLM
- Block addressing

2 Hardware

2.1 Power Supply Requirements

2.1.1 External Power Supply Requirements

The DLPM980E2EVM kit does not include a power supply. The external power supply requirements are:

- Nominal voltage: 12V DC –5%/+10%
- Current: 5A
- DC connector size:
  - Inner diameter: 2.5mm
  - Outer diameter: 5.5mm
  - Shaft: 9.5mm female, center positive
- A recommended power supply is Digi-Key part number 102-3811-ND or equivalent.

Note

External Power Supply Regulatory Compliance Certifications: Recommend selection and use of an external power supply that meets TI's required minimum electrical ratings in addition to complying with applicable regional product regulatory and safety certification requirements such as (by example) UL, CSA, VDE, CCC, PSE, and so on.

- In addition to the 12V DC power supply listed above, a variable DC power supply unit is required for Mirror Bias. The supply requirements are:
  - DC Voltage range: –0.5V to 2.5V
  - Current: 100mA

2.2 DLPM980E2EVM Connections

Figure 2-1 depicts the DLPM980E2EVM switches and connectors with their respective locations.

Note

The Apps FPGA / front end board, power supply (with cable), and USB cable are NOT included within the DLPM980E2EVM kit and will need to be purchased separately.

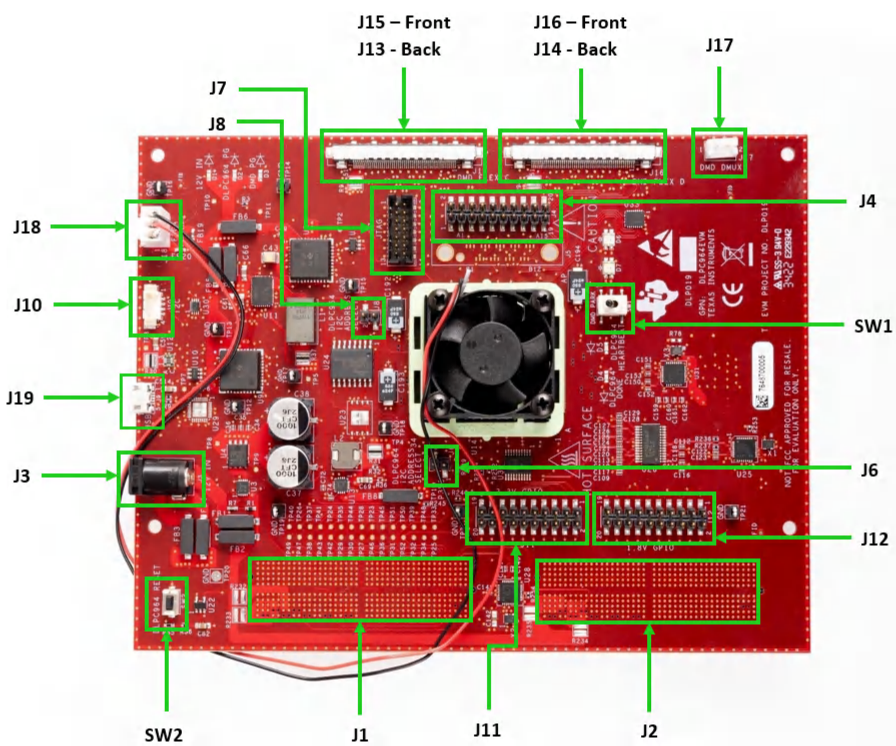

Figure 2-1. DLPM980E2EVM Connectors (Top View)

2.2.1 J1, J2—HPC FMC Connector (Male)

The 400 position HPC FMC male connectors J1 and J2 are used to connect a front-end Apps FPGA board to the DLPC641 Controller board. The front-end board is used to help enable customers with interfacing to the DLPC641 Controller for sending high-speed pattern data to the DLPM980E PLM.

The matching part numbers are:

- Samtec part number: SEAF-40-05.0-S-10-2-A-K-TR
- Digi-Key part number: SAM8009CT-ND

If using ribbon cables to connect between the front-end Apps FPGA and DLPM980E2EVM, the matching part numbers are:

- Samtec part number: ASP-134488-01 or ASP-134602-01
- Digi-Key part number: SAM8730-ND or 612-ASP-134602-01CT-ND

2.2.2 J3—Input Power

Connecter J3 accepts a +12 VDC input power to the DLPM980E2EVM board. The power socket J3 pins are shown in Table 2-1.

The matching part numbers are:

- CUI Devices part number: PP3-002A
- Digi-Key part number: CP3-1000-ND

Note

The power supply and cable are not included inside the DLPM980E2EVM kit and needs to be purchased separately. Please see External Power Supply Requirements for more details.

Table 2-1. Power Connector Pins

Description	Pin	Supply Range
Input supply	1	12+ V DC –5%/+10%
Ground	2	0V
Ground	3	0V

2.2.3 J4 - TestMux Connector

The TESTMUX connector J4 pins are shown in Table 2-2.

Table 2-2. TESTMUX Connector Pins

Description	Pin	Supply Range
Ground	1	0V
Ground	2	0V
TESTMUX_0	3	1.8V
TESTMUX_8	4	1.8V
TESTMUX_1	5	1.8V
TESTMUX_9	6	1.8V
TESTMUX_2	7	1.8V
TESTMUX_10	8	1.8V
TESTMUX_3	9	1.8V
TESTMUX_11	10	1.8V
TESTMUX_4	11	1.8V
TESTMUX_12	12	1.8V
TESTMUX_5	13	1.8V
TESTMUX_13	14	1.8V
TESTMUX_6	15	1.8V
TESTMUX_14	16	1.8V
TESTMUX_7	17	1.8V
TESTMUX_15	18	1.8V
Ground	19	0V
Ground	20	0V

2.2.4 J6, J8 - I^{2}C Address Selectors

The I^{2}C_ADDR_SEL[1:0] input pins allow the user to select the DLPC641 I^{2}C Secondary address. Table 2-3 describes the relationship between the I2C_ADDR_SEL[1:0] pins and the DLPC641 I^{2}C Secondary address.

Note

If pins are left unconnected, the default I^{2}C address is 0x0C.

Table 2-3. DLPC641 I^{2}C Secondary Address Selection Table

I^{2}C_ADDR_SEL[1]	I^{2}C_ADDR_SEL[0]	I^{2}C Secondary address
0	0	0x0F
0	1	0x0E
1	0	0x0D
1	1	0x0C

2.2.5 J7 - JTAG Boundary Scan

Connector J7 provides a direct connection for an AMD JTAG programming cable. J7 is used when customers want to load firmware configuration files into the FPGA (DLPC641 Controller). The JTAG Boundary connector J7 pins on the DLPM980E2EVM pins are listed in Table 2-4.

Two matching fourteen position connector part numbers are:

- Molex part number: 051110-1451
- Digi-Key part number: WM18047-ND

The corresponding terminal (crimp) part numbers are:

- Molex part number: 087396-8051
- Digi-Key part number: WM23602CT-ND

Note

For instructions on programming the DLPC641 Controller, see Section 4.1.5.2 for more details.

Table 2-4. JTAG Boundary Scan Connector Pins

Description	Pin	Supply Range
Ground	1	0V
Supply Voltage	2	1.8V
Ground	3	0V
TMS	4	1.8V
Ground	5	0V
TCK	6	1.8V
Ground	7	0V
TDO	8	1.8V
Ground	9	0V
TDI	10	1.8V
Ground	11	0V
NC	12	N/A
Ground	13	0V
NC	14	N/A

2.2.6 J9 - Micro-B USB Connector

Connector J9 is used to connect the USB cable from users PC running the DLPC964 GUI. The Micro-B USB connector J9 pins are shown in Table 2-5.

Note
The USB Micro-B to USB type A cable is not included inside the DLPM980E2EVM kit and needs to be purchased separately.

Table 2-5. Micro-B USB Receptacle Connector Pins

Description	Pin	Supply Range
VBUS	1	5.0V
DMINUS	2	5.0V
DPLUS	3	5.0V
NC	4	0V
Ground	5	0V
Ground	6	0V
Ground	7	0V
Ground	8	0V
Ground	9	0V

2.2.7 J10 - I^{2}C Connector

The connector J10 is used for 3.3V external I^{2}C operations. The I^{2}C connector J10 pins are shown in Table 2-6.

Two matching four-pin, 1.25mm connector part numbers are:

- Molex part number: 0510210400
- Digi-Key part number: WM1722-ND

The corresponding terminal (crimp) part numbers are:

- Molex part number: 0500798100
- Digi-Key part number: 0500798100

Table 2-6. I^{2}C Connector Pins

Description	Pin	Supply Range
I^{2}C SCL	1	3.3V
I^{2}C SDA	2	3.3V
3.3V supply	3	3.3V
Ground	4	0V
Ground	5	0V
Ground	6	0V

2.2.8 J11 - 3.3V GPIO Connector

The pins for J11 are available for customers definition. The 3.3V GPIO connector J11 pins are shown in Table 2-7.

Table 2-7. 3.3V GPIO Connector Pins

Description	Pin	Supply Range
GPIO_3P3_0	1	3.3V
Ground	2	0V
GPIO_3P3_1	3	3.3V
Ground	4	0V
GPIO_3P3_2	5	3.3V
Ground	6	0V
GPIO_3P3_3	7	3.3V
Ground	8	0V
GPIO_3P3_4	9	3.3V
Ground	10	0V
GPIO_3P3_5	11	3.3V
Ground	12	0V
GPIO_3P3_6	13	3.3V
Ground	14	0V
GPIO_3P3_7	15	3.3V
Ground	16	0V
3.3V Supply	17	3.3V
Ground	18	0V
3.3V Supply	19	3.3V
Ground	20	0V

2.2.9 J12 - 1.8V GPIO Connector

The pins for J12 are available for customers definition. The 1.8V GPIO connector J12 pins are shown in Table 2-8.

Table 2-8. 1.8V GPIO Connector Pins

Description	Pin	Supply Range
GPIO_1P8_0	1	1.8V
Ground	2	0V
GPIO_1P8_1	3	1.8V
Ground	4	0V
GPIO_1P8_2	5	1.8V
Ground	6	0V
GPIO_1P8_3	7	1.8V
Ground	8	0V
GPIO_1P8_4	9	1.8V
Ground	10	0V
GPIO_1P8_5	11	1.8V
Ground	12	0V
GPIO_1P8_6	13	1.8V
Ground	14	0V
GPIO_1P8_7	15	1.8V
Ground	16	0V
1.8V Supply	17	1.8V
Ground	18	0V
1.8V Supply	19	1.8V
Ground	20	0V

2.2.10 J13, J14, J15, J16 - PLM Flex Cable Connectors

Connectors J13, J14, J15, and J16 are used to connect the DLPC641 Controller board to the DLPM980E PLM board. All four PLM Flex Cables must be connected so there can be a proper data interface to the PLM.

Two matching fifty-one position connector part numbers are:

- JAE Electronics part number: FI-RE51HL
- Digi-Key part number: 670-1205-ND

The corresponding terminal (crimp) part numbers are:

- JAE Electronics part number: FI-RC3-1A-1E-15000
- Digi-Key part number: 670-1195-1-ND

2.2.11 J17 - DMD_DMux Connector

The DMD_DMux connector J17 is connected to the DMUX_LATCHED signal on the DLPM980E PLM board. The J17 connector pins are shown in Table 2-9.

Two matching two-pin, 2.5mm connector part numbers are:

- JST Sales America Inc. part number: EHR-2
- Digi-Key part number: 455-1000-ND

The corresponding terminal (crimp) part numbers are:

- JST Sales America Inc. part number: SEH-001T-P0.6
- Digi-Key part number: 455-1042-1-ND

Table 2-9. DMD_DMUX Connector Pins

Description	Pin	Supply Range
DMD_DMUX	1	3.3V
Ground	2	0V

2.2.12 J18 - FanSink Connector

Connector J18 is a 3-pin +12 VDC fan connector used to control the temperature of the DLPC641 Controller from overheating. The FanSink connector J18 pins on the DLPM980E2EVM are listed in Table 2-10.

Two matching three-pin, 2.54mm connector part numbers are:

- Molex part number: 0022013037
- Digi-Key part number: 900-0022013037-ND

The corresponding terminal (crimp) part numbers are:

- Molex part number: 0008650804
- Digi-Key part number: WM2756CT-ND

Note

Before powering on the DLPM980E2EVM, make sure J18 is connected to the FanSink to prevent damaging the DLPC641 Controller.

Table 2-10. Fan Connector Pins

Description	Pin	Supply Range
Ground	1	0V
Power	2	12V
Power	3	NC

2.2.13 Switches

This section describes the switches on the DLPM980E2EVM with the respective locations.

2.2.13.1 SW1 - PLM park (PARK_Z)

SW1 is a toggle switch that issues a park command to the PLM that stops the DLPC641 logic. When ON, SW1 forces the PLM micromirrors to the parked state.

Note

TI highly recommends switching SW1 ON prior to removing power via J3 to prevent damage to the EVM board. Please see Power-down of the PLM System for more information.

Table 2-11. SW1 ON/OFF State

SW1 State	Description
ON (facing toward DLPC641 controller)	Sets PARK_Z low and unparks the attached PLM.
OFF (facing away from DLPC641 controller)	Sets PARK_Z high and issues a park on the PLM micromirrors.

2.2.13.2 SW2 - DLPC641 Reset

SW2 is a contact switch that resets the DLPC641 Controller code running on the DLPM980E2EVM. When SW2 is released, the DLPC641 Controller boots from reset.

2.2.14 DLPM980E2EVM LEDs

This section describes the power and status LEDs of the DLPM980E2EVM.

2.2.14.1 DLPM980E2EVM Power and Status LEDs

Figure 2-2 depicts the DLPM980E2EVM LEDs with the respective locations.

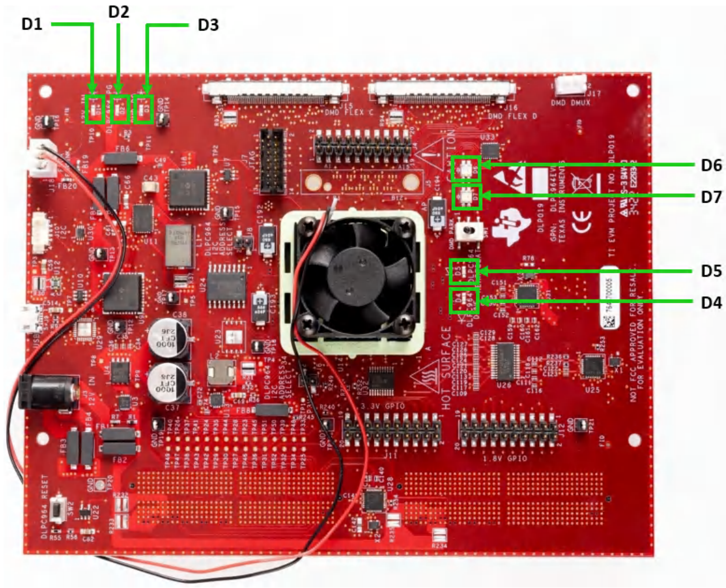

Figure 2-2. DLPM980E2EVM LEDs (Top View)

Table 2-12. DLPM980E2EVM LED References

Connector Reference	EVM Function	Description or Use
D1	12V Power	External +12 VDC present.
D2	DLPC641 Power Good (PG)	All voltages are stable and present from controller board.
D3	DMD Power Good (PG)	All voltages are stable and present from PLM board.
D4	DLPC641 Done	DLPC641 initialization complete.
D5	DLPC641 Heartbeat (Flashing)	Flashes when the DLPC641 is running.
D6	Phased-Locked Loop (PLL)	Indicator that the Phase-Locked Loop (PLL) clock circuity of the controller is locked.
D7	DMD HSSI sync error	Indicator on whether a DMD HSSI sync error was detected.

2.3 EVM Assembly

This section describes how to assemble the DLPM980E2EVM hardware.

2.3.1 PLM Assembly

The DLPM980E board comes preassembled. Figure 2-3 shows how to assemble the PLM board if the board must be reassembled. Although a heat sink **is not** included in the DLPM980E2EVM kit, TI strongly recommends adding a heat sink, as this board can reach high temperatures (temperatures above 55°C) without one. Please see the Safety and Caution Labels for more information on the EVM kit.

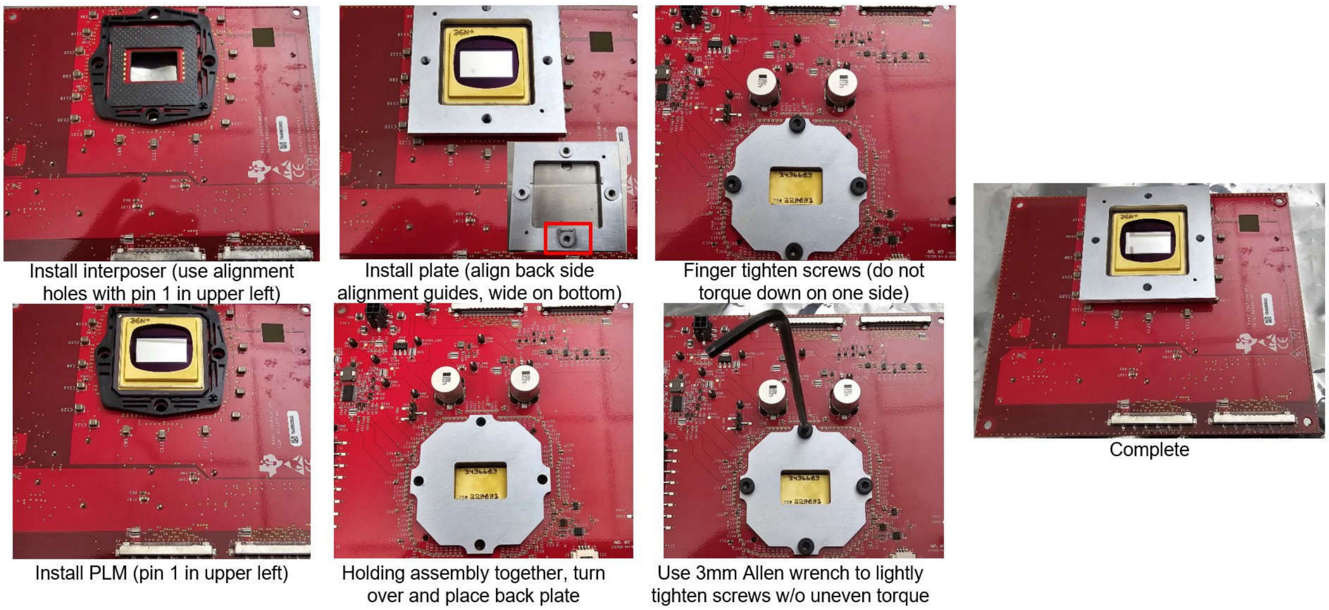

Figure 2-3. DLPM980E PLM Board Assembly

2.3.2 Hardware Assembly

The DLPC641 controller board requires a DLPM980E PLM board and four PLM Flex Cables for assembling a standalone system.

- The PLM Flex Cable connectors are to be connected between the EVM boards.
- The ends of each PLM flex cable are identical.
- The DLPM980E PLM board has flex cable connectors labeled J1, J2, J3, and J4.
- The DLPC641 controller board has flex cable connectors labeled J13, J14, J15, and J16.
- Orient the DLPC641 controller board and the DLPM980E PLM board as shown in Figure 2-5.
- The silkscreen layer of both the DLPM980E PLM board and the DLPC641 controller board show where each flex connector goes, as shown in Figure 2-4. The flex connectors are marked A through D, and must match letter-to-letter from the controller board to PLM board.
  - J13 on the controller board connects to J1 on the PLM board.
  - J14 on the controller board connects to J2 on the PLM board.
  - J15 on the controller board connects to J3 on the PLM board.
  - J16 on the controller board connects to J4 on the PLM board.
- Connect the four flex cables as shown in Figure 2-5.

Figure 2-5 shows how to successfully connect the PLM Flex Cables between the DLPC641 controller board and DLPM980E PLM board.

If desired, customers can use shorter PLM Flex Cables offered by JAE Electronics. Please see the other PLM Flex Cable connector options below:

- JF08R0R051030UA - 12" cable length
- JF08R0R051020UA - 8" cable length

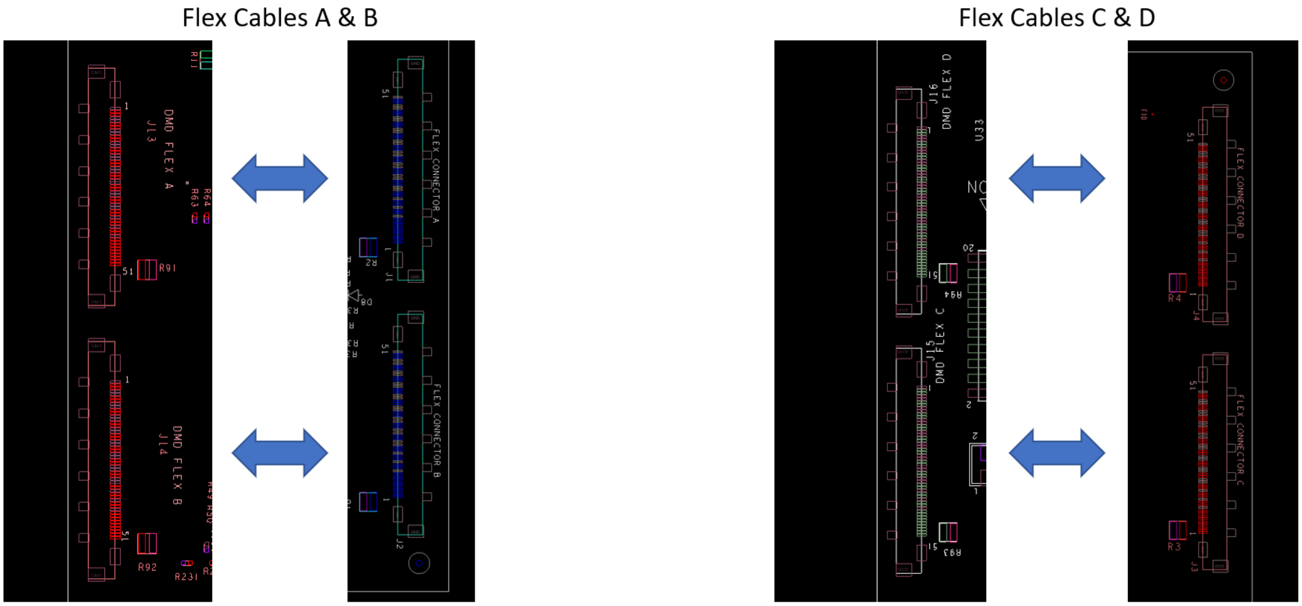

Figure 2-4. Flex Cable Connections Between PLM Board and Controller Board

Figure 2-5. Standalone DLPC641 Controller Board and DLPM980E PLM Board

2.3.3 Connecting a Front End Board to the Controller Board

This section explains how to assemble the Apps FPGA front end to the DLPC641 controller board.

If desired, customers can connect a front end board (such as the AMD VC707) to the DLPC641 controller board to send images or patterns to the DLPM980E2EVM

Locate the DLPC641 controller board's HPC FMC connectors (J1 and J2). Line up both HPC FMC connectors and verify that the connectors are aligned correctly before applying pressure to connect the boards together as shown in Figure 2-8.

Note

After initially applying pressure to connect both boards, apply pressure at one end and then the other to make sure connectors are fully connected together.

The 300mm Samtec HPC FMC ribbon cables (HDR-169468-01) are an alternative for these connections. Two cables are needed.

- Attach the HPC FMC female connector end of the cables to the male HPC FMC connectors on the DLPC641 controller board.
- Attach the HPC FMC male connector end of the cables to the female HPC FMC connectors on the Apps FPGA board.

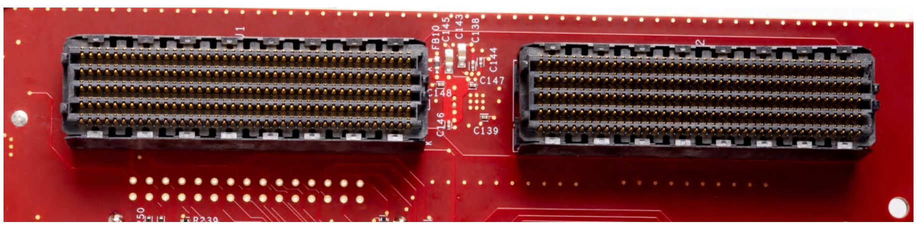

Figure 2-6. DLPC641 Controller Board Male HPC FMC Connector

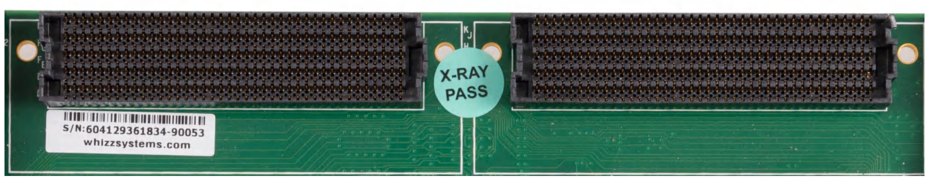

Figure 2-7. Front End Female HPC FMC Connector

Figure 2-8. Fully Assembled DLPC641 Controller Board With Front End

3 Quick Start

This chapter explains how to properly power on, test, and power off the DLPM980E2EVM.

3.1 Set PLM Mirror Bias

Before starting the PLM system, run a quick test. With the standalone system (DLPC641 controller board and DLPM980E PLM board only), assemble the hardware as shown in Figure 2-5 and Figure 3-1.

Note

Before powering up the DLPC641 controller board and front end board, follow the instructions for turning on Mirror Bias. Mirror Bias must be turned on first.

Mirror Bias is an analog voltage connected to the mirrors that has a range of -0.5V to 2.5V.

To set Mirror Bias, make sure the DC power supply meets a current capability of 100mA. On the DLPM980E PLM board, connect the positive terminal of the DC power supply to pin 3 of J10 and the ground lead to one of the ground test points nearby as shown in Figure 3-1. Apply power to Mirror Bias using the variable DC power supply. Ensure the voltage applied is in range and vary as needed.

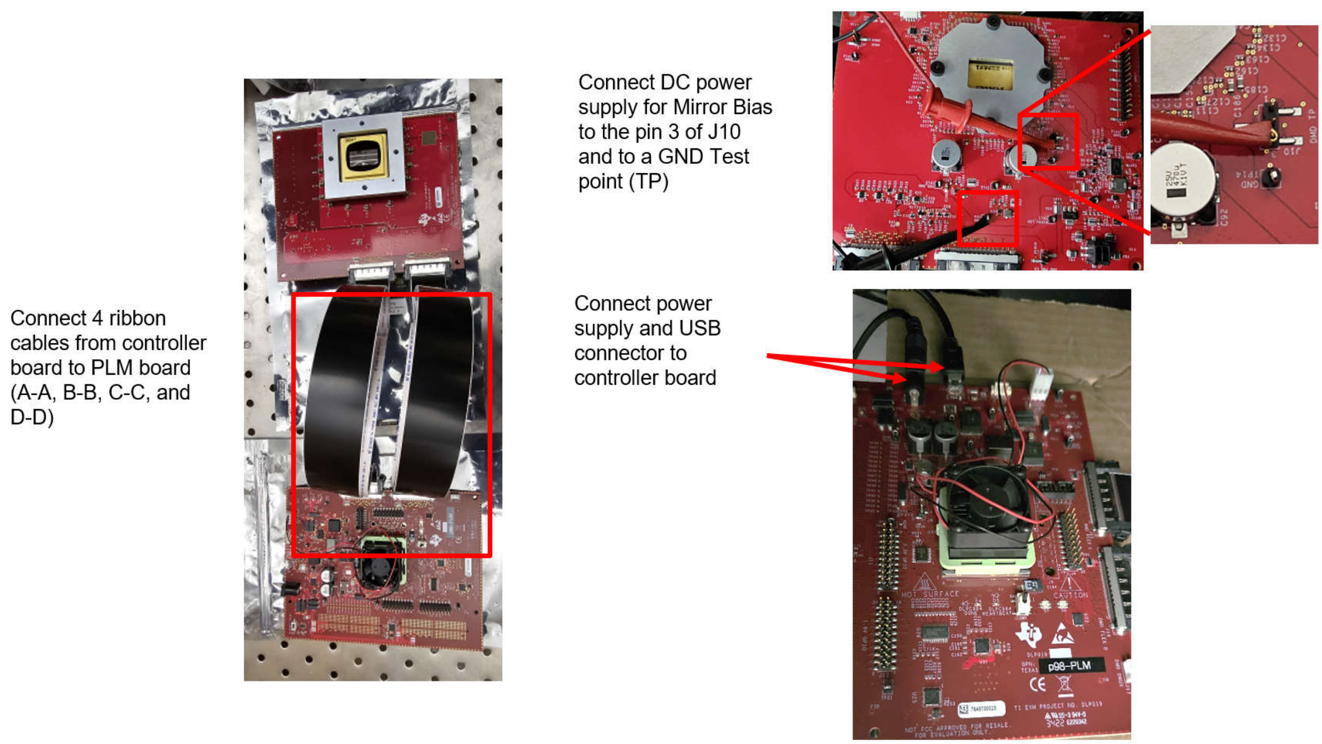

Figure 3-1. Assembly for Testing MirrorBias of PLM

Next, power up the DLPC641 controller board.

On the controller board, look for 12V power LED (D1), POWERGOOD LED (D2), DMD_POWERGOOD LED (D3), and a blinking heartbeat LED (D5). The heartbeat LED blinks only if the DLPM980E2EVM has configured correctly.

Make sure the toggle switch (SW1) on the controller board shown is switched toward the main IC of the board, the DLPC641.

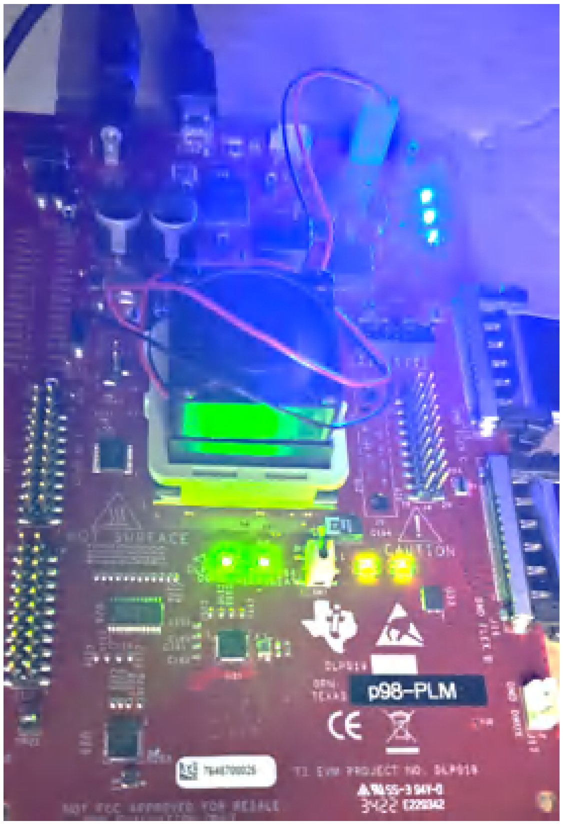

Figure 3-2. Controller Board: Powergood, Heartbeat, and Toggle Switch

Now, illuminate the PLM with a laser and verify the diffraction dots.

Figure 3-3. Illumination of DLPM980E PLM Device

3.2 Power-up of the DLPM980E2EVM PLM System

The PLM EVM is ready for use once assembled with the DLPC641 controller board and a front end board such as the AMD Xilinx VC707 EVM. The following steps show how to apply mirror bias, apply system power, display an image, and connect the EVM to a PC.

Note

Follow the instructions under Programming Firmware if user wants to reload the firmware for either the standalone system (DLPM980E2EVM) or with the front end device (AMD Xilinx VC707 EVM).

Power-up instructions:

1. Apply Mirror Bias.
2. On the DLPC641 controller board, make sure switch SW1 is OFF and facing away the DLPC641 IC Heat Sink Fan [PLM in parked state].
3. Power on the front end such as the AMD Xilinx VC707 board

Note

Allow sufficient time for the front end, such as the VC707 board to configure (DS1 and DS10 illuminates, which indicates successful power up on the example front end).

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4. On the controller board, connect a 12V, 5A DC power supply to the barrel jack connector J3.
5. Flip SW1 on the controller board to the ON position so that the switch faces the DLPC641 IC. This is the unparked state of the PLM.
6. On the controller board, D1, D2, and D3 LEDs illuminate indicating that power is present on the DLPC641 controller Board and DLPM980E PLM boards.
7. LED D4 on the controller board illuminates indicating that the PROM has configured the DLPC641.
8. LED D6 & D7 illuminate on the controller board, indicating that there are no PLM HSSI sync errors and that the DLPC641 User clock is locked.
9. LED D5 flashes (heartbeat) on the controller board indicating that the DLPC641 controller board is running.
10. Connect a USB cable from a PC to connector J19 on the DLPC641 controller board. The first time the cable is connected on a PC, the DLPC641 Controller Board enumerates. The required drivers are installed as part of the Controller Board GUI installation.
11. Open and run the DLP LightCrafter DLPC964 GUI. When the GUI application opens, look at the bottom left. The GUI is going to display *Hardware Connected*.
12. The DLPC641 Controller can be controlled through the DLPC964 GUI software available for download from the DLPM980E2EVM Tool Folder.

3.3 Connecting to the DLPC964 GUI

1. Connect the boards as shown in previous pages. There are two configurations:
   a. Front end with DLPC641 controller board and DLPM980E PLM board
   b. Standalone DLPC641 controller board with DLPM980E PLM board
2. Power DLPC641 controller board using 12V DC input.
3. Power on AMD EVM (if present).
4. Connect USB from DLPC641 controller board to PC.
5. Run TI DLP® DLPC964 GUI.
6. GUI displays *Hardware Connected* message in bottom left corner of status bar.

3.4 Modulating Mirror Bias

Follow the instructions above for how to set PLM Mirror Bias and illuminate the PLM with a laser.

Using the DLPC964 GUI, go to the *DLPC964* tab and select *1x1 Horizontal Lines* pattern and enable under *Pattern Generator*. Be sure *Pattern Cycle* is disabled.

Figure 3-4. Enable 1x1 Horizontal Lines Pattern

Set Mirror Bias and see the diffraction pattern change. Next, change Mirror Bias and confirm the difference in light steered. Modulate Mirror Bias to minimize the 0th order energy (the middle dot).

Note

When setting mirror bias, start high at 2.5V and slowly decrease until optimum voltage is achieved. Avoid going >0.2V below optimum mirror bias when tuned for red (~625nm) as this could overextend the mirrors and lead to damage to the device.

The top two images of Figure 3-5 show an example of mirror bias being set. The bottom two images of Figure 3-5 show how changing Mirror Bias changes the light steered.

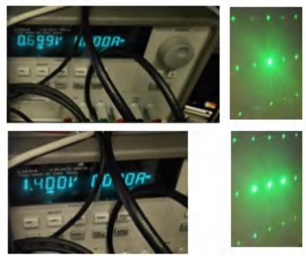

Figure 3-5. Example: Effects of Changing Mirror Bias

3.5 Test PLM Quadrants

Illuminate each quadrant of the PLM shown in Figure 3-6 to make sure all data cables and pins are working.

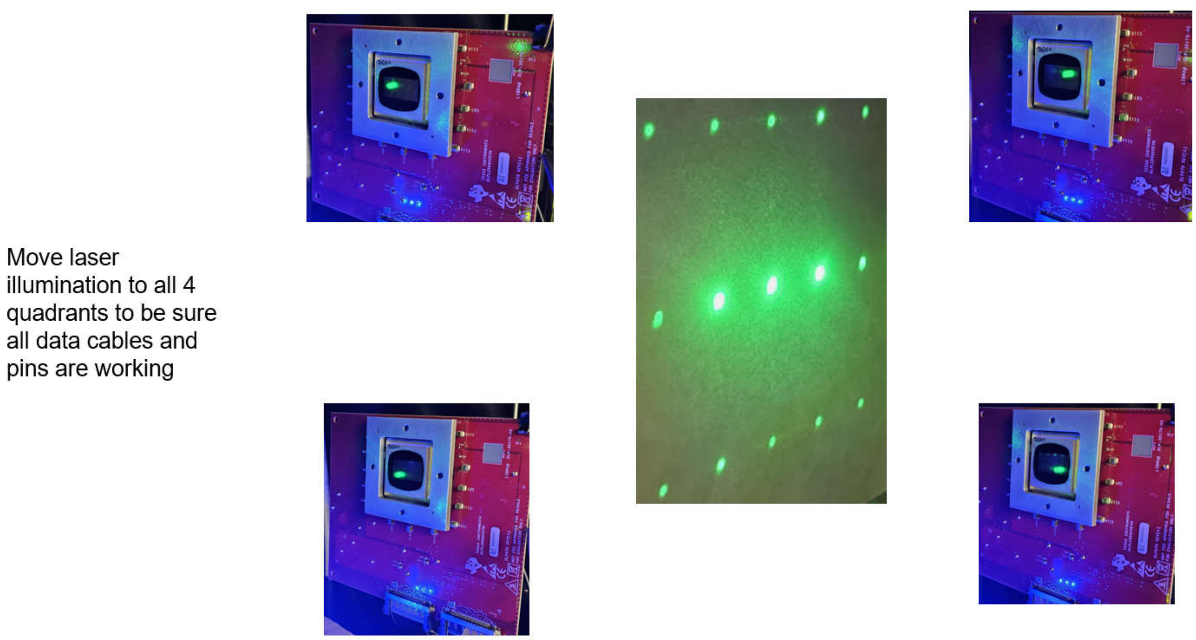

Figure 3-6. Testing DLPM980E PLM Device Quadrants

3.6 Power-down of the PLM System

Follow the steps below to properly power down the DLPC641 Controller Board:

1. Flip toggle switch SW1 to the OFF position on the DLPC641 controller board so the switch is facing away from the DLPC641 Fan Sink [PLM in parked state]
2. Remove power from the barrel jack connector J3 of the DLPC641 Controller Board
3. Power off the front end such as the AMD Xilinx VC707 board
4. Turn off/disconnect Mirror Bias

4 Software

This chapter explains the DLPC964 GUI software used to control the DLPM980E2EVM.

4.1 Operating the DLPM980E2EVM

4.1.1 DLPLCRC964 GUI and Apps FPGA Software

The DLPM980E2EVM-SW includes a DLPC964 GUI application to control the DLPC641 Controller, front end Apps FPGA, GUI source code, and Apps FPGA VHDL source code.

For details on the Apps FPGA VHDL source code, please see DLPC964 Apps FPGA User's Guide.

4.1.2 PC Software

Upon execution of the DLPC964 GUI application, the panel shown in Figure 4-1 is displayed. The GUI interface contains the following:

- Menu Bar (top)
- Main window with five sub-windows
- Hardware Connected - information bar (bottom)
- Log window (bottom)
- Online Resources

The five sub-windows are:

- Start Page
- DLPC964 Tab
- DLPC964 Registers Tab
- Apps FPGA Tab
- Apps FPGA Registers Tab

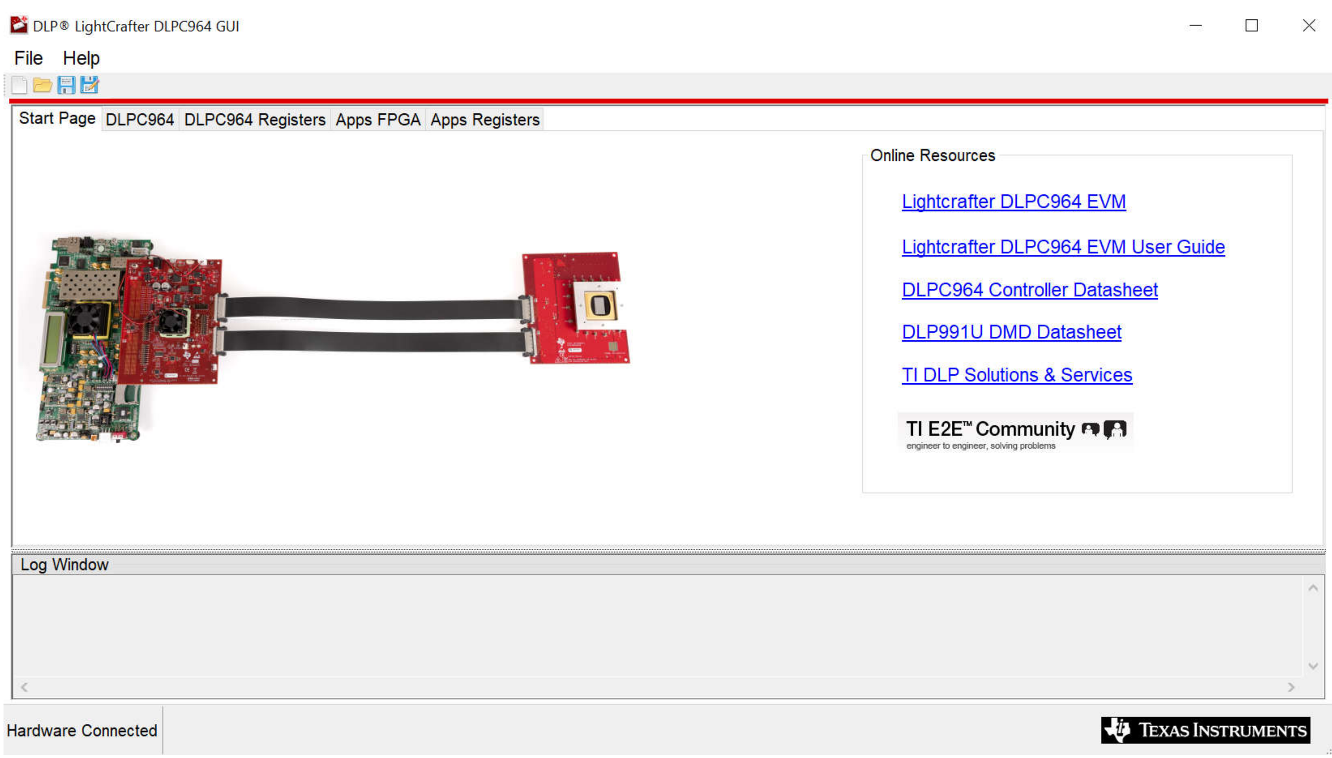

Figure 4-1. DLPC964 GUI

4.1.3 Menu Bar

The DLPC964 GUI Menu bar consists of two items:

1. File Menu
   - **New Log** empties the Status sub-window to record a new command log sequence.
   - **Open Log** opens a dialogue box to select an existing command log sequence file from the disk.
   - **Save Log** saves the current contents of the Status sub-window to the current script file. If the file is not yet saved the save as dialogue opens.
   - **Save Log As** opens a dialogue box to save the current command log sequence with a new name.

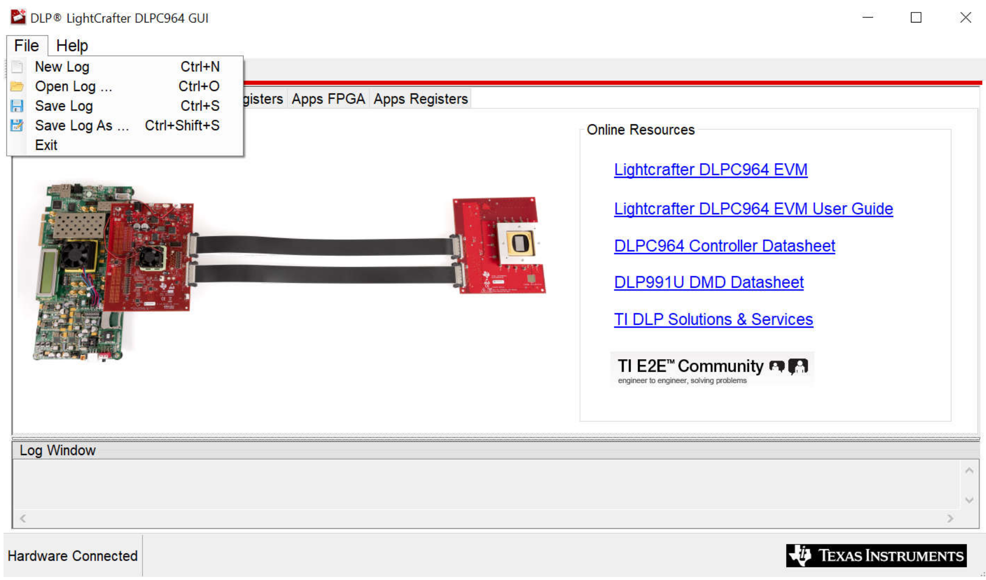

Figure 4-2. Menu Log Items

2. Help Menu
   - About DLP® LightCrafter DLPC964 GUI displays the Software Version (X.X.X) and USB DLL Version information box:

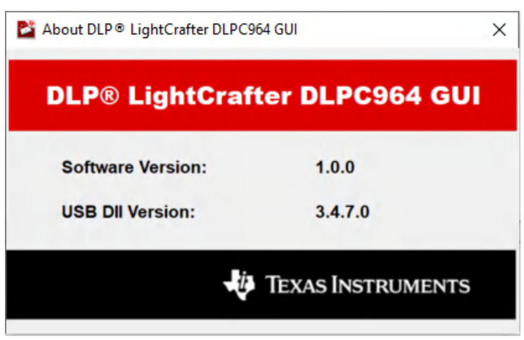

Figure 4-3. DLPC964 GUI About Box

4.1.4 Main Window

The main window consists of five sub-windows:

4.1.4.1 Start Page

The Start Page is the first window that users see upon executing the DLPC964 GUI.

This window has the image of a standard setup for the Apps FPGA (AMD EVM) with the DLPM980E2EVM.

There are also online resources to help enable customers in getting Evaluation Module Kits started.

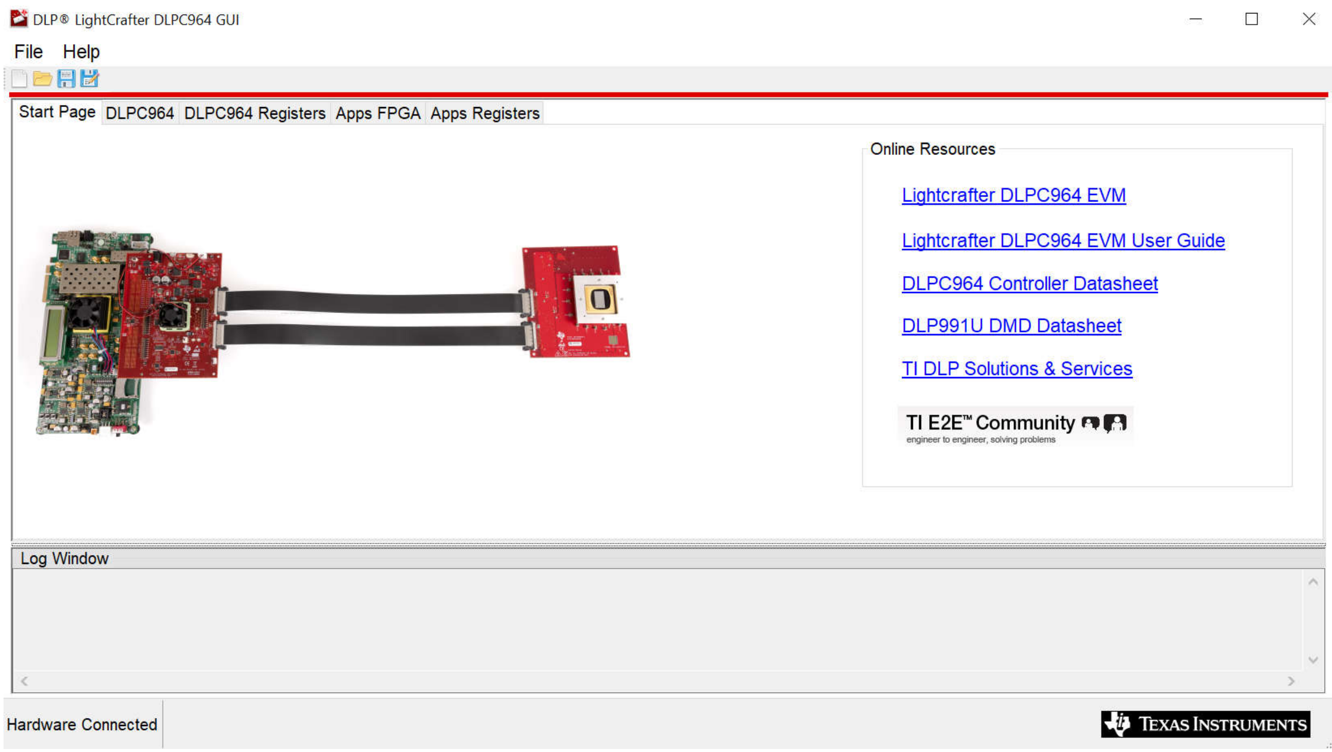

Figure 4-4. DLPC964 GUI Start Window

If the DLPC964 GUI states that Hardware is not connected, then check:

- The USB connection on J9 and/or the USB connection via the user's PC.
- The DLPC964 driver in Device Manager with the .inf file provided from the GUI software installation.

Note

The .inf file is located under the directory: C:\Program Files\Texas Instruments\DLPC964REF-SW-VX.X.XX\Driver\Win10\x64.

4.1.4.2 DLPC964 Tab

The **DLPC964 tab** read the status of the DLPC641 features and functions. HSSI, HSS, PLL, select test patterns and configure test pattern settings.

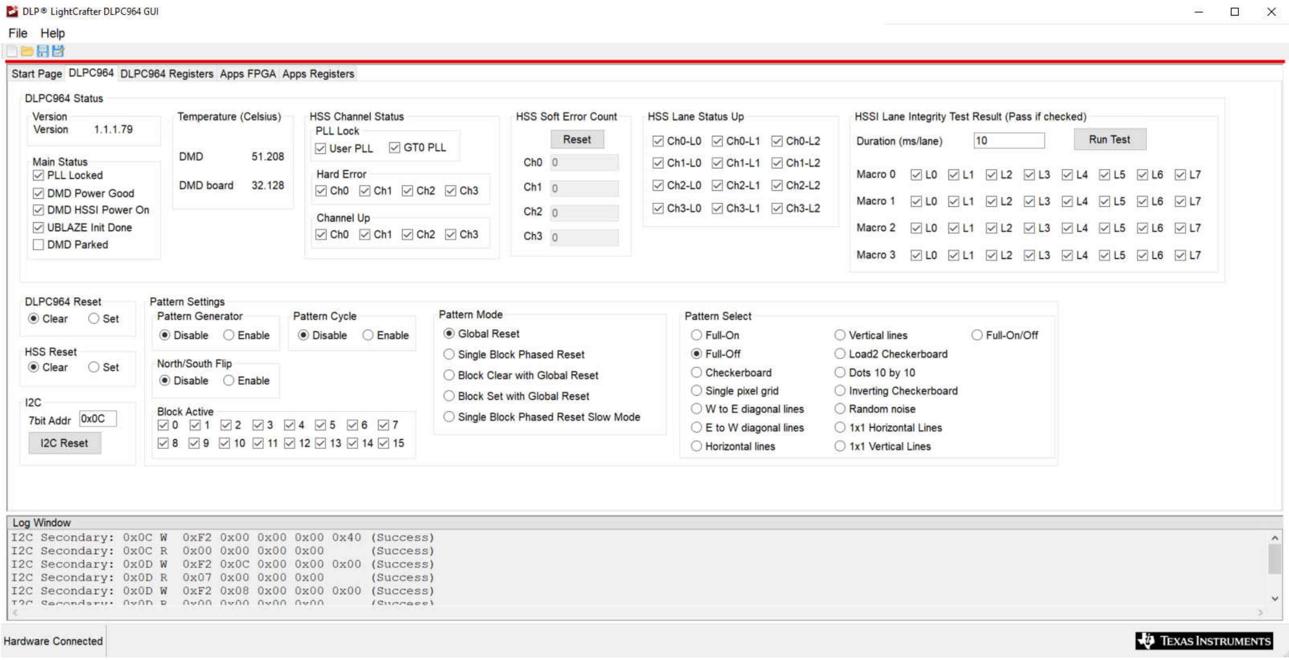

Figure 4-5. DLPC964 Tab

4.1.4.2.1 DLPC964 Status

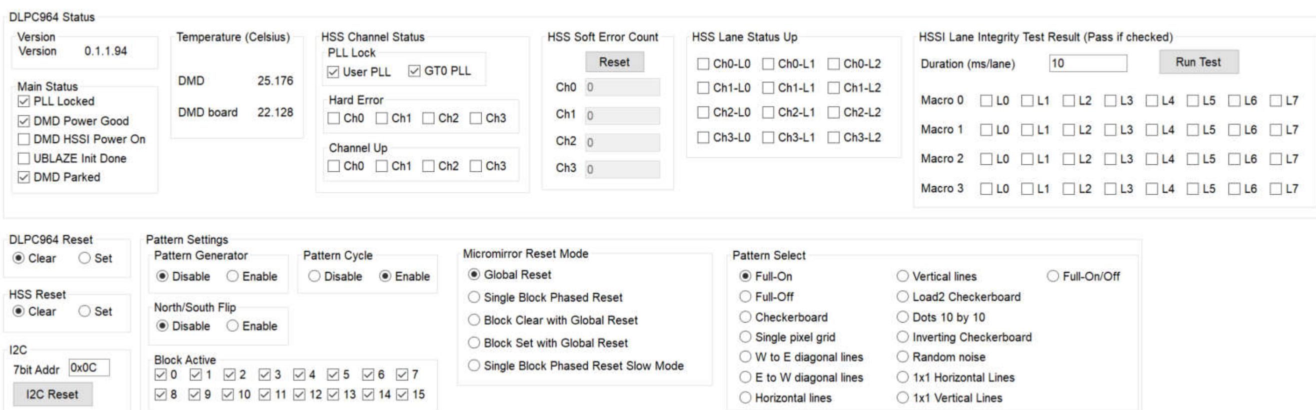

Figure 4-6. DLPC964 Status

- **DLPC641 Version** - Contains the build number and version information for the DLPC641 Firmware.
- **DLPC641 Temperature** - Displays the temperature of the PLM in Celsius
  - **DMD** - PLM internal temperature
  - **DMD Board** - Surface temperature of physical PLM board
- **Main Status** - Contains the status of the DLPC641 PLL Lock, DMD POWERGOOD, DMD High Speed Interface, UBLAZE, and DMD Parked.
- **HSS Channel Status** - Indicates the status of the Aurora 64B/66B inputs to the DLPC641 Controller.
  - **PLL Lock**
    - **User PLL** - When unchecked, the user clock is not lock. When checked, user clock is locked.
    - **GT0 PLL** - The source for the MMCM to generate the user clock and determines if the PLL is lock.
  - **Hard Error** - Indicates if the HSS requires a reset to recover from a hard error condition.
  - **Channel Up** - Determines if the Aurora Channels 0-3 are up and running.

- **HSS Soft Error Count** - Contains the Aurora 64B/66B Channel 0-3 total soft error count.
- **HSS Lane Status Up** - Indicates the status of each individual lane of the Aurora 64B/66B input to the DLPC641 Controller.
- **HSSI Lane Integrity Test Results** - The Lane Integrity Test contains the testing results of PLM High Speed Serial Interface for Channels 0-3. Each lane for this interface (7:0) can be checked for passing results.

Note

If the Channels are not passing, this results in a PLM Interface D-Sync Error.

4.1.4.2.2 DLPC964 Reset

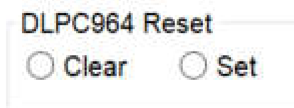

Figure 4-7. DLPC964 Reset

The **DLPC964 Reset** command causes the mirrors to change from the current state to the state of that in memory. The contents of memory are determined by the pattern that is currently selected from Pattern Select. You can choose to reset all the blocks (**Global**), or you can choose to reset blocks individually using **Single Block Mode**.

4.1.4.2.3 HSS Reset

Figure 4-8. HSS Reset

The HSS Reset command causes the HSS input and output buses to reset the data going to the DLPC641.

4.1.4.2.4 I^{2}C 7-bit Addr

Figure 4-9. DLPC641 I2C 7-bit Addr

This allows for an alternate I^{2}C address to be reset.

Note

When J6 and J8 are left unconnected, the default I^{2}C address is 0x0C. To communicate with the alternate I2C addresses, please see Table 2-3 for information regarding the jumpers that must be populated.

4.1.4.2.5 Pattern Settings

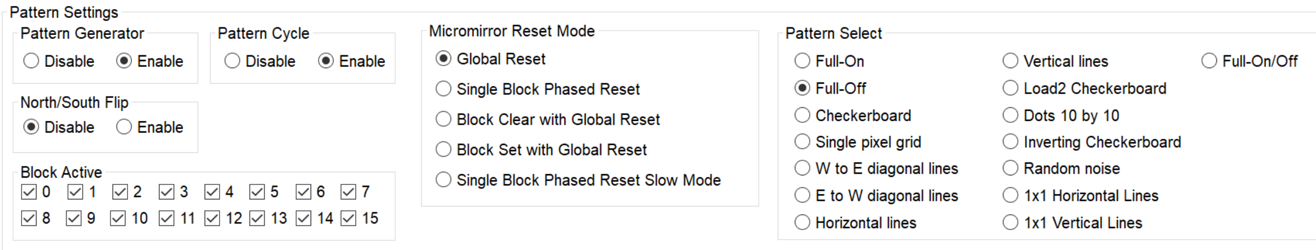

Figure 4-10. DLPC964 Pattern Settings

- **Pattern Generator** - When enabled, patterns are displayed onto the PLM. When disabled, no patterns are going to be displayed on PLM.
- **Pattern Cycle** - When enabled, the PLM cycles through the first eight predefined patterns, each being displayed every 2 seconds. When disabled, a single selected pattern is sent to the PLM.
- **North/South Flip** - Having this enabled flips the image being displayed on the PLM vertically.

Note

Certain **pattern selections** (e.g., checkerboard, grid, diagonal lines) are not applicable for the PLM and can be disregarded when using the GUI. For optimal perfromance, please use the pattern settings outlined below under *'Pattern Select'*.

- **Pattern Select**
  - **Full-On** - Full white background where all mirrors on the PLM are going to be in the on position.
  - **Full-Off** - Full black background where all mirrors on the PLM are going to be in the off position.
  - **1x1 Horizontal lines** (every row alternating black/white) - used to check for issues with row loads.
  - **1x1 Vertical lines** (every column alternating black/white) - used to check for issues with data bus lines.
  - **Full-On/Off** - Toggles between the Full-On and Full-Off pattern.
- **Micromirror Reset Mode**
  - **Global Reset** - In global reset mode, all enabled blocks are going to be loaded with data sequentially. Once all blocks have been loaded, the MCP_Start signal resets all the blocks at the same time.
  - **Single Block Phased Reset** - In single reset mode, a single block is loaded at a time and once the DLPC641 has loaded the PLM with the data sent, the MCP_Start signal resets that single block.
  - **Block Clear with Global Reset** - This mode shows how the Clear block load type is used in the DLPC641 system. A clear load type does not require any data since the block puts all of the mirrors in the off state (0). Since the clear load type does not have any data to be sent after, the command valid signal is not needed so only the PLM load signal is sent. The MCP_Start signal follows the same pattern as Global Mode.
  - **Block Set with Global Reset** - This mode shows how the Set block load type is used in the DLPC641 system. A set load type does the opposite of the clear load type and also does not require any data. The set load type sets all the mirrors in the on state (1). Just like the clear load type, there is no need for the command valid signal, only the PLM load signal. The MCP_Start signal follows the same pattern as Global Mode.
  - **Single Block Phased Reset Slow Mode** - Slow mode (or disabling the fast mode) causes the DLPC641 to receive data across a single channel only (4x 10Gbps lanes compared to 12x). To do this, each segment of a block must be sent sequentially across 1 Aurora 64B/66B channel instead of parallel. The segments must be sent in the following order: D (0x3) C (0x2) B (0x1) A (0x0). Once all four segments are sent, the MCP_Start signal can be issued. The MCP_Start signal behaves the same as in Single Mode.
- **Block Active** - There are 16 blocks [0-15] in the DLPM980E PLM. The blocks that are checked inside the GUI are going to determine what blocks are going to be reset and loaded with new data from the PLM.

4.1.4.3 DLPC964 Registers Tab

The DLPC964 Registers tab uses the I^2C Interface to communicate with the DLPC641 controller registers. This tab shows the DLPC641 controller register list and settings for each register which use Get/Set buttons to read/write to specific registers.

Note

Access to the DLPC641 registers must not begin until INIT_DONE has transitioned high (logic 1).

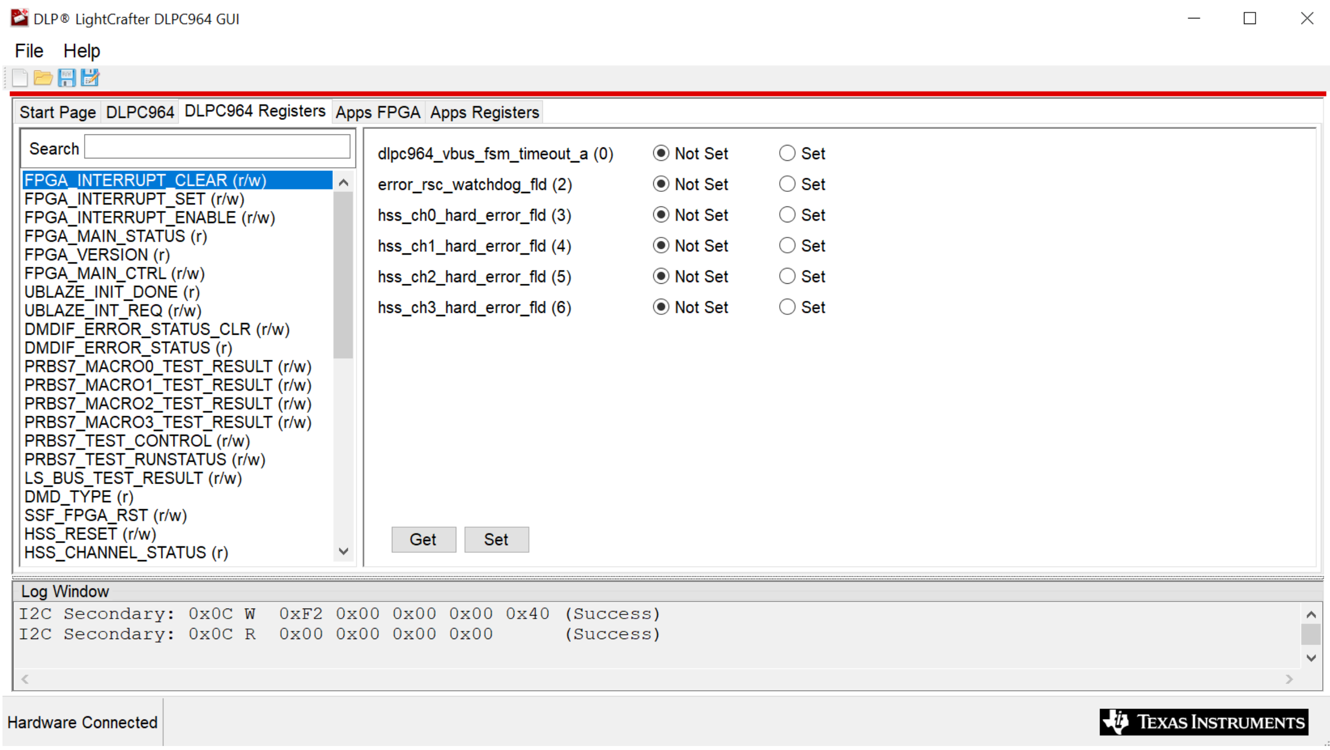

Figure 4-11. DLPC964 Register List

Register Definitions

The following designations are used throughout this section of the document:

- R - designates read only
- W - designates write only
- R/W - designates read and write
- S - designates status of register
- I - designates interrupt only
- P - designates pulse only

Please visit the DLPC964 data sheet for detailed descriptions of each DLPC641 register offered in the DLPC964 GUI.

4.1.4.4 Apps FPGA Tab

The **Apps FPGA tab** reads the status of Apps FPGA features and functions, select test patterns and configure pattern settings.

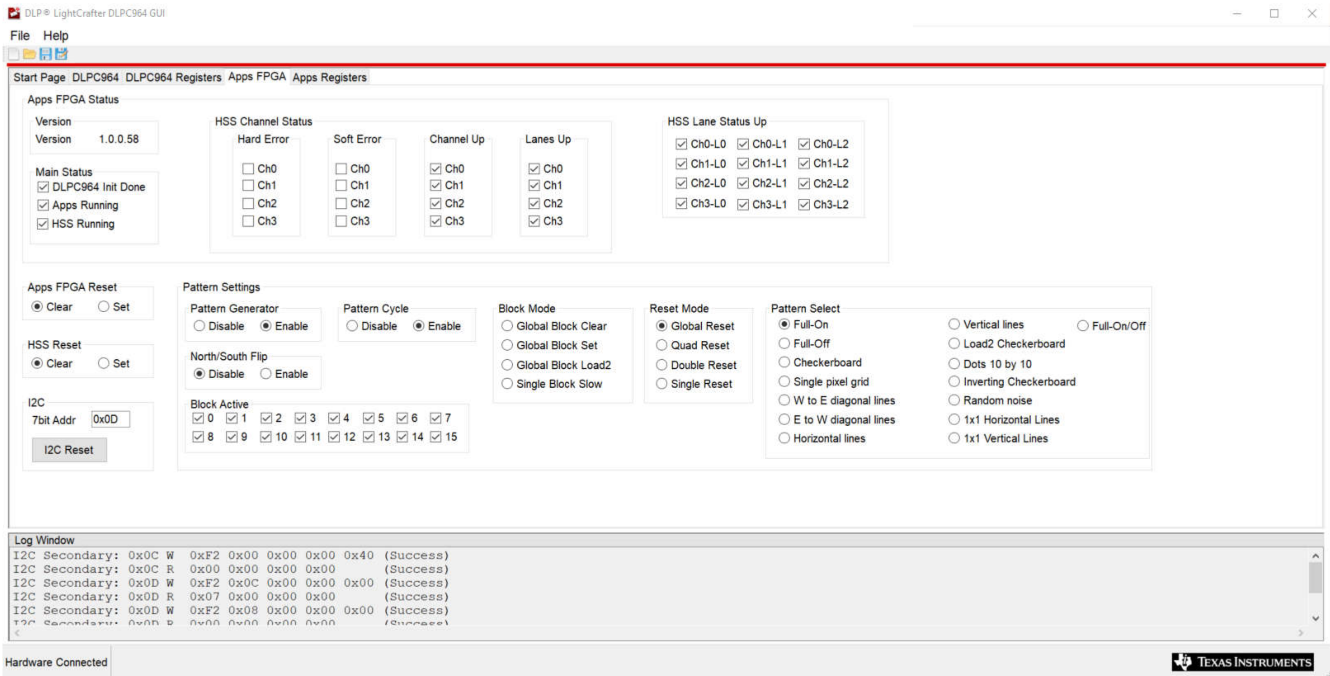

Figure 4-12. Apps FPGA Tab

4.1.4.4.1 Apps FPGA Status

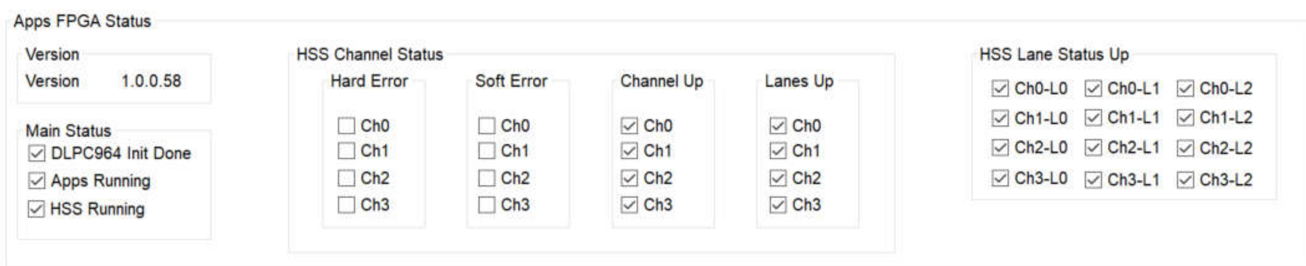

Figure 4-13. Apps FPGA Status

- **Apps FPGA Version** - Contains the build number and version information for the Apps FPGA Firmware.
- **Main Status** - This contains the status for the DLPC641, Apps FPGA, and HSS status determining if each one is up and running.
- **HSS Channel Status** - HSS Channel Status indicates the status of the Aurora 64B/66B inputs to the DLPC641 Controller.
  - **Hard Error** - Input Aurora Channel 0-3 hard error and indicates failure in the GTH.
  - **Soft Error** - The HSS Soft Error Count indicates corrupted data received on each individual channel.
  - **Channel Up** - Determines if the HSS Aurora Channels 0-3 are initialized.
  - **Lanes Up** - Determines if the HSS Aurora Lane Channels 0-3 are initialized.
- **HSS Lane Status Up** - The HSS Lane Status Up indicates the status of each individual lane of the Aurora 64B/66B input to the DLPC641 Controller.

4.1.4.4.2 Apps FPGA Reset

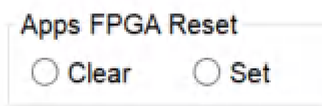

Figure 4-14. Apps FPGA Reset

The **Apps FPGA Reset** command causes the mirrors to change from the current state to the state of that in memory. The contents of memory are determined by the pattern that is currently selected from Pattern Select. You can choose to reset all the blocks (**Global**), or you can choose to reset blocks individually using **Single Block Mode**.

4.1.4.4.3 HSS Reset (Apps)

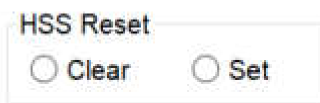

Figure 4-15. HSS Reset

The HSS Reset command causes the HSS input and output buses to reset the data of the Aurora 64B/66B interface.

4.1.4.4.4 Apps I^{2}C 7-bit Addr

Figure 4-16. DLPC641 I^{2}C 7-bit Addr

This allows for an alternate I^{2}C address to be set.

Note

When J6 and J8 are left unconnected, the default I^{2}C address is 0x0D. To communicate with the alternate I2C addresses, please see Table 2-3 for information regarding the jumpers that must be populated.

4.1.4.4.5 Pattern Settings (Apps)

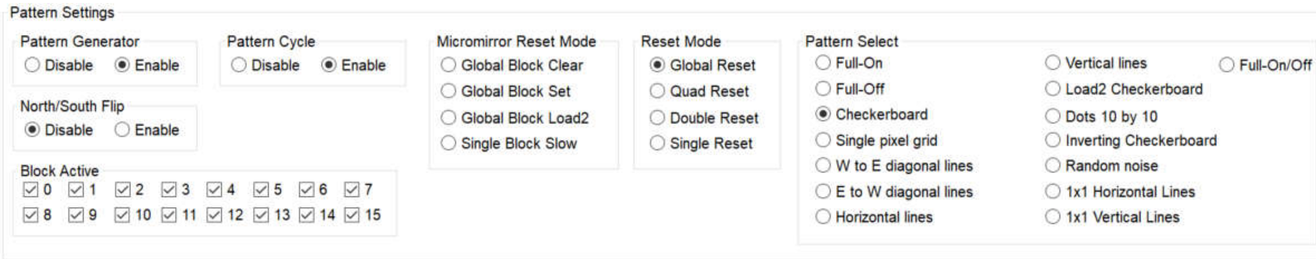

Figure 4-17. Apps FPGA Pattern Settings

- **Pattern Generator** - When enabled, patterns are displayed onto the PLM. When disabled, no patterns are going to be displayed on PLM.
- **Pattern Cycle** - When enabled, the PLM cycles through the first 8 predefined patterns, each being displayed every 2 seconds. When disabled, a single selected pattern is sent to the PLM.
- **North/South Flip** - Having this enabled flips the image being displayed on the PLM vertically.

Note

Certain **pattern selections** (e.g., checkerboard, grid, diagonal lines) are not applicable for the PLM and can be disregarded when using the GUI. For optimal perfromance, please use the pattern settings outlined below under *'Pattern Select'*.

- **Pattern Select**
  - **Full-On** - Full white background where all mirrors on the PLM are going to be in the on position.
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  - **1x1 Horizontal lines** (every row alternating black/white) - Used to check for issues with row loads.
  - **1x1 Vertical lines** (every column alternating black/white) - Used to check for issues with data bus lines.
  - **Full-On/Off** - Toggles between the Full-On and Full-Off pattern.
- **Micromirror Reset Mode**
  - **Global Block Clear** - This mode shows how the Clear block load type is used in the DLPC641 system. A clear load type does not require any data since the block puts all of the mirrors in the off state (0). Since the clear load type does not have any data to be sent, the command valid signal is not needed so only the PLM load signal is sent. The MCP_Start signal follows the same pattern as Global Mode.
  - **Global Block Set** - This mode shows how the Set block load type is used in the DLPC641 system. A set load type does the opposite of the clear load type and also does not require any data. The set load type sets all the mirrors in the on state (1). Just like the clear load type, there is no need for the command valid signal, only the PLM load signal. The MCP_Start signal follows the same pattern as Global Mode.
  - **Global Block Load2** - Enabling the Load2 operation tells the PLM to load 1 line of data received into 2 rows of the PLM. The role of the DLPC641 Apps FPGA during a Load2 operation is to verify that 68 lines, at most, are sent over the Aurora HSSI channels. Asserting LOAD2 causes the DLPC641 controller and attached PLM to load 2 rows for every row of data sent, reducing the pattern load time to half of a full PLM load. This function does not reduce the MCP timing.
  - **Single Block Slow** - Slow mode (or disabling the fast mode) causes the DLPC641 Apps FPGA to send data across a single Aurora 64B/66B channel only (4x 10Gbps lanes compared to 12x). To do this, each segment of a block must be sent sequentially across 1 channel instead of parallel. The segments must be sent in the following order: D (0x3) C (0x2) B (0x1) A (0x0). Once all four segments are sent, the MCP_Start signal can be issued. The MCP_Start signal behaves the same as in Single Mode.
- **Block Active** - There are 16 blocks [0-15] in the DLPM980E PLM. The blocks that are checked inside the GUI are going to determine what blocks are going to be reset and loaded with new data to the PLM.

4.1.4.5 Apps FPGA Registers Tab

The Apps FPGA Registers tab uses the I²C Interface to communicate with the Apps FPGA registers. This tab shows the Apps FPGA register list and settings for each register which use Get/Set buttons to read/write to specific registers.

Note

Access to the Apps FPGA registers must not begin until INIT_DONE has transitioned high (logic 1).

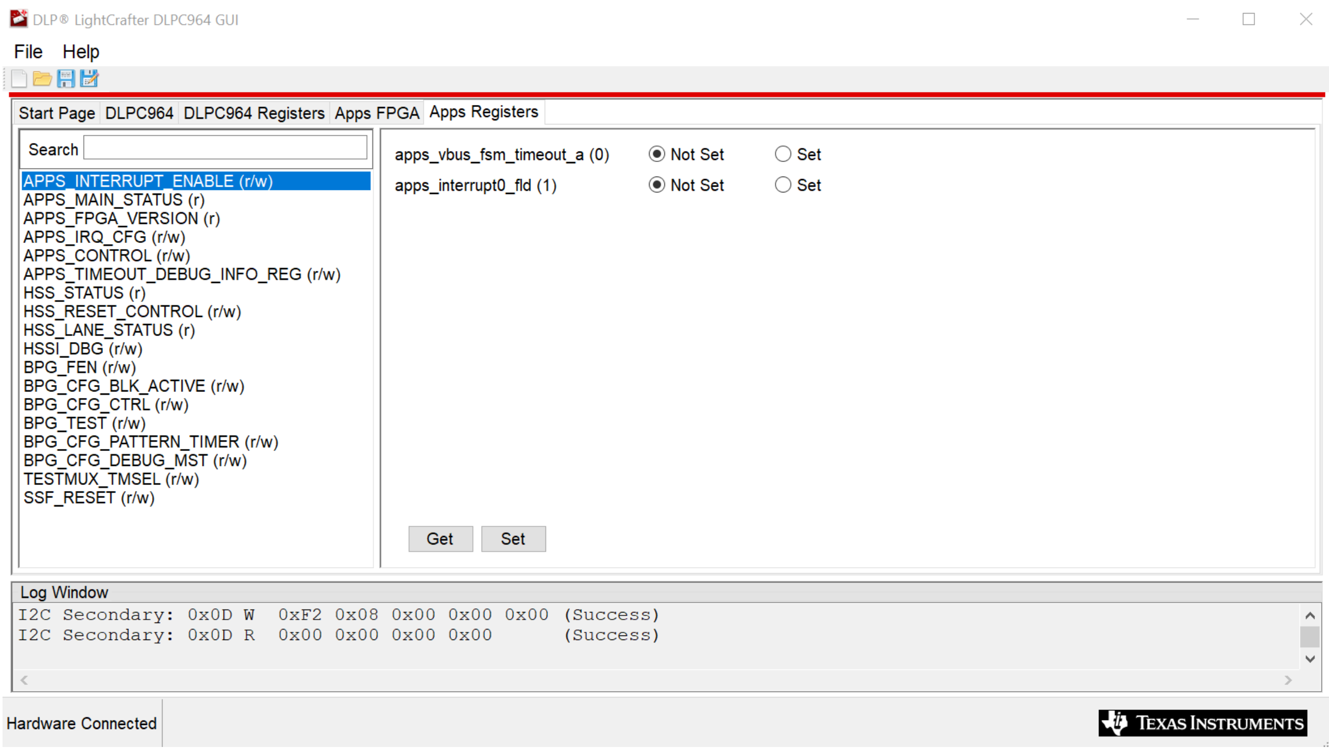


Figure 4-18. Apps FPGA Register List

Register Definitions

The following designations are used throughout this section of the document:

- R - designates read only
- W - designates write only
- R/W - designates read and write
- S - designates status of register
- I - designates interrupt only
- P - designates pulse only

Please visit the DLPC964 data sheet for detailed descriptions of each Apps FPGA register offered in the DLPC964 GUI.

4.1.5 Programming Firmware

4.1.5.1 Connecting to the DLPC964 GUI

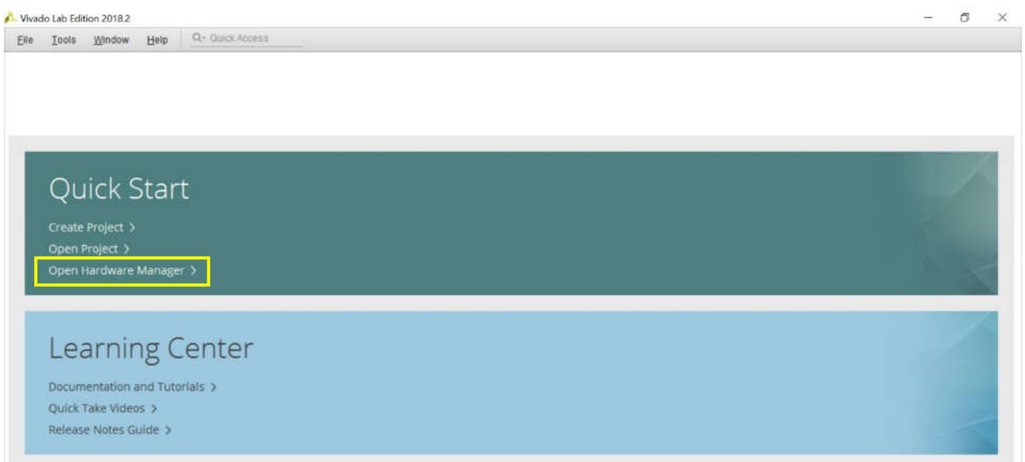
1. Connect the boards as shown in previous pages. There are two configurations:
   a. Front end with DLPC641 controller board and DLPM980E PLM board
   b. Standalone DLPC641 controller board with DLPM980E PLM board
2. Power DLPC641 controller board using 12V DC input.
3. Power on AMD EVM (if present).
4. Connect USB from DLPC641 controller board to PC.
5. Run TI DLP® DLPC964 GUI.
6. GUI displays *Hardware Connected* message in bottom left corner of status bar.

4.1.5.2 Programming the DLPC641 Controller

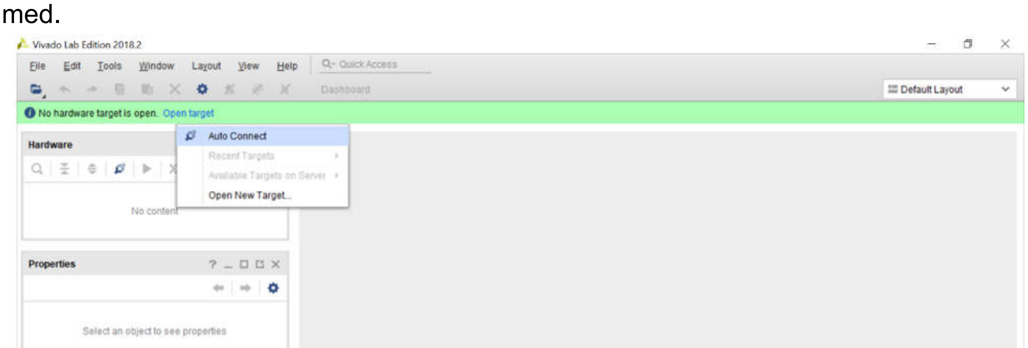
1. Launch the Vivado Lab Solutions 2018.2 application. Once the application opens, select *Open Hardware Manager* from the main window.

Note

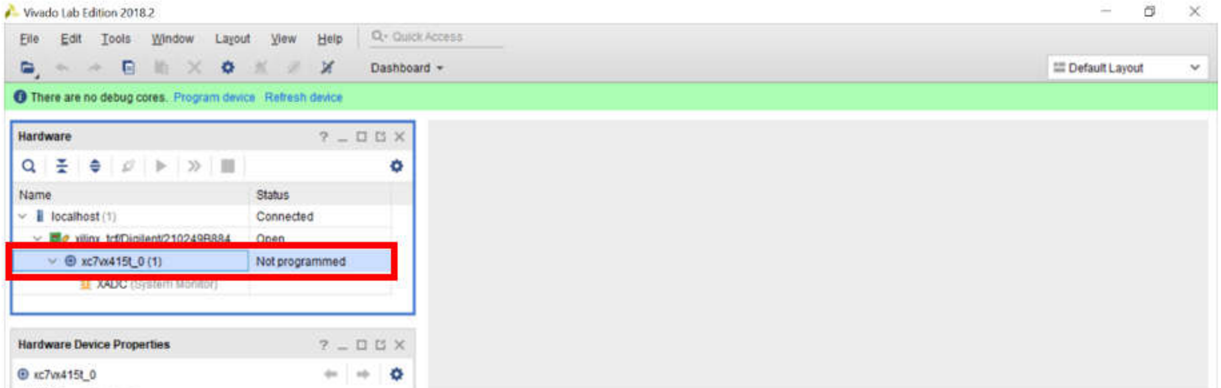
Click the link above to download Vivado Lab Solutions 2018.2. Once the web page is loaded, find the archived 2018.2 folder and then navigate to the Vivado Lab Solutions 2018.2 downloadable link and download the installation.



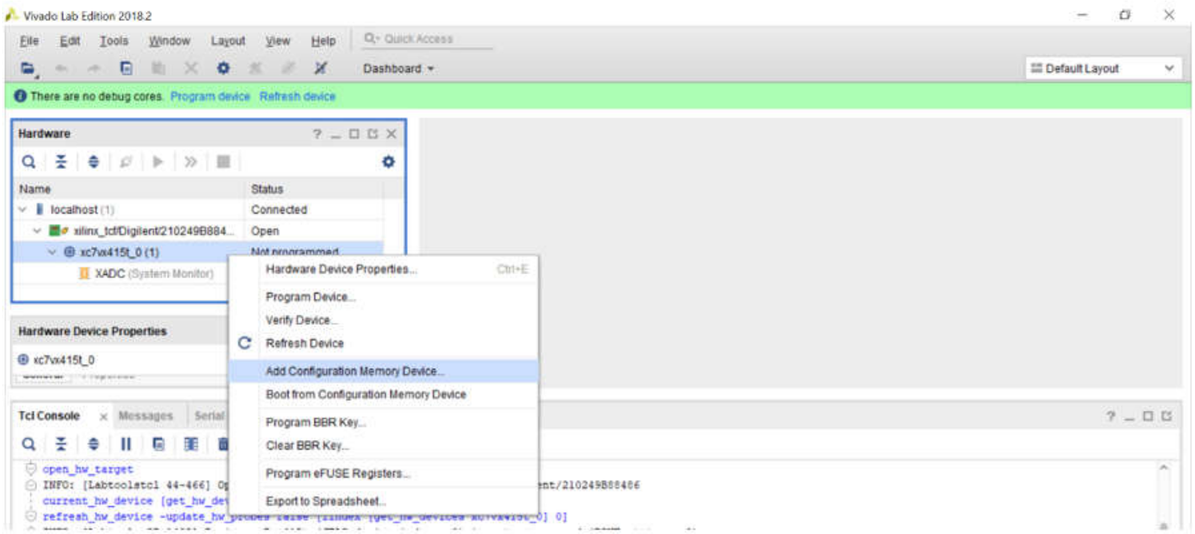
2. Once the Hardware Manager is open, check that the JTAG is connected to jumper J7 on the DLPM980E2EVM board and that the port is connected to a PC. Once JTAG is properly connected, plug the 12V DC power supply into the barrel jack on the board and power on.
3. Once JTAG is properly connected and the board is powered on, the next step is selecting the target device that is going to be programmed.
4. In the *Hardware Manager* window, select *Open Target* > *Auto Connect* to find the target device being programmed.



5. Once the target device is detected, the target device is going to be displayed in the bottom left corner, showing current status of device.



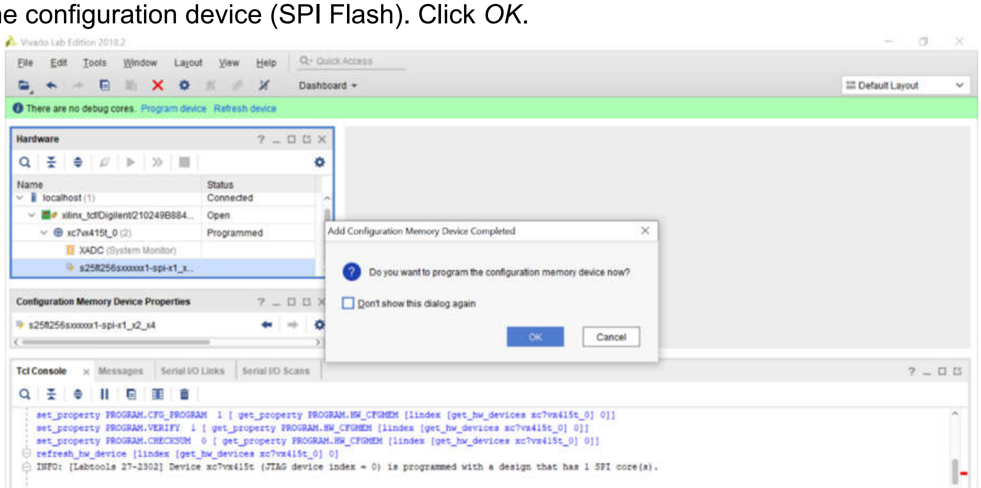
6. Right-click on the FPGA and select "*Add Configuration Memory Device*."



7. Select the correct flash device that is connected to the FPGA device on the DLPM980E2EVM board. Input the parameters below to select the correct flash device.

Manufacturer = Spansion	Type = SPI
Density = 256Mb	Width = x1_x2_x4
Part Number = s25fl256sxxxxxx1	

8. Once the appropriate flash device is selected, a dialog box is going to pop up asking if the user wants to program the configuration device (SPI Flash). Click *OK*.

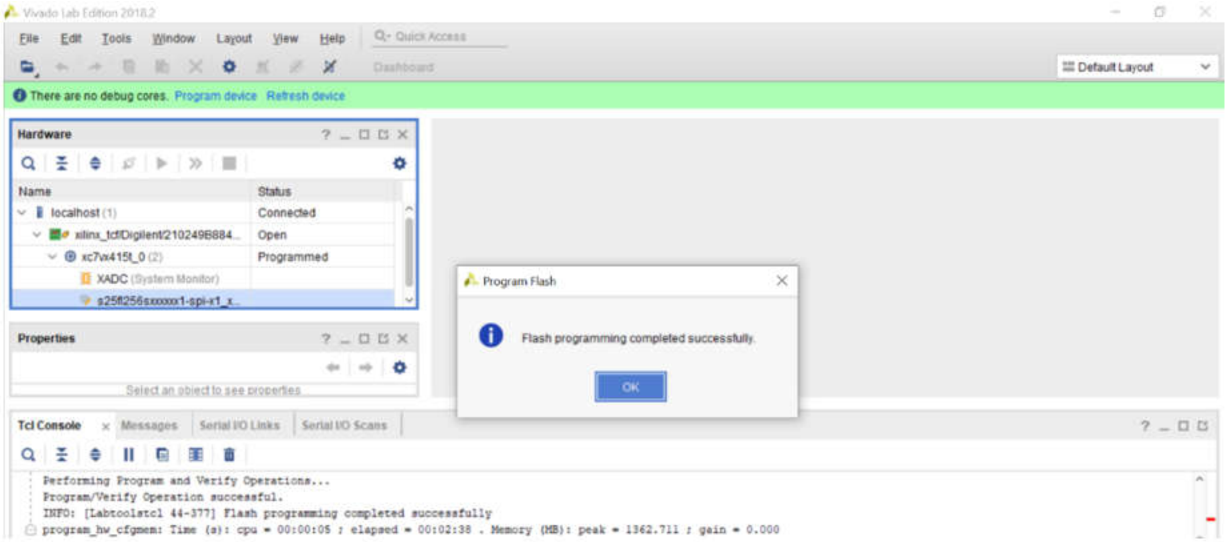


9. Go to Configuration file and select the appropriate `.mcs` file needed to program the flash device.

Note

The `.mcs` can be downloaded from the DLPM980E2EVM Tool Folder. Locate and download the DLPR964-FW package which includes the appropriate `.mcs` to program the DLPC641 Controller.

10. After clicking *OK*, the Vivado Hardware Manager is going to program the flash of the board and verify that the flash was programmed successfully.



11. Complete a power cycle on the DLPM980E2EVM board. Unplug power from the barrel jack connector J3 and then plug power back into barrel jack connector. After the FPGA is programmed successfully, DLPC641 Done (D4) is going to illuminate green and the DLPC641 Heartbeat (D5) has a heartbeat that flashes on/off.

4.1.5.3 Programming the Apps FPGA (AMD EVM)

4.1.5.3.1 Programming the Apps FPGA with Bitstream Loading

Follow the instructions below for loading the DLPC641 Apps binary onto the FPGA via a bitstream using Vivado Lab Solutions 2018.2:

Note

Click the link above to download Vivado Lab Solutions 2018.2. Once the web page is loaded, find the archived 2018.2 folder and then navigate to the Vivado Lab Solutions 2018.2 downloadable link and download the installation.

Note

The FPGA needs to be reloaded each time power is lost or disconnected from the AMD EVM.

---

1. Plug in the Micro-B USB cable into the side of the VC707 and the other end into the computer running Vivado.
2. Start Vivado Lab Solutions 2018.2 on the computer.
3. Select *Open Hardware Manager* from the main window..
4. Click *open target* located in the top left of the hardware manager then *Auto Connect*.
    a. If the AMD EVM is the only FPGA plugged into the computer, then Vivado automatically connects to the AMD EVM.
5. Right-click on the FPGA and select *Program Device*.
6. Navigate to the appstop.mcs file and select *Program*.

4.1.5.3.2 Programming Apps FPGA by Flash

Follow the instructions below for loading the DLPC641 Apps binary onto the flash via a bitstream using Vivado Lab Solutions 2018.2:

Note

Click the link above to download Vivado Lab Solutions 2018.2. Once the web page is loaded, find the archived 2018.2 folder and then navigate to the Vivado Lab Solutions 2018.2 downloadable link and download the installation.

Note

The bitstream is always loaded onto the FPGA upon power-up of the AMD EVM.

---

1. Plug in the micro USB into the side of the AMD EVM and the other end into the computer running Vivado.
2. Make sure to set SW11 to 00010 (1 = on, Position 1 → Position 5, left to right).

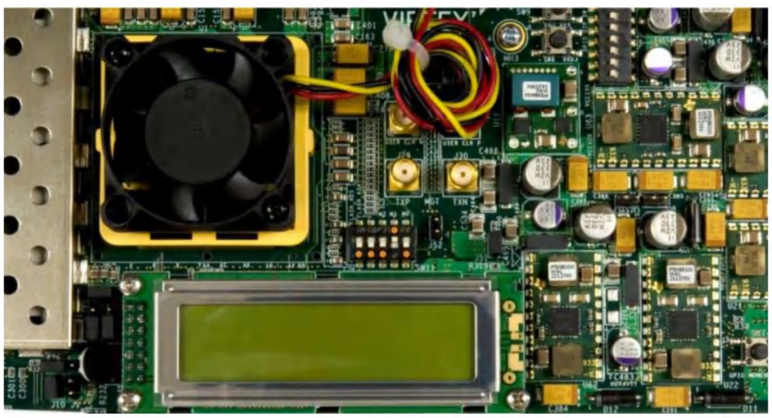


Figure 4-19. FPGA Configuration Mode

3. Set SW2 to 00000000 (1 = on, Position 1 → Position 8, left to right).

Figure 4-20. GPIO Dip Switches (VC707)

4. Start Vivado Lab Studios 2018.2 on the computer.
5. Select *Open Hardware Manager* from the main window.
6. Click *open target* located in the top left of the hardware manager then *Auto Connect*.
    a. If the AMD EVM is the only FPGA plugged into the computer, then Vivado automatically connects to the AMD EVM. Otherwise, the process is slightly more involved.
7. Right-click on the FPGA and select *Add Configuration Memory Device*.
8. Find the Flash name mt28gu01gaax1e-bpi-x16 and click *OK*.
9. Select OK again and select the configuration file (appstop.mcs).
    a. Make sure all other settings match.
10. Once setup, click *OK*. The programming can take a few minutes.
11. Once completed, power cycle the AMD EVM, and the DLPC641 Apps Bitstream automatically loads onto the AMD EVM.

5 Hardware Design Files

5.1 Schematics

The schematics are available for download on the DLPM980E2EVM Tool Folder.

5.2 PCB Layout

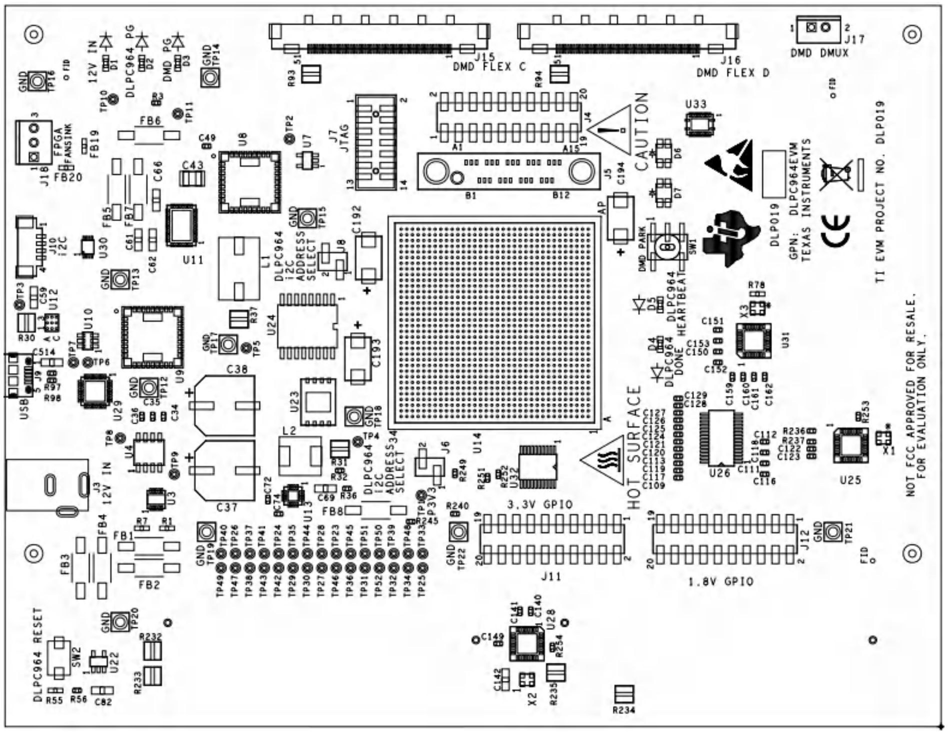


Figure 5-1. DLPM980E2EVM PCB (Front)

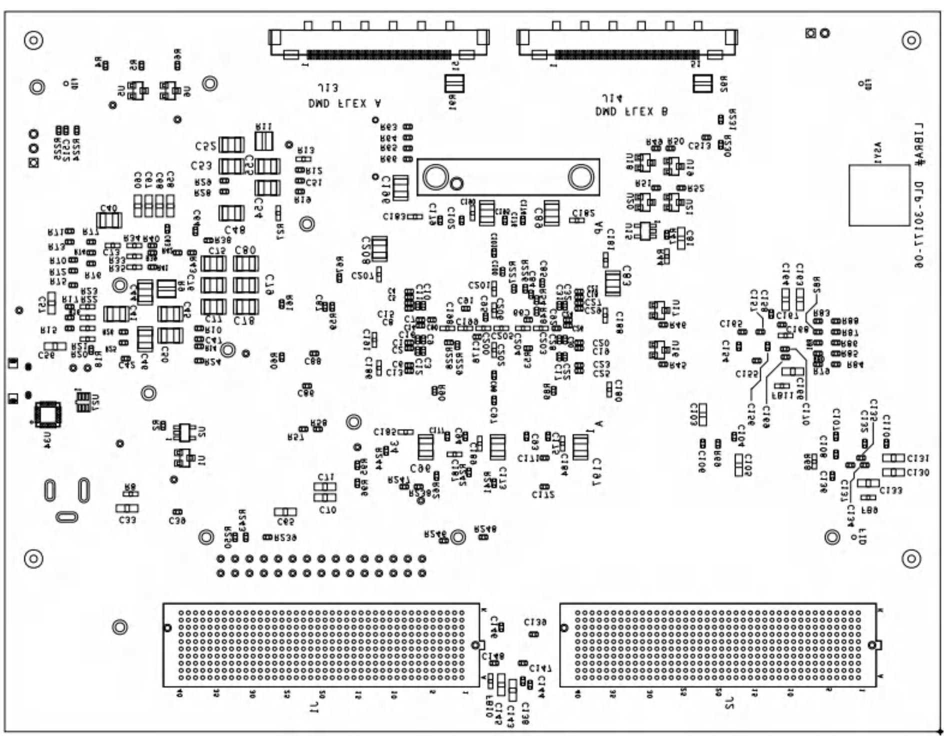


Figure 5-2. DLPM980E2EVM PCB (Back)

5.3 Bill of Materials (BOM)

Table 5-1 lists the Bill of Materials for the DLPM980E2EVM.

Table 5-1. DLPM980E2EVM Bill of Materials

Reference	Quantity	Part	MFG	MFG Part Number
C1,C2,C3,C4,C5,C6,C7,C8,C9,C10,C11,C12,C13,C14,C15,C16,C17,C18,C19,C20,C21,C22,C23,C24,C25,C26,C27,C28,C29,C30,C31,C32	32	0.1u	American Technical Ceramics	530L104KT16T
C33	1	22u	Samsung	CL21A226MOCLRNC
C34,C35,C36,C39,C42,C49,C64,C84,C85,C86,C87,C88,C90,C91,C92,C93,C94,C95,C97,C98,C99,C100,C101,C102,C104,C106,C107,C108,C109,C111,C112,C113,C116,C117,C118,C119,C120,C121,C122,C123,C124,C125,C126,C127,C128,C129,C132,C134,C135,C136,C139,C140,C141,C144,C146,C147,C148,C150,C151,C152,C153,C154,C155,C156,C157,C159,C160,C161,C162,C165,C167,C168,C169,C171,C172,C174,C175,C176,C177,C178,C179,C513	82	0.1u	Samsung	CL05A104KA5NNNC
C37,C38	2	1000u	Panasonic	EEE-FT1C102AV
C40,C45,C46,C48,C50,C52,C53,C54,C77,C78,C79,C80,C89,C96,C173,C196,C197	17	100u	KEMET	C0402C822K5RACTU
C41,C43,C83,C195	4	47u	KEMET	C1210C476M4PACTU
C44,C55	2	220u	Murata	GRM32ER60J227ME05L
C47,C51	2	0.01u	KEMET	C0402C103K5RACTU
C56,C57,C58,C69,C81,C82,C514	7	1u	Yageo	CC0805KKX7R9BB105
C59,C60,C61,C62,C65,C66,C67,C68,C70,C71	10	22u	Samsung	CL21A226MOCLRNC
C63	1	2200p	Yageo	AC0402KRX7R8BB222
C72,C110,C138,C158	4	0.01u	KEMET	C0402C103K5RACTU
C73,C180,C181,C182,C183,C184,C185,C186,C187,C188,C189,C190,C191,C198,C199,C200,C201,C202,C203,C204,C205,C206,C207	23	4.7u	TDK	C1608X5R1E475K080AC
C74	1	3900p	KEMET	C0402C392K5RAC7867
C75,C76,C208	3	330u	Taiyo Yuden	MSASA32MAC6337MPCDT1
C103,C105,C130,C131,C133,C142,C143,C145,C163,C164,C166	11	10u	Samsung	CL21A106KAYNNNE
C137,C149,C170	3	0.047u	Murata	GRM155C71H473KE19D
C192,C193,C194	3	680u	Panasonic	ETCF680M6L
C512	1	36p	KYOCERA	04025A360JAT2A
D1,D2,D3	3	LED_BLUE_SMT	Lite-On	LTST-C193TBKT-5A
D4,D5	2	LED_GREEN_SMT	Lite-On	LTST-C193KGKT-5A
D6,D7	2	DUAL_LED_GRN_RED_SMT	Lite-On	LTST-C155GEKT
FB1,FB2,FB3,FB4,FB5,FB6,FB7,FB8	8	FB	Laird	35F0121-1SR-10
FB9,FB10,FB11,FB19,FB20	5	FB	Laird	HI0603P600R-10
J1	1	FMC 400POS CONNECTOR	SAMTEC	SEAM-40-11.0-S-10-2-A-K-TR
J1,J2	2	SEAM-40-11.0-S-10-2-A-K-TR	SAMTEC	SEAM-40-11.0-S-10-2-A-K-TR

Table 5-1. DLPM980E2EVM Bill of Materials (continued)

Reference	Quantity	Part	MFG	MFG Part Number
J3	1	PJ-002AH	CUI	PJ-002AH
J4,J11,J12	3	TSM-110-01-L-DV-P	Samtec	TSM-110-01-L-DV-P
J5	1	EM,CONN,P6419 Footprint		
J6,J8	2	TSM-102-01-L-SV	Samtec	TSM-102-01-L-SV
J7	1	JTAG	Molex	878321420
J9	1	10118194-0001LF	Amphenol	10118194-0001LF
J10	1	53398-0471	Molex	533980471
J13,J14,J15,J16	4	FI-RE51S-HF-R1500	JAE	FI-RE51S-HF-R1500
J17	1	B2B-EH	JST	B2B-EH-A(LF)(SN)
J18	1	22-23-2031	Molex	22232031
L1	1	150n	Eaton	FP1107R2-R15-R
L2	1	1uH	TDK	SPM6530T-1R0M120
R1,R27	2	1 Meg	Vishay Dale	CRCW06031M00DHEAP
R2,R47,R56,R62,R67,R238,R239,R240,R241,R242,R243,R244,R245,R246,R247,R248,R249,R250	18	10k	Samsung	RC1005F103CS
R3,R15,R16,R17,R18,R57,R76,R77	8	2.2K	Panasonic	ERJ-2RKF2201X
R4,R5,R6	3	1.8K	Panasonic	ERJ-2GEJ185X
R7	1	150k	Panasonic	ERJ-3EKF1503V
R8	1	130K	Yageo	RC0603FR-07130KL
R9,R11,R30,R31,R37,R91,R92,R93,R94	9	10m	Rohm	LTR18EZPFU10L0
R10,R12,R38,R72,R73,R74,R81,R83,R84,R85,R87,R97,R98,R230,R231,R236,R237,R253,R254	19	0	Samsung	RC1005J000CS
R13,R21,R22,R23,R78	5	100K	TE Connectivity	CRG0603F100K
R14	1	316	Vishay Dale	CRCW0402316RFKED
R19	1	2.15K	Panasonic	ERJ-2RKF2151X
R20,R33,R34,R35,R68	5	100K	TE Connectivity	CRG0603F100K
R24,R39	2	90.9K	Panasonic	ERJ-2RKF9092X
R25,R26,R28,R29,R43,R70,R71,R75,R79,R80,R82,R86,R88	13	0	Samsung	RC1005J000CS
R32	1	80.6K	Panasonic	ERJ-2RKF8062X
R36	1	160k	Panasonic	ERJ-2GEJ164X
R40	1	133k	Yageo	AC0402FR-07133KL
R41	1	42.2K	Panasonic	ERJ-2RKF4222X
R42	1	61.9K	Panasonic	ERJ-2RKF6192X
R44,R55	2	20K	Yageo	ERJ-3EKF2002V
R45,R46,R49,R50,R51,R52	6	270	Panasonic	ERJ-2RKF2700X
R48,R53,R63,R64,R65,R66	6	4.7K	Samsung	RC1005J472CS
R54	1	330	Panasonic	ERJ-2RKF3300X
R58,R61,R224,R225	4	22	Panasonic	ERJ-2GEJ220X
R59,R60	2	2.2K	Panasonic	ERJ-2RKF2201X
R69,R89,R90,R226,R227,R228,R229,R251,R252	9	100	Samsung	RC1005F101CS
R95	1	80.6K	Panasonic	ERJ-2RKF8062X
R96	1	160k	Panasonic	ERJ-2GEJ164X
R232,R233,R234,R235	4	10m	Rohm	LTR18EZPFU10L0
SW1	1	SW SPST	C&K COMPONENTS	GT12MSCBE

Table 5-1. DLPM980E2EVM Bill of Materials (continued)

Reference	Quantity	Part	MFG	MFG Part Number
SW2	1	EVQ-PE105K	Panasonic	EVQ-PE105K
TP1,TP2,TP3,TP4,TP5,TP6,TP7,TP8,TP9,TP10,TP11,TP23,TP24,TP25,TP26,TP27,TP28,TP29,TP30,TP31,TP32,TP33,TP34,TP35,TP36,TP37,TP38,TP39,TP40,TP41,TP42,TP43,TP44,TP45,TP46,TP47,TP48,TP49,TP50,TP51,TP52	41	Testpoint		
TP12,TP13,TP14,TP15,TP16,TP17,TP18,TP19,TP20,TP21,TP22	11	GND Testpoint	Keystone	5006
U1	1	N-CHANNEL MOSFET	Diodes Inc	DMN67D8L-7
U2,U7	2	SN74LVC1G07	Texas Instruments	SN74LVC1G07DBVR
U3	1	TPS259241	Texas Instruments	TPS259241DRCT
U4	1	CSD17579	Texas Instruments	CSD17579Q5AT
U5,U6,U16,U17,U18,U19,U20,U21	8	N-CHANNEL MOSFET	FAIRCHILD SEMI	FDV303N
U8,U9	2	LMZ31710	Texas Instruments	LMZ31710RVQR
U10	1	LM3880-1AE	Texas Instruments	LM3880QMFE-1AE/NOPB
U11	1	TPS548B22	Texas Instruments	TPS548B22RVFT
U12	1	TPS8268180	Texas Instruments	TPS8268180SIPT
U13	1	TPS62095	Texas Instruments	TPS62095RGTR
U14	1	DLPC641ZUM	DLP	DLPC641ZUM
U15,U22	2	SN74LVC1G17	Texas Instruments	SN74LVC1G17DBVRG4
U23	1	S25FS256SAGNF	Cypress	S25FS256SAGNFI000
U24	1	S25FL256SAGMFI011	Cypress	S25FL256SAGMFI011
U25	1	CDCM61002	Texas Instruments	CDCM61002RHBR
U26	1	DS90LV110T	Texas Instruments	DS90LV110TMTC/NOPB
U27	1	TPD4E1U06	Texas Instruments	TPD4E1U06DCKR
U28	1	CDCM61001	Texas Instruments	CDCM61001RHBT
U29	1	CY7C65215	Cypress	CY7C65215-32LTXI
U30	1	TCA9406	Texas Instruments	TCA9406DCUR
U31	1	CDCM61004	Texas Instruments	CDCM61004RHBT
U32	1	TXB0108PWR	Texas Instruments	TXB0108PWR
U33	1	SN74AUC245	Texas Instruments	SN74AUC245RGYR
U34	1	CY7C65211A	Infineon	CY7C65211A
X1,X2	2	PLMK6CE02400CDLFT	Texas Instruments	PLMK6CE02400CDLFT
X3	1	PLMK6CE02812CDLFT	Texas Instruments	PLMK6CE02812CDLFT

6 Additional Information

6.1 Abbreviations and Acronyms

The following lists abbreviations and acronyms used in this manual:

Apps FPGA	AMD Xilinx Virtex 7 FPGA on the VC-707 EVM or similar board for customer applications
BOM	Bill of Materials
BPG	Bitplane Pattern Generator
DLL	Dynamic Link Library
DMD	Digital Micromirror Device
EVM	Evaluation Module (Board)
FMC	FPGA Mezzanine Connector
FPGA	Field Programmable Gate Array
FW	Firmware
GPIO	General Purpose Input Output
GUI	Graphical User Interface
HPC	High Pin Count
HSS	High Speed Serial
HSSI	High Speed Serial Interface
HW	Hardware
I^2C	Inter-Integrated Circuit
LED	Light Emitting Diode
MCP	Mirror Clocking Pulse
NC	Not Connected
PC	Personal Computer
PCB	Printed Circuit Board
PG	Power Good
PLL	Phase-Locked Loop
PLM	Phase Light Modulator
PROM	Programmable Read-Only Memory
SW	Switch
USB	Universal Serial Bus
VHDL	Verification and Hardware Description Language

6.2 Trademarks

DLP® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

6.3 Safety

6.3.1 Caution Labels

CAUTION

The DLPM980E2EVM contains ESD-sensitive components. Handle with care to prevent permanent damage.

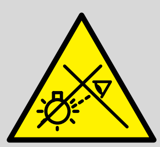
CAUTION

The DLPC641 controller board that comes with the DLPM980E2EVM has an FPGA core voltage of 12V to 1.2V at 25A. Exercise caution when handling the DLPM980E2EVM boards to avoid potential damage to components.

CAUTION

To minimize the risk of fire or equipment damage, make sure that air is allowed to circulate freely around the DLPC641EVM controller board and DLPM980E2EVM PLM board while operating.

CAUTION



When choosing your illumination component (not included with this EVM), the end user must consult the illuminator data sheet supplied by the illuminator manufacturer to identify and review any potential eye hazards associated with the illuminator chosen. Always consider and implement the use of effective light filtering and darkening protective eye wear and be fully aware of surrounding laboratory-type setups when viewing intense light sources that can be required to minimize or eliminate such risks to avoid accidents relating to temporary blindness.

7 Reference Documentation

1. DLPM980E2EVM Tool Folder
2. DLPC964 Apps FPGA User's Guide
3. Getting Started with the Virtex-7 FPGA VC707 Evaluation Kit
4. VC707 Evaluation Board for Virtex-7 FPGA

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from March 11, 2024 to October 31, 2024 (from Revision * (March 2024) to Revision A (October 2024)) **Page**

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI’s recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI’s recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI’s instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

    8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

    8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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