参考資料

デザイン・ガイド: TIDA-010015
94.5%効率、500Wの産業用AC/DCのリファレンス・デザイン

概要

このリファレンス・デザインは、小型、高効率、24V DC、500Wの産業用AD/DC電源です。このデザインは、UCC28064Aを基礎とするフロント・エンドの2相インターリーブ遷移モード(TM)力率補正(PFC)で構成されます。これにより、PFCのインダクタのサイズが最小化され、EMIフィルタの要件が軽減します。このDC/DCは、TIのUCC256301デバイスを使用したHB-LLC段により実装されます。効率性向上のため、2次側にはUCC24612による同期整流を使用しています。

リソース

TIDA-010015	デザイン・フォルダ
UCC28064A	プロダクト・フォルダ
UCC256301	プロダクト・フォルダ
UCC24612	プロダクト・フォルダ
CSD19505KCS	プロダクト・フォルダ
UCC27517	プロダクト・フォルダ
LP2951-N	プロダクト・フォルダ
TL431A	プロダクト・フォルダ
TL331	プロダクト・フォルダ
TLV171	プロダクト・フォルダ
INA181	プロダクト・フォルダ

TI E2E™ Community

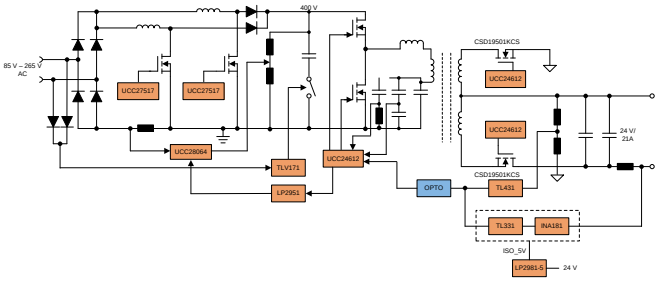
E2E™エキスパートに質問

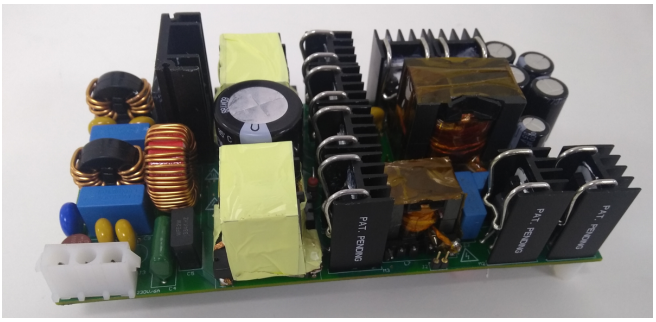
特長

- 全負荷時の総合効率 94.5%、ピーク効率は 95% を超え、スタンバイ電力は 200mW 未満
- 強制冷却不要で最大 330W で動作
- 0.99を上回る高い力率で、PFC規制およびIEC 61000-3-2 Class Aの電流THD規格に準拠
- *伝導EMI規格*(EN55011 Class B)の要件に合致
- LLCコントローラのZCS(ゼロ電流スイッチング)防止機能とOVPセンシング機能により堅牢性が向上し、システムを過電流、短絡、過電圧から保護して安全性を保証
- 160 x 80 x 35mm の小型 PCB フォーム・ファクタ

アプリケーション

- 産業用 AC/DC
- DIN レール電源
- コンシューマ用AC/DC
- バッテリ充電器





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1 System Description

Industrial AC/DC power supplies are used in various applications such as process control, data logging, machinery control, instrumentation, factory automation, and security systems. These AC/DC supplies provide a convenient means for powering DC operated devices including programmable logic controllers (PLCs), sensors, transmitters and receivers, analyzers, motors, actuators, solenoids, relays, and so on. These supplies are convection cooled and need to support features like power boost where it supplies a increased output load for a short duration. The supplies operate over a wide input range from 85- to 265-V AC, delivering full load for entire input voltage range. The output voltages from these supplies range from 5 to 56 V with power ratings from 7.5 to 500 W. Many of these supplies can be connected in parallel for higher power applications.

This reference design is a 500-W high efficiency industrial AC/DC power supply. The design consists of a two-phase-interleaved, critical conduction mode (CrCM) PFC converter, which operates from an input voltage range of 85- to 265-V AC RMS and generates a 400-V DC bus. The second stage is made up of an isolated half-bridge LLC stage, which generates a 24-V, 20-A nominal output. Industrial power supplies have requirements of high efficiency over their entire operating voltage range and wide load variations from a 50% to 100% load. This design demonstrates high efficiency operation in a small form factor (155 × 125 mm) and delivers continuous 480 W of power over the entire input operating voltage range from 85- to 265-V AC. It gives an efficiency of > 94.5% for 230-V AC nominal operation and 92% for 115-V AC nominal operation.

The UCC28064A PFC integrated circuit (IC) controls the interleaved CrCM PFC stage. Interleaved critical conduction mode (CrCM) and continuous conduction mode (CCM) are the two popular topologies for PFC applications with greater than 300-W output power. CrCM PFC has the advantage of minimizing the turnon losses on the PFC MOSFET and eliminates the reverse recovery on the boost diode to reduce losses. CrCM PFC also has a much smaller inductor value than the CCM PFC. The reduced boost inductor value helps to develop the low-profile magnetics necessary for meeting the thin-profile requirement in the design. By interleaving two CrCM power stages, the effective input ripple current is reduced and helps to minimize the EMI filter requirement. The HB-LLC power stage is controlled through the stage of the art UCC256301 resonant controller, which implements current mode control for increased control bandwidth. This increased control bandwidth reduces the output capacitors required to suppress the AC ripple on the output. To achieve high efficiency, the output of the LLC stage uses synchronous rectification based on the UCC24612 device and the CSD19505KCS MOSFET.

The design has low standby power of < 200 mW and meets ENERGY STAR rating requirements as well as 2013 EU eco-design directive ErP Lot 6. The EMI filter is designed to meet EN55011 class-B conducted emission levels. The design is fully tested and validated for various parameters such as regulation, efficiency, EMI signature, output ripple, start-up, and switching stresses. Overall, the design meets the key challenges of industrial power supplies to provide safe and reliable power with all protections built-in, while delivering high performance with low power consumption and low bill-of-material (BoM) cost.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CONDITIONS					
Input voltage (V_{INAC})	–	85	230	265	VAC
Frequency (f_{LINE})	–	47	50	63	Hz
No load power (PSB)	–	–	200	–	mW
OUTPUT CONDITIONS					
Output voltage	Full load (500 W)		24		V
Output current	Full load (500 W)		21		A
Line regulation	V_{IN} from 85 VAC to 265 VAC, 500-W load			0.5	%
Load regulation	V_{IN} = 230 V, output load from 50 W–500 W			1	%
Output voltage ripple	V_{IN} = 230 V, load = 500 W,		200		mV
Output power (nominal)				500	W
SYSTEM CHARACTERISTICS					
Efficiency (η)	V_{IN} = 230-V AC RMS and full load at 24-V output		94.5		%
	V_{IN} = 115-V AC RMS and 230-W load at 24-V output		92		%
Protections	Output overcurrent		25		A
	Output overvoltage		30		V
Operating ambient	Open frame	-10	25	55	°C
Standards and norms	Power line harmonics	As per IEC 61000-3- 2 Class A			
	Conducted emissions	EN55022 Class B			
	EFT	As per IEC-61000-4-4			
	Surge	As per IEC-61000-4-5			
Board form factor	FR4 material, 2-layer, 2-oz copper	160 × 80 × 35			mm

2 System Overview

2.1 Block Diagram

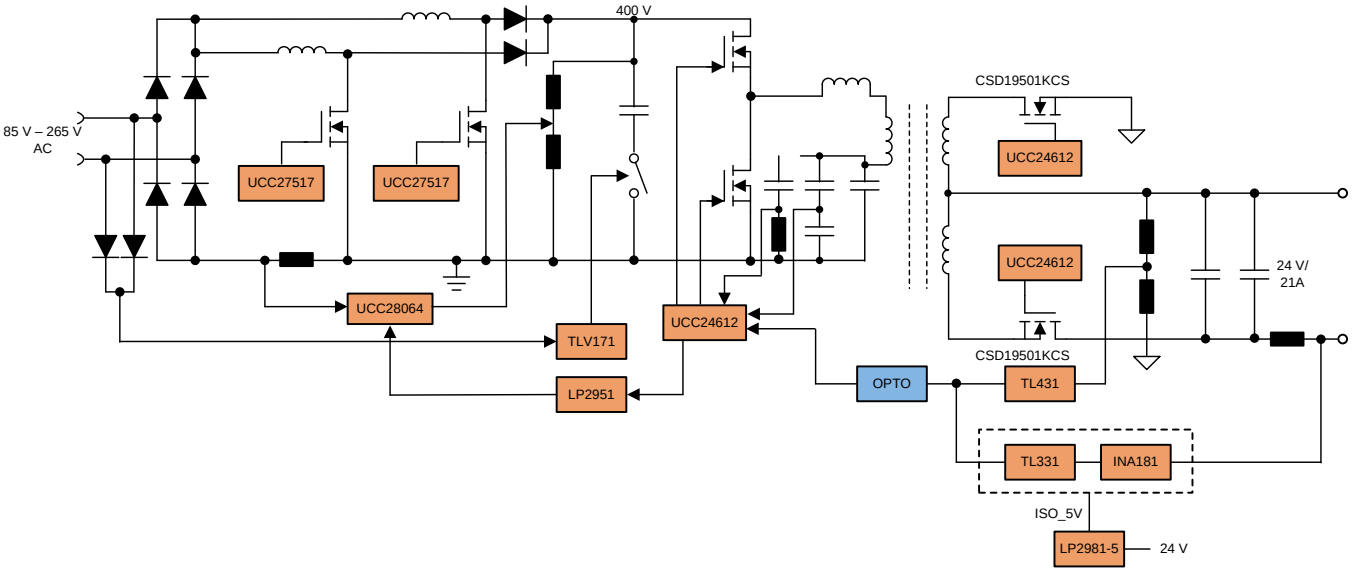

図 1. TIDA-010015 Block Diagram

図 1 shows the high-level block diagram of this reference design. The main parts of this design are the UCC28064A (PFC controller), UCC256301 (LLC controller), UCC24612-2 (multi-mode synchronous rectifier controller), and CSD19505KCS (80-V MOSFET).

2.2 Highlighted Products

2.2.1 UCC28064A

The UCC28064A is a two-phase, naturally-interleaved, transient-mode power factor correction (PFC) controller for implementing a high-efficiency, low-component-count, front-end AC/DC PFC stage. The two phase interleaved power stage reduces the filter requirements for input current ripple electromagnetic interference (EMI).

Interleaving control and phase management facilitates high efficiency 80+ and Energy Star designs with reduced input and output ripple. The Natural Interleaving method allows TM operation and achieves 180 degrees between the phases by On-time management and does not rely on tight tolerance requirements on the inductors. The Crossover Notch Reduction block implements a non-linear current shaping characteristic on the instantaneous voltage sense (VINAC) to reduce distortion and increase Power Factor. Negative current sensing is implemented on the total input current instead of just the MOSFET current which prevents MOSFET switching during inrush surges or in any mode where the inductor current may become substantially continuous (CCM). This prevents reverse recovery conduction events between the MOSFET and output rectifier.

2.2.2 UCC256301

Series resonant converters like LLC are one of the most widely used topologies for implementing medium- to high-power isolated DC/DC power stages in consumer and industrial power supplies. LLC resonant converters are quite popular due to their ability to achieve soft-switching (ZVS turnon) for high-voltage MOSFETs, thereby improving the overall efficiency of a system.

The UCC256301 has a unique, hybrid hysteretic control that provides excellent line and load transient response, minimizing the requirement for output filter capacitors. The wide frequency range of the device can be used to reduce the PFC bulk capacitor required to meet the holdup time requirement in the industrial power supplies. With the integrated high-voltage gate drive, X-Cap discharge function, and additional output overvoltage protection, the UCC256301 reduces the amount of external discreet components required to implement a high-efficiency industrial power supply.

2.2.3 UCC24612-2

The UCC24612-2 is a multi-mode synchronous rectifier controller for active clamp flyback and LLC applications. Along with its 4-A sink and 1-A source capability, this device has a proportional gate drive, which helps when using this synchronous rectifier in LLC applications where the system can operate far above the resonant frequency. The adaptive off-time feature adds robustness to the synchronous rectifier by preventing false triggering.

2.2.4 CSD19505KCS

The CSD19505KCS is an 80-V NexFET™ power MOSFET, with 2.6-mΩ resistance and 76-nC gate charge. In this reference design, the CSD19505KCS is used as the synchronous field-effect transistor (FET) to lower the losses in the output stage of the LLC converter.

2.3 System Design Theory

This reference design provides a universal AC mains-powered, 500-W nominal output at 24 V and 20 A. This design comprises a front-end AC/DC PFC power stage followed by an isolated DC/DC LLC power stage.

2.3.1 PFC Regulator Stage Design

For high power levels such as 500 W, either the single-phase CCM PFC or interleaved CrCM PFC is the preferred topology for implementing PFC. Interleaved CrCM PFC offers certain advantages at these power levels because it ensures valley switching for the PFC MOSFET and ZCS turnoff diode, which reduces the losses in the PFC stage. Cheaper diodes can be used because the PFC diode does not have a hard turnoff. CrCM PFC requires a smaller PFC inductor. By interleaving two CrCM power stages, the overall input ripple current is also reduced. Alternatively, CCM PFC requires a larger inductor and is not very effective in low-profile designs.

This reference design uses the UCC28064A-based interleaved CrCM PFC. The following subsections detail the design process and component selection.

2.3.1.1 Design Parameters

表 2. Design Parameters for PFC Power Stage Design

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
INPUT					
V_{IN}	Input Voltage	85	230	265	V
f_{LINE}	Input frequency	47		63	Hz
OUTPUT					
V_{OUT}	Output voltage		390		VDC
$P_{OUT(nom)}$	Output power			500	W
	Line Regulation			5%	
	Load Regulation			5%	
PF	Targeted power factor		0.99		
η	Targeted efficiency		98%		
iTHD	Targeted input current THD		5%		

2.3.1.2 Input Current Calculations

The input fuse, bridge rectifier, and input capacitor are selected based on the input current calculations. First, determine the maximum average output current, $I_{OUT(max)}$ as per 式 1:

$$I_{OUT(max)} = \frac{P_{OUT(max)}}{V_{OUT(max)}} = \frac{500}{390} = 1.28 \quad A \tag{1}$$

Calculate the maximum input root mean square (RMS) for the line current, $I_{INrms(max)}$, using the parameters from the 表 2 and the initial assumptions of the efficiency and power factor:

$$I_{IN_{RMS}(max)} = \frac{P_{OUT(max)}}{\eta \times V_{IN(min)} \times pF} = \frac{500}{0.945 \times 85 \times 0.99} = 6.29 \quad A \tag{2}$$

2.3.1.3 Boost Inductor

Calculate the boost inductor using the minimum input voltage and the minimum desired frequency of operation. First calculate the duty cycle, $DUTY_{(max)}$, at the peak of the minimum input voltage:

$$DUTY_{max} = \frac{V_{OUT(nom)} - V_{IN_{RMS}(min)} \times \sqrt{2}}{V_{OUT(nom)}} = \frac{390 - (1.414 \times 85)}{390} = 0.691 \tag{3}$$

式 4 calculates the boost inductor value.

$$L1 = L2 = \frac{\eta \times \left(V_{IN_{RMS}(min)}\right)^2 \times DUTY_{(max)}}{P_{OUT(max)} \times F_{MIN}} \tag{4}$$

The minimum switching frequency of the converter (f_{MIN}) under low line conditions occurs at the peak of low line and is set between 25 kHz and 50 kHz to avoid audible noise. The minimum switching frequency chosen for this design is 40 kHz. Substituting the final values, the boost inductor's inductance is calculated by 式 5

$$L1 = L2 = \frac{0.945 \times 85^2 \times 0.69}{500 \times 40000} = 236 \quad \mu H \tag{5}$$

The actual value of the boost inductor used is 240 µH. Calculate the required saturation current for the boost inductor is using 式 6 for the minimum input voltage and under the assumption that both phases equally share the load.

$$I_{L(max)} = \left(\sqrt{2} \times \frac{P_{OUT(max)}}{\eta \times V_{IN_{RMS}(min)}}\right) = 8.8 \quad A \tag{6}$$

The inductor RMS current can be calculated as per 式 7

$$I_{L_{RMS}} = \frac{I_{L(max)}}{\sqrt{6}} = \frac{8.8 \ A}{\sqrt{6}} = 3.6 \quad A \tag{7}$$

2.3.1.4 Output Capacitor

The output capacitor (C_{OUT}) is selected based on the holdup requirement of 10 ms and an output ripple of 25 Vp-p, as 式 8 and 式 9 show.

$$C_{OUT} = \frac{2 \times P_{OUT(max)} \times t_{hold\_up}}{\eta \times \left(V_{OUT(nom)}^2 - V_{OUT(min)}^2\right)} = \frac{2 \times 500 \times 10 \ ms}{0.945 \times \left(390^2 - 250^2\right)} = 123 \quad \mu F \tag{8}$$

$$C_{OUT} \geq 2 \times P_{OUT(max)} \times \frac{1}{V_{OUT} \times 4 \times \pi \times F_{LINE} \times V_{PFCRipple}} = 2 \times 500 \times \frac{1}{390 \times 4 \times \pi \times 47 \times 25} = 173.7 \quad \mu F \tag{9}$$

In this reference design, a 220-µF PFC output capacitor is used.

2.3.1.5 Current Sense Resistor

The current sense resistor detects the sum of the inductor currents through both phases. The overcurrent protection limit in UCC28064A is 200 mV. The required value of the current sense resistor is calculated for the lowest input voltage and a 25% overload condition. Estimate the peak current first by 式 10 before calculating the current sense resistor:

$$I_{PEAK_{CS}} = \frac{2 \times \sqrt{2} \times P_{OUT(max)} \times 1.25}{\eta \times V_{IN_{RMS}(min)}} = \frac{2 \times \sqrt{2} \times 500 \times 1.2}{0.945 \times 85} = 21 \text{ A} \quad (10)$$

This result gives the value of the current sense resistor as:

$$Rcs = \frac{200 \text{ mV}}{21 \text{ A}} \cong 9 \text{ m}\Omega \quad (11)$$

This design uses two 20-mΩ resistors in parallel.

2.3.1.6 PFC MOSFET

式 12 calculates the RMS current through the PFC MOSFET.

$$IDS_{RMS} = \frac{I_{PEAKcs}}{2} \times \sqrt{\frac{1}{6} - \frac{4\sqrt{2} \times V_{IN_{RMS}(min)}}{9\pi \times V_{OUT_{PFC}}}} = \frac{21}{2} \times \sqrt{\frac{1}{6} - \frac{4\sqrt{2} \times 85}{9\pi \times 390}} = 3.7 \text{ A} \quad (12)$$

Select a MOSFET with a low figure of merit for this application. The key MOSFET specifications that are important for minimizing losses in this design are:

- Low $R_{DS(on)}$, for reducing the conduction losses in the MOSFET
- Low QG, for fast turnoff

2.3.1.7 PFC Diode

式 13 calculates the RMS current through the boost diode.

$$IDS_{RMS} = \frac{\left(\frac{I_{PEAKcs}}{2}\right) \times \sqrt{\left(4\sqrt{2} \times V_{IN_{RMS}(min)}\right)}}{9\pi \times V_{OUT_{PFC}}} = 2.2 \text{ A} \quad (13)$$

2.3.1.8 Brownout Protection Configuration

The brownout voltage in UCC28064A can be set through the potential divider on the VINAC pin. In this reference design, the brownout voltage is set to 70 V with a hysteresis of 12 V. The following equations determine the value of the resistors in the potential divider network. R_A refers to the top three resistors in the potential divider (式 14) and R_B refers to the bottom resistor in the potential divider (式 15).

$$R_A = 12 \times \frac{1.414}{I_{BO_{HYS}}} = \frac{17}{2 \times 10^{-6}} = 8.5 \text{ M}\Omega \quad (14)$$

Three resistors of 2.87 MΩ are connected in series to form RA, with the bottom resistor using 式 15.

$$R_B = \frac{1.4 \times R_A}{70\sqrt{2} - 1.414} = 123.5 \text{ k}\Omega \quad (15)$$

A standard value of 124 kΩ is chosen for R_B.

2.3.1.9 Control Loop Compensation

This design uses a type-2 compensator for the voltage loop compensation. Resistor R42 and capacitors C34 and C36 form the compensator. Start with a value of 7.5 kΩ for R42. Place a zero close to 10 Hz to give a phase boost close to the gain crossover frequency. This zero is formed by R42 and C36.

$$C36 = \frac{1}{2\pi \times 10 \times 7500} = 2.12 \text{ µF} \quad (16)$$

Choose a 2.2-µF capacitor for the C36 capacitor.

Place a pole at a frequency much lower than the lowest switching frequency, around 20 KHz, to attenuate the switching noise. This pole is formed by R42 and C34.

$$C34 = \frac{1}{2\pi \times 20000 \times 7500} = 1.06 \text{ nF} \quad (17)$$

2.3.1.10 Programming VOUT and HVSEN

The Vsense pin sets the output voltage regulation point. To minimize the no-load losses, use high-value resistances to construct this potential divider network. Use three 3.01-MΩ resistors to form the top resistor in the potential divider. Calculate the bottom resistor using 式 18.

$$R_D = V_{REF} \times \frac{R_C}{V_{OUT(nom)} - V_{REF}} = \frac{6 \times 9 \times 10^6}{390 - 6} = 140.63 \quad k\Omega \tag{18}$$

Use a standard value of 142 kΩ for the bottom resistor on the Vsense pin.

This reference design uses the HVSEN pin to set the fail-safe output overvoltage protection (OVP). Three 3.01-MΩ resistors form the top resistor in the potential divider. Calculate the bottom resistor using 式 19.

$$R_F = \frac{4.87 \times R_E}{V_{OUT(pk)} - 4.87} = \frac{4.87 \times 9 \times 10^6}{430 - 4.87} = 103.1 \quad k\Omega \tag{19}$$

A standard 103-kΩ bottom resistor has been used in the design.

2.3.2 LLC Converter Stage Design

Increased demands for high-power-density power supplies have resulted in the increase in switching frequency of the converters designed. While component sizes tend to decrease with an increase in the switching frequency, device switching losses (which are proportional to frequency) have significantly increased contributing to resulting in significant efficiency loss. Resonant converters use soft-switching techniques to alleviate switching loss problems and attain high efficiencies. Further, soft-switching helps attain low losses during light load conditions, very-low device stress, and reduced EMI.

The LLC resonant converter is based on the series resonant converter (SRC). By utilizing the transformer magnetizing inductor, zero-voltage switching can be achieved over a wide range of input voltage and load. As a result of multiple resonances, zero-voltage switching can be maintained even when the switching frequency is higher or lower than the resonant frequency.

In this design, the LLC converter operates at a high nominal switching frequency of around 100 kHz. This allows to minimize the dimension of the LLC transformer to meet the low profile requirements. The converter achieves the best efficiency when operated close to its resonant frequency at a nominal input voltage. As the switching frequency is lowered, the voltage gain is significantly increased. This allows the converter to maintain regulation when the input voltage falls low. These features make the converter ideally suited to operate from the output of a high-voltage boost PFC pre-regulator, allowing it to hold up through brief periods of AC line-voltage dropout.

With its hybrid hysteretic control and ZCS avoidance feature, the UCC256303 LLC controller enables safe operation of the LLC power stage while minimizing the dimension of the output capacitors. In addition, the controller delivers complete system protection functions including overcurrent, undervoltage lockout (UVLO), and overvoltage protection (OVP).

表 3 lists the design parameters for the LLC power stage design.

表 3. Design Parameters for LLC Power Stage Design

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
INPUT					
V_{INDC}	Input voltage	250	390	410	V DC
OUTPUT					
V_{OUT}	Output voltage		24		V
P_{OUT}	Max output power			500	W
f_{sw_nom}	Nominal switching frequency		100		kHz

表 3. Design Parameters for LLC Power Stage Design (continued)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
	Line regulation		1		%
	Load regulation		1		%
η	Targeted efficiency		0.965		

2.3.2.1 Determine LLC Transformer Turns Ratio N

The LLC tank is designed to have a nominal gain, M_g, of 1 at the resonant frequency. Use 式 20 to estimate the required turns ratio.

$$n = M_g \times \frac{\frac{V_{DCIN(nom)}}{2}}{V_{O(nom)} + V_F} \quad ; \quad M_g = 1 \tag{20}$$

where

- M_g is the voltage gain
- $V_{DCIN(nom)}$ is the nominal PFC output
- $V_{O(nom)}$ is the output voltage
- V_F is the voltage drop across the synchronous rectifier

From the specifications, the nominal values for input voltage and output voltage are 390 V and 24 V, respectively. Assuming an average drop of 100 mV on the synchronous rectifier, the turns-ratio can be calculated as:

$$n = 1 \times \left(\frac{390}{24 + 0.1}\right) = 8.07 \tag{21}$$

The transformer turns ratio is set to 8.

2.3.2.2 Determine M_{g_min} and M_{g_max}

Determine M_{g_min} and M_{g_max} using 式 22 and 式 23, respectively.

$$M_{g\_min} = n \times \left(\frac{V_O + V_F}{\frac{V_{DCIN(max)}}{2}}\right) = 8.0 \times \left(\frac{24.1\ V}{\frac{410\ V}{2}}\right) = 0.94 \tag{22}$$

$$M_{g\_max} = n \times \left(\frac{V_{O(nom)} + V_F}{\frac{V_{DCIN(min)}}{2}}\right) = 8.0 \times \left(\frac{24.1\ V}{\frac{250\ V}{2}}\right) = 1.542 \tag{23}$$

The dimensioned M_{g_max} is increased to 1.1 times the required value to have some margin = M_{g_max} = 1.1 × 1.542 ≈ 1.697.

2.3.2.3 Determine Equivalent Load Resistance (Re) of Resonant Network

式 24 calculates the equivalent load resistance at nominal and peak load under nominal output voltage and peak output voltage.

$$R_e = \frac{8 \times n^2}{\pi^2} \times \left(\frac{V_{O(nom)}}{I_{O(nom)}}\right) = \frac{8 \times 8^2}{\pi^2} \times \left(\frac{24}{20}\right) = 62.25\ \Omega \tag{24}$$

2.3.2.4 Select Lm and Lr Ratio (Ln) and Qe

Set the resonance point for the LLC converter close to 100 kHz to minimize the dimension of the LLC transformer set. The operating point of the LLC power stage is close to this frequency during a full load condition. Choose a value of L_r = 27 µH and C_r = 94 nF to calculate the value of the resonant frequency as follows:

$$F_r = \frac{1}{2 \times \pi \times \sqrt{L_r \times C_r}} = 99.9\ \text{kHz} \tag{25}$$

The magnetizing inductance to resonant inductance ratio is chosen as 6.6:1 to develop a sufficient Q while simultaneously minimizing the magnetizing current in the LLC transformer. A PQ 32/30 core has been used to realize the LLC transformer. The required leakage inductance is provided through an additional shim inductor built on a 20/20 PQ core.

2.3.2.5 Determine Primary-Side Currents

Use 式 26 to calculate the primary-side RMS load current (I_{pri}) at a full load condition:

$$I_{pri} = \frac{\pi}{2\sqrt{2}} \times \frac{I_{O(nom)}}{n} = 1.11 \times \frac{20}{8.0} = 2.775 \quad A \tag{26}$$

As calculated in 式 27, the RMS magnetizing current (I_m) at f_{SW_min} = 70 kHz is:

$$I_m = \frac{2\sqrt{2}}{\pi} \times \left(n \times \frac{V_{O(nom)} + V_F}{2 \times \pi \times f_{SW(min)} \times L_M}\right) = \frac{2\sqrt{2}}{\pi} \times \left(\frac{8.0 \times 24}{2 \times \pi \times 70 \text{ kHz} \times 240 \text{ µH}}\right) = 1.64 \quad A \tag{27}$$

式 28 calculates the resonant circuit current (I_r):

$$I_r = \sqrt{I_m^2 + I_{pri}^2} = \sqrt{1.64^2 + 2.775^2} = 3.22 \quad A \tag{28}$$

This value is also equal to the transformer primary winding current at f_{SW_min}.

2.3.2.6 Determine Secondary-Side Currents

The secondary-side RMS currents can be calculated from the average load current. Assuming the LLC power stage is operating close to its second resonant frequency, the RMS current through each rectifier in the secondary-side push-pull output is calculated in 式 29:

$$I_{sec_{RMS}} = I_{sec} \times \frac{\pi}{4} = 15.71 \quad A \tag{29}$$

where:

- I_{sec} is the full-load, secondary-side output current (equal to 20 A)

2.3.2.7 Primary Side MOSFETs

Consider each MOSFET to have an input voltage equal to its maximum applied voltage. A MOSFET with a maximum drain source voltage greater than 500 V is feasible for this design. The turnon losses can be neglected for an LLC power stage working in ZVS. Choose the MOSFET based on the values for $R_{DS(on)}$ and COSS. Optimizing the COSS helps to minimize the dead time required for achieving ZVS, thereby minimizing the duty cycle loss. This reference design uses the STP24N60M2 MOSFET. The adaptive dead-time optimization feature of the UCC256301 helps to maximize the duty cycle, which improves the efficiency.

2.3.2.8 Secondary-Side Synchronous MOSFETs

式 30 calculates the synchronous rectifier maximum voltage rating.

$$V_{DSmax_{sec}} = 1.2 \times 2 \times V_{O(nom)} = 57.6 \quad V \tag{30}$$

The current rating of the MOSFET is determined as I_{sec_Mrms} = 15.7 A.

This reference design uses TI's CSD19505KCS MOSFET with very low $R_{DS(on)}$ (< 3 mΩ) and Q_g (< 80 nC). The very low $R_{DS(on)}$ of the device helps to reduce the overall loss in the synchronous rectifier.

2.3.2.9 Soft Start—UCC256301

The UCC256301 is configured to provide a maximum 400-ms soft-start period. During start-up the soft-start capacitor charges using the internal 25-µA current source. The UCC256301 exits soft start when the closed-loop control takes over or when the voltage on the soft-start capacitor reaches 7 V. Select the value of the soft-start capacitor using 式 31.

$$C_{SS} = C33 = 400 \quad ms \times \frac{25 \text{ µA}}{7 \text{ V}} = 1.5 \quad \mu F \tag{31}$$

2.3.2.10 Current Sense Circuit (ISNS Pin)—UCC256301

The overcurrent limit OCP3 is set to trigger at 1.2 times the peak overload capability of the system.

$$V_{ISNSFullload} = \frac{OCP3}{1.2} = \frac{0.6}{1.2} = 0.5 \quad V \tag{32}$$

The current sense ratio is then calculated as:

$$K_{ISNS} = \frac{V_{ISNSFullload}}{\frac{P_{OUTMax}}{\eta} \times \frac{1}{V_{DCIN(nom)}}} = \frac{0.5}{500 \times \frac{1}{390}} = 0.39 \quad \Omega \tag{33}$$

Select the current sense capacitor C_{ISNS} = C39 = 150 pF. 式 34 calculates the current sense resistor R_{ISNS}.

$$R_{ISNS} = R3 = K_{ISNS} \times \frac{C_R}{C_{ISNS}} = 0.39 \times \frac{94 \times 10^{-9}}{150 \times 10^{-12}} = 244 \quad \Omega \tag{34}$$

Use a standard 240-Ω resistor for R3.

2.3.2.11 Overvoltage Protection (BW Pin)—UCC256301

The BW pin senses the output voltage through the bias winding mounted on the LLC transformer. This pin can be used to provide an additional OVP in the system. In this reference design, the bias winding has 0.67 number of turns as the secondary winding. When the OVP voltage is set to 32 V, the bias winding voltage will be 21.3 V. After implementing this setting, the BW pin potential divider is configured in such a way that it acknowledges the 4 V at the 32-V output.

$R_{BWLOWER}$ = R12 = 10 kΩ. Thus $R_{BWUPPER}$ is calculated as per 式 35:

$$R_{BWUPPER} = R9 = R12 \times \frac{21.3\ V - 4\ V}{4\ V} = 43.25 \quad k\Omega \tag{35}$$

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware

3.1.1 Test Conditions

Input conditions:

- VIN: 85- to 265-V AC
- IIN: Current limit to 8 A

Output Conditions:

- V_{OUT} – 24 V
- I_{OUT} – 0 A to 20 A

3.1.2 Required Equipment

A list of required equipment follows:

- Isolated AC Source
- Single phase power analyzer
- Digital Oscilloscope
- 6½ Digit Multimeter
- Resistive load
- 12-V DC Fan

3.1.3 Procedure

The testing procedure follows:

1. Turn on the 12-V DC fan and set the current to obtain approximately 200 LFM airflow on the board
2. Connect the input terminals (connector J3) of the reference board to the AC power source.
3. Solder output connections on the board, output is marked with 24V and GND, to the resistive load
4. Set a minimum load of approximately 50 mA
5. Gradually increase the input voltage from 0 V to turn on a voltage of 85-V AC. As the voltage across the PFC bulk capacitor crosses 90 V, the LLC section begins working and supplies the auxiliary power to the PFC controller. At this point, the PFC starts and boosts the PFC stage output voltage to 390-V DC.
6. Observe the start-up conditions for smooth switching waveforms.
7. Apply load and perform tests to determine the efficiency, obtain regulation data, and observe steady state operating conditions.

3.2 Testing and Results

3.2.1 Efficiency, Regulation, PF, and iTHD

This section shows the efficiency, power factor, regulation, and iTHD results at 115-V AC and 230-V AC input.

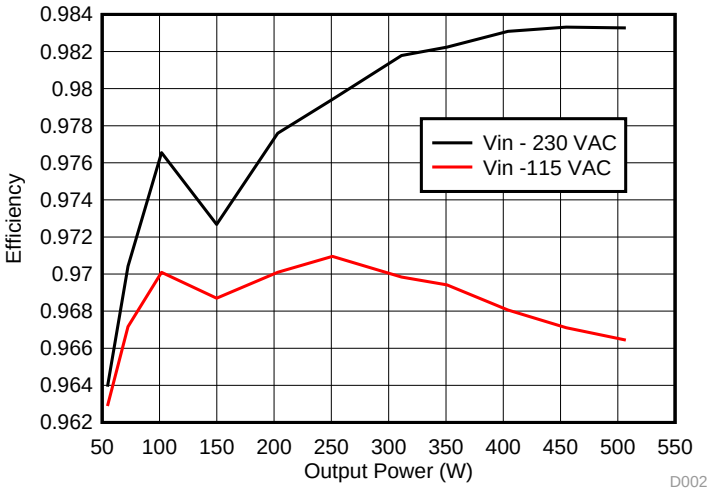

図 2. PFC Stage Efficiency

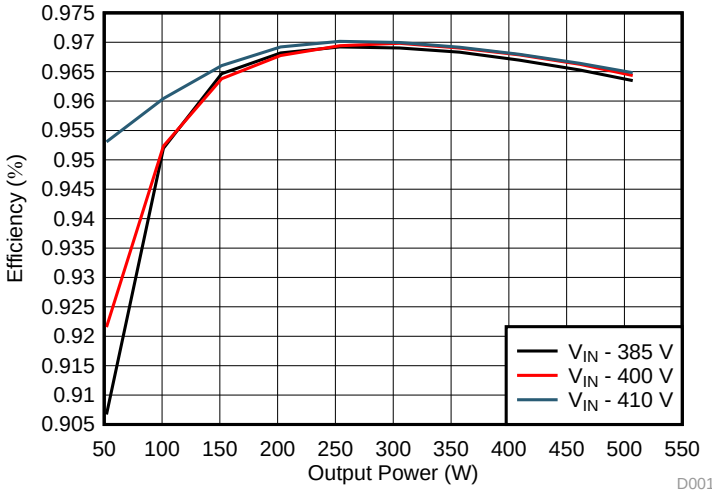

図 3. LLC Stage Efficiency

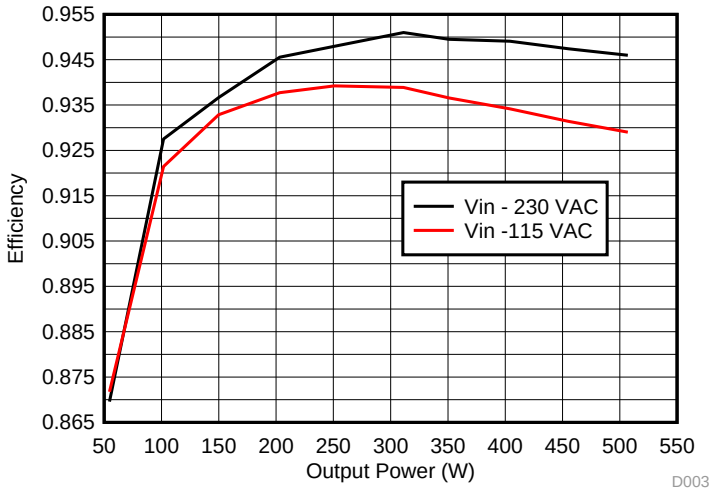

図 4. System Overall Efficiency

図 5. Load Regulation

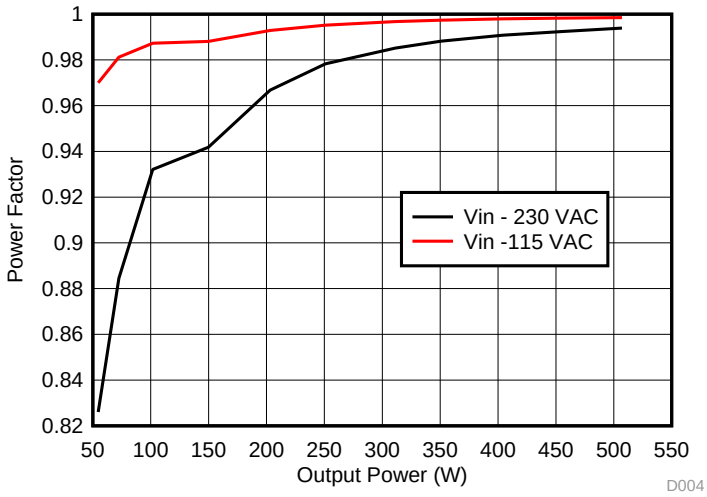

図 6. Power Factor

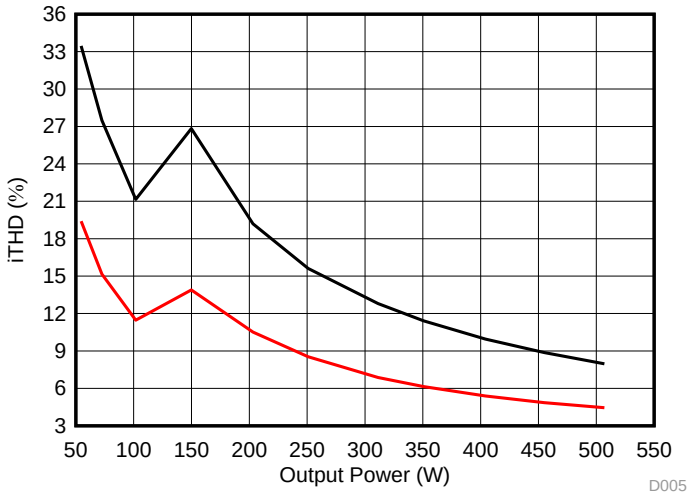

図 7. iTHD Data

3.2.2 Standby Power

The standby power consumption at no load is shown in 表 4.

表 4. Standby Power

VIN AC	Pin
115 V	170 mW
230 V	190 mW

3.2.3 Load Transient Response

図 8 shows the transient response of the system when the 24-V output load varies from 5 A to 20 A at a slew rate of 500 mA/µs.

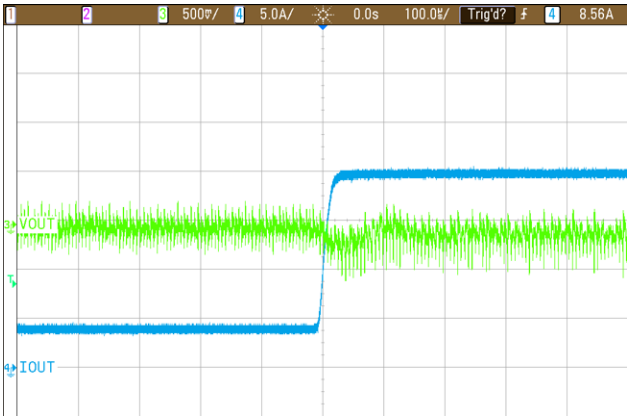

図 8. Transient Response at 24-V Output

3.2.4 PFC MOSFET Switching Waveforms

This section shows the PFC MOSFET turnon and turnoff switching waveforms. 図 9 shows the turn on of PFC MOSFET at 115 V, 図 10 shows the turn off of PFC MOSFET at 115 V, 図 11 shows the turn on of PFC MOSFET at 230 V and 図 12 shows the PFC MOSFET turn off switching waveform at 230 V.

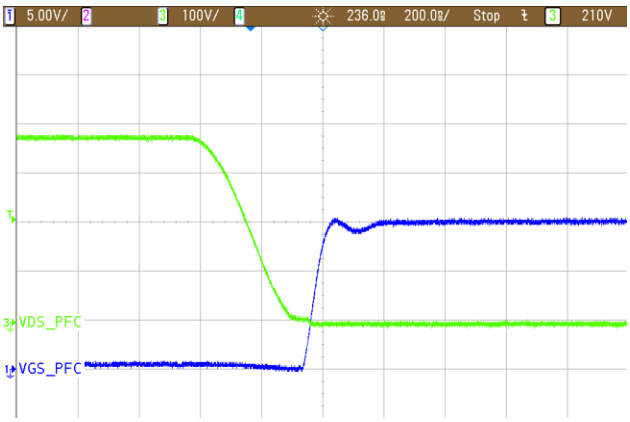

図 9. PFC MOSFET Turnon Waveform at 115 V

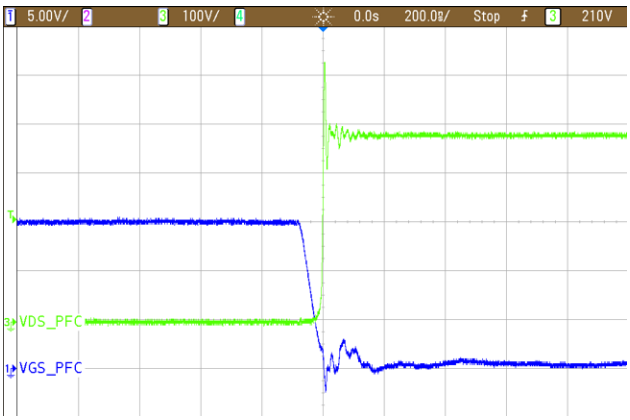

図 10. PFC MOSFET Turnoff Waveform at 115 V

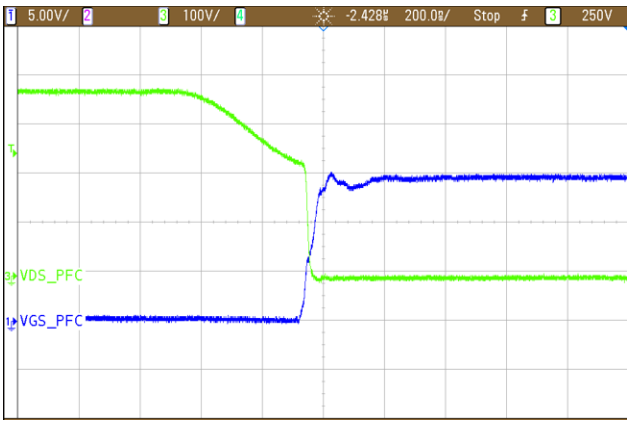

図 11. PFC MOSFET Turnon Waveform at 230 V

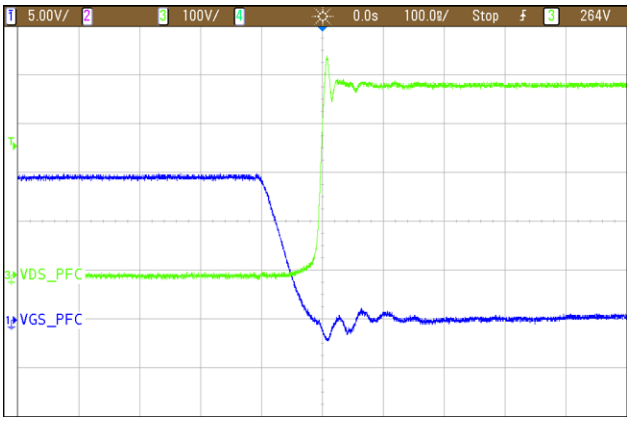

図 12. PFC MOSFET Turnoff Waveform at 230 V

3.2.5 LLC Stage Switching Waveform

図 13 shows the primary-side switching waveform of the LLC stage depicting the tank current and low-side MOSFET switching waveform.

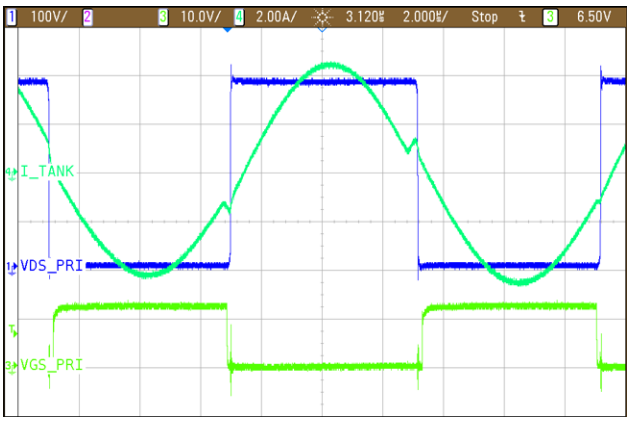

図 13. LLC Stage Primary-Side Tank Current and MOSFET Switching Waveform

図 14 shows the synchronous MOSFET and synchronous drive output waveform.

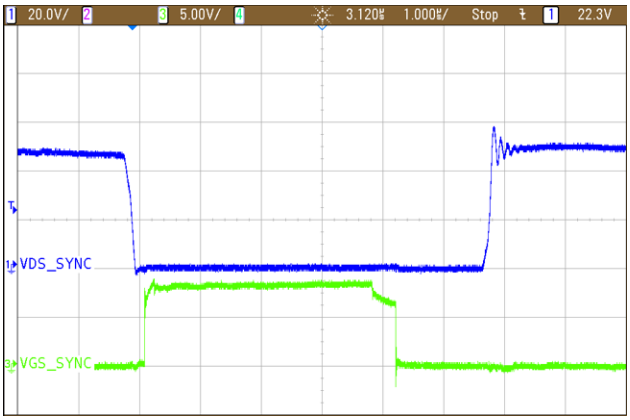

図 14. Synchronous MOSFET V_{DS} and Proportional Gate Drive Signal

3.2.6 Full-Load Thermal Image

図 15 shows the full-load thermal image at 230 VAC input after letting the board run for 20 minutes and with a FAN cooling of 200 LFM.

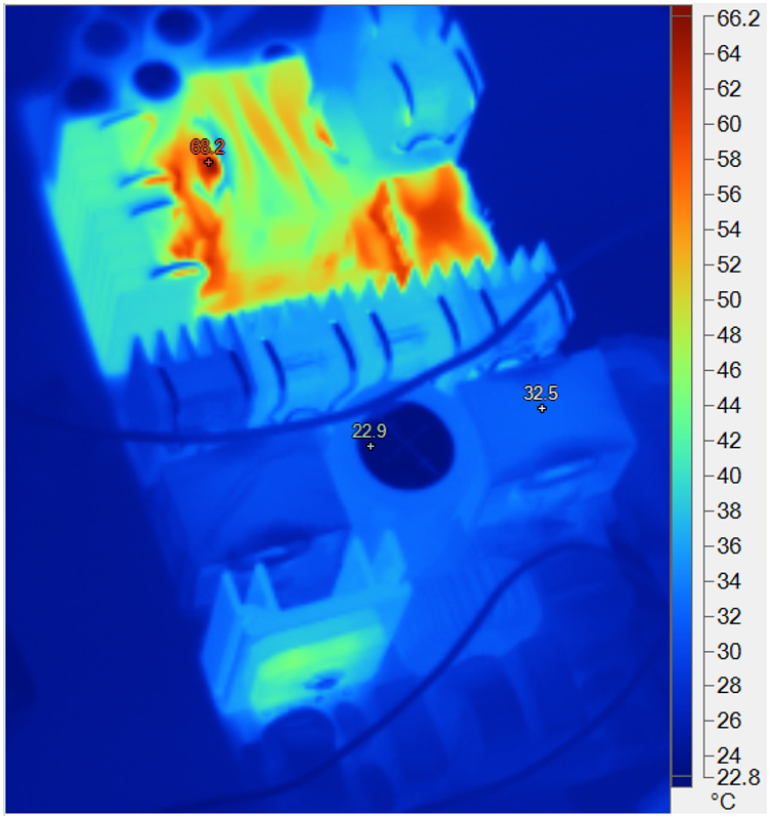

図 15. Thermal Image at Full Load, 230-VAC Input

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010015.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010015.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010015.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010015.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010015.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010015.

5 Software Files

To download the software files, see the design files at TIDA-010015.

6 Related Documentation

1. Texas Instruments, *UCC28064A Natural Interleaving™ Transition-Mode PFC Controller with High Light-Load Efficiency Data Sheet*
2. Texas Instruments, *UCC256301 Hybrid Hysteretic Mode Wide V_{IN} LLC Resonant Controller Enabling Ultra-Low Standby Power Data Sheet*
3. Texas Instruments, *UCC24612 High Frequency Synchronous Rectifier Controller Data Sheet*

6.1 商標

7 About the Author

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改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2018年10月発行のものから更新 **Page**

- アプリケーションのリンクを 変更 1
- 400 mW to 200 mW 変更 2
- nominal value of no load power from 400 mW to 200 mW in *Key System Specifications* table 変更 3
- pin values in *Standby Power* table 変更 18

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