

# BUF634ADRB and BUF634ADDA Evaluation Modules



## ABSTRACT

The BUF634ADRBEVM and BUF634ADDAEVM are evaluation modules (EVMs) for the BUF634A high-speed buffer in the DRB (8-pin SON) and DDA (8-pin SO PowerPAD) packages. Each EVM features two BUF634A devices and are designed to quickly demonstrate the functionality and versatility of the buffer. Optionally, the buffers can be configured as outputs for a dual SOIC amplifier in a composite loop. Each EVM is ready to connect to power, signal sources, and test instruments by using onboard connectors. The default configuration uses split supplies and subminiature version A (SMA) input and output connectors with a 50-Ω output impedance for standard test equipment. The EVMs can be easily configured for other connections and single-supply operation. Dual-channel path configuration is also available for the RCA™ audio input jacks and a 3.5-mm output jack.

Throughout this document, the terms *EVM* and *evaluation module* are synonymous with the BUF634ADRBEVM and BUF634ADDAEVM.

Section 8 lists the related documentation available through the Texas Instruments web site at [www.ti.com](http://www.ti.com).

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### 1 Trademarks

RCA™ is a trademark of Technicolor SA.

All trademarks are the property of their respective owners.

## 2 Overview

This section provides a general description of the BUF634ADRBEVM and BUF634ADDAEVM. [Table 2-1](#) lists the input and output limits for these EVMs in the default configuration. [Table 2-2](#) lists the input and output limits when the BUF634A EVMs are used in a composite loop configuration with the OPA2810 device.

**Table 2-1. EVM Input and Output Limits (Default Configuration)**

PARAMETERS	MIN	TYP	MAX	UNIT
Split-supply voltage range (VS+ – VS–)	±2.25	±15	±18	V
Single-supply voltage range (VS– = ground)	4.5	30	36	V
Supply current, I <sub>S</sub> with BW = VS–		17	24	mA
Input voltage, V <sub>I</sub>		(VS+) - 2 to (VS–) + 2		V
Output drive, I <sub>O</sub> with ±12-V or 24-V supply		±250		mA

**Table 2-2. EVM Input and Output Limits (Dual Composite Loop Configuration Without OPA2810)**

PARAMETERS	MIN	TYP	MAX	UNIT
Split-supply voltage range (VS+ – VS–)	±2.375	±12	±13.5	V
Single-supply voltage range (VS– = ground)	4.75	24	27	V
Supply current, I <sub>S</sub> with BW = V–		24.4	32.2	mA
Input voltage, V <sub>I</sub>		(VS+) + 0.3 to (VS–) – 0.3		V
Output drive, I <sub>O</sub> with ±12-V or 24-V supply		±250		mA

## 3 Power Connections

The BUF634ADRBEVM and BUF634ADDAEVM are equipped with banana jacks to easily connect to power. The positive supply input is labeled V+, the negative supply input is labeled V–, and ground is labeled GND.

### 3.1 Split-Supply Operation

To operate in split supply, apply the positive supply voltage to V+, the negative supply voltage to V–, and the ground reference from supply to GND.

### 3.2 Single-Supply Operation

To operate in single supply, apply jumper V– to GND and apply the positive supply voltage to V+. Inputs and outputs must be biased per data sheet specifications for proper operation.

## 4 Input and Output Connections

The BUF634ADRBEVM and BUF634ADDAEVM are equipped with SMA connectors to easily connect to the benchtop signal generators and analysis equipment. Additionally, the EVM also includes RCA input jacks and a 3.5-mm output jack that can be used with the two BUF634A devices in a differential audio buffer configuration. The connections to the SMA outputs include 50-Ω termination resistors to easily connect to 50-Ω impedance test equipment. The inputs are high impedance, but can be easily terminated to 50 Ω as well by populating resistors R1 and R4. Route the outputs to the test equipment using cables with a 50-Ω characteristic impedance, and connect the inputs to the signal source with as short of cables as possible for best results in the default configuration.

### 4.1 Use With a Dual SOIC Amplifier in a Composite Loop

The BUF634ADRBEVM and BUF634ADDAEVM feature the option to configure the BUF634A devices in two composite amplifier loops using a dual SOIC package amplifier, such as the OPA2810. The BUF634A forms an output driving stage for the chosen input amplifier in the composite loop and forms a differential composite amplifier useful for applications (such as audio amplification) with the dual paths on the EVM. Populate the device U1; resistors R2, R3, R4, and R5; capacitors C2 and C4; and remove resistors R11 and R16 when configuring the EVM to use the composite loop.

## 5 Schematic

Figure 5-1 shows a schematic for the BUF634ADRBEVM.

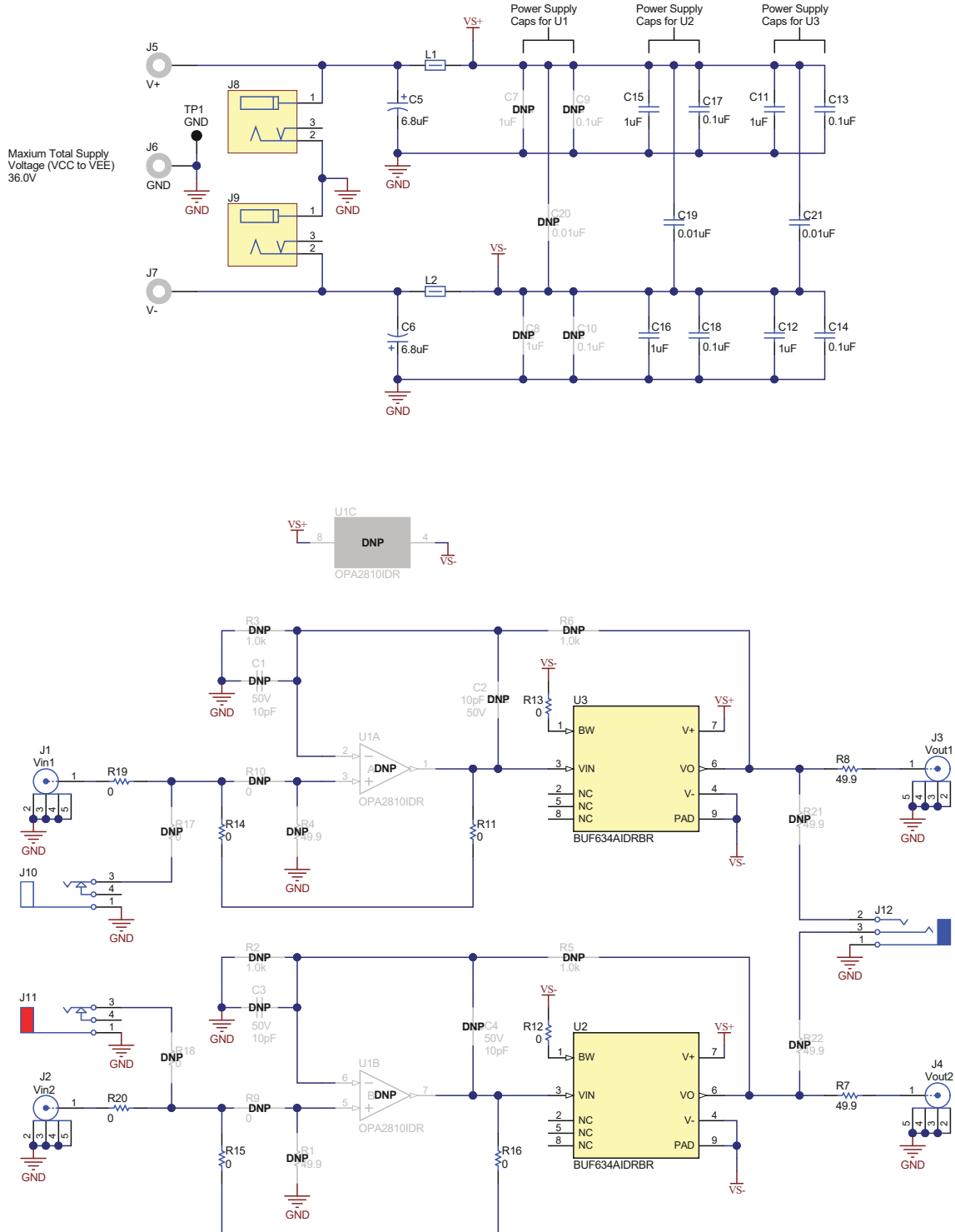


Figure 5-1. BUF634ADRBEVM Schematic

Figure 5-2 shows a schematic for the BUF634ADDAEVM.

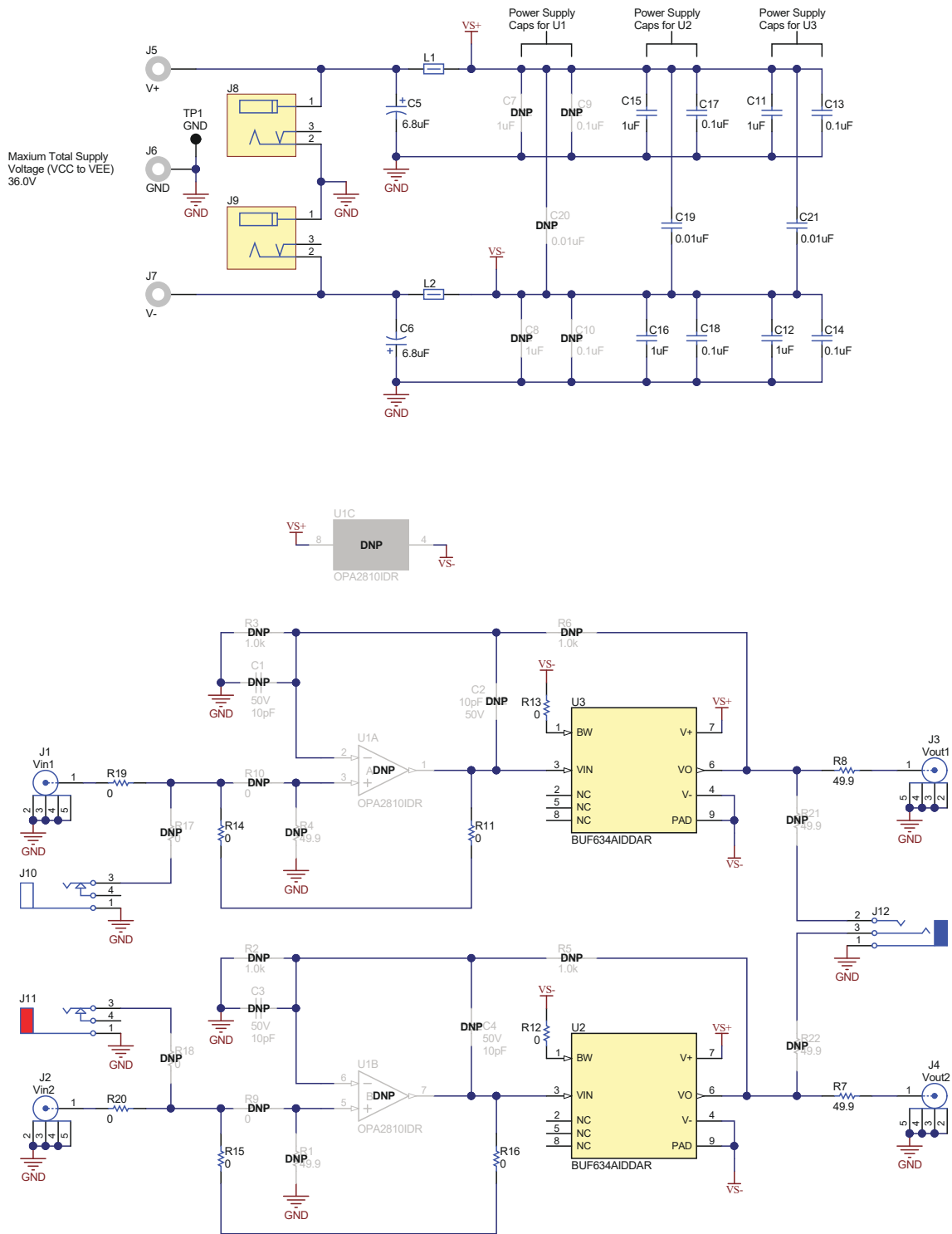


Figure 5-2. BUF634ADDAEVM Schematic

## 6 Layout

Figure 6-1 and Figure 6-2 illustrate the layers for the BUF634ADRBEVM.

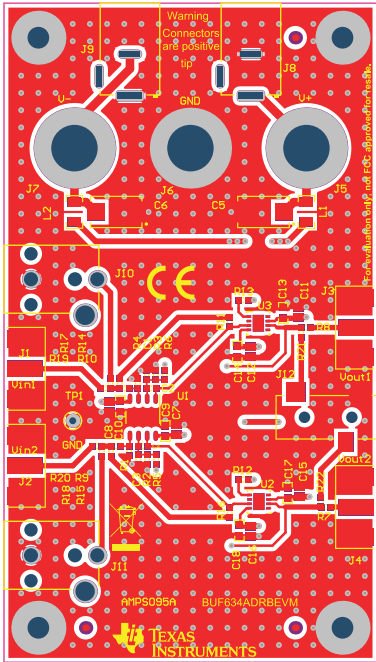


Figure 6-1. BUF634ADRBEVM Top Layer

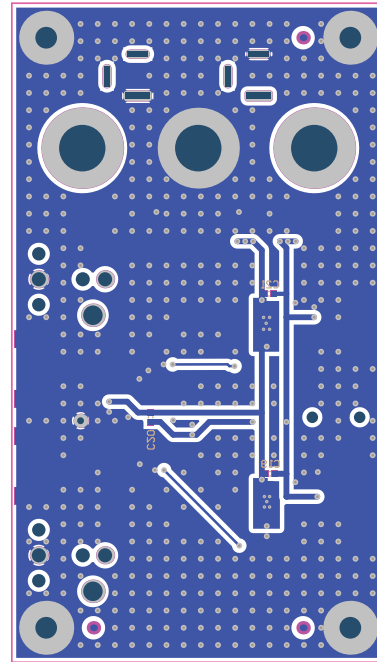


Figure 6-2. BUF634ADDAEVM Bottom Layer

Figure 6-3 through Figure 6-4 illustrate the various layout silk screens for the BUF634ADDAEVM.

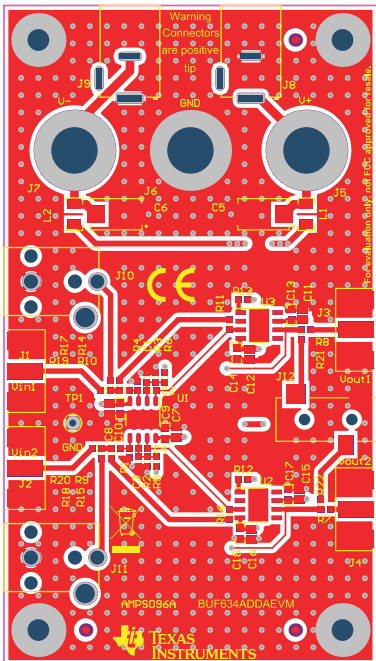


Figure 6-3. BUF634ADRBEVM Top Layer

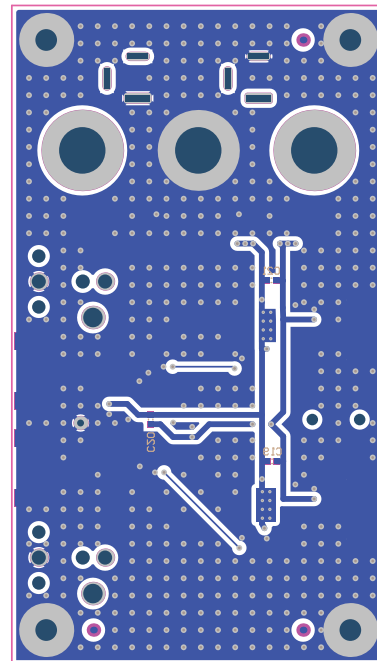


Figure 6-4. BUF634ADDAEVM Bottom Solder

## 7 Bill of Materials

Table 7-1 lists the bill of materials for the BUF634ADRBEVM and BUF634ADDAEVM. Note: the only difference in the BOM between both boards is the BUF634A package that is used.

**Table 7-1. Bill of Materials**

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
C5, C6	2	6.8 $\mu$ F	CAP, TA, 6.8 $\mu$ F, 50 V, $\pm$ 10%, 0.3 $\Omega$ , SMD	7343-31	T495D685K050ATE300	Kemet
C11, C12, C15, C16	4	1 $\mu$ F	CAP, CERM, 1 $\mu$ F, 50 V, $\pm$ 10%, X7R, 0805	0805	08055C105KAT2A	AVX
C13, C14, C17, C18	4	0.1 $\mu$ F	CAP, CERM, 0.1 $\mu$ F, 50 V, $\pm$ 10%, X5R, 0603	0603	C1608X5R1H104K080A A	TDK
C19, C21	2	0.01 $\mu$ F	CAP, CERM, 0.01 $\mu$ F, 100 V, $\pm$ 10%, X7R, 0603	0603	06031C103KAT2A	AVX
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1, J2, J3, J4	4		Connector, End launch SMA, 50 $\Omega$ , SMT	End Launch SMA	142-0701-801	Cinch Connectivity
J5, J6, J7	3		Standard Banana Jack, Uninsulated	Keystone_6095	6095	Keystone
J8, J9	2		Power Jack, 2.1 $\times$ 5.5 mm, R/A, TH	Power Jack, 2.1 $\times$ 5.5 mm, R/A, TH	EJ508A	Memory Protection Devices
J10	1		RCA Jack, White, R/A, TH	PC Mount Phono Jack-White, TH	970	Keystone
J11	1		RCA Jack, Red, R/A, TH	PC Mount Phono Jack-Red, TH	971	Keystone
J12	1		Audio Jack, 3.5 mm, Stereo, R/A, SMT	Audio Jack SMD	SJ-3523-SMT	CUI Inc.
L1, L2	2	80 $\Omega$	Ferrite Bead, 80 $\Omega$ at 100 MHz, 3 A, 1206	1206	HI1206N800R-10	Laird-Signal Integrity Products
R7, R8	2	49.9	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060349R9FKEA	Vishay-Dale
R11, R12, R13, R14, R15, R16, R19, R20	8	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
TP1	1		Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone
U2, U3	2		36-V, 210-MHz, 250-mA Output, High-Speed Buffer, DRB0008F (VSON-8) or DDA0008B (HSOIC- 8)	DRB0008F or DDA0008B	BUF634AIDRBR or BUF634AIDDA	Texas Instruments
C1, C2, C3, C4	0	10 pF	CAP, CERM, 10 pF, 50 V, $\pm$ 1%, C0G/NP0, 0603	0603	C0603C100F5GAC7867	Kemet
C7, C8	0	1 $\mu$ F	CAP, CERM, 1 $\mu$ F, 50 V, $\pm$ 10%, X7R, 0805	0805	08055C105KAT2A	AVX
C9, C10	0	0.1 $\mu$ F	CAP, CERM, 0.1 $\mu$ F, 50 V, $\pm$ 10%, X5R, 0603	0603	C1608X5R1H104K080A A	TDK
C20	0	0.01 $\mu$ F	CAP, CERM, 0.01 $\mu$ F, 100 V, $\pm$ 10%, X7R, 0603	0603	06031C103KAT2A	AVX
R1, R4, R21, R22	0	49.9	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060349R9FKEA	Vishay-Dale
R2, R3, R5, R6	0	1.0 k	RES, 1.0 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K00JNEA	Vishay-Dale

## 8 Related Documentation

- Texas Instruments, [BUF634A 36-V, 210-MHz, 250-mA Output, High-Speed Buffer data sheet](#)
- Texas Instruments, [BUF634 250-mA High-Speed Buffer data sheet](#)
- Texas Instruments, [OPA2810 Dual-Channel, 27-V, Rail-to-Rail Input/Output FET-Input Operational Amplifier data sheet](#)

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