

TI UHF Gen2 Protocol

Reference Guide

TI UHF Gen2 Protocol

Reference Guide

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Preface	7
1 Introduction	9
1.1 General	10
1.2 System Description	10
1.3 Product Description	11
1.4 Functional Description	11
1.5 Memory Organization	12
1.5.1 Reserved Memory	12
1.5.2 Electronic Product Code™ (EPC) Memory	13
1.5.3 TID Memory	13
1.5.4 User Memory	13
2 IC Commands	15
2.1 Command Set	16
2.1.1 Select Command	16
2.1.2 Query Command	17
2.1.3 QueryAdjust Command	18
2.1.4 QueryRep Command	18
2.1.5 ACK Command	18
2.1.6 NAK Command	19
2.1.7 Req_RN Command	20
2.1.8 Read Command	21
2.1.9 Write Command	21
2.1.10 KILL Command	22
2.1.11 Lock Command	23
2.1.12 Access Command	25
2.1.13 BlockWrite Command	26
2.1.14 BlockErase Command	27
3 Regulatory, Safety, and Warranty Notices	29
3.1 Regulatory and Safety Notices	30
3.2 Warranty and Liability	30
3.3 Hazards From Electrostatic Discharge (ESD)	30
A Terms and Abbreviations	31

List of Figures

1-1	System Overview	10
1-2	IC States	11
1-3	The Memory Structure	12
1-4	Default EPC Data	13
2-1	Select Command	17
2-2	Query Command	17
2-3	QueryAdjust Command	18
2-4	QueryRep Command	18
2-5	ACK Command	18
2-6	ACK Command: Nontruncated Response	19
2-7	ACK Command: Truncated Response	19
2-8	NAK Command	19
2-9	Req_RN Command	20
2-10	Req_RN Response	20
2-11	Read Command	21
2-12	Read Response	21
2-13	Write Command	22
2-14	Write Response	22
2-15	KILL 1 Command	22
2-16	KILL 1 Response	23
2-17	KILL 2 Command	23
2-18	KILL 2 Response	23
2-19	Lock Command	25
2-20	Lock Response	25
2-21	Access 1 Command	25
2-22	Access 1 Response	26
2-23	Access 2 Command	26
2-24	Access 2 Response	26
2-25	BlockWrite Command	27
2-26	BlockWrite Response	27
2-27	BlockErase Command	27
2-28	BlockErase Response	28

List of Tables

2-1	Command Set	16
2-2	Lock Command Payload	24
2-3	Lock Command Mask Bits	24
2-4	Lock Command Action Bits	24
2-5	Lock Command Action Bits Table.....	24

Read This First

This is the first edition of the Texas Instruments (TI) *UHF Gen2 Protocol Reference Guide*.

This reference guide contains a description of the IC, its functionality, command set, and operations.

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About This Guide

This reference guide (11-09-21-700) is written for the use by TI partners who are engineers experienced with radio frequency identification devices (RFIDs).

Regulatory and safety notes that need to be followed are given in Chapter 3.

Conventions

WARNING

A warning is used where care must be taken or a certain procedure must be followed, in order to prevent injury or harm to your health.

CAUTION

This indicates information on conditions, which must be met, or a procedure, which must be followed, which if not heeded could cause permanent damage to the system.

Note: Indicates conditions, which must be met, or procedures, which must be followed, to ensure proper functioning of any hardware or software.

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Introduction

This chapter describes the TI Gen2 IC.

Topic	Page
1.1 General	10
1.2 System Description	10
1.3 Product Description	11
1.4 Functional Description.....	11
1.5 Memory Organization	12

1.1 General

Large retailers, such as Wal-Mart™ and Target™ in the USA and Metro™ in the European Union (EU), have issued mandates to their suppliers to ship cases and pallets of goods/products with radio-frequency identification (RFid) smart labels attached. TI's Generation 2 (Gen2) IC is intended to be used primarily in case- and pallet-level retail supply-chain applications, and is based on the EPCglobal™ Gen2 Specification Version 1.0.9 approved in December 2004.

TI's UHF Gen2 IC operates with extremely low power and yet provides long read and write ranges, fast data transfer, and high smart-label throughput, which are all crucial for the following applications:

- Express parcel delivery
- Airline baggage handling
- Distribution logistics and supply-chain management
- Building access badges
- Asset tagging

This low-power passive IC is designed to operate on the energy extracted from the radio frequency (RF) signals transmitted from the reader (interrogator) via its antenna. The IC does not require a battery to operate. The IC returns data to the reader using modulated backscatter.

1.2 System Description

To form a functional transponder, the IC (sometimes called a die) requires bonding to an antenna. When the parameters of this antenna match the characteristics of the IC, the antenna resonates at the required frequency and is capable of receiving power and instructions and returning data.

For operation, a reader with antenna is required to send a command to the transponder and to receive its response (see [Figure 1-1](#)). The inlay does not transmit data until the reader sends a valid request (reader talks first principle).

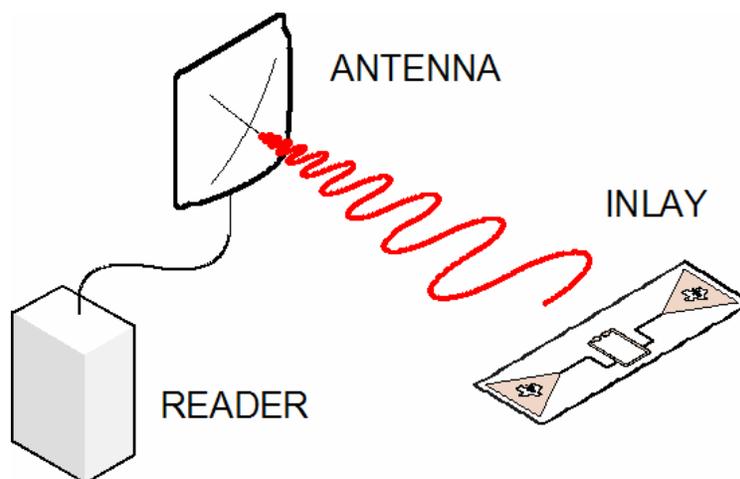


Figure 1-1. System Overview

1.3 Product Description

The IC has been manufactured to fully meet the EPCglobal Gen2 specification and can be used to create a functional transponder in three main ways:

- Forming an inlay
The TI Gen2 IC can be bonded to an antenna, printed on a plastic or paper substrate, or etched from copper or aluminum. This creates an 'inlay' that can then be converted into a 'wet inlay' having a peel-off adhesive layer, or integrated directly into a smart label. Currently, the majority of the RFID applications use inlays to make smart labels for use on cases and pallets.
- Direct attach to label
The TI Gen2 IC can be mounted directly on an antenna that is part of a printed label substrate, to construct a smart label. Currently, a number of manufacturers are exploring this approach.
- Attach to FR4
The TI Gen2 IC can also be mounted on FR4 antennas or antennas designed on printed circuit boards.

1.4 Functional Description

The IC is composed of a number of building blocks that include the analog front end (AFE), which converts RF to digital, digital logic, and memory.

The digital logic includes a state machine, where groups of commands become available once the chip has transitioned to the correct state. This manual describes the functional operation of the state machine.

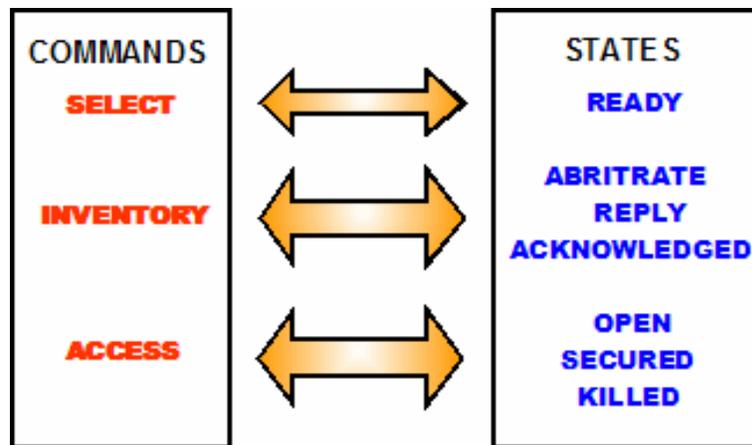


Figure 1-2. IC States

As soon as the chip enters the RF field, it changes to the **Ready** state and accepts **Select** commands. **Select** commands are sent to all ICs to inform each one if it is to take part in the **Inventory** process that is to follow. Multiple **Select** commands can be used to precisely define which ICs are to respond. All exchanges between readers and ICs start with one or more **Select** commands. ICs do not respond to the **Select** command.

Now, the **Inventory** group of commands can be used to initiate the singulation process, where each individual IC is identified and processed. Each **Inventory** round starts with a **Query** command being broadcast – this command passes a Q-value (0 to 15) from which each IC generates a slot counter number in the range (0, 2Q – 1). Most readers dynamically adjust the Q-value depending on the number of ICs in the field, thereby increasing the potential reading rate.

If an IC generates a slot counter value of zero, it is allowed to reply by sending a 16-bit random number and at the same time transitioning to the **Reply** state. The other ICs change state to **Arbitrate** and wait for further commands. If the ICs response is successfully received, the reader replies by sending an **ACK** command, together with the same 16-bit random number. This response now allows the IC to send back its Electronic Product Code™ (EPC) data and change state to **Acknowledged**.

It is at this point that the reader is able to transition the IC to the **Open** (or **Secured**) state allowing operations such as Read, Write, Lock, and KILL (which are described in the following sections), but normally this exchange would terminate when the reader sends a **QueryAdjust** command and the IC switches state back to the **Ready** state and changes its inventoried flag to show it has been singulated. The **QueryAdjust** command also affects the other ICs, causing them to decrement their slot counters, and any IC whose counter is now zero is allowed to reply – so in this way, with successive **QueryAdjust** or **QueryRep** commands, all ICs will be found.

If two ICs reply at the same time, unless the reader is able to identify each one and send an **ACK** and the correct 16-bit random number, each one will time out, regenerate a slot counter value, and return to **Arbitrate**.

If further actions need to be performed on an IC, once the IC has returned its EPC number and is in the **Acknowledged** state, the reader sends a request random number (**Req_RN**) command. The IC replies with a new 16-bit random number that is called the Handle and changes its state to **Open**. The Handle then becomes the token for further commands, such as **Reading, Writing or Killing**. If the **Lock** command is required and the ACCESS password is non-zero, the **Access** command (complete with ACCESS password) must be sent, to cause the IC to change to the **Secured** state. Once in **Secured** state, all commands are available.

1.5 Memory Organization

The memory structure conforms to the EPCglobal UHF Gen2 Specification Version 1.0.9. During manufacturing, TI probes each chip, and wafer lot information is programmed into the EPC field. Later, this information is overwritten when the IC is put into service but, in the meantime, it serves as a unique identifier of each chip.

Data Bank	Address	Default IC Data _{hex}	Description
Reserved (Bank 00 _{bin})	00~1F _{hex}	00000000	KILL Password ACCESS Password
	20~3F _{hex}	00000000	
EPC (Bank 01 _{bin})	00~1F _{hex}	CRC 2800	CRC-16 / Protocol Bits } Wafer (EPC) Data
	20~3F _{hex}	01234567	
	40~5F _{hex}	00240154	
	60~7F _{hex}	30020000	
TID (Bank 10 _{bin})	00~1F _{hex}	E2002000	TID Data

Figure 1-3. The Memory Structure

1.5.1 Reserved Memory

This data is Bank 00_{binary} and contains the KILL password in locations 00 to 1F_{hex} and the ACCESS password in locations 20 to 3F_{hex}. These locations are shipped full of zeroes and unlocked. The passwords are only valid when programmed with non-zero values and (optionally) locked. When the passwords are locked, they become unreadable and unwriteable. If the ACCESS password is zero, the IC automatically transitions to the **Secured** state rather than the normal **Open** state.

1.5.2 Electronic Product Code™ (EPC) Memory

This data is Bank 01_{binary} and contains a 16-bit CRC that is calculated by the chip on the rest of the data in the EPC memory – 16 bits that are the Protocol Control bits and 96 bits that contain the EPC number.

TI programs unique wafer data, similar to the following, into the EPC field:

EPC (Bank 01 _{bin})	00~0F _{hex}	CRC	CRC-16
	10~1F _{hex}	2800	Protocol Bits
	20~2F _{hex}	0123	} Wafer Lot (01234567)
	30~3F _{hex}	4567	
	40~4F _{hex}	0024	Wafer # (0024)
	50~5F _{hex}	0154	IC X-coordinate (0154)
	60~6F _{hex}	3002	IC Y-coordinate (3002)
	70~7F _{hex}	0000	Not Used

Figure 1-4. Default EPC Data

1.5.3 TID Memory

This data is Bank 10_{binary} and contains manufacture information. E2 is prescribed in the EPC Gen2 specification as a class identifier for EPCglobal; 002 identifies the manufacturer as Texas Instruments and 000 is the IC revision number. TID memory is permanently locked.

1.5.4 User Memory

There is no user memory.

IC Commands

The T1 Gen2 IC implements all mandatory and optional commands as defined in the EPCglobal Gen2 Specification Version 1.0.9.

Topic	Page
2.1 Command Set	16

2.1 Command Set

2.1.1 Select Command

Table 2-1. Command Set

COMMAND	CODE	GROUP	MANDATORY
Select	1011	SELECT	Yes
ACK	01	INVENTORY	Yes
NAK	11000000	INVENTORY	Yes
Query	1000	INVENTORY	Yes
QueryAdjust	1001	INVENTORY	Yes
QueryRep	00	INVENTORY	Yes
Req_RN	11000001	INVENTORY	Yes
Read	11000010	ACCESS	Yes
Write	11000011	ACCESS	Yes
Kill	11000100	ACCESS	Yes
Lock	11000101	ACCESS	Yes
Access	11000110	ACCESS	No
BlockWrite	11000111	ACCESS	No
BlockErase	11001000	ACCESS	No

The **Select** command is the first message that is sent to the IC. It contains user-defined criteria to allow the precise selection of groups of ICs. It also can set or reset the IC SL flag or change the Inventoried flag.

The following parameters are sent:

- Target: Instructs the IC to select one of four sessions and either the SL flag or the Inventoried flag associated with that session
- Action: How to set the selected flag
- MemBank: Selects a memory bank (EPC or TID)
- Pointer: Where to look in that memory bank
- Length: How many bits (0 to 255) from the memory bank
- Mask: Data string (“Length” bits long) that are compared with the data selected in the memory bank
- Truncate: If a **Query** command specifies Sel=10 or Sel=11, the response is truncated to only the EPC data after the mask and not the complete 96 bits.
- CRC-16: Checksum calculated on command string

For a more comprehensive description of this command, please consult the EPCglobal Gen2 specification.

Example:

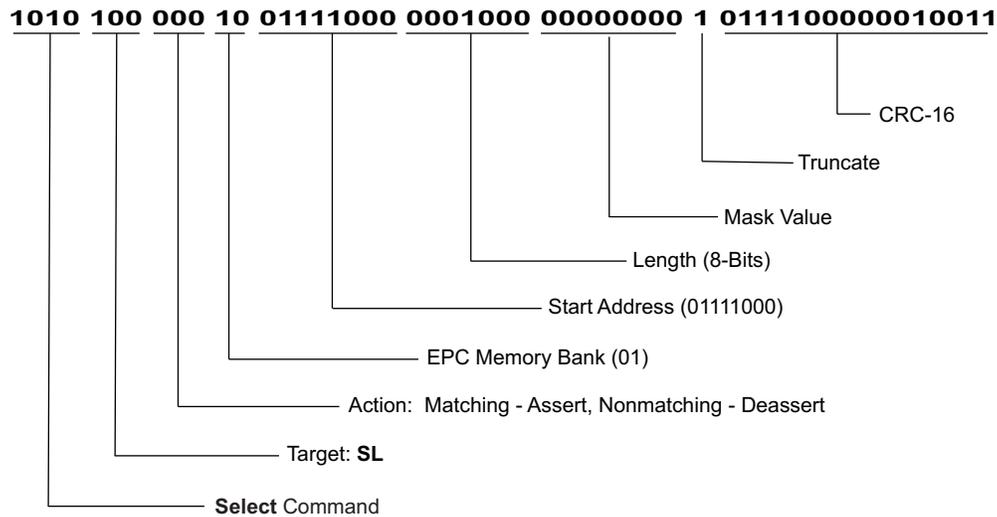


Figure 2-1. Select Command

There is no response to a **Select** command.

2.1.2 Query Command

The mandatory **Query** command initiates the **Inventory** process where individual ICs are identified. It takes the following parameters:

- DR (divide ratio): This is where the IC to reader link frequency is defined.
- M (cycles per second): Sets the IC to reader data rate and modulation format
- TRext: Switches the preamble pilot tone ON/OFF
- Sel: Chooses which ICs respond (all, SL, or ≈SL)
- Session: Selects a session (S0, S1, S2, or S3)
- Target: Selects between A and B Inventoried flags
- Q: Sets the number of slots for the Inventory round
- CRC-5: 5-bit checksum calculated on command string

Example:

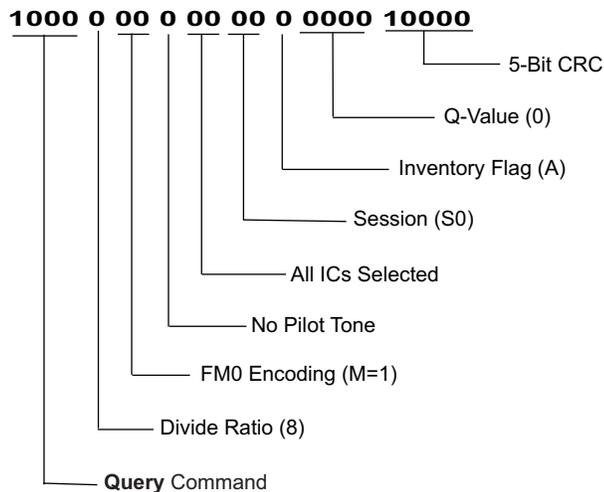


Figure 2-2. Query Command

If an IC slot counter is zero, the response is a 16-bit random number similar to the following:

0100111111001000

2.1.3 QueryAdjust Command

The mandatory **QueryAdjust** command instructs the IC to increment or decrement its slot counter value. It takes the following parameters:

- Session: By sending the session number (S0, S1, S2, or S3), it confirms to the IC that it is responding to the correct reader.
- UpDn: Instructs the IC to count up or down

Example:

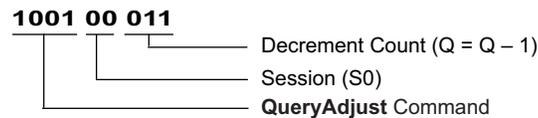


Figure 2-3. QueryAdjust Command

If an IC slot counter value is zero as the result of the decrement, the response is a 16-bit random number similar to:

0000111111001000

2.1.4 QueryRep Command

The **QueryRep** command instructs ICs to decrement their slot counters and, if the resulting value is zero, backscatter a 16-bit random number to the reader.

There is only one parameter:

- Session: Confirms the session for this inventory round

Example:



Figure 2-4. QueryRep Command

If an IC slot counter value is zero as the result of the decrement, the response is a 16-bit random number similar to:

0111111111001000

2.1.5 ACK Command

The mandatory **ACK** command is used to acknowledge the 16-bit random number response from a singulated IC.

Example:

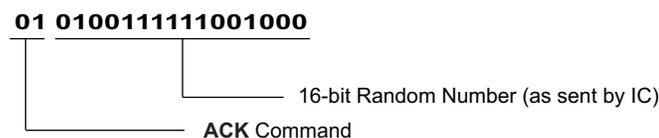


Figure 2-5. ACK Command

2.1.7 Req_RN Command

The mandatory **Req_RN** command instructs the IC to generate and return a new 16-bit random number. The reader request and IC response depends on the state:

- **Acknowledged** state: The reader must include the last 16-bit random number with the request. In return, the IC sends a new 16-bit CRC called the Handle that will be the identifier between the IC and the reader for future commands. At the same time, the IC changes to the **Open** or **Secured** state, depending on the ACCESS password.
 - ACCESS password = 0: IC changes to **Secured** state
 - ACCESS password <> 0: IC changes to **Open** state
 - **Open** or **Secured** state: The reader must send the Handle with the request. The state will remain as set.

Example:



Figure 2-9. Req_RN Command

The response to the command is similar to:

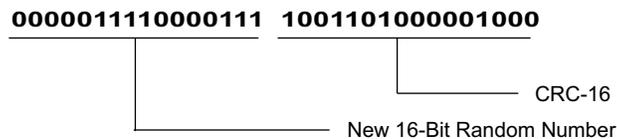


Figure 2-10. Req_RN Response

2.1.8 Read Command

The mandatory **Read** command allows reading of part or all of the IC memory. Data is read in multiples of 16-bit blocks. The command takes the following parameters:

- MemBank: Specifies which of the three memory areas (Reserved, EPC, or TID) to read
- WordPtr: Specifies the start word address, e.g., WordPtr = 00hex specifies the first word in the memory bank
- WordCount: Specifies the number of 16-bit words to be read, starting at WordPtr
- Handle: Identifier used between IC and reader
- CRC-16: This checksum is calculated from the first command bit to the last handle bit.

Example:

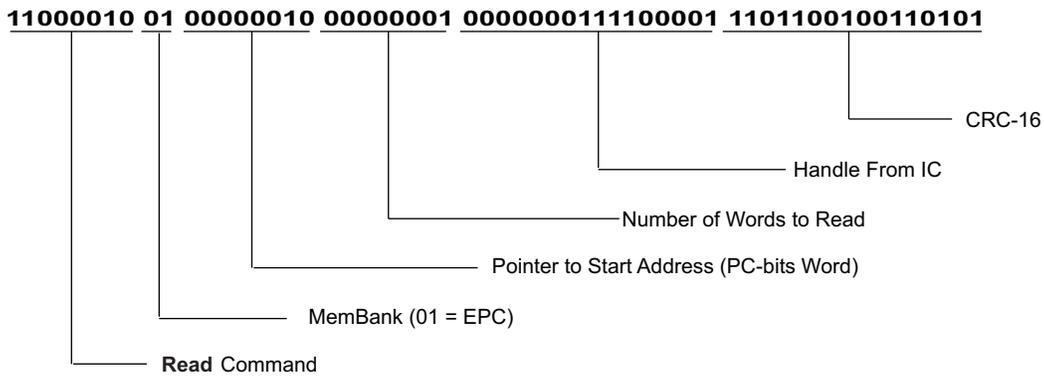


Figure 2-11. Read Command

The response to a **Read** command is similar to:

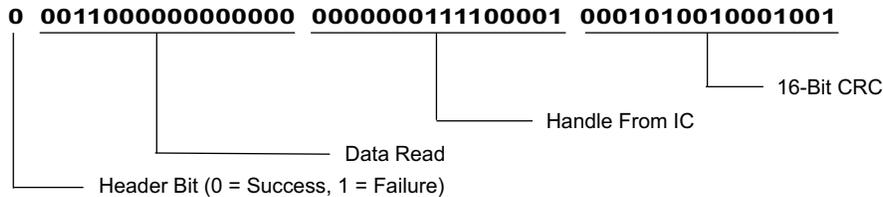


Figure 2-12. Read Response

2.1.9 Write Command

The mandatory **Write** command allows a word of data to be written to any of the IC memory locations. Before a **Write** command can be sent, a new RN16 must be requested from the IC. The data is link cover coded by exclusive ORing the data with the RN16. The command takes the following parameters:

- MemBank: Specifies which memory bank to write
- WordPtr: Start address for the data to be written
- Data: 16 bits to be written (XORed with RN16)
- Handle: Identifier used between IC and reader
- CRC-16: 16-bit checksum calculated on the command string

Example:

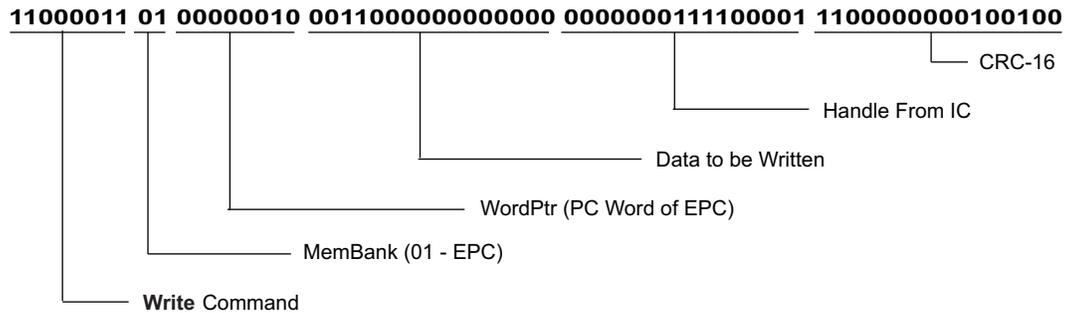


Figure 2-13. Write Command

The response to a **Write** command is similar to:

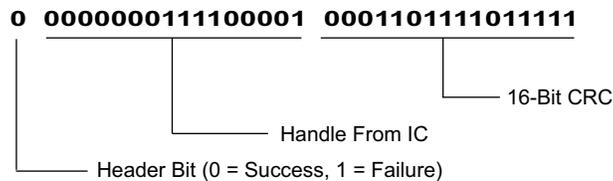


Figure 2-14. Write Response

2.1.10 KILL Command

The mandatory **KILL** command permanently disables the IC. This is a multistep command:

- Request a new 16-bit random number (RN16) from the IC.
- The 16 most significant bits (MSBs) of the KILL password are XORed with the RN16 (link cover coding) and sent to the IC.
- Request a new 16-bit random number (RN16) from the IC.
- The 16 least significant bits (LSBs) of the KILL password are XORed with new RN16 and sent to the IC.

For the **KILL** command to be accepted by the IC, the password must be written with a nonzero number and the state must be **Open** or **Secured**.

2.1.10.1 KILL 1 (Send 16 MSBs of KILL Password)

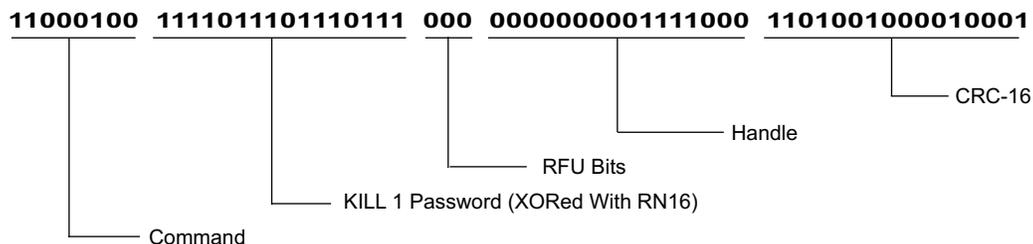


Figure 2-15. KILL 1 Command

2.1.10.2 KILL 1 Response

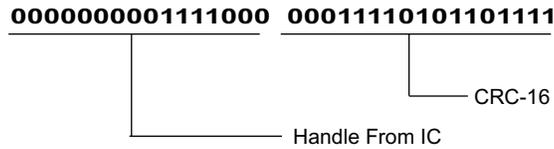


Figure 2-16. KILL 1 Response

2.1.10.3 Kill 2 (Send 16 LSBs of KILL Password)

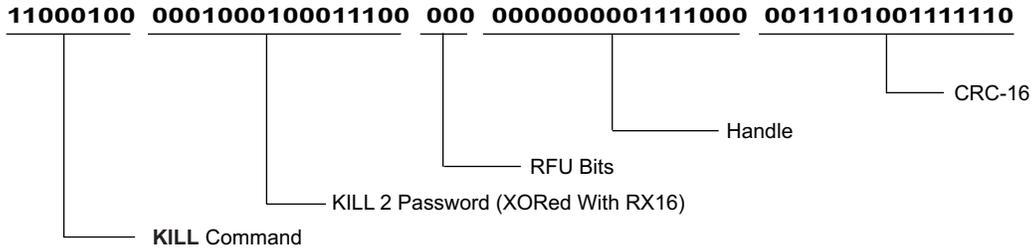


Figure 2-17. KILL 2 Command

2.1.10.4 KILL 2 Response

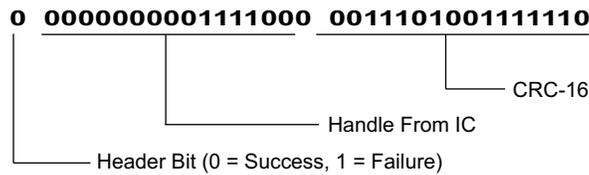


Figure 2-18. KILL 2 Response

After the second successful response, the IC has transitioned to the **Killed** state and the IC will not reply again.

2.1.11 Lock Command

The mandatory **Lock** command is used to:

- Lock individual passwords – preventing or allowing subsequent reads and/or writes of that password
- Lock individual memory banks – preventing or allowing subsequent writes to that memory bank
- Permalock – make the lock status permanently unchangeable for a password or memory bank

For the **Lock** command to be accepted, the IC must be in the **Secured** state. If the ACCESS password is set to zero, the IC automatically changes to this state when a **Req_RN** command is sent. If the ACCESS password is nonzero, the IC has to be forced into the **Secured** state by issuing an **Access** command with the ACCESS password. The **Lock** command takes the following parameters:

- Payload: 20-bit mask that indicates memory locations and the actions to be performed at those locations
- Handle: 16-bit random number used for mutual identification
- CRC-16: Checksum on the preceding data

Command Set

The 20-bit **Lock** command payload comprises Mask and Action fields:

Table 2-2. Lock Command Payload

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
KILL Mask		ACCESS Mask		EPC Mask		TID Mask		USER Mask		KILL Action		ACCESS Action		EPC Action		TID Action		USER Action	

The first ten payload bits are Mask bits and defined as:

- Mask = 0: Ignore this action, keep present settings.
- Mask = 1: Implement the associated Action field.

Table 2-3. Lock Command Mask Bits

KILL Mask		ACCESS Mask		EPC Mask		TID Mask		USER Mask	
0	1	2	3	4	5	6	7	8	9
Skip/write	Skip/write	Skip/write	Skip/write	Skip/write	Skip/write	Skip/write	Skip/write	N/A	N/A

The second ten payload bits are Action bits and are defined as:

- Action = 0: Deassert lock for the associated location.
- Action = 1: Assert lock or perma-lock for the associated location.

Table 2-4. Lock Command Action Bits

KILL Action		ACCESS Action		EPC Action		TID Action		USER Action	
0	1	2	3	4	5	6	7	8	9
Pwd read/write	Perma lock	Pwd read/write	Perma lock	Pwd write	Perma lock	Pwd write	Perma lock	N/A	N/A

The combinations of Action bits are shown in [Table 2-5](#).

Table 2-5. Lock Command Action Bits Table

Pwd Write	Perma Lock	DESCRIPTION
0	0	Associated memory bank is writeable from either Open or Secured state.
0	1	Associated memory bank is permanently writeable from either Open or Secured state and can never be locked.
1	0	Associated memory bank is writeable from the Secured state, but not from the Open state.
1	1	Associated memory bank is not writeable in any state.
Pwd Read/Write	Perma Lock	
0	0	Associated password is readable and writeable from either Open or Secured state.
0	1	Associated password is permanently readable and writeable from either Open or Secured state.
1	0	Associated password is only readable and writeable from the Secured state.
1	1	Associated password is not readable or writeable in any state.

Example:

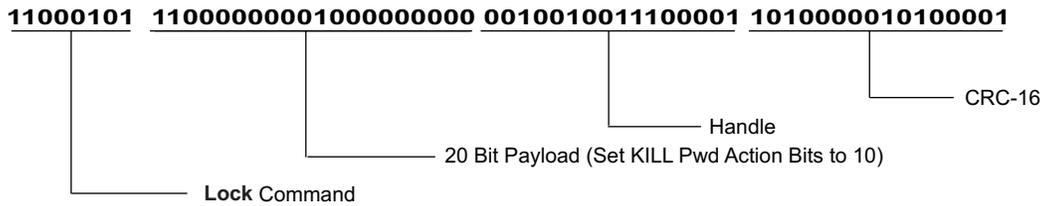


Figure 2-19. Lock Command

The response from a **Lock** command is similar to:

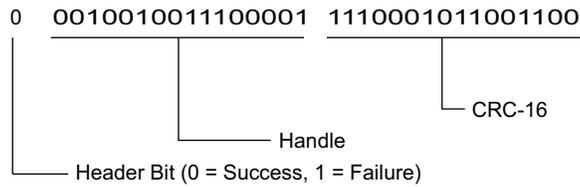


Figure 2-20. Lock Response

2.1.12 Access Command

The optional **Access** command is required when the ACCESS password is set (nonzero) and the IC has to be put into the **Secured** state, to allow the use of the **Lock** command. This is a multipart command requiring separate commands for each 16 bits for the 32-bit ACCESS password:

- Request a new 16-bit random number (RN16) from the IC.
- The 16 MSBs of the password are XORed with the RN16 (link cover coding) and sent to the IC.
- Request a new 16-bit random number (RN16) from the IC.
- The 16 LSBs of the password are XORed with the new RN16 and sent to the IC.

For the **Access** command to be accepted by the IC, the password must be written with a nonzero number.

2.1.12.1 Access 1 (Send 16 MSBs of ACCESS Password)

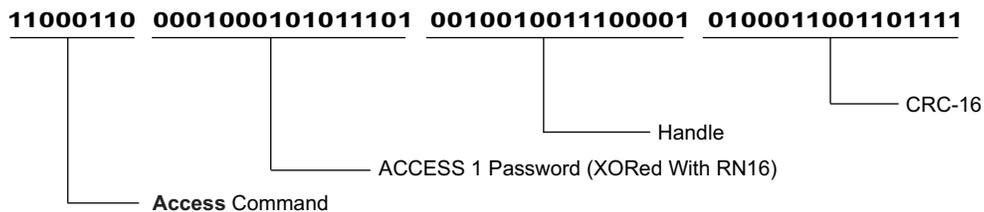


Figure 2-21. Access 1 Command

The response to the **Access** command is similar to:

2.1.12.2 Access 1 Response

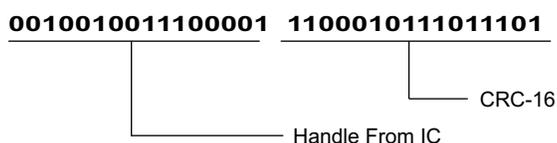


Figure 2-22. Access 1 Response

2.1.12.3 Access 2 (Send 16 LSBs of ACCESS Password)

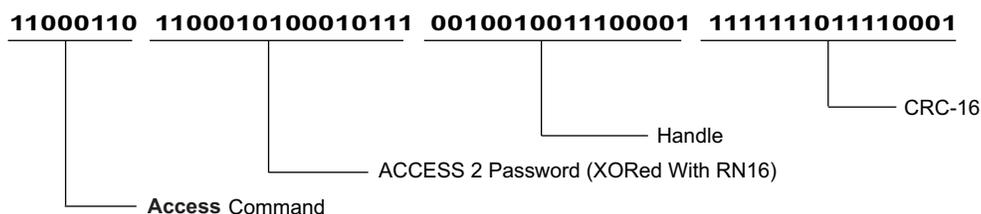


Figure 2-23. Access 2 Command

2.1.12.4 Access 2 Response

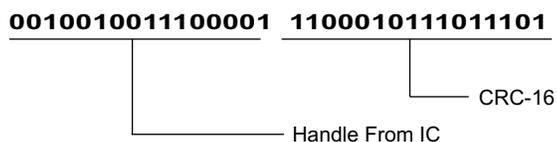


Figure 2-24. Access 2 Response

After the second successful response, the IC is in the **Secured** state.

2.1.13 BlockWrite Command

The optional **BlockWrite** command allows multiple words to be written to the IC's reserved or EPC memory with a single command. Words are 16 bits long.

The command takes the following parameters:

- MemBank: Memory bank to be written (reserved, EPC)
- WordPtr: Starting word address for the data
- WordCount: Number of 16-bit words to be written
- Data: Data to be written
- Handle: Identifier between IC and reader
- CRC-16: Checksum calculated on the data string

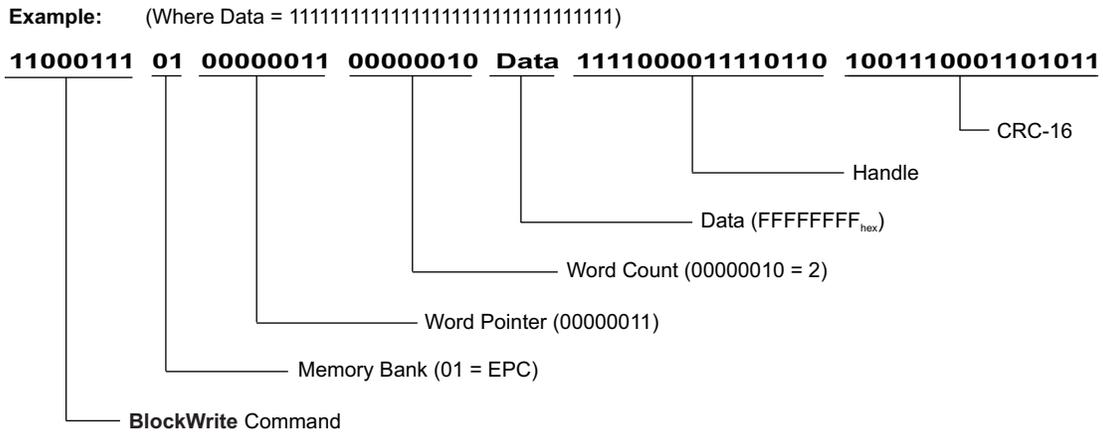


Figure 2-25. BlockWrite Command

The **BlockWrite** command response is similar to:

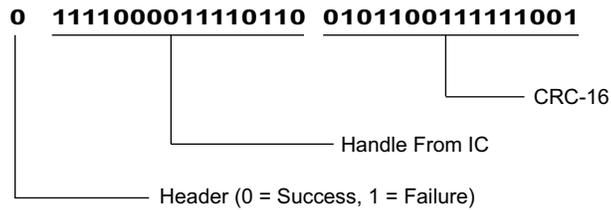


Figure 2-26. BlockWrite Response

2.1.14 BlockErase Command

The optional **BlockErase** command allows the erasing of multiple words in a single command. The command takes the following parameters:

- MemBank: Memory bank to erase (reserved, EPC)
- WordPtr: Starting word address for deletion
- WordCount: Number of 16-bit words to be erased
- Handle: Identifier between IC and reader
- CRC-16: Checksum calculated on the data string

Example

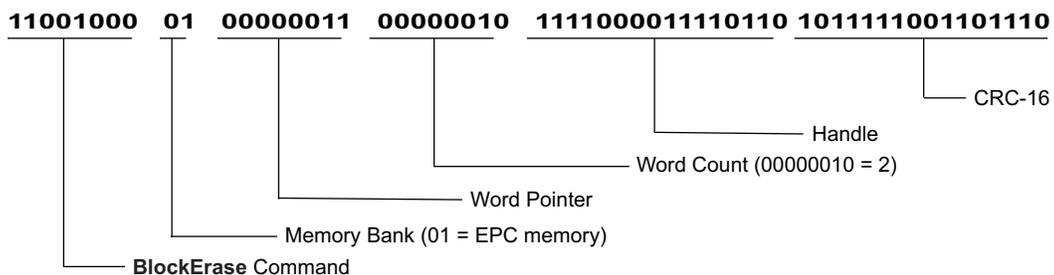


Figure 2-27. BlockErase Command

The **BlockErase** command response is similar to:

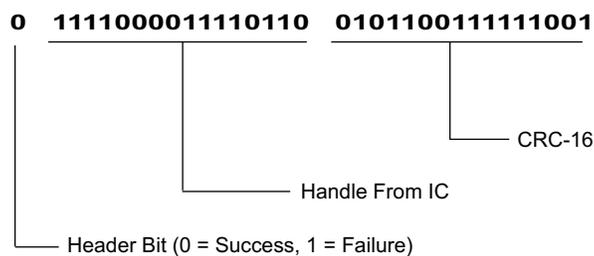


Figure 2-28. BlockErase Response

Regulatory, Safety, and Warranty Notices

Topic	Page
3.1 Regulatory and Safety Notices.....	30
3.2 Warranty and Liability.....	30
3.3 Hazards From Electrostatic Discharge (ESD).....	30

3.1 Regulatory and Safety Notices

An RFID system comprises an RF transmission device and is, therefore, subject to national and international regulations.

Any system reading from or writing to a transponder created from an IC may only be operated under an experimental license or final approval issued by the relevant approval authority. Before any such device or system can be marketed, an equipment authorization must be obtained from the relevant approval authority.

TI Gen2 ICs have been manufactured using state-of-the-art technology and in accordance with the recognized safety rules.

Observe precautions in operating instructions:

- Condition for the safe processing, handling, and fault-free operation of TI Gen2 ICs is the knowledge of the basic safety regulations.
- All persons who handle TI Gen2 ICs must observe the guidelines and particularly the safety precautions outlined in this document.
- In addition, basic rules and regulations for accident prevention applicable to the operating site must also be considered.

3.2 Warranty and Liability

- The "General Conditions of Sale and Delivery" of Texas Instruments Incorporated or a TI subsidiary apply.

CAUTION

TI's transponder ICs are 100% thoroughly tested. It is the responsibility of TI's customers to evaluate their equipment to ensure, through appropriate process controls, that machine and material parameters are met on an ongoing basis.

Note: TI does not accept warranty claims for material that has already undergone packaging or conversion process.

3.3 Hazards From Electrostatic Discharge (ESD)

During handling of ICs and wafers, due regard must be given to the buildup of electrostatic charges (see the data sheet).

CAUTION

Electronic devices can be destroyed by electrostatic energy.

Terms and Abbreviations

A list of the abbreviations and terms used in the various TI manuals can be found in a separate manual:

TI-RFID Product Manuals – Terms & Abbreviations (literature number 11-03-21-002)

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