

THS1050/1060 EVM

User's Guide

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Read This First

About This Manual

This user's guide describes the characteristics, operation, and use of the THS1050/1060 EVM.

How to Use This Manual

This document contains the following chapters:

- Chapter 1 EVM Overview
- Chapter 2 Getting Started
- Chapter 3 User Configurations
- Chapter 4 Control Modes
- Appendix A Schematics

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Data Sheets:	Literature Number
<input type="checkbox"/> THS1060	SLAS212
<input type="checkbox"/> THS1050	SLAS278
<input type="checkbox"/> SN74AHC00	SCLS227F
<input type="checkbox"/> THS4141	SLOS320A
<input type="checkbox"/> THS3201	SLOS242
<input type="checkbox"/> TLV2772ACD	SLOS209D
<input type="checkbox"/> TL1431	SLVS062F
<input type="checkbox"/> SN74ABT244	SCBS099I
<input type="checkbox"/> SN74AHC574DW	SCLS148C
<input type="checkbox"/> OPA681U	SBOS084

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EVM Overview

Chapter 1 gives a general overview of the THS1050/1060 evaluation module (EVM), and describes the features and functions that must be considered when using this module.

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1.1 System Overview

The THS1050/1060 EVM provides a practical platform for evaluating the THS1050 and THS1060 analog-to-digital converters (ADCs): 10-bit resolution, 50/60-MSPS, low-power CMOS, parallel-data output, IF-sampling communications analog-to-digital converter.

The THS1050/THS1060 (sometimes referred to as the ADC or device) is designed to operate at 50/60 MHz maximum clock frequency, making the device suitable for IF sampling of baseband radio signals. The device's internal reference can be powered down when using an external voltage reference.

The EVM supports the HTQFP (heat-dissipating TQFP) PowerPAD™ package style. Refer to the *Package Styles Available* table for details.

Table 1–1. Package Styles Available

Device	HTQFP Package† Supported
THS1050	48-pin (S-PQFP-G48)
THS1060	48-pin (S-PQFP-G48)

† The HTQFP package is a high-temperature plastic quad flatpack device, with pins on a 0.50-mm pitch.

Appendix A contains the schematic diagrams. The THS1050/1060 EVM is formed by:

- Clock-input buffer circuits
- External crystal (clock) oscillator
- ADC internal reference power-down control logic
- External V_{ref} circuit
- Input voltage regulator circuit
- Data bits output buffers
- 1:2 voltage ratio step up transformer (used for converting a single-ended input clock signal to a differential clock signal)
- 1:1 voltage ratio transformer (used for converting a single-ended analog input to a differential input signal)
- Analog input signal conditioning operational amplifier
- Differential amplifier (used to drive the ADC analog inputs directly)

The EVM is a four-layer board constructed from FR4 material. This system allows users to explore and test various clock driving and analog input interface circuits.

This section provides a general overview of the EVM's features and functions. Users must refer to the schematic diagrams in Appendix A, to Texas Instruments *PowerPAD™ Thermally Enhanced Package document* (literature number SLMA002), and to the device's data sheets, literature numbers SLAS212 and SLAS278.

1.2 THS1050/1060 ADC System Outline

This printed-wiring board (PWB) EVM supports the THS1050/1060 analog-to-digital converter. The EVM can be used to evaluate several types of clock-driving and analog-input interface circuits provided on the EVM.

The THS1050/1060 ADC generates 2s-complement data in parallel-data form. The D[9:0] output lines are suitable for driving load capacitances up to 15 pF. General features of the ADC are given in Table 1-2.

Table 1–2. General ADC Features

Device	Resolution	Output Channels	Supports Vref_Int/Vref_Ext	Throughput AV _{DD} = 5 V DV _{DD} = 5 V	Available Package	EVM Order Number
THS1050	10-bit	D[9–0]	Vref_Int /Vref_Ext	50 MSPS	HTQFP(PHP)	THS1050
THS1060	10-bit	D[9–0]	Vref_Int /Vref_Ext	60MSPS	HTQFP(PHP)	THS1060

1.2.1 THS1050/1060 ADC

The THS1050/1060 CMOS pipelined ADC device integrates a nominal 2.4-V bandgap reference, a sample/hold circuit, timing/synchronizing logic, cascade gain stages—consisting of ADC, digital-to-analog converter (DAC) and amplifier—and digital error-correction logic for correcting the device outputs. The device has good linearity and excellent spurious-free dynamic range (SFDR) specification, and can directly drive 15 pF of load capacitance. The THS1050/1060 can tolerate up to 10 pS of analog input-signal jitter and 250 ps skew between CLK+ and CLK– without noticeable performance degradation. This device operates from a 5-V analog supply and a 5-V digital supply. The power dissipation at 5 V is less than 600 mW. Reference voltages for the THS1050/1060 are provided by the on-chip bandgap reference voltage or by an external precision reference voltage.

In addition to its peak processing performance of 50/60 MSPS, the THS1050/1060 analog-to-digital converter (ADC) has an effective number of bits (ENOB) of 9.5, an SFDR of 73 dBc, and is compatible with Texas Instruments existing 10-, 12-, and 14-bit CommsDAC™ devices. The THS1050/1060 die is bonded directly to a copper (Cu) alloy plate on the bottom side of the device package. The Cu alloy plate is often connected to the PCB ground plane to enhance heat conduction.

Input PWD (pin 13) disables the device internal voltage reference when set to logic high.

1.2.2 THS1050/1060 Clocking Scheme

The clock driver circuit can be implemented with a differential amplifier. The schematic in Appendix A shows three circuits for implementing the ADC differential clock. Transformer T2 and resistors R28 and R29 must be removed from the circuit when using a differential amplifier. The device requires a differential clock input of ≥ 6.5 Vp-p. For the purpose of testing the device, a

single-ended clock signal is normally derived from a signal source that can output a sine-wave or a square-wave clock (HP8133A pulse generator). Transformer T2 is used to convert the single-ended clock to differential inputs. This minimizes clock skew and simplifies the design task. It is good design practice to balance the differential outputs from the transformer feeding the ADC's CLK+/CLK- pins. Be aware that the transformer has a certain amount of insertion loss at the frequency of operation.

An SN74ABT244 is used to buffer a TLL level input clock, often the most readily available and convenient signal source. When testing the ADC, it is convenient to plug in a crystal oscillator and use its output to provide the desired ADC clock. Crystal oscillator X1 provides the clock.

1.2.3 Analog Input Drive Circuits

The 1:1 RF transformer is used for impedance matching, dc isolation, and interface between the U6 (ADC) balanced differential pair input and an unbalanced single-ended analog input. Resistors R25 and R26 are used to form a network that reflects 50 Ω across the primary circuit (across J4).

The THS3201/OPA681 is used to provide gain and input signal buffering.

The THS4141 differential amplifier is used to convert the single-ended analog input signal to differential output.

1.2.3.1 Operational Amplifier Interface Circuits

The THS3201/OPA681 is the basic circuit element of the operational amplifier interface circuit used in this design. The device is a high-speed, current-feed-back operational amplifier suitable for driving a high capacitance load. Some of the other THS3201 device features are: 3300-V/ μ S slew rate, –96-dBc distortion figure, 1-GHz bandwidth, 15-nS settling time to 0.01% of the input, and \pm 5-V supply voltages. The OPA681 features 200-V/ μ s slew rate, 280-MHz bandwidth, and 77-dBc distortion figure.

The operational amplifier interface circuit is used to buffer the analog input signal on its way to the ADC input channels. The amplifier provides a noninverting gain of 2.

The THS4141 differential amplifier is used to do single-ended to differential output conversion, thereby eliminating the need for the rf transformer. This device has the following features: –3-dB bandwidth of 200 MHz, slew rate >650 V/ μ S, –84-dBc distortion figure, 7-nS settling time, and supply range of \pm 5 V to \pm 15 V.

1.2.3.2 Internal Reference Voltage Circuit

The on-chip bandgap circuit is used to generate the nominal 3-V REFOUT+ output and the nominal 2-V REFOUT– output. A fixed internal-reference voltage is produced when REFOUT+ is directly connected to REFIN+, and REFOUT– is connected to REFIN–. The reference-circuit input resistance is approximately 200 Ω –240 Ω . W4, W5, and W14 are all opened when using the internal reference.

1.2.3.3 External Voltage Reference Circuit

A Max1682 charge pump, a Thaler Corp VRE3050 precision voltage reference, a resistor network, and two TLE2227 operational amplifiers, configured as unity-gain noninverting buffer amplifiers, are used to provide the device's adjustable external reference voltages VREF+ and VREF-. The VRE3050 has 0.01% initial accuracy and a temperature coefficient (TC) of 0.6 ppm/°C, making it a suitable voltage reference for the ADC. The Max1682 requires an input voltage ≥5 V for a 10-V output.

Using the external reference voltage requires that W6 and W7 be opened and W4 and W5 be connected; W14 may or may not be connected.

Output Buffers

Two SN74AHC574 are used for buffering the ADC output to connector J7. These buffers are required for driving load capacitances >15 pF.

TL1431 Shunt Regulator

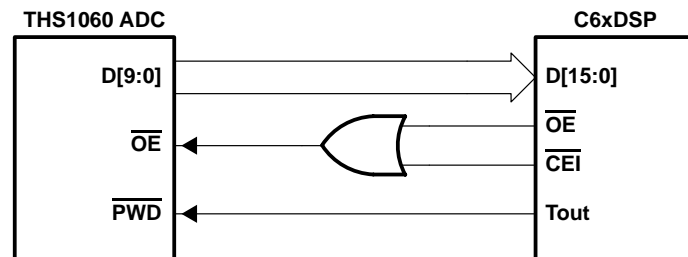
A TL1431 precision-shunt voltage regulator is used to generate the 3.3-V DVcc supply. This device has an initial accuracy of 0.4% and a temperature coefficient (TC) of 30 ppm/°C, making the device a suitable 3.3-V voltage regulator for a 10-bit ADC operating in a temperature-controlled environment.

1.2.3.4 DSP interface

The THS1050/1060 has 10 parallel data output lines (D9:0). There are various options for interfacing to DSPs; a C6201 DSP interface is used in this document. A DSP is used to provide chip-select (\overline{OE}), input clock (CLKOUT), and power-down signal input (\overline{PWD}) to the device.

Figure 1–2 shows the pin-to-pin connections between the THS1050/1060 EVM and the TMS320C6x EVM. The configuration shown in Figure 1–2 uses the DSP to collect the ADC samples and store them in DSP memory.

Figure 1–1. THS1060 to C6X DSP Interface



1.2.3.5 Logic Analyzer/Signal Generator Interface

Connector J7 is used to interface a logic analyzer to the EVM. The SMA connector J5 interfaces directly to an HP8133A clock source, and connector J4, through a BNC to SMA cable, interfaces to an HP33120A or HP8644B signal generator that provides the analog input to the EVM.

1.2.3.6 THS56X1 EVM Parallel DAC Interface

The THS56X1 EVM, with either a 12-bit resolution THS5661A or a 14-bit resolution THS5671A DAC, mates directly to connector J7 on the THS1050/1060 EVM board. Each DAC output can supply up to 20 mA of current. Ten data lines (D9:0), two address lines (A0, A1), an IOSTROBE~ control line or W1 (grounded), and the CLK signal from the ADC are used to interface the DAC to the ADC.

1.3 EVM Operating Modes

The EVM has two modes of operation:

- DSK/microprocessor mode
- Logic analyzer/signal generator mode

Each of these modes is discussed below.

1.4 Power and Cabling Requirements

The EVM dc supply voltages are analog ± 5 V and digital 5 V. These voltages must be supplied to the EVM through shielded-twisted-pair wire for best performance. This type of power cabling minimizes any stray or transient pickup from the higher-frequency digital circuitry. A TLC1431 shunt regulator is used to generate the 3.3-V DV_{CC} supply for the onboard output buffers U8 and U9 (provided on the EVM for driving high-capacitance loads) and for the ADC's output-driver power supply DRV_{DD} . The best signal-to-noise (SNR) performance is achieved when both DRV_{DD} and DV_{CC} are 3.3 V.

If a ribbon cable is used for interfacing to J7, this cable must be shielded to minimize the crosstalk between adjacent conductors.

1.5 ADC Output Configuration

The ADC generates 2s-complement data in a parallel format. It is not necessary to buffer the output from the device for load capacitances less than 15 pF.

1.6 Printed-Circuit Assembly Options Available

A variety of input-drive circuits is provided on the THS1050/1060 EVM to ensure the flexibility of the printed-circuit board (PCB). This simplifies the evaluation of different drive techniques.

Table 1–3. Possible ADCs

ADC Part No.	No. of Bits	Speed	EVM Order No.
THS1050	10	50 MSP	THS1050
THS1060	10	60 MSP	THS1060

Ensure that the printed-circuit assembly (PCA) has the correct check mark on the silkscreen.

Additional hardware may have to be installed on the PCA as required.

Getting Started

This chapter describes the physical characteristics and PCB layout of the EVM and lists the components used on the module.

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2.2 PowerPAD™	2-2
2.3 Parts List	2-6

2.1 Physical Description

The PWB is constructed in four layers (FR4 material) as shown in the following illustrations. The dimensions of the PWB are 4.625 in × 3.000 in (117,48 mm × 76,20 mm). See Figure 2–1.

2.2 PowerPAD™

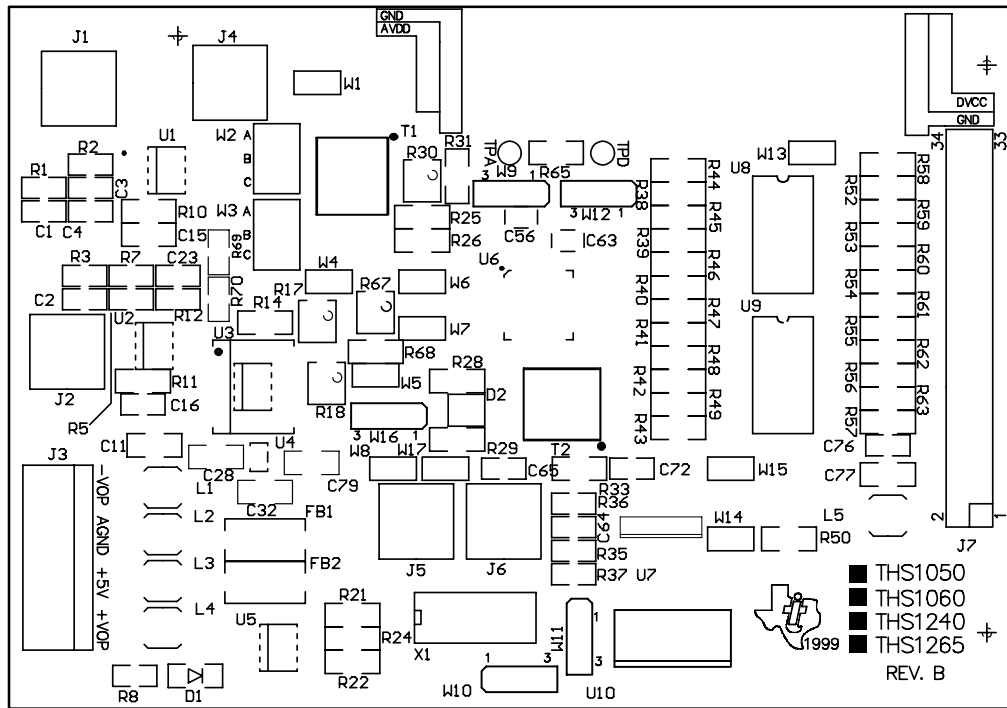
The THS1050/1060 comes in a 48-pin HTQFP package with a Cu alloy plate on the bottom side of the package. The PowerPAD package provides good heat-transfer performance from the die to the surroundings. The THS1050/1060 has power consumption of approximately 600 mW for 60-MHz operation.

Figures 2–2 and 2–3 show the actual size of the thermal pad used to connect the device Cu alloy plate to the PCB ground plane. A 6-mil thick laser-cut stencil is used to dispense the solder paste during manufacturing of the EVM board.

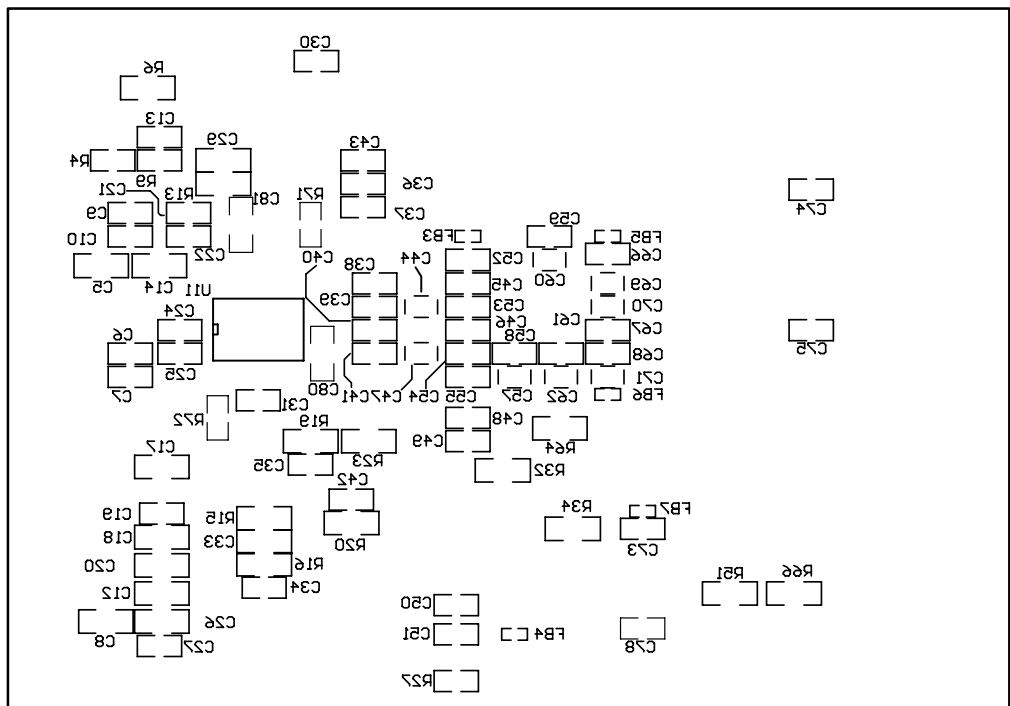
Refer to the THS1050/1060 data sheet for more information on the device performance with the PowerPADsoldered to the board versus the performance when the PowerPAD is not soldered to the board. The actual test results were taken using the THS1050/1060/1240 EVM.

Figures 2–2 through 2–5 show the tracking for each layer.

Figure 2–1. PWB Layers



TOP VIEW



BOTTOM VIEW

Figure 2–2. Layer 1

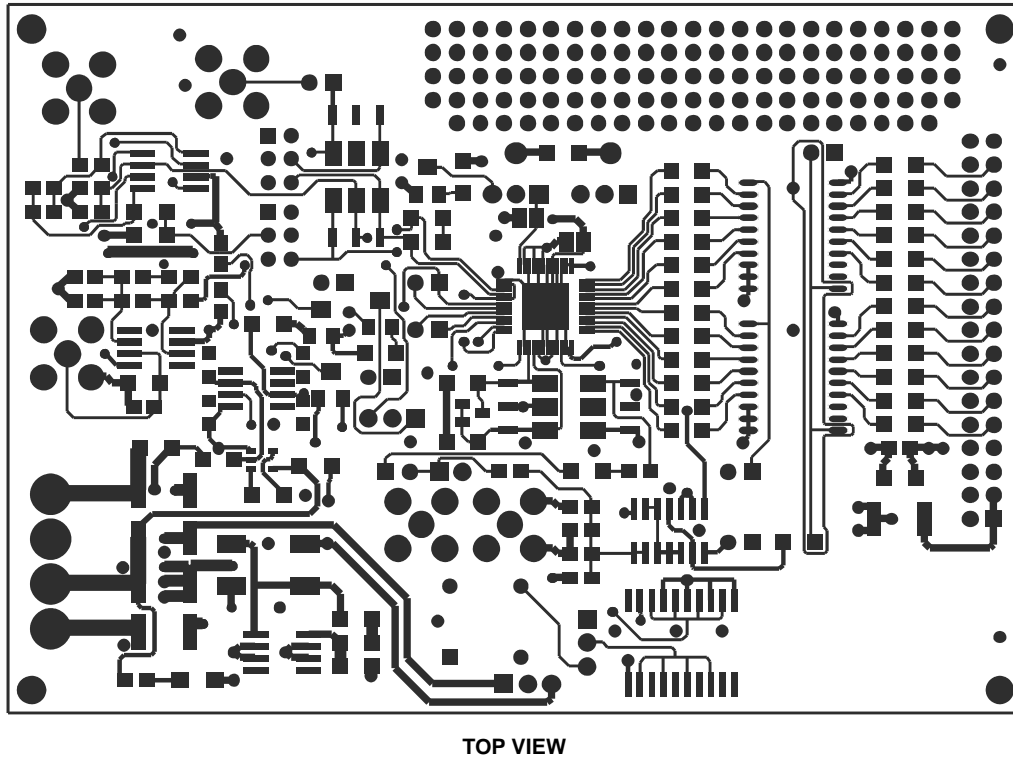


Figure 2–3. Layer 2

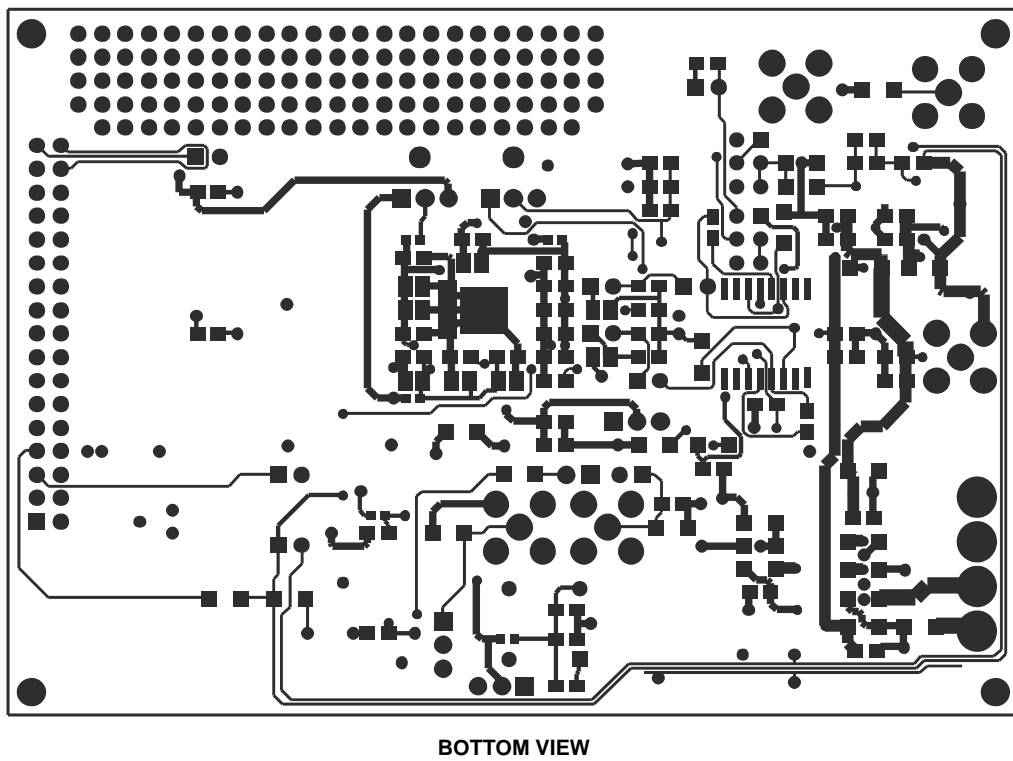
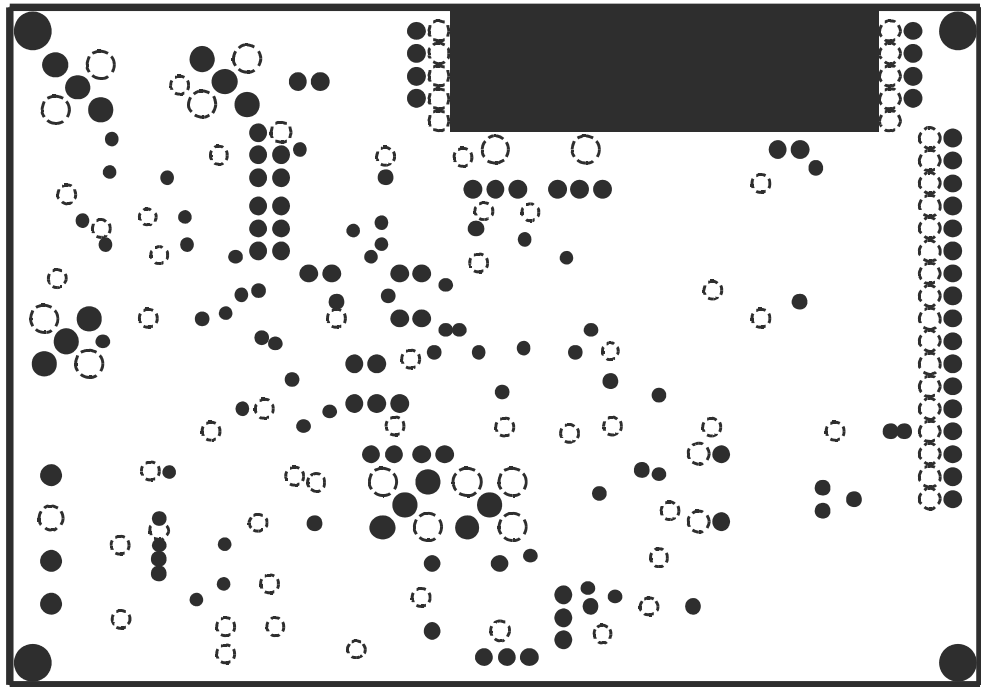
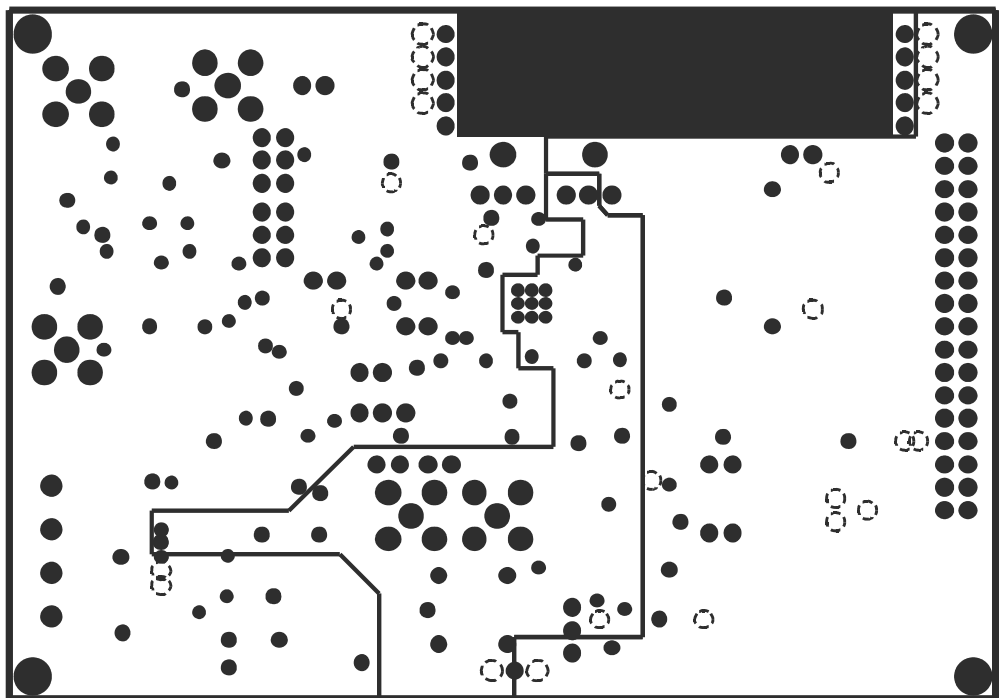


Figure 2–4. Layer 3



GROUND PLANE

Figure 2–5. Layer 4



POWER PLANE



2.3 Parts List

Quantity		Reference Description	Value	Footprint	Description	Manufacturer	Part Number
1050	1060						
1	1	N/A	PCB FAB	N/A	THS1265 EVM Fabrication – Rev B		
12	12	C30 C44 C47 C56 C57 C60 C62 C63 C69 C70 C71 C72	0.1 μ F	0508	Ceramic, X7R, 16 V, 15%	AVX/Murata	0508YC104MAT1W/LL0508X7R104K16
15	15	C10 C19 C22 C25 C27 C3 C34 C51 C65 C7 C73 C74 C75 C76 C78	0.1 μ F	0805	Ceramic, X7R, 16 V, 10%	AVX/Murata	0805YC104KAT1A/GRM40X7R104K016A
16	16	C11 C12 C14 C17 C18 C20 C26 C28 C32 C33 C5 C77 C8 C79 C80 C81	10 μ F	1206	Ceramic, Y5V, 10 V, 80/–20%	AVX/Murata	1206ZG106ZAT2A/GRM42-6Y5V106Z010A
2	2	C15 C29	22 pF	0805	Ceramic, COG, 25 V, 10%	AVX/Murata	08053A220KAT2A/GRM42-6COG220K025A
13	13	C21 C24 C4 C45 C46 C58 C59 C6 C61 C66 C67 C68 C9	0.01 μ F	0805	Ceramic, X7R, 16 V, 10%	AVX/Murata	0805YC103KAT1A/GRM40X7R103K016A
1	1	C23	4.7 pF	0805	Ceramic, COG, 25 V, 10%	AVX/Murata	08053A4R7KAT2A/GRM40COG5R0C025A
3	3	C39 C41 C52	4.7 μ F	0805	Ceramic, Y5V, 10 V, 80/–20%	AVX/Murata	0805ZG475ZAT1A/GRM40Y5V475Z010A
8	8	C31 C35 C36 C38 C40 C53 C54 C55	1 μ F	0805	Ceramic, X7R, 10 V, 20%	AVX/Murata	0805ZC105MAT1A/GRM40X7R105M010A
2	2	C43 C48	0.47 μ F	0805	Ceramic, X7R, 16 V, 10%	AVX/Murata	0805YC474KAT1A/GRM40X7R474K016A
3	3	C37 C49 C50	1 nF	0805	Ceramic, X7R, 16 V, 10%	AVX/Murata	0805YC102KAT1A/GRM40X7R102K016A
1	1	D1	Green LED	1206	Green 1206 size chip LED	Chicago Miniature	CMD15-21VGC
2	2	FB1 FB2	Ferrite Bead		Surface mount ferrite bead	Fair Rite	2743037447
5	5	FB3 FB4 FB5 FB6 FB7	Ferrite Bead	0603	Surface mount ferrite bead	Murata/Fair Rite	BLM11HB601SD/2506033017Z0
5	5	J1 J2 J4 J5 J6	SMA Jack		PCB mount SMA jack	Johnson Components/Lighthouse Tech.	142-0701-206/LTI-SASF54NT

Quantity		Reference Description	Value	Footprint	Description	Manufacturer	Part Number
1050	1060						
1	1	J3	Terminal Block		4 Terminal screw connector	Lumberg/Kaltron	KRMZ4/TB-04SLA
1	1	J7	17 × 2 × 0.1		34 Pin dual row header	Samtec	TWS-117-07-L-D
5	5	L1 L2 L3 L4 L5	4.7 μH	DO1608C	4.7uH, ±20%, 1.5 A	Coil Craft	DO1608C-472
3	3	R1 R2 R9	511	0805	0805 Chip resistor, 1%	Bourns	CR0805-FX-5110
28	28	R10 R11 R13 R34 R38 R39 R40 R41 R42 R43 R44 R45 R46 R47 R48 R49 R52† R53 R54 R55 R56 R57 R58† R59 R60 R61 R62 R63 R66 R6	49.9 ohm	1206	1206 Chip resistor, 1%	Bourns	CR1206-FX-49R9
13	13	R12 R15 R24 R64 R65 R32 R33 R50 R69 R70 R71 R72	0 ohm	1206	1206 Chip resistor, 5%	Bourns	CR1206-FX-000
1	1	R14	2.94K	1206	1206 Chip resistor, 1%	Bourns	CR1206-FX-2941
4	4	R17 R18 R30 R67	2K Pot		4 mm, 5T, SM potentiometer	Bourns	3214W-2-202E
2	2	R28 R29	100	1206	1206 Chip resistor, 1%	Bourns	CR1206-FX-1000
2	2	R31 R68	750	1206	1206 Chip resistor, 1%	Bourns	CR1206-FX-7500
1	1	R19	1.5K	1206	1206 Chip resistor, 1%	Bourns	CR1206-FX-1501
1	1	R23	1.05K	1206	1206 Chip resistor, 1%	Bourns	CR1206-FX-1051
3	3	R16 R25 R26	24.9	1206	1206 Chip resistor, 1%	Bourns	CR1206-FX-24R9
1	1	R22	24.9K	1206	1206 Chip resistor, 1%	Bourns	CR1206-FX-2492
5	5	R27 R3 R36 R5 R8	1K	0805	805 Chip resistor, 1%	Bourns	CR0805-FX-1001
2	2	R35 R37	383	0805	805 Chip resistor, 1%	Bourns	CR0805-FX-3830
1	1	R4	523	0805	805 Chip resistor, 1%	Bourns	CR0805-FX-5230
2	2	TPA TPD	Test Point		Turret type test pin	Cambion	180-7337-02-05
1	1	U1	THS4141	8-SOIC(D)	200 MHz differential op amp	Texas Instruments	THS4141CD/THS4141ID
1	1	U2	THS3201/OPA681	8-SOIC(D)	1000 MHz, high speed amp	Texas Instruments	THS3201CD/ THS3201ID/OPA681U
1‡	1‡	U3	VRE3050	8-SOP(D)	Precision voltage regulator	Thaler Corp.	VRE3050ASN/ VRE3050JSN

† R52 and R58 not used with THS1050/60

‡ Alternative device MAX6250

Quantity		Reference Description	Value	Footprint	Description	Manufacturer	Part Number
1050	1060						
1	1	U4	MAX1682	5-SOT(DBV)	Switched capacitor voltage doubler	Maxim	MAX1682EUK-T
1	1	U5	TL1431	8-SOP(D)	Precision programmable reference	Texas Instruments	TL1431CD/TL1431QD
1		U6	THS1050	48-HTQFP(PHP)	10 bit, 50 MSPS ADC	Texas Instruments	THS1050CPHP/THS1050IPHP
	1	U6	THS1060	48-HTQFP(PHP)	10 bit, 60 MSPS ADC	Texas Instruments	THS1060CPHP/THS1060IPHP
1	1	U7	SN74AHC00	14-SOP(D)	Quad NAND gate	Texas Instruments	SN74AHC00DR
2	2	U8 U9	SN74AHC574	20-SOIC(DW)	3.3 V octal D-FF, 3-state	Texas Instruments	SN74AHC574DW
2	2	U10	SN74ABT244DW	20-SOIC(DW)	Octal buffer/driver	Texas Instruments	SN74ABT244DW
1	1	U11	TLE2227	16-SOIC(DW)	High speed, low noise, dual	Texas Instruments	TLS2227CDW
11	11	W1 W2 W3 W4 W5 W6 W7 W13 W14 W15	Shunt Jumper	2X2X.1	0.025"sq, 2 pin header, 0.1" centers	Samtec	TWS-102-07-L-S
4	4	W10 W11 W12 W9 W16	2 Position Jumper	2X3X.1	0.025"sq, 3 pin header, 0.1" centers	Samtec	TWS-103-07-L-S
1	1	X1	50, 60, 40 or 65 MHz Oscillator		Crystal oscillator	Epson	SG-8002DC-50 MHz/SG-8002DC-60 MHz/ SG-8002DC-40 MHz/SG-8002DC-65 MHz
§	§	U3 Alternate	MAX6250	8-SOP(D)	Precision voltage regulator	Maxim	MAX6250BCSA/MAX6250ACSA
Wire Jumper Defaults:							
MASK	MASK		Jumper Option		24 AWG solid bus wire		
Customer Installed Options							
2	2	R20 R34	49.9 Ω	1206	1206 Chip resistor, 1%	Bourns	CR1206-FX-49R9
2	2	C42 C16	100 pF	0805	Ceramic, COG, 25 V, 10%	AVX/Murata	08053A101KAT2A/GRM40COG101K025A
1	1	C64	220 pF	0805	Ceramic, COG, 25 V, 10%	AVX/Murata	08053A221KAT2A/GRM40COG221K025A
1	1	C2	10 pF	0805	Ceramic, COG, 25 V, 10%	AVX	08053A100KAT2A/GRM40COG100K025A
1	1	D2	BAV99	SOT-23	Dual, small signal diode	General Semi.	BAV99
2	2	C1 C13	1.8 pF	0805	Ceramic, COG, 25 V, 10%	AVX/Murata	08053A1R8KAT2A/ GRM40COG1R8K025A

§ Replacement device for VRE3050

User Configurations

This chapter describes the user-definable options.

Topic	Page
3.1 User Options	3-2
3.2 Analog/Digital Supply Voltages	3-3
3.3 Digital Input Configurations	3-4
3.4 Generating a Voltage Reference	3-6
3.5 Clock Source	3-7
3.6 Connector Pin and Function Assignments	3-7

3.1 User Options

The PCA ships in a state that enables immediate evaluation of the analog-to-digital converter (ADC). However, you can reconfigure various options through hardware. This chapter discusses these options to ensure that any reconfiguration is conducted properly.

The hardware on the PCA falls into various groups:

- Jumpers (shunts)
- Wire links

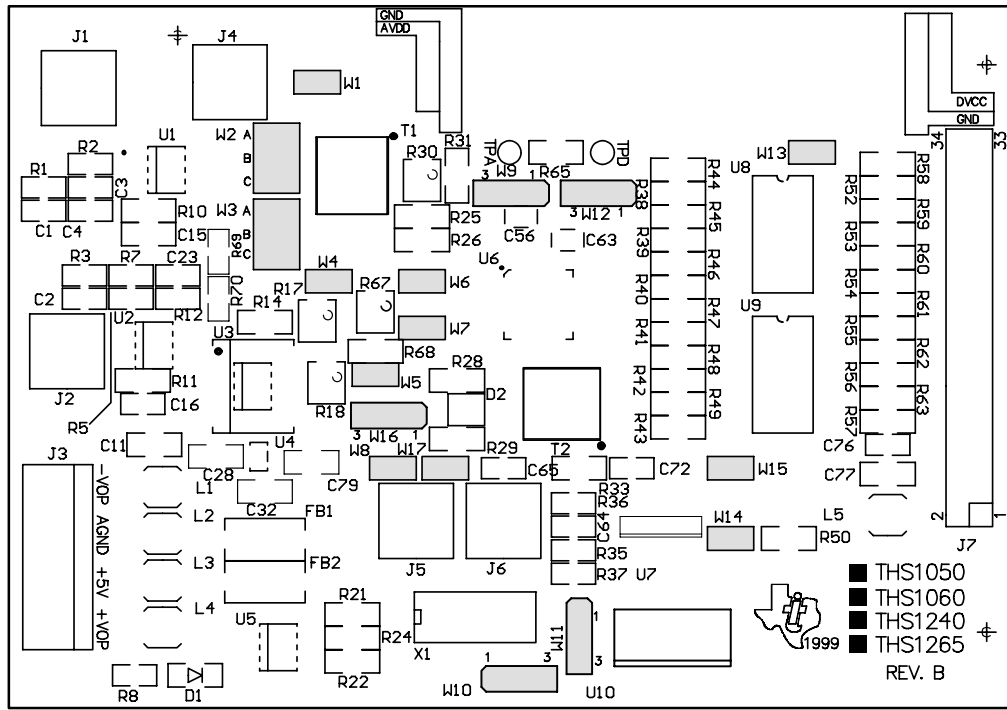
Table 3–1 lists jumper options, a brief description of each function, and information on where to find the options.

Table 3–1. Jumper Functions

Jumper Reference	Function Description
W1	For bypassing C30
W2A	Connects pin 6 of transformer T1 to GND
W2B	Use to connect transformer T1 to a differential voltage source
W2C	Connects –ve output of differential amp to the VIN– pin of the ADC
W3A	Connects amplifier THS3201/OPA681 to T1 primary winding
W3B	Use to connect transformer T1 to a differential voltage source
W3C	Connects +ve output of differential amp to the VIN+ pin of the ADC
W4	Connects external REF– to REFIN–
W5	Connects external REF+ to REFIN–
W6	Connects REFOUT– to REFIN–
W7	Connects REFOUT+ to REFIN+
W8	Connects the clock signal from J5 to circuit used to derive CLK signal
W9	Selects transformer T1 secondary dc bias: either V _{cm} from the ADC, or the external adjustable common-mode dc-biasing voltage
W10	Selects 5 V(DV _{DD}) or 3.3 V(DV _{CC}) as the V _{CC} supply to the on-board oscillator and the circuit used to generate the CLK output signal
W11	Selects clock source J6 or 50, 60, or 65 MHz osc output
W12	Selects 3.3 V or 5 V as DR _{DD} input voltage
W13	Connects CLK signal to J7
W14	GND W14 to disable internal VREF+/VREF–
W15	Use to GND $\overline{\text{OE}}$ of U8/U9
W16	Selects transformer T2 secondary dc bias: either V _{cm} from the ADC, or the external adjustable common-mode dc-biasing voltage
W17	Connects U10A output to T2 and to the circuit that generates the CLK to J7–33

Figure 3–1 indicates the physical locations of this hardware.

Figure 3–1. Physical Location of Each Jumper



TOP VIEW

3.2 Analog/Digital Supply Voltages

Two options supply power to the analog/digital sections of the EVM:

- 3.3 V (DV_{CC}) or 5 V digital DV_{DD} (the THS1050/1060 output buffer is powered from 3.3 V or 5 V, while the V_{CC} input to the two SN74AHC574 buffers is tied to 3.3 V.)
- 5 V analog AV_{DD}
- 5 V (+V_{OP}) operational amplifier positive-supply voltage
- 5 V (-V_{OP}) operational amplifier negative-supply voltage

Configure the power supply voltages in accordance with Table 3–2.

Table 3–2. Analog Voltage Supply Configuration Options

J3 Connector	Function
J3–1	5 V (+V _{OP})
J2–2	5 V (AV _{DD})
J3–3	AGND
J3–4	-5 V (-V _{OP})

3.3 Digital Input Configurations

A variety of options is available to configure the digital inputs. This section describes these options, along with the jumper settings required.

Table 3–3. Digital Input Options

Digital Input Option	Connector Reference and Type (Schematics Rev. B)	Connector Reference and Type (Schematics Rev. C)
	IDC	IDC
Apply input \overline{PWD} signal from DSP to J7	J7 – 7 × 17 plug	J7 – 31 × 17 plug
Apply output buffer control signal, \overline{OE} , from DSP to J7 (pin 5)	J7 – 5 × 17 plug	J7 – 29 × 17 plug
3.3 V DVcc supply from J7	J7 – 1/3 × 17 plug	J7 – 25/27 × 17 plug

The user selects the above configurations based on the test equipment available. These are discussed below.

When jumper W15 is in place, the outputs of U8 and U9 are enabled. This configuration is used when the EVM is not hooked up to a DSP board. When using the EXT_VREF+/EXT_VREF– inputs, W14 can be used to power down the internal voltage reference. Thus, no connection may be made to W14 when using the internal voltage reference.

A few control lines from a DSP allow the use of J7 to store the 2s-complement ADC output data in memory.

Figure 3–2. Direct Connect Jumper Configuration for THS1050/1060 EVM

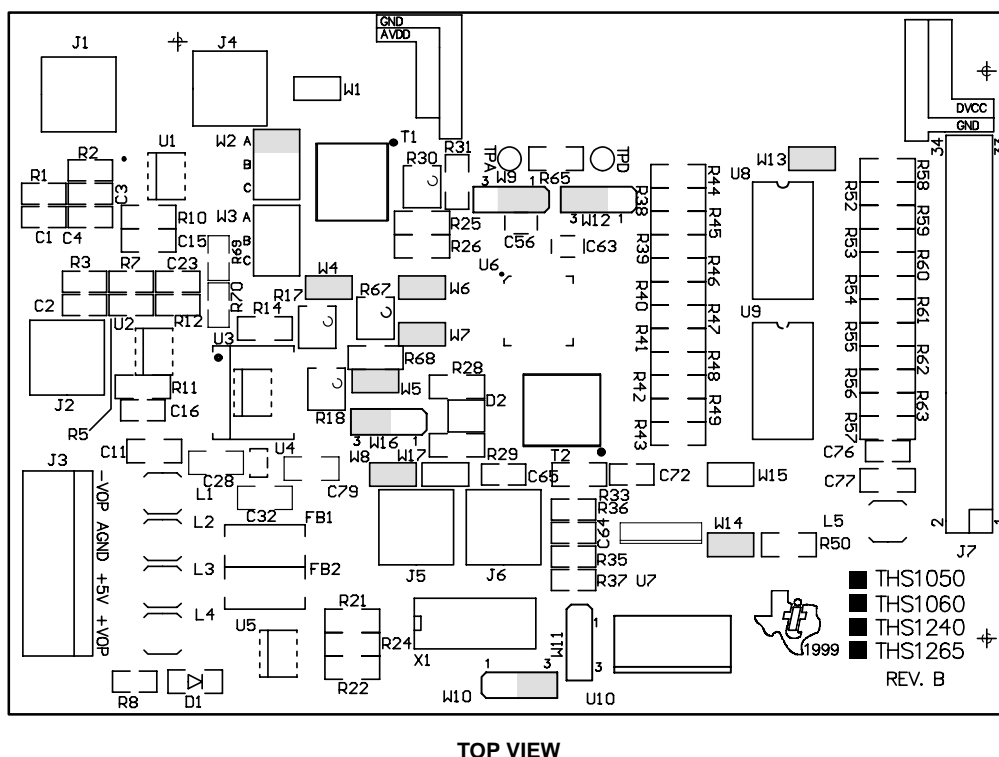


Table 3–4. Shipping Condition of Jumpers W1 Through W17

Jumper	Pins 1 and 2	Pins 2 and 3
W1	Jumper not installed	N/A
W2A	Jumper installed	N/A
W2B	Jumper not installed	N/A
W2C	Jumper not installed	N/A
W3A	Jumper not installed	N/A
W3B	Jumper not installed	N/A
W3C	Jumper not installed	N/A
W4	Jumper not installed	N/A
W5	Jumper not installed	N/A
W6	Jumper not installed	N/A
W7	Jumper installed	N/A
W8	Jumper installed	N/A
W9	Jumper installed	Jumper not installed
W10	Jumper installed	Jumper not installed
W11	Jumper installed	Jumper not installed
W12	Jumper not installed	Jumper installed
W13	Jumper installed	N/A
W14	Jumper not installed	N/A
W15	Jumper installed	N/A
W16	Jumper not installed	Jumper installed
W17	Jumper not installed	N/A

3.4 Generating a Voltage Reference

The voltage reference can be provided by the internal reference, or by the on-board external reference.

3.4.1 Internal Reference

To set the THS1050/1060 to use REFOUT+ and REFOUT– as input voltages to the on-chip internal reference circuit requires the jumper configuration shown in Table 3–5.

Table 3–5. Jumper Configuration for Internal Reference Voltage

Jumper	Pins 1 and 2	Pins 2 and 3
W4 (EXT_VREF+)	Jumper not installed	N/A
W5 (EXT_VREF–)	Jumper not installed	N/A
W6 (+2V)	Jumper installed	N/A
W7 (+3V)	Jumper installed	N/A
W14	Jumper not installed	N/A

3.4.2 Onboard External Reference

To select the onboard external reference voltage, the user should follow the jumper configuration shown in Table 3–6.

Table 3–6. External VREF for U6 Jumper Configuration

Jumper	Pins 1 and 2	Pins 2 and 3
W4 (EXT_VREF+)	Jumper installed	N/A
W5 (EXT_VREF–)	Jumper installed	N/A
W6	Jumper not installed	N/A
W7	Jumper not installed	N/A

It is important to understand that the reference voltage plays a fundamental part in the conversion process. Changes in the value of the reference voltage are reflected in the full-scale range of the device. The variation in voltage for the reference should ideally contribute less than 1/2 an LSB of error to the total conversion process.

When using the onboard external precision voltage reference, install W14 or take the $\overline{\text{PWD}}$ line low to power down the device's internal-voltage reference. Disabling the internal-voltage reference while using an external-voltage reference avoids the need for the 4.7- μF capacitor on pins 8 and 9 of U6. The normal ADC operation with an external-voltage reference and U6–13 tied to GND requires a 1- μF (or greater) capacitor on pins 8 and 9 of U6.

3.5 Clock Source

The THS1050/1060 requires an external clock. There are three possible external sources for the ADC clock on the EVM. To attain optimum device performance, the user should adhere to the minimum data-to-clock transition setup and hold times specified in data sheets SLAS212 and SLAS278. Violating these timing parameters may result in increased converter-output noise level.

The clock for the ADC is derived from either the DSP, a crystal oscillator, a generator driving an ABT244 buffer, or a low jitter clock source. The clock is normally a sine wave or square wave signal of ≥ 3.5 -V amplitude.

3.5.1 External Clock Generation

The maximum operational speed of the THS1050/1060 is 50/60 MHz when operating from 5-V AV_{DD} and DV_{DD} supplies. The clock signal is derived from either a low-jitter clock source such as the HP8133A, or from the DSP CLKOUT signal, which is usually a less precise clock source.

3.5.2 Digital Output Circuit

Two SN74AHC574 buffers are used to interface the ADC to output connector J7. The resistor shown connected to Q[6:1] improves damping of the ADC buffered output lines.

3.6 Connector Pin and Function Assignments

This section details the pinouts and functions for all user connectors.

Table 3–7. Connector Pin and Function Assignments

Reference Designator	Function
J7	ADC 2s-complement parallel output/DSP interface
W11, J5, J6	Clock input
J3	Digital circuit supply voltage
J3	Analog supply voltages
J1, J2, J4	Analog input

Table 3–8. J3 Power Connector

Pin Number	Function
J3–1	Operational amplifier +5 V power
J3–2	5-V AV_{DD} /5-V DV_{DD}
J3–3	AGND
J3–4	Operational amplifier –5 V power

Table 3–9. J1, J2, and J4 Analog Input Signal Connectors

SMA	Function	SMA	Function
J1–1	Single-ended analog input via differential amplifier	J1–2	AGND
J2–1	Single-ended analog input via operational amplifier	J6–2	AGND
J4–1	Single-ended input to T1 transformer	J4–2	AGND

Table 3–10. W11, J5, and J6 Clock Input Connectors

SMA	Function	SMA	Function
W11 pin 2/3	Single-ended clock oscillator input to T2 via SN74ABT244 buffer		
J5–1	Single-ended clock input to T2, 1:2 ratio step-up voltage transformer	J5–2	AGND
J6–1	Single-ended input via SN74ABT244 to T2, 1:2 ratio step-up transformer	J6–2	AGND

Table 3–11. J7, 2s-Complement Parallel Data Connector/DSP Interface Connector (for Schematics Revision B)

Pin Number	Function	Pin Number	Function
1	DVcc (3.3 V output)	2	Ground (digital)
3	DVcc (3.3 V output)	4	Ground (digital)
5	\overline{OE} (input)	6	Ground (digital)
7	\overline{PWD} (input)	8	Ground (digital)
9	D11(MSB) (output)	10	Ground (digital)
11	D10 (output)	12	Ground (digital)
13	D09 (output)	14	Ground (digital)
15	D08 (output)	16	Ground (digital)
17	D07 (output)	18	Ground (digital)
19	D06 (output)	20	Ground (digital)
21	D05 (output)	22	Ground (digital)
23	D04 (output)	24	Ground (digital)
25	D03 (output)	26	Ground (digital)
27	D02 (output)	28	Ground (digital)
29	D01 (output)	30	Ground (digital)
31	D00 (LSB) (output)	32	Ground (digital)
33	CLK/CLKOUT (input—W13 opened—or output—W13 connected)	34	Ground (digital)

**Table 3–12. J7, 2s-Complement Parallel Data Connector/DSP Interface Connector
(for Schematics Revision C)**

Pin Number	Function	Pin Number	Function
1	D11(MSB) (output)	2	Ground (digital)
3	D10 (output)	4	Ground (digital)
5	D09 (output)	6	Ground (digital)
7	D08 (output)	8	Ground (digital)
9	D07 (output)	10	Ground (digital)
11	D06 (output)	12	Ground (digital)
13	D05 (output)	14	Ground (digital)
15	D04 (output)	16	Ground (digital)
17	D03 (output)	18	Ground (digital)
19	D02 (output)	20	Ground (digital)
21	D01 (output)	22	Ground (digital)
23	D00 (LSB) (output)	24	Ground (digital)
25	DV _{CC} (3.3 V output)	26	Ground (digital)
27	DV _{CC} (3.3 V output)	28	Ground (digital)
29	\overline{OE} (i/p)	30	Ground (digital)
31	\overline{PWD} (i/P)	32	Ground (digital)
33	CLK/CLKOUT (input: W13 opened; output: W13 connected)	34	Ground (digital)



Control Modes

The PWD, DRVDD, REFIN+, REFIN-, REFOUT+, REFOUT- and Vcm pins of the THS1050/1060 control various ADC features and functions. This section describes the function of these pins.

Topic	Page
4.1 $\overline{\text{PWD}}$ Input Pin	4-2
4.2 DRVDD Input Pin	4-2
4.3 REFOUT+ Output Pin	4-2
4.4 REFIN+ Input Pin	4-2
4.5 REFOUT- Output Pin	4-2
4.6 REFIN- Input Pin	4-2
4.7 Vcm Output Pin	4-2

4.1 $\overline{\text{PWD}}$ Input Pin

The $\overline{\text{PWD}}$ pin is used for powering down the device's internal-voltage reference. It is an active-high asynchronous power-down input. The device has an internal pulldown. Either W14 or the $\overline{\text{PWD}}$ input signal is used to control the power-down input.

4.2 DRVDD Input Pin

DRVDD = 3.3 V

The device output buffer is configured for 3-V logic voltage levels when pin DRVDD is connected to 3.3 V (DV_{CC}), .

DRVDD = 5 V

The device output buffer is configured for 5-V logic voltage levels when pin DRVDD is connected to 5 V.

4.3 REFOUT+ Output Pin

REFOUT+ is nominally 3 V. Since the THS1050/1060 voltage-reference circuit requires very low current, REFOUT+ is ideal for supplying the REFIN+ input voltage. Jumper W7 is used to connect REFOUT+ to pin REFIN+.

When using the external-reference voltage provided through W5, shunt W7 should be removed from the board.

4.4 REFIN+ Input Pin

The REFIN+ dc-input voltage is provided either from the REFOUT+ output or from the onboard precision-voltage-reference circuit. When using REFOUT+ to drive the REFIN+ input pin, connect W7 and ensure that shunt W5 is removed from the board.

4.5 REFOUT– Output Pin

REFOUT– is nominally 2 V dc and is one of the two voltage sources used to supply input voltage to input pin REFIN– of the THS1050/1060. The second source for supplying REFOUT– is the precision-voltage-reference circuit via W4.

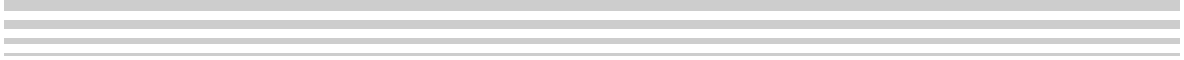
4.6 REFIN– Input Pin

The REFIN– dc-input voltage is provided either from the REFOUT– or from the on-board precision-voltage-reference circuit. Connect W6 and disconnect W4 when using REFOUT– to drive input pin REFIN–.

4.7 Vcm Output Pin

The THS1050/1060 outputs a nominal 2.4-V dc common-mode voltage (V_{cm}). This voltage is used to dc-bias the secondary side of both RF transformers and to provide the common-mode voltage to the THS4141 differential amplifier.

Schematics



A complete schematic including all power supply line decoupling is shown in Appendix A.

