TSW3085EVM Evaluation Module

The TSW3085EVM is a circuit board that allows designers to evaluate the performance of Texas Instruments' dual-channel, ultralow-power, 16-bit, 1.25-GSPS, DAC3482 digital-to-analog converter (DAC) with 16-bit wide DDR LVDS data input, integrated 2x/4x/8x/16x interpolation filters, 32-bit NCO and PLL, and exceptional linearity at high IFs. The EVM provides a flexible environment to test the DAC3482 under a variety of clock, and data-input and RF-output conditions. For ease of use as a complete RF transmit solution, the TSW3085EVM includes the LMK04806B (National Semiconductor) low-noise clock generator/jitter cleaner for clocking the DAC3482, as well as a TRF3705, a 300-MHz to 4-GHz quadrature modulator, for up-converting I/Q outputs from the DAC to real signals at RF.

The EVM can be used along with TSW3100 to perform a wide range of test procedures. The TSW3100 generates the test patterns that are fed to the DAC3482 through a 1.25-GSPS LVDS port. The LMK04806B is also used to synchronize the TSW3100 board to the TSW3085EVM. The RF signal path also includes an amplifier and programmable attenuator.

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1 Introduction

1.1 Overview

The TSW3085 evaluation module (EVM) provides a basic platform to evaluate the DAC3482, which is a 1.25-GSPS, up to 16x interpolation, 16-bit, high-speed dual digital-to-analog converter (DAC) in a complete RF transmit signal chain. Along with the DAC3482, the EVM includes a LMK04806B clock cleaner and generator source which provides the clocks required for the DAC and an external pattern generator. The EVM also includes an onboard TRF3705 modulator which provides onboard IF-to-RF upconversion for basic transmitter evaluation. This EVM is ideally suited for mating with the TSW3100 pattern generation board for evaluating WCDMA, LTE, or other high-performance modulation schemes.

1.2 EVM Block Diagram

Figure 1 TSW3085EVM Block Diagram.

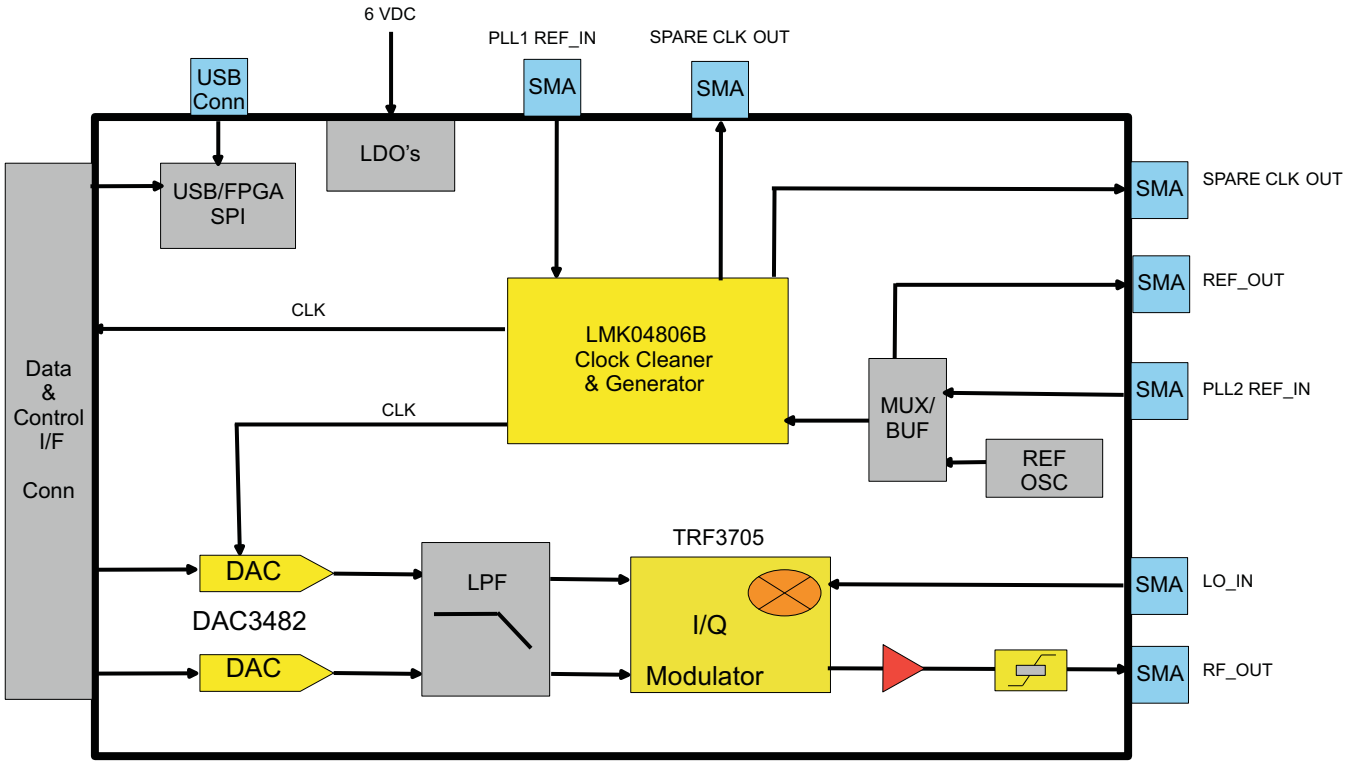

Figure 1. TSW3085EVM Block Diagram

2 Software Control

2.1 Installation Instructions

Perform the following steps to install the software.

1. Open the folder named TSW3085_Installer_vxpx (xpx represents the latest version).
2. Run Setup.exe.
3. Follow the on-screen instructions.
4. Once installed, navigate to C:\program files\tsw3085vi. Start the GUI by clicking on the file named TSW3085.exe.
5. When plugging in the USB cable for the first time, you are prompted to install the USB drivers.

   (a) When a pop-up screen opens, select *Continue Downloading*.

(b) Follow the on-screen instructions to install the USB drivers.

(c) If needed, the drivers can be accessed directly in the install directory.

2.2 Software Operation

The software allows programming control of the DAC, the LMK, and the attenuator devices. The front panel provides a tab for full programming of each device. The GUI tabs provide a more convenient and simplified interface to the most-used registers of each device.

Each device has its own custom control interface. At the top level of the GUI are five control tabs. The first four are used to configure the DAC3482 and the last for the LMK04806B. The attenuator control window on the right side of the GUI is used to program the attenuator.

2.2.1 Input Control Options

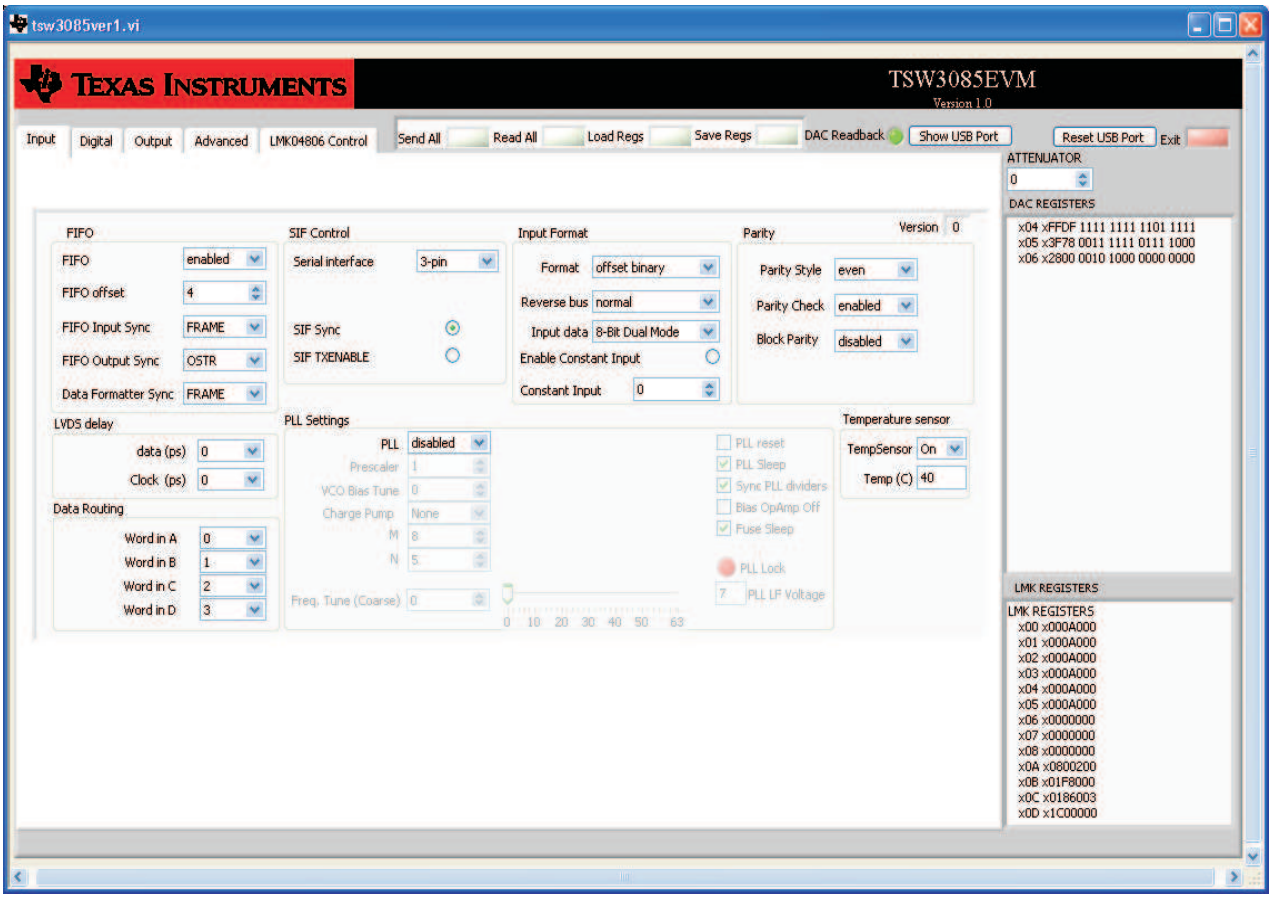

Figure 2. Input Tab Control Options (DAC3482)

- FIFO: allows the configuration of the FIFO and FIFO synchronization (sync) sources.
- LVDS delay: provides internal delay of either the LVDS DATA or LVDS DATACLK to help meet the input setup/hold time.
- Data Routing: provides flexible routing of the A, B, C, and D sample input data to the appropriate digital path. **Note:** the DAC3482 does not support this mode.
- SIF Control: provides control of the Serial Interface (3-wire or 4-wire) and Serial Interface Sync (*SIF Sync*).
- Input Format: provides control of the input data format (i.e., 2's complement or offset binary).
- Parity: provides configuration of the parity input.
- PLL Settings: provides configuration of the on-chip PLL circuitry.
- Temperature Sensor: provides temperature monitoring of DAC3482 die temperature.

2.2.1.1 LVDS Delay Settings

The TSW3100 pattern generator sends out LVDS DATA and DATACLK as edge-aligned signals. The following options can be implemented to meet the minimum setup and hold time of DAC3482 data latching:

- Set the on-chip LVDS DATACLOCK delay. Typical setting of 160 ps or more helps meet the timing requirement for most of the TSW3100 + TSW3085EVM setup. This LVDS DATACLOCK delay does not account for additional printed-circuit board (PCB) trace-to-trace delay variation, only the internal DATACLK delay.
- Modify the external LVDS DATACLK PCB trace delay: Additional trace length on the bottom side of the PCB can be added to the GC_TX9 P&N PCB trace lengths. Set SJP4, SJP5, SJP6, and SJP7 to the 1-2 position for approximately 400 ps of trace delay.

2.2.1.2 PLL Settings

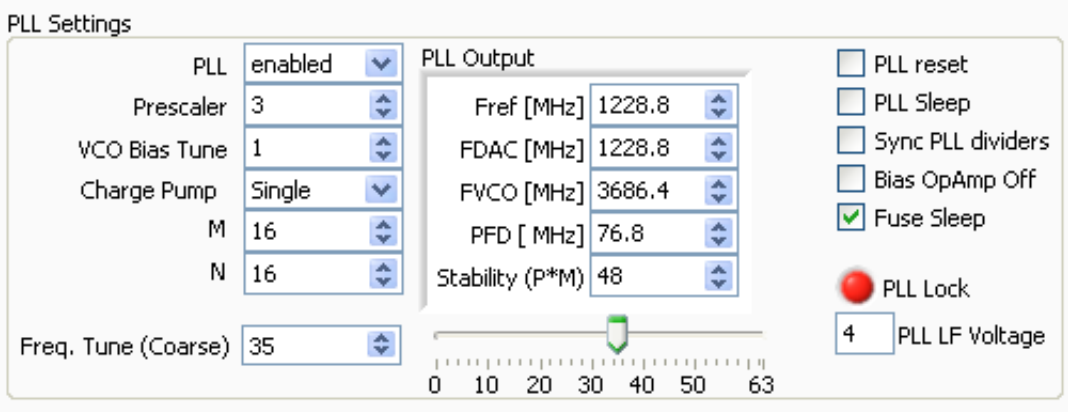

Figure 3. PLL Configuration

Perform the following steps to configure the PLL.

1. Enable PLL.
2. Uncheck *PLL reset* and *PLL sleep*.
3. Set *M* and *N* ratio such that F_{DAC} = (M)/(N) × Fref.
4. Set the *prescaler* such that the F_{DAC} × prescaler is within 3.3 GHz and 4 GHz.
5. Set *VCO Bias Tune* to 1.
6. *Charge Pump* setting
   (a) If stability (P×M) is less than 120, then set to *Single*.
   (b) If stability (P×M) is greater than 120, then set to *Double* or install external loop filter.
7. Adjust the *Freq. Tune (Coarse)* accordingly.

2.2.2 Digital Block Options

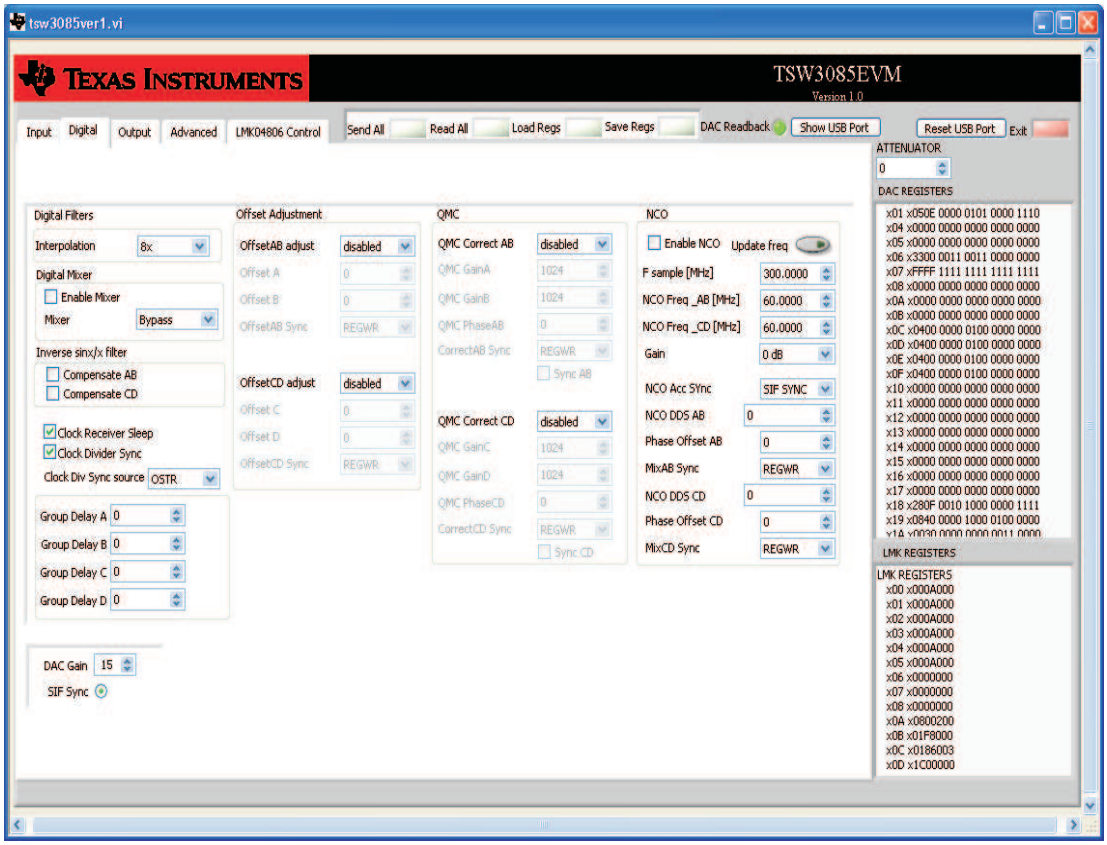

Figure 4. Digital Tab Control Options (DAC3482)

- Interpolation: allows control of the data rate versus DAC sampling rate ratio (i.e., data rate × interpolation = DAC sampling rate).
- Digital Mixer: allows control of the coarse mixer function.
  Note: If fine mixer (NCO) is used, the Enable Mixer button must be checked, and the coarse mixer must be bypassed. See the following NCO bullet for detail.
- Inverse sinx/x filter: allows compensation of the sinx/x attenuation of the DAC output.
  Note: If inverse sinx/x filter is used, the input data digital full-scale must be backed off accordingly to avoid digital saturation.
- Clock Receiver Sleep: allows the DAC clock receiver to be in sleep mode. The DAC has minimum power consumption in this mode.
- Clock Divider Sync: allows the synchronizing of the internal divided-down clocks using either Frame, Sync, or OSTR signal. Enables the divider sync as part of the initialization procedure or resynchronization procedure.
- Group Delay: allows adjustment of group delay for each I/Q channel. This is useful for wideband sideband suppression.
- Offset Adjustment: allows adjustment of dc offset to minimize the LO feedthrough of the modulator output. This section requires synchronization for proper operation. The synchronization options follow:
  - *REGWR*: auto-sync from SIF register write.
  - *OSTR*: sync from the external LVPECL OSTR signal. Clock divider sync must be enabled with OSTR set as sync source.
  - *SYNC*: sync from the external LVDS SYNC signal.
  - *SIF SYNC:* **sync from SIF Sync. Uncheck and check the SIF Sync button for sync event.**

- QMC Adjustment: allows adjustment of the gain and phase of the I/Q channel to minimize sideband power of the modulator output.
  - *REGWR*: auto-sync from SIF register write.
  - *OSTR*: sync from the external LVPECL OSTR signal. Clock Divider Sync must be enabled with OSTR set as sync source.
  - *SYNC*: sync from the external LVDS SYNC signal.
  - *SIF SYNC:* **sync from SIF Sync. Uncheck and check the SIF Sync button for sync event.**
- NCO: allows fine mixing of the I/Q signal. The procedure to adjust the NCO mixing frequency are listed below:
  1. Enter the DAC sampling frequency in Fsample.
  2. Enter the desired mixing frequency in both NCO freq_AB and NCO freq_CD.
  3. Press Update freq.
  4. Sync the NCO block from the following options:
     - *REGWR*: auto-sync from SIF register write. Writing to either *Phase OffsetAB* or *Phase OffsetCD* can create a sync event.
     - *OSTR*: sync from the external LVPECL OSTR signal. Clock Divider Sync must be enabled with OSTR set as sync source. Refer to the data sheet for OSTR period requirement.
     - *SYNC*: sync from the external SYNC signal.
     - *SIF SYNC:* **sync from SIF Sync. Uncheck and check the SIF Sync button for sync event.**

2.2.3 Output Control Options

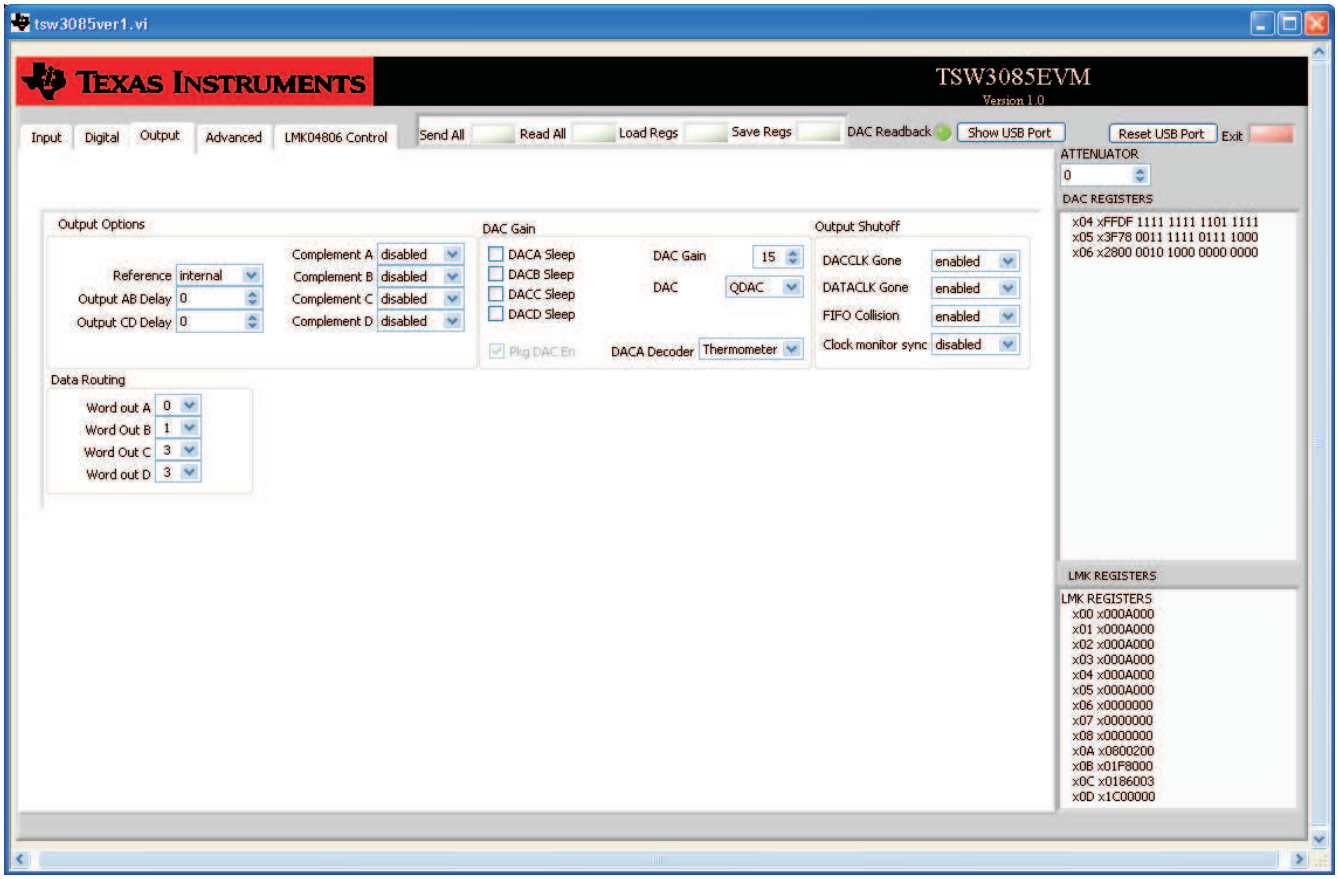

Figure 5. Output Tab Control Options (DAC3482)

- Output Options: allows the configuration of reference, output polarity, and output delay
- Data Routing: provides flexible routing of the A, B, C, and D digital path to the desired output channels. **Note:** The DAC3482 does not support this mode.
- DAC Gain: configures the full-scale DAC current and DAC3484/DAC3482 mode. With Rbiasj resistor set at 1.28 kΩ:
  - O DAC Gain = 15 for 30-mA, full-scale current.
  - O DAC Gain = 10 for 20-mA, full-scale current (default).
  - O DAC3484 = QDAC
  - O DAC3482 = DDAC
    - This allows the DAC3484 to be configured as DAC3482 (see the DAC3484 data sheet, SLAS749, for more information).
    - DAC Sel = Enable inner outputs of Ch. B and Ch. C as the DAC3482 output.
    - DAC Sel = Enable outer outputs of Ch. A and Ch. D as the DAC3482 output. Outer channels are grounded for the DAC3482 device.
- Output Shutoff On: allows outputs to shut off when DACCLK GONE, DATACLK GONE, or FIFO COLLISION alarm event occurs.

2.2.4 LMK04806B

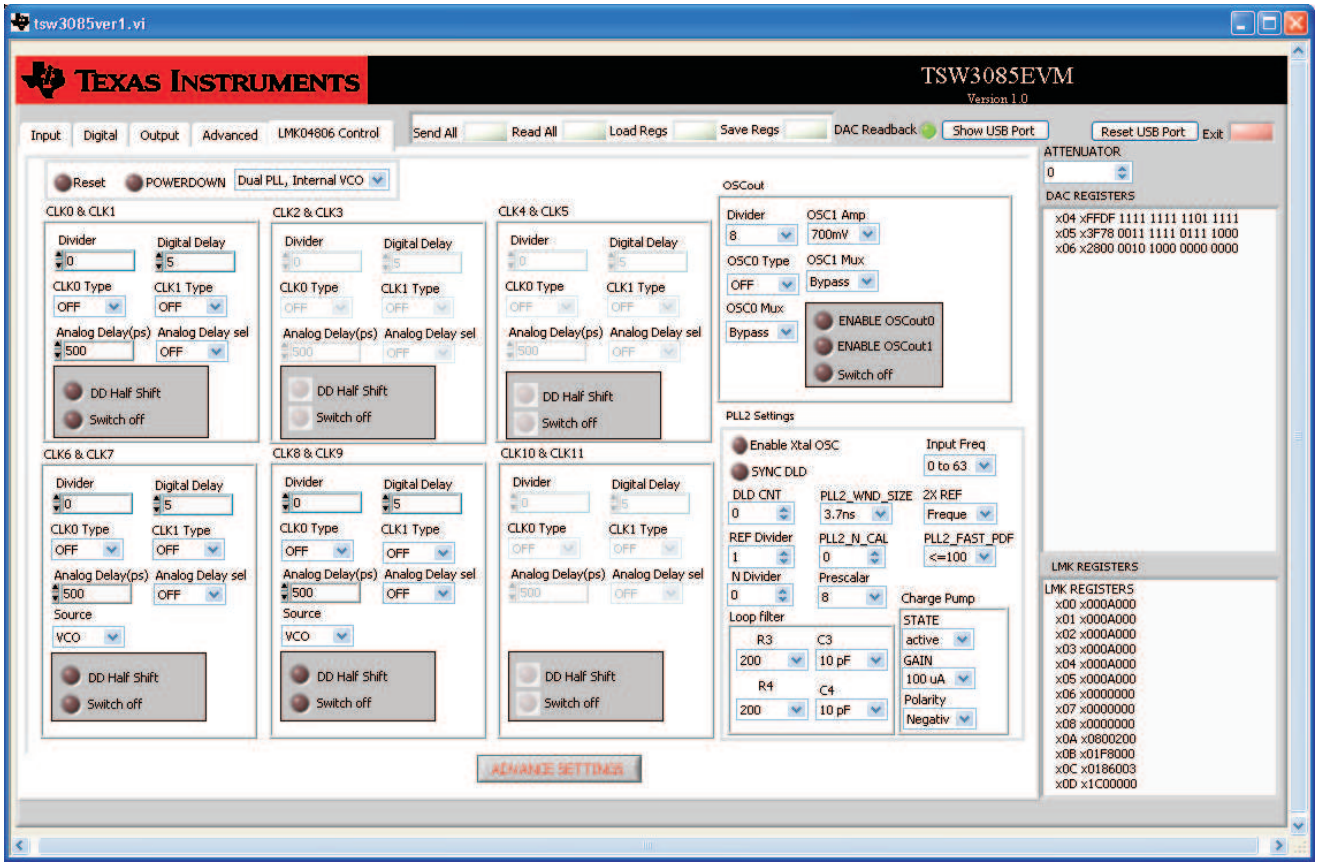

Figure 6. LMK04806B Tab Control Options (LMK04806B)

Clock control is determined by register values in the LMK04806B Control tab. See the LMK04800 family data sheet for detailed explanations of the register configurations.

The LMK04806B has 12 available output clocks. The following LMK04806 outputs are used by the TSW3085EVM :

- CLK0: DAC3482 DAC sampling clock. If the DAC3482 is configured for internal PLL mode, this becomes the reference clock input for the PLL block.
- CLK8: TSW3100 FPGA clock. The clock rate for this is F_{DAC}/interpolation/4.
- CLK6: Spare output clock at SMA J5.

The CLOCK settings are divided into subcontrol sections. These sections allow the user to set the divide ratio, digital delay, type, analog delay, and ON/OFF control. Note that clock pairs share several settings.

The OSCout control section allows the user to configure the settings for the OSCIN input. The TSW3085EVM uses this input as the reference input for Single Loop Mode of operation (default configuration).

The PLL2 Settings control section allows the user to configure the settings for the internal PLL2. The VCO range of the LMK048006B is 2370 MHz to 2600 MHz . The TSW3085EVM default test case uses settings to set the internal VCO to 2457.6 MHz and is locked to the 10-MHz input source on OSCIN.

The default settings provided by the example file provide a 614.4-MHz clock on CLK0 for the DAC3482, a 76.8-MHz clock on CLK8 for the TSW3100 pattern generator input clock, and a 24.576-MHz clock on CLK6 for SMA J5.

After the default settings are loaded, the output clocks are synchronized with the onboard 10-MHz reference oscillator as indicated by LED D6 (Lock status) being illuminated.

Clicking on the Advance Settings tab at the bottom of the GUI opens a new window allowing the user to set other internal registers for different modes of operation as shown in Figure 7.

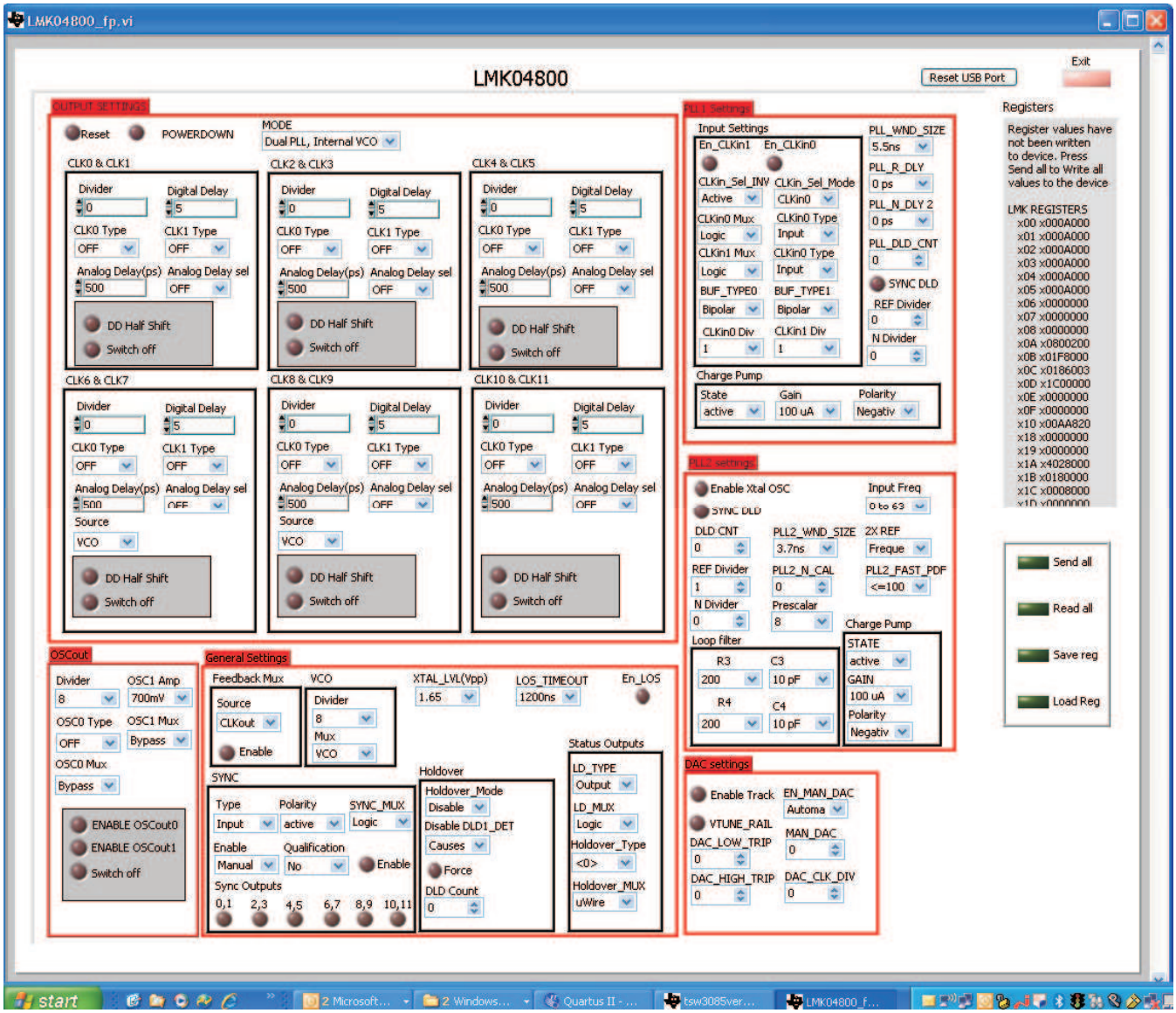

Figure 7. LMK04806B Advanced Settings Control panel

2.2.5 Register Control

- Send All: sends the register configuration to all devices.
- Read All: reads register configuration from DAC3482 and LMK04806B devices.
- Load Regs: loads a register file for all devices. A sample configuration file for a common frequency plan is located in the install directory.
  - Select *Load Regs* button.
  - Double click on the *data* folder.
  - Double click on the desired register file.
  - Click on *Send All* to ensure all of the values are loaded properly.
- Save Regs: saves the register configuration for all devices.

2.2.6 Attenuator Control

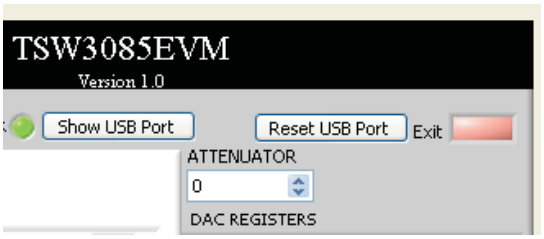

Figure 8. RF Attenuator Control

The RF path on the TSW3085EVM contains a 50-Ω, RF digitally controlled attenuator that operates from dc to 4 GHz. This highly versatile Digital Step Attenuator (DSA) covers a 0-dB to 31.75-dB attenuation range in 0.25-dB steps. It maintains high attenuation accuracy over frequency and temperature and exhibits very low insertion loss (1.9 dB, typical) and low-power consumption. The user can enter a value from 0 (minimum attenuation) to 31.75 (maximum attenuation) in 0.25 increments inside the Attenuator window (Figure 8) or by clicking on the drop-up/-down arrows.

2.2.7 Miscellaneous Settings

- Reset USB: toggle this button if the USB port is not responding. This generates a new USB handle address.
  - Note: It is recommended that the board be reset after every power cycle, and the reset USB button on the GUI be clicked.
- Exit: stops the program

3 Basic Test Procedure

This section outlines the basic test procedure for testing the EVM.

3.1 Test Block Diagram

The test setup for general testing of the TSW3085EVM with the TSW3100 pattern generation board is shown in Figure 9.

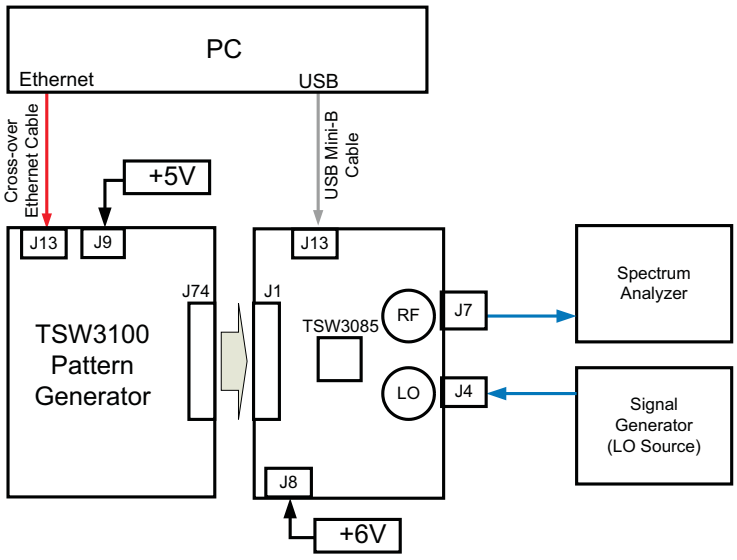

Figure 9. Test Setup Block Diagram

3.2 Test Setup Connection

- TSW3100 Pattern Generator
  1. Connect 5-V power supply to J9, 5V_IN jack of the TSW3100EVM.
  2. Connect the PC's Ethernet port to J13, Ethernet port of the TSW3100. The cable must be a standard crossover Cat5e Ethernet cable.
- TSW3085EVM
  1. Connect J1 connector of TSW3085EVM to J74 connector of TSW3100EVM
  2. Connect 6 V to the J8, *Power In* jack of the TSW3085EVM or use banana jacks J9 (+6 Vdc) and J10 (RTN) if using a laboratory-style power supply.
  3. Connect PC's USB port to J13 USB port of the TSW3085EVM. The cable must be a standard A to mini-B connector cable.
  4. Provide 12-dBm maximum, 350-MHz to 4-GHz LO source at J4. This provides the LO source to the TRF3705 modulator.
  6. Connect the RF output port J7 to a spectrum analyzer.
  7. If an external reference is to be used with single PLL mode, provide a 3-V p-p maximum,500-MHz maximum clock to SMA J11. Set JP5 to pins 2-3, and install R70 and R72.
- TSW3085EVM jumpers: ensure that the following jumpers are at their default setting.
  1. SJP2, SJP4-7 on pins (2,3)
  2. SJP3 on pins (1,2)
  3. JP1-5 on pins (1,2)

3.3 TSW3100 Quick-Start Operation

See the TSW3100 user's guide (SLLU101) for more detailed explanations of the TSW3100 setup and operation. This document assumes that the TSW3100 software is installed and functioning properly. This information can be found at http://focus.ti.com/docs/toolsw/folders/print/tsw3100evm.html. The TSW3085 needs TSW3100 operating software version 2.5 or higher with TSW3100 board Rev D (or higher).

Start the TSW3100_CommsSignalPattern Software.

Do the following steps to set up the TSW3100 for a default configuration (WCDMA) test case.

- Change the default Interpolation value from 96 to 80 (DAC sample rate / Interpolation / chip rate, **i.e., 614.4 / 2/ 3.84 = 80)**
- Set Offset Frequency to a an appropriate value. For this test case, use 30-MHz for Carrier 1.
- All other settings must be selected as shown in Figure 10.
- Press the green Create button

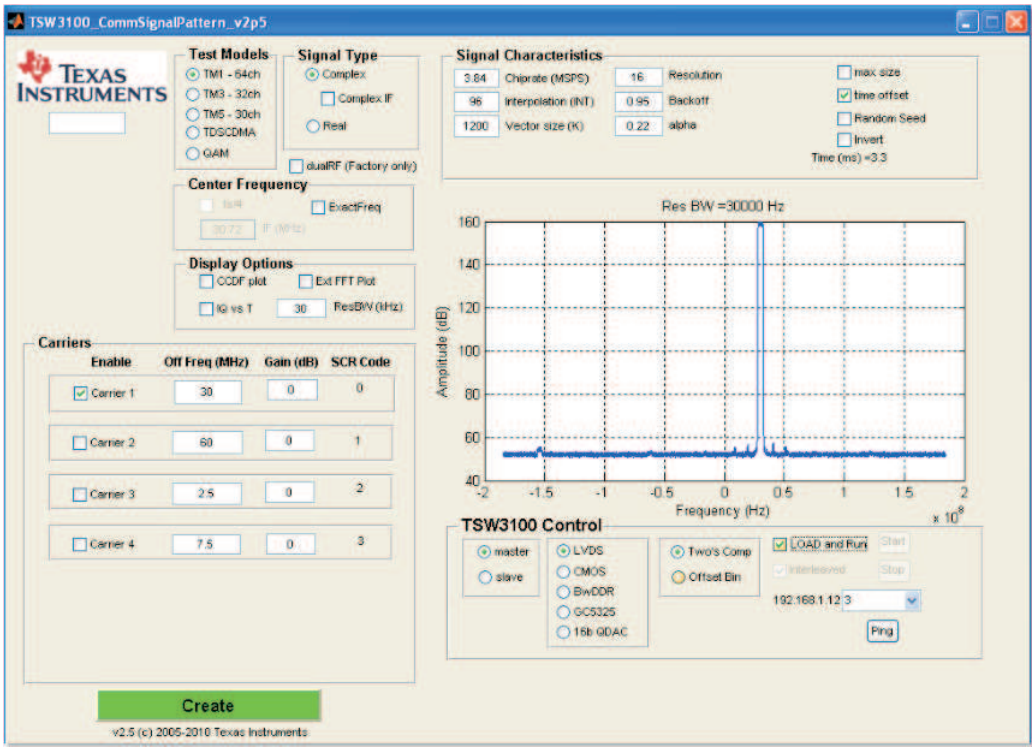

Figure 10. TSW3100 CommsSignalPattern (WCDMA) Programming GUI

3.4 TSW3085 Software Quick-Start Guide

- Turn on power to both boards, and press the reset button SW1 on the TSW3085EVM.
- Press the Reset USB Port button in the GUI, and verify USB communication.
- Switch to the INPUT tab of the GUI.
- Click on *LOAD REGS*, browse to the TSW3085 installation folder, and load example file *config1.txt*. This file contains settings for 2x interpolation with the DAC3482 running at 614.4 MSPS. Load this file, and wait a couple of seconds for the settings to go into effect.
- Click on *Send All* to write all of the values to the devices. If the devices were programmed properly, Lock LED D6 is now illuminated and SMA J5 has a clock present operating at 24.567 MHz. The updated register configuration for the LMK04806B now appears as shown in Figure 11.
- Verify the spectrum using a spectrum analyzer at the RF output of the TSW3085EVM (J7) is as shown in Figure 12.
- **(Toggle the SIF SYNC button to synchronize the appropriate digital blocks if the NCO setting is used.)**

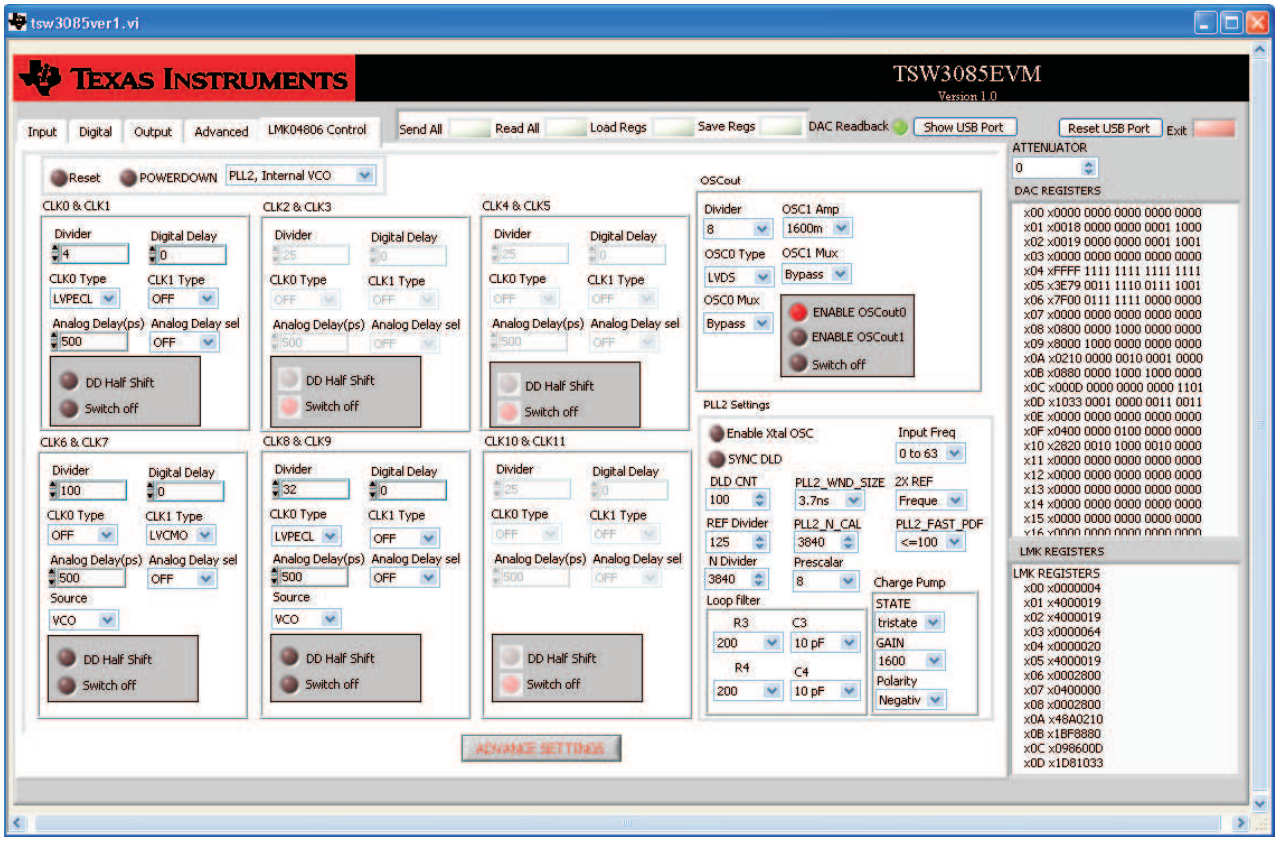

Figure 11. LMK04806B Test Case Register Configuration

4 Optional Configuration

4.1 Configuring the LMK0480x for Dual PLL Mode.

The TSW3085EVM has an option to operate the LMK04806B in Dual PLL mode. To use this mode, the following steps must be made to the EVM:

- Replace oscillator Y1 with a VCXO, such as a FVXO-HC73 series 3.3V VCXO from Fox.
- Install R273, R274, R76, C116, and C122.
- Provide an external reference at SMA J12.

Consult the LMK0480x data sheet for proper device configuration for this mode of operation.

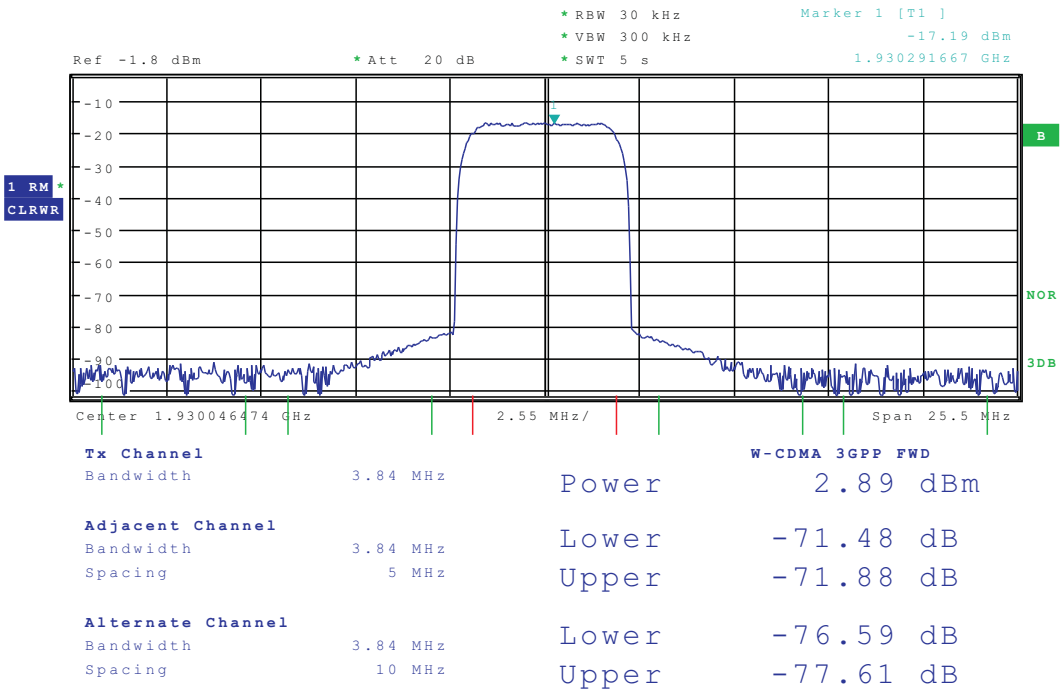

Figure 12. TSW3085EVM RF Output

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 5.5 V to 7 V and the output voltage range of 0 V to 3.3 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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