REF

NOTE: This chapter is an excerpt from the *MSP430x5xx and MSP430x6xx Family User's Guide*. The latest version of the full user's guide can be downloaded from http://www.ti.com/lit/pdf/slau208.

The REF module is a general-purpose reference system that generates voltage references required for other subsystems on a given device such as digital-to-analog converters, analog-to-digital converters, or comparators. This chapter describes the REF module.

Topic **Page**

1.1 REF Introduction

The reference module (REF) generates all critical reference voltages that can be used by various analog peripherals in a given device. These include, but are not necessarily limited to, the ADC10_A, ADC12_A, CTSD16, DAC12_A, LCD_B, and COMP_B modules (availability of a given module depends on the particular device). The heart of the reference system is the bandgap from which all other references are derived by unity or noninverting gain stages. The REFGEN subsystem consists of the bandgap, the bandgap bias, and the noninverting buffer stage, which generates the three primary voltage reference available in the system, namely 1.5 V, 2.0 V, and 2.5 V. In addition, when enabled, a buffered bandgap voltage is also available.

Features of the REF include:

- Centralized factory-trimmed bandgap with excellent PSRR, temperature coefficient, and accuracy
- 1.5-V, 2.0-V, or 2.5-V user-selectable internal references
- Buffered bandgap voltage available to rest of system
- Power saving features
- Backward compatibility to existing reference system

Figure 1-1 shows the block diagram of the REF module in an example device with ADC12_A. Figure 1-2 shows the block diagram of the REF module in an example device with a CTSD16 module.

NOTE: For devices with the CTSD16 module, external reference V_{eREF+} cannot be applied while internal reference V_{REFBG} is being used by another module, because they share the same pin, and contention on the signal line will occur. Therefore, if the external reference is used, make sure that no modules request the internal reference V_{REFBG}.

Devices with ADC10_A might not include the reference voltage output to an external pin. Refer to the device-specific data sheet.

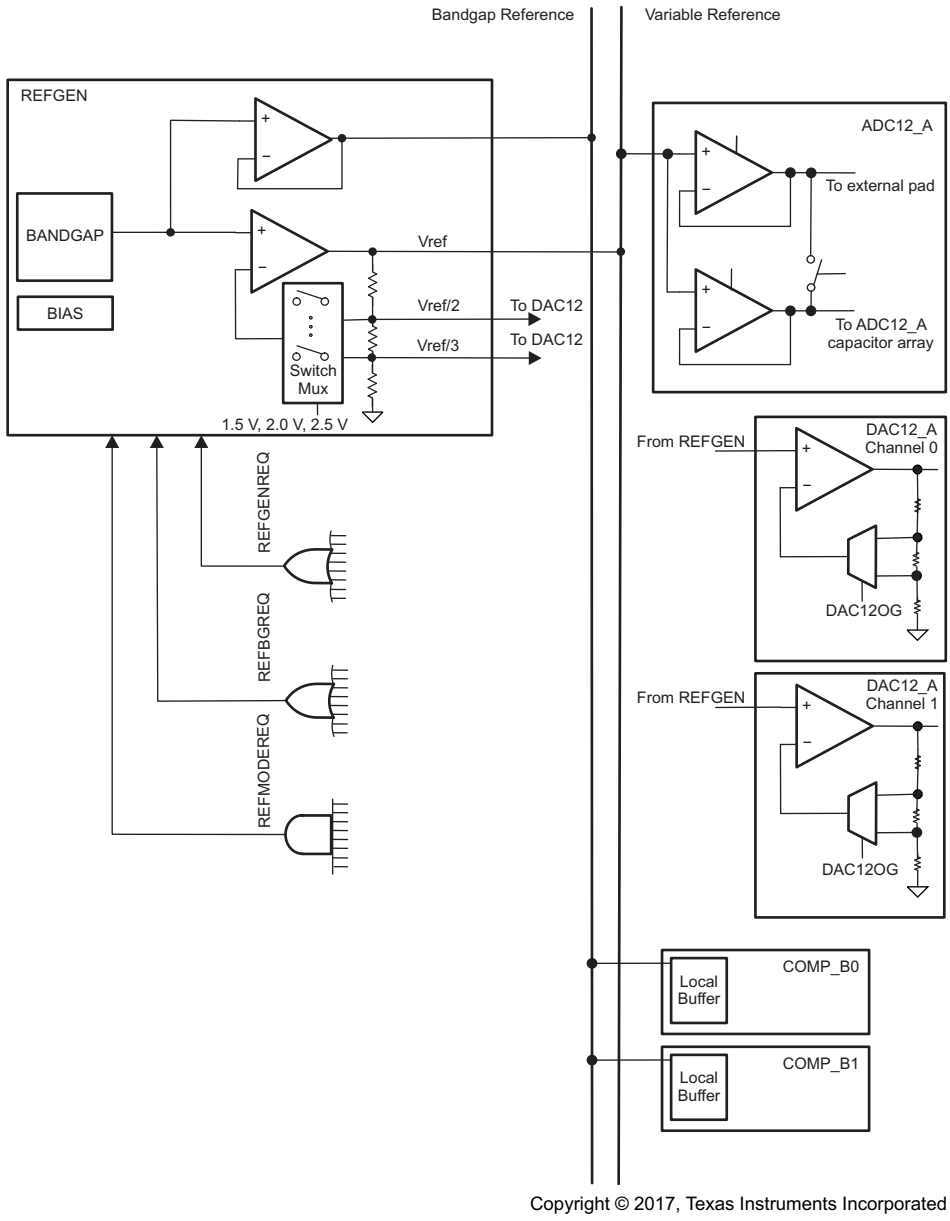

Figure 1-1. REF Block Diagram

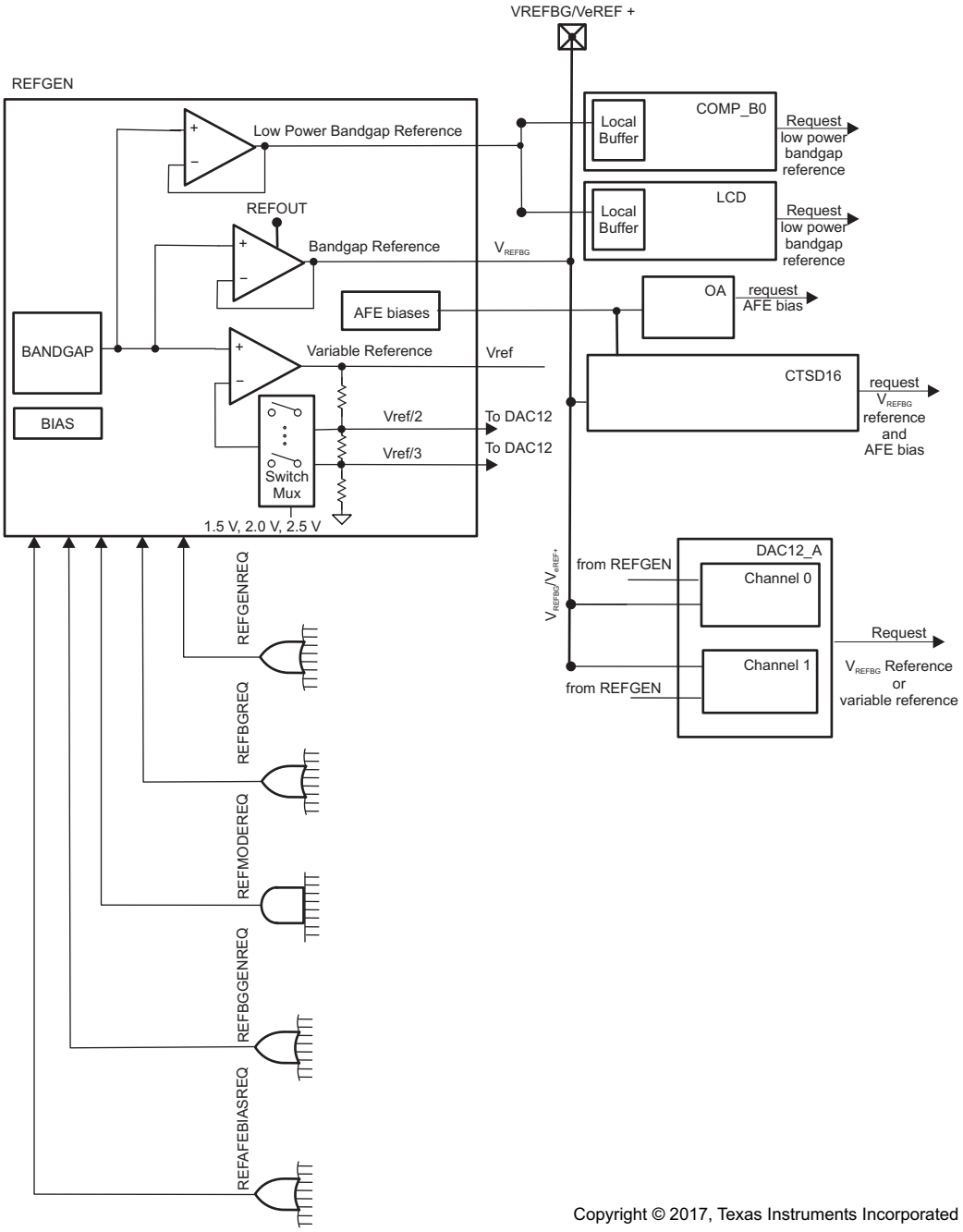

Figure 1-2. REF Block Diagram for Devices With a CTSD16 Module

1.2 Principle of Operation

The REF module provides all of the necessary voltage references to be used by various peripheral modules throughout the system. These peripherals include but are not limited to the ADC10_A, ADC12_A, CTSD16, DAC12_A, LCD_B, and COMP_B.

The REFGEN subsystem contains a high-performance bandgap. This bandgap has very good accuracy (factory trimmed), low temperature coefficient, and high PSRR even while operating at low power. The bandgap voltage is used to generate three voltages (1.5 V, 2.0 V, and 2.5 V) through a noninverting amplifier stage. One voltage can be selected at a time.

One output of the REFGEN subsystem is the variable reference line. The variable reference line provides either 1.5 V, 2.0 V, or 2.5 V to the rest of the system.

A second output of the REFGEN subsystem provides a buffered bandgap reference line that can also be used by modules throughout the system. Devices with a CTSD16 module have a second buffered bandgap reference line, V_{REFBG}, which is available internally as well as external to the device (refer to the device-specific data sheet for PxSEL.y bit requirements).

Additionally, the REFGEN supports the voltage references required for the DAC12_A module, when available. Lastly, the REFGEN subsystem also includes the temperature sensor circuitry, because it is derived from the bandgap. The temperature sensor is used by an ADC to measure a voltage proportional to temperature.

Table 1-1 describes the difference reference voltages that are available and how to enable them.

Table 1-1. Reference Voltage Generation for Different Devices(1)

REF Voltage	Voltage Available	How to Enable on Devices Without CTSD16	How to Enable On Devices With CTSD16	External Reference Input to Device (VeREF+) is Available
Low-power bandgap	Internal on request from module	Module requests it	Module requests it	Y
	Internal continuously	REFON = 1	REFON = 1	Y
V_{REF} 1.5 V, 2.0 V, 2.5 V	Internally on request from module	Module requests it, set REFVSEL as desired	DAC requests it, set REFVSEL as desired	Y
	Internally continuously	REFON = 1, set REFVSEL as desired	REFON = 1, set REFVSEL as desired	Y
	Internally and externally continuously	REFOUT = 1, set REFVSEL as desired	NA	Not when VREF and VeREF+ (external reference input to device) share a single pin
V_{REFBG}	Internally and externally, on request from module	NA	REFOUT = 1, Set PxSEL.y, and request from module V_{REFBG} is always available inside the device and on the pin. If PxSEL.y is not set, V_{REFBG} is not available inside the chip.	N(2)
	Internally and externally continuously	NA	REFON = 1, REFOUT = 1, and set PxSEL.y. V_{REFBG} is always available inside the device and on the pin. If PxSEL.y is not set, V_{REFBG} is not available inside the chip.	N(2)

(1) Refer to the block diagrams in this user's guide for each module to determine which reference voltages are available for each module.

(2) External reference V_{eREF+} cannot be applied while internal reference V_{REFBG} is being used by another module, because they share the same pin, and contention on the signal line will occur. Therefore, if the external reference is selected, make sure that no other modules are requesting internal reference V_{REFBG}. V_{eREF+} is available when V_{REFBG} is not enabled.

1.2.1 Low-Power Operation

The REF module supports low-power applications such as LCD generation. Many of these applications do not require a very accurate reference, compared to data conversion, yet power is of prime concern. To support these kinds of applications, the bandgap can be used in a sampled mode. In sampled mode, the bandgap circuitry is clocked by the VLO at an appropriate duty cycle. This reduces the average power of the bandgap circuitry significantly, at the cost of accuracy. When not in sampled mode, the bandgap is in static mode. Its power is at its highest, but so is its accuracy.

Modules automatically can request static mode or sampled mode using their own individual request lines. In this way, the particular module determines which mode is appropriate for its proper operation and performance. If any one active module requests static mode, all other modules use static mode, even if another module requests sampled mode. In other words, static mode always has higher priority than sampled mode.

1.2.2 REFCTL

The REFCTL registers provide a way to control the reference system from one centralized set of registers. By default, REFCTL is used as the primary control of the reference system.

1.2.2.1 REFMSTR = 1

This mode is implemented in all devices with ADC10_A and CTSD16. Also all ADC12_A devices except for MSP430F5438 and MSP430F5438A support this mode.

Setting the reference master bit (REFMSTR = 1), allows the reference system to be controlled through the REFCTL register. This is the default setting.

Devices with ADC12_A: In this mode (REFMSTR = 1), the legacy control bits inside the ADC register set (ADC12REFON, ADC12REF2_5V, ADC12TCOFF, and ADC12REFOUT) are don't care. The ADC12SR and ADC12REFBURST are still controlled through the ADC12_A, because these are very specific to the ADC12_A module. If REFMSTR is cleared, all settings in the REFCTL are don't care and the reference system is controlled completely by the legacy control bits inside the ADC12_A module.

Devices with ADC10_A: This is the only mode supported. REFMSTR must be set at all times. ADC10SR is controlled by the ADC10_A, because these are very specific to the ADC10_A module.

Devices with CTSD16: This is the only mode supported. REFMSTR must be set at all times.

Table 1-2 summarizes the REFCTL bits and their effect on the REF module for all devices except those with CTSD16. Table 1-3 summarizes the REFCTL bits and their effect on the REF module for devices with CTSD16.

Table 1-2. REF Control of Reference System (REFMSTR = 1) (Default) for Devices Without CTSD16

REF Register Setting	Function
REFON	Setting this bit enables the REFGEN subsystem, which includes the bandgap, the bandgap bias circuitry, and the 1.5-V, 2.0-V, or 2.5-V buffer. Setting this bit causes the REFGEN subsystem to remain enabled regardless of whether or not any module has requested it. Clearing this bit disables the REFGEN subsystem only when there are no pending requests for REFGEN from any module. REFON must also be set to enable the temperature sensor when required.
REFVSEL	Selects 1.5 V, 2.0 V, or 2.5 V to be present on the variable reference line when REFON = 1 or REFGEN is requested by any module.
REFOUT	Setting this bits enables the variable reference line voltage to be present external to the device through a buffer (external reference buffer).
REFTCOFF	Setting this bit disables the temperature sensor (when available) to conserve power.

Table 1-3. REF Control of Reference System (REFMSTR = 1) (Default) for Devices With CTSD16

REF Register Setting	Function
REFON	Setting this bit enables the REFGEN subsystem, which includes the bandgap, the bandgap bias circuitry, AFE biases, and the 1.5-V, 2.0-V, or 2.5-V buffer. Setting this bit causes the REFGEN subsystem to remain enabled regardless of whether or not any module has requested it. Clearing this bit disables the REFGEN subsystem only when there are no pending requests for REFGEN from any module. REFON must also be set to enable the temperature sensor when required.
REFVSEL	Selects 1.5 V, 2.0 V, or 2.5 V to be present on the variable reference line when REFON = 1.
REFOUT	Setting this bits enables the V_{REFBG} voltage to be present internally and external to the device through a buffer when REFON = 1 or a module requests V_{REFBG}.
REFTCOFF	Setting this bit disables the temperature sensor (when available) to conserve power.

1.2.2.2 REFMSTR = 0

Devices with ADC10_A: Do not support this mode. REFMSTR bit must not be cleared.

Devices with CTSD16: Do not support this mode. REFMSTR bit must not be cleared.

Devices with ADC12_A: This setting is applicable. On legacy devices, the ADC12_A provided the control bits necessary to configure the reference system, namely ADC12REFON, ADC12REF2_5V, ADC12TCOFF, ADC12REFOUT, ADC12SR, and ADC12REFBURST. The ADC12SR and ADC12REFBURST bits are very specific to the ADC12 operation and, therefore, are not included in REFCTL. All legacy control bits can still be used to configure the reference system, which allows for backward compatibility by clearing REFMSTR. In this case, the REFCTL register bits are don't care.

Table 1-4 summarizes the ADC12_A control bits and their effect on the REF module. See the ADC12_A module description for further details.

NOTE: Although the REF module supports using the ADC12_A bits as control for the reference system, it is recommended that the use of the new REFCTL register be used and older code migrated to this methodology. This allows the logical partitioning of the reference system to be separate from the ADC12_A system and forms a more natural partitioning for future products.

Table 1-4. Control of Reference System (REFMSTR = 0, ADC12_A Only)

ADC12_A Register Setting	Function
ADC12REFON	Setting this bit enables the REFGEN subsystem which includes the bandgap, the bandgap bias circuitry, and the 1.5-V, 2.0-V, or 2.5-V buffer. Setting this bit causes the REFGEN subsystem to remain enabled regardless of whether or not any module has requested it. Clearing this bit disables the REFGEN subsystem only when there are no pending requests for REFGEN from any module.
ADC12REF2_5V	Setting this bits causes 2.5 V to be present on the variable reference line when ADC12REFON = 1. Clearing this bit causes 1.5 V to be present on the variable reference line when ADC12REFON = 1.
ADC12REFOUT	Setting this bits enables the variable reference line voltage to be present external to the device through a buffer (external reference buffer).
ADC12TCOFF	Setting this bit disables the temperature sensor to conserve power.

As stated previously, the ADC12REFBURST has an effect on the reference system and can be controlled through the ADC12_A. This bit is in effect regardless of whether REFCTL or the ADC12_A is controlling the reference system. Setting ADC12REFBURST = 1 enables burst mode when REFON = 1 and REFMSTR = 1 or when ADC12REFON = 1 and REFMSTR = 0. In burst mode, the internal buffer (ADC12REFOUT = 0) or the external buffer (ADC12REFOUT = 1) is enabled only during a conversion and is disabled automatically to conserve power.

NOTE: The legacy ADC12_A bit ADC12REF2_5V only allows for selecting either 1.5 V or 2.5 V. To select 2.0 V, the REFVSEL control bits must be used (REFMSTR = 1).

1.2.3 Reference System Requests

There are three basic reference system requests that are used by the reference system. Each module can use these requests to obtain the proper response from the reference system. The three basic requests are REFGENREQ, REFBGREQ, and REFMODEREQ. No interaction is required by the user code. The modules select the proper requests automatically.

A reference request signal, REFGENREQ, is available as an input into the REFGEN subsystem. This signal represents a logical OR of individual requests coming from the various modules in the system that require a voltage reference to be available on the variable reference line. When a module requires a voltage reference, it asserts its corresponding REFGENREQ signal. When the REFGENREQ is asserted, the REFGEN subsystem is enabled. After the specified settling time, the variable reference line voltage is stable and ready for use. The REFVSEL settings determine which voltage is generated on the variable reference line.

In addition to the REFGENREQ, a second reference request signal, REFBGREQ is available. The REFBGREQ signal represents a logical OR of requests coming from the various modules that require the bandgap reference line. When the REFBGREQ is asserted, the bandgap, along with its bias circuitry and local buffer, is enabled if it is not already enabled by a prior request.

The REFMODEREQ request signal is available that configures the bandgap and its bias circuitry to operate in a sampled or static mode of operation. The REFMODEREQ signal basically represents a logical AND of individual requests coming from the various analog modules. A REFMODEREQ occurs only if a REFGENREQ or REFBGQ is also asserted by a module, otherwise it is a don't care. When REFMODEREQ = 1, the bandgap operates in sampled mode. When a module asserts its corresponding REFMODEREQ signal, it is requesting that the bandgap operate in sampled mode. Because REMODEREQ is a logical AND of all individual requests, any modules that request static mode cause the bandgap to operate in static mode. The BGMODE bit can be read as an indicator of static or sampled mode of operation.

1.2.3.1 Specifics for Devices With CTSD16

Devices with a CTSD16 module have two additional request signals.

The REFBGGENREQ signal represents a logical OR of individual requests coming from the various modules in the system that require the bandgap voltage reference V_{REFBG} to be available on the V_{REFBG}/V_{eREF+} signal line. When a module requires a bandgap voltage reference V_{REFBG}, it asserts its corresponding REFBGGENREQ signal. When the REFBGGENREQ is asserted, the REFGEN subsystem required to generate the bandgap voltage is enabled. This is different from the bandgap reference line, labeled as low-power bandgap reference in the block diagram (Figure 1-2), which is requested with the REFGENREQ.

The second request signal specific to devices with a CTSD16 module is the REFAFEBIASREQ. This signal represents a logical OR of individual requests coming from the various modules in the system that require the AFE biases. When a module requires the AFE biases, it asserts its corresponding REFAFEBIASREQ signal. When the REFAFEBIASREQ is asserted, the REFGEN subsystem required to generate the AFE biases is enabled.

1.2.3.2 REFBGACT, REFGENACT, REFGENBUSY

Any module that uses the variable reference line causes REFGENACT to be set inside the REFCTL register. This bit is read only and indicates whether the REFGEN is active or off. Similarly, the REFBGACT is active any time one or more modules is actively using the bandgap reference line and indicates whether the REFBG is active or off.

The REFGENBUSY signal is asserted to indicate that a module is using the reference and that reference settings cannot be changed. For example, during an active ADC12_A conversion, the reference voltage level should not be changed.

REFGENBUSY is asserted when any of the following are true:

- There is an active ADC12_A conversion (ADC12BUSY = 1).
- The DAC12_A is actively converting [DAC12AMPx > 1 and DAC12SREFx = 0 or on devices with CTSD16 if DAC12SREFx = {2,3} and REFOUT = 1 and REFON = 1 (or bandgap is requested)].
- The CTSD16 is actively converting (CTSD16SC = 1 and CTSD16REFS = 1).

REFGENBUSY when asserted, write protects the REFCTL register. This prevents the reference from being disabled or its level changed during any active conversion. Note that there is no such protection for the DAC12_A if the ADC12_A legacy control bits are used for the reference control. If the user changes the ADC12_A settings and the DAC12_A is using the reference, the DAC12_A conversion is affected.

1.2.3.3 ADC10_A

For devices that contain an ADC10_A module, the ADC10_A module contains only one local buffer. This buffer is required when using the internal reference voltage and must be enabled and stable prior to a conversion.

In devices without a reference output buffer, REFOUT must be written 0. Refer to the device-specific data sheet.

In devices with ADC10_A, the REFMSTR bit must be set at all times.

In devices with ADC10_A, the REFON bit must be set if the internal reference voltage is used.

1.2.3.4 ADC12_A

For devices that contain an ADC12_A module, the ADC12_A module contains two local buffers. The larger buffer can be used to drive the reference voltage, present on the variable reference line, external to the device. This buffer has larger power consumption due to a selectable burst mode as well as its need to drive larger DC loads that may be present outside the device. The large buffer is enabled continuously when REFON = 1, REFOUT = 1, and ADC12REFBURST = 0. When ADC12REFBURST = 1, the buffer is enabled only during an ADC conversion, shutting down automatically upon completion of a conversion to save power. In addition, when REFON = 1 and REFOUT = 1, the second smaller buffer is automatically disabled. In this case, the output of the large buffer is connected to the capacitor array through an internal analog switch. This ensures the same reference is used throughout the system. If REFON = 1 and REFOUT = 0, the internal buffer is used for ADC conversion and the large buffer remains disabled. The small internal buffer can operate in burst mode as well by setting ADC12REFBURST = 1.

1.2.3.5 CTSD16

For devices that contain a CTSD16 module, the V_{REFBG} signal is driven external to the device even if it is only used internally and requires that PxSEL.y bit = 1. If PxSEL.y is not set, V_{REFBG} is not driven even internal to the chip. The V_{REFBG} signal is enabled continuously when REFON = 1 and REFOUT = 1. The CTSD16 module only requests V_{REFBG} during active conversions, when CTSD16SC = 1, and bursts the V_{REFBG} signal unless REFON = 1 and REFOUT = 1. The DAC12_A similarly bursts the request for the voltage.

1.2.3.6 DAC12_A

Some devices contain a DAC12_A module. The DAC12_A can use the 1.5 V, 2.0 V, or 2.5 V from the variable reference line, and on devices with a CTSD16 module, the DAC12_A can use the 1.16 V from the V_{REFBG} reference line for its reference. The DAC12_A can request its reference directly by the settings within the DAC12_A module itself except the 1.16 V, which also requires REFOUT = 1. Therefore, if the DAC is enabled and the internal reference is selected, the DAC requests the reference voltage from the REF module. In addition, setting REFON = 1 (REFMSTR = 1) or ADC12REFON = 1 (REFMSTR = 0) can enable the variable reference line independent of the DAC12_A control bits.

The REFGEN subsystem provides divided versions of the variable reference line for use in the DAC12_A module. The DAC12_A module requires either /2 or /3 of the variable reference. The selection of these depends on the control bits inside the DAC12_A module (DAC12IR, DAC12OG) and is handled automatically by the REF module.

When the DAC12_A selects AV_{cc} or V_{eREF+} or V_{REFBG} (if available) as its reference, the DAC12_A has its own /2 and /3 resistor string available that scales the input reference appropriately based on the DAC12IR and DAC12OG settings.

1.2.3.7 LCD_B, LCD_C

In devices that contain an LCD module, the LCD module requires a reference to generate the proper LCD voltages. The bandgap reference line from the REFGEN subsystem is used for this purpose. The LCD is enabled when LCDON = 1 of the LCD_B or LCD_C module. This causes a REFBGREQ from the LCD module to be asserted. The buffered bandgap is available on the bandgap reference line for use by the LCD module.

1.3 REF Registers

The REF registers are listed in Table 1-5. The base address can be found in the device specific datasheet. The address offset is listed in Table 1-5.

NOTE: All registers have word or byte register access. For a generic register *ANYREG*, the suffix "_L" (*ANYREG_L*) refers to the lower byte of the register (bits 0 through 7). The suffix "_H" (*ANYREG_H*) refers to the upper byte of the register (bits 8 through 15).

Table 1-5. REF Registers

Offset	Acronym	Register Name	Type	Access	Reset	Section
00h	REFCTL0	REF Control Register 0	Read/write	Word	0080h	Section 1.3.1
00h	REFCTL0_L		Read/write	Byte	80h	
01h	REFCTL0_H		Read/write	Byte	00h	

1.3.1 REFCTL0 Register (offset = 00h) [reset = 0080h]

REF Control Register 0

Figure 1-3. REFCTL0 Register

15	14	13	12	11	10	9	8
Reserved				BGMODE	REFGENBUSY	REFBGACT	REFGENACT
r0	r0	r0	r0	r-(0)	r-(0)	r-(0)	r-(0)
7	6	5	4	3	2	1	0
REFMSTR	Reserved	REFVSEL		REFTCOFF	Reserved	REFOUT	REFON
rw-(1)	r0	rw-(0)	rw-(0)	rw-(0)	r0	rw-(0)	rw-(0)

Can be modified only when REFGENBUSY = 0.

Table 1-6. REFCTL0 Register Description

Bit	Field	Type	Reset	Description
15-12	Reserved	R	0h	Reserved. Always reads as 0.
11	BGMODE	R	0h	Bandgap mode. Read only. 0b = Static mode 1b = Sampled mode
10	REFGENBUSY	R	0h	Reference generator busy. Read only. 0b = Reference generator not busy 1b = Reference generator busy
9	REFBGACT	R	0h	Reference bandgap active. Read only. 0b = Reference bandgap buffer not active 1b = Reference bandgap buffer active
8	REFGENACT	R	0h	Reference generator active. Read only. 0b = Reference generator not active 1b = Reference generator active
7	REFMSTR	RW	1h	REF master control. ADC10_A and CTSD16 devices: Must be written 1. 0b = Reference system controlled by legacy control bits inside the ADC12_A module when available. 1b = Reference system controlled by REFCTL register. Common settings inside the ADC12_A module (if exists) are don't care.
6	Reserved	R	0h	Reserved. Always reads as 0.
5-4	REFVSEL	RW	0h	Reference voltage level select for devices 00b = 1.5 V available when reference requested or REFON = 1 01b = 2.0 V available when reference requested or REFON = 1 10b = 2.5 V available when reference requested or REFON = 1 11b = 2.5 V available when reference requested or REFON = 1
3	REFTCOFF	RW	0h	Temperature sensor disabled 0b = Temperature sensor enabled 1b = Temperature sensor disabled to save power
2	Reserved	R	0h	Reserved. Always reads as 0.
1	REFOUT	RW	0h	Reference output buffer. ADC10_A devices without reference output buffer: Must be written 0. 0b = Reference output not available externally 1b = Reference output available externally. If ADC12REFBURST = 0, or DAC12_A is enabled, output is available continuously. If ADC12REFBURST = 1, output is available only during an ADC12_A conversion. For devices with CTSD16, REFON must also be set to 1 for V_{REFBG} to be available continuously. Otherwise, V_{REFBG} is only available externally when a module requests it.

Table 1-6. REFCTL0 Register Description (continued)

Bit	Field	Type	Reset	Description
0	REFON	RW	0h	Reference enable. ADC10_A: The ADC10_A does not support the reference request. REFON must be set if the internal reference voltage is used. 0b = Disables reference if no other reference requests are pending. 1b = Enables reference.

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