CTSD16

NOTE: This chapter is an excerpt from the *MSP430x5xx and MSP430x6xx Family User's Guide*. The most recent version of the full user's guide is available from http://www.ti.com/lit/pdf/slau208.

The CTSD16 is a multiple-input multiple-converter sigma-delta analog-to-digital conversion module. This chapter describes the operation of the CTSD16 module.

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1.1 CTSD16 Introduction

The CTSD16 module consists of up to seven independent sigma-delta analog-to-digital converters, referred to as channels. The converters are based on second-order oversampling sigma-delta modulators and digital decimation filters. The decimation filters are comb-type filters with selectable oversampling ratios of up to 256. Additional filtering can be done in software.

Features of the CTSD16 include:

- Second-order sigma-delta architecture
- Up to seven independent simultaneously-sampling ADCs (the number of channels is device dependent, see the device-specific data sheet)
- Up to six single-ended external analog inputs, up to four differential or single-ended external analog inputs (which can also be configured as single-ended), internal temperature sense input, internal AVCC sense input, internal VBAT sense, and internal shorted differential inputs to V_{REFBG}/V_{eREF+} signal or DAC0 output per channel (the number of inputs is device dependent, see the device-specific data sheet)
- Fixed 1.024-MHz modulator input frequency
- Software-selectable internal or external voltage reference
- Software-selectable AVCC sense, VBAT sense, and temperature sensor accessible by all channels

Figure 1-1 shows the block diagram of the CTSD16 module.

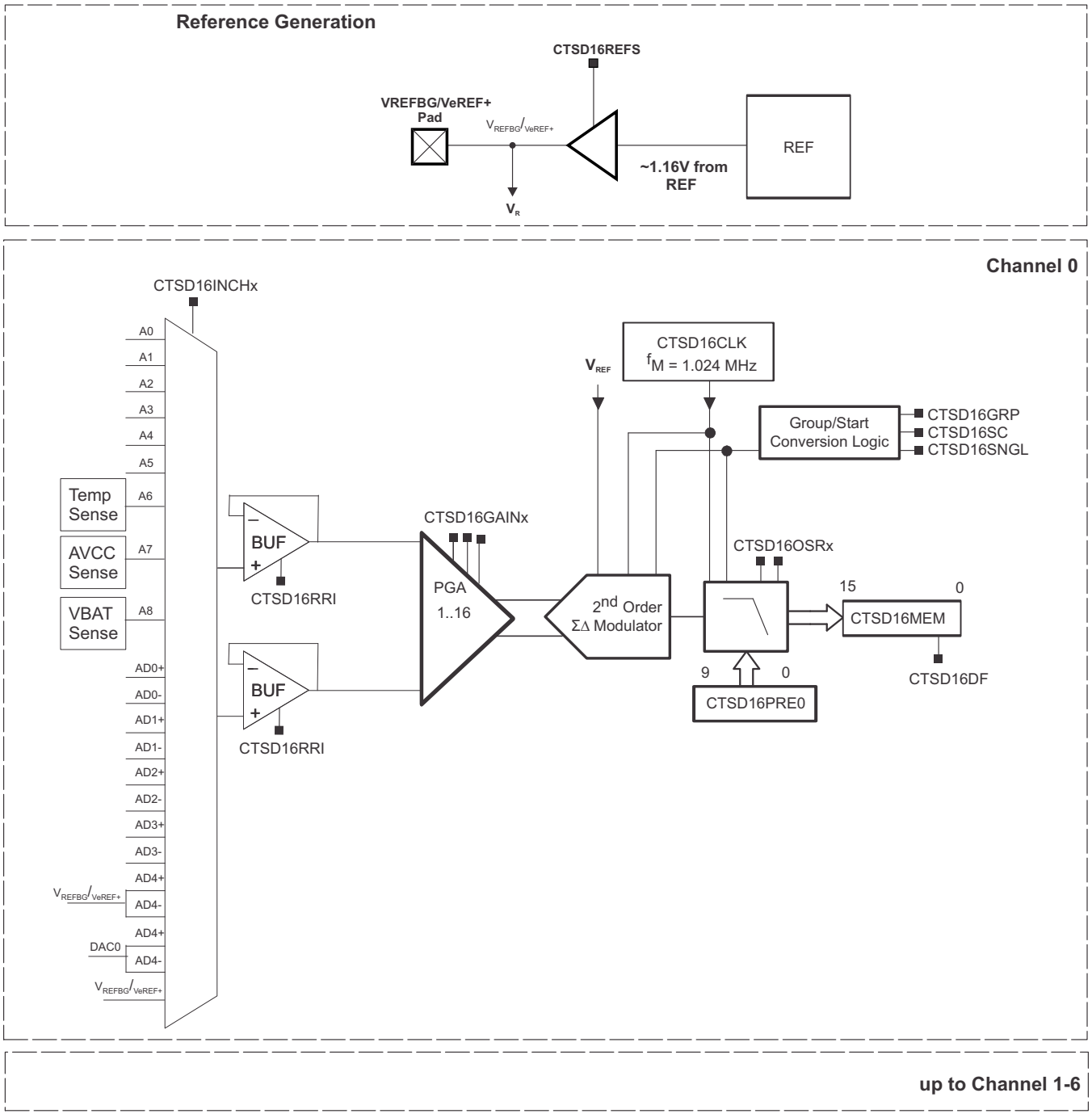

Figure 1-1. CTSD16 Block Diagram

1.2 CTSD16 Operation

The CTSD16 module is configured with user software. The following sections describe the setup and operation of the CTSD16.

1.2.1 Principle of Operation

A sigma-delta analog-to-digital converter consists of two parts: the analog part (called the modulator) and the digital part (called the decimation filter). The modulator of the CTSD16 provides a bitstream of zeros and ones to the digital decimation filter. The digital filter averages the bitstream from the modulator over a given number of bits (specified by the oversampling rate) and provides samples at a reduced rate for further processing to the CPU.

Averaging can be used to increase the signal-to-noise performance of a conversion [see Figure 1-2 a) and b)]. With a conventional ADC, each factor-of-4 oversampling improves the SNR by approximately 6 dB or 1 bit. To achieve a 16-bit resolution out of a simple 1-bit ADC would require an impractical oversampling rate of 4^{15} = 1 073 741 824. To overcome this limitation, the sigma-delta modulator implements a technique called noise shaping. Due to a feedback loop and integrators, the quantization noise is pushed to higher frequencies, and thus much lower oversampling rates are sufficient to achieve high resolutions [see Figure 1-2 c)].

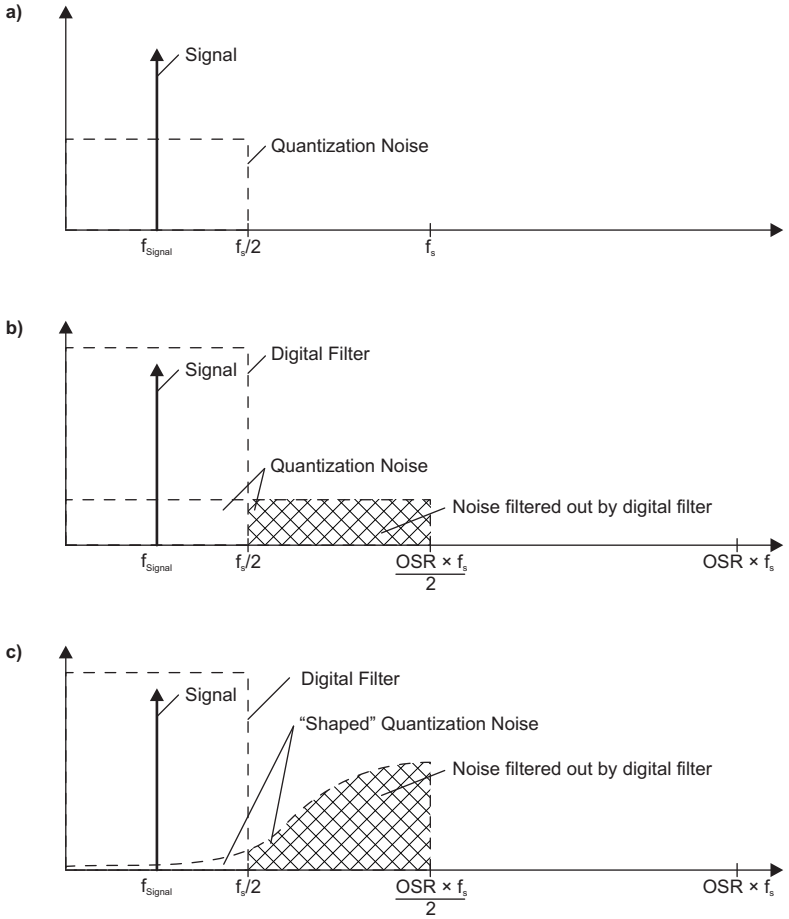

Figure 1-2. Sigma-Delta Principle

1.2.2 ADC Core

The analog-to-digital conversion is performed by a 1-bit second-order sigma-delta modulator. A single-bit comparator within the modulator quantizes the input signal with the modulator frequency f_M. The resulting 1-bit data stream is averaged by the digital filter for the conversion result.

1.2.3 Voltage Reference

The CTSD16 module can use an external reference voltage with CTSD16REFS = 0 or an internal reference with CTSD16REFS = 1. CTSD16 uses the shared reference (REF) module as its internal voltage reference source and will request it when needed. REF is used for each CTSD16 channel when requested with CTSD16REFS = 1. When using the internal reference, refer to the device-specific data sheet for PxSEL.y bit requirements for the internal reference pin. Also, TI recommends using an external capacitor connected from the VREFBG pin to AVSS to reduce noise with the internal reference. See the device-specific data sheet for the capacitor value and other reference parametrics.

An external voltage reference must be applied to the VeREF+ input when CTSD16REFS = 0.

NOTE: The external reference VeREF+ cannot be applied while the internal reference V_{REFBG} is being used by another module, because VeREF+ and V_{REFBG} share the same pin, and contention on the signal line will occur. Therefore, if the user selects the external reference, care must be taken to ensure no other modules are requesting the internal reference V_{REFBG}.

Table 1-1. Voltage Reference Signal Selection Requirements

Signal Selected	REFOUT	REFON	PxSEL.y	CTSD16REFS(1)
VeREF+	0	x	1	If the CTSD16 module is used, CTSD16REFS must be set to 0.
V_{REFBG}	1	1	1(2)	If the CTSD16 module is used, CTSD16REFS must be set to 1.

(1) If the CTSD16 module is used, CTSD16REFS bit must be set according to this table.

(2) V_{REFBG} is always available inside the device and on the pin. If PxSEL.y is not set, V_{REFBG} will not be available inside the chip.

1.2.4 CTSD16 Clock

The CTSD16 clock (CTSD16CLK) generates a 1.024-MHz fixed frequency clock (f_M). This clock is supplied to all modulators so that all modulators convert synchronously. It also supplies the device charge pump used for rail-to-rail CTSD16 inputs and rail-to-rail operational amplifier (OA) operation on devices with an OA module. This is not a free running clock, and it runs only when a CTSD16 channel conversion is active or if the charge pump is on (CTSD16RRIBURST = 0 or OARRI = 1).

The CTSD16CLK has fault detection. If the CTSD16CLK detects any abnormality, then the CTSD16OFFG bit is set to 1 to indicate a CTSD16CLK fault. After it is set, the fault bit remains set until reset in software, even if the fault condition no longer exists. If the user clears the fault bit and the fault condition still exists, the fault bit is automatically set again; otherwise, it remains cleared. The fault condition is removed when CTSD16CLK is powered off. Note that if only the CTSD16 is requesting the CTSD16CLK, the clock is powered down when not actively converting to save power, so if the fault condition still exists when the CTSD16CK is powered down and the user clears the fault bit, the fault will not reappear until the CTSD16CLK is powered up again.

The CTSD16OFFG bit also sets the OFIFG bit in SFRIFG1 register, which is shared with the system oscillators fault conditions. OFIFG can source a nonmaskable interrupt to the CPU when the OFIE bit is enabled in the SFRIE1 register. CTSD16OFFG is a status bit and is set or cleared based on CTSD16CLK fault indication. OFIFG is a sticky bit that is set when CTSD16OFFG is set, and it cannot be cleared as long as CTSD16OFFG is set. When CTSD16OFFG is cleared by software, OFIFG is not cleared automatically and must be cleared by software.

1.2.5 Automatic Power Down

The CTSD16 module is designed for low-power applications. When a CTSD16 channel is not actively converting, it is automatically disabled and the CTSD16CLK request removed and automatically re-enabled when a conversion is started. When a channel is disabled, it consumes no current. If CTSD16REFS = 1, the CTSD16 module bursts the request for the V_{REFBG} signal to the REF module so it is only requested when CTSD16 is actively converting.

1.2.6 Analog Inputs

1.2.6.1 Analog Input Range and PGA

The full-scale input voltage range for each analog input pair is dependent on the gain setting of each channel. See the device-specific data sheet for full-scale input specifications.

1.2.6.2 Analog Input Pair Selection

The CTSD16 can convert up to 15 inputs multiplexed into the buffer and PGA. Up to four differential analog input pairs (AD0 to AD3) and up to six single-ended analog inputs (A0 to A5) are available externally on the device. The four differential analog input pairs (AD0 to AD3) can also be configured as single-ended with CTSD16INCHx to save an input pin if differential input is not needed. For lowest noise, differential input should be used even for single-ended signals. When any singled-ended input is selected, the positive input is the Ax input and the negative input is internally connected to the V_{REFBG}/V_{eREF+} signal. Thus, it is pseudo single-ended as only one external pin is needed but internally the full differential path is used. An internal temperature sensor is available using the A6 multiplexer input. A resistive divider to measure the supply voltage is available using the A7 multiplexer input. VBAT can be measured on the internal input A8. Inputs AD4+ and AD4- are tied together, and when CTSD16INCHx = 0x11, they are connected to the V_{REFBG}/V_{eREF+} signal. When CTSD16INCHx = 0x12, they are connected to the DAC0 output to calibrate the offset of each CTSD16 input stage. Note that the measured offset depends on the impedance of the external circuitry; thus, the actual offset seen at any of the analog inputs may be different.

1.2.6.3 Analog Input Setup

The analog input of each channel is configured using the CTSD16INCTLx register. These settings can be independently configured for each CTSD16 channel.

The gain for each PGA is selected by the CTSD16GAINx bits. A total of five gain settings are available.

During conversion, any modification of the CTSD16INCTLx register bits INTDLYx, GAINx, and INCHx becomes effective with the next decimation step of the digital filter. After these bits are modified, the next three conversions may be invalid due to the settling time of the digital filter. This can be handled automatically with the CTSD16INTDLY bit. When CTSD16INTDLY = 0b, conversion interrupt requests do not begin until the fourth conversion after a start condition. The preferred method is to modify the CTSD16INCTLx register when CTSD16 is not converting (CTSD16SC = 0).

An external RC anti-aliasing filter is recommended for the CTSD16 to prevent aliasing of the input signal. The cutoff frequency should be <10 kHz for a 1-MHz modulator clock and OSR = 256. The cutoff frequency may be set to a lower frequency for applications that have lower bandwidth requirements.

1.2.6.3.1 Rail-to-Rail Input

The input buffers allow rail-to-rail operation when CTSD16RRI = 1. Rail-to-rail operation can be useful for signals whose common mode voltage is close to the rail (see device-specific data sheet OA section V_{CM} parameter for the input range supported when CTSD16RRI (OARRI) = 0 or 1) as it allows linear operation over a wider range with the charge pump enabled at the cost of additional current. Refer to the device-specific data sheet OA section I_{CP} for the charge pump current consumption as well as other parametrics such as turnon time. For more details on rail-to-rail operation, refer to . Rail-to-rail requires a single external capacitor from the CPCAP terminal to ground for proper operation. See the data sheet for proper value and tolerances. Rail-to-rail input mode ready is indicated by CTSD16RRIRDY bit being set or refer to device-specific data sheet OA section for charge pump settle time.

Rail-to-rail input mode takes time to enable if the charge pump is not already on. CTSD16RRIRDY bit is set once rail-to-rail input is ready or refer to device-specific data sheet OA section for charge pump settle time. If power is a concern and the OA module is not in rail-to-rail input mode (OARRI = 1), the CTSD16RRIBURST bit can be set to allow the CTSD16 to only request the charge pump for rail-to-rail input mode when CTSD16 is converting.

1.2.6.4 Analog Port Selection

The CTSD16 inputs are multiplexed with digital port pins. When analog signals are applied to digital gates, parasitic current can flow from VCC to GND. This parasitic current occurs if the input voltage is near the transition level of the gate. Disabling the digital part of the port pin eliminates the parasitic current flow and, therefore, reduces overall current consumption. The PxSEL.y bits provide the ability to disable the port pin input and output buffers.

1.2.7 Digital Filter

The digital filter processes the 1-bit data stream from the modulator using a SINC^3 comb filter.

1.2.7.1 SINC^3 Filter

The structure of a SINC^3 filter is shown in Figure 1-3.

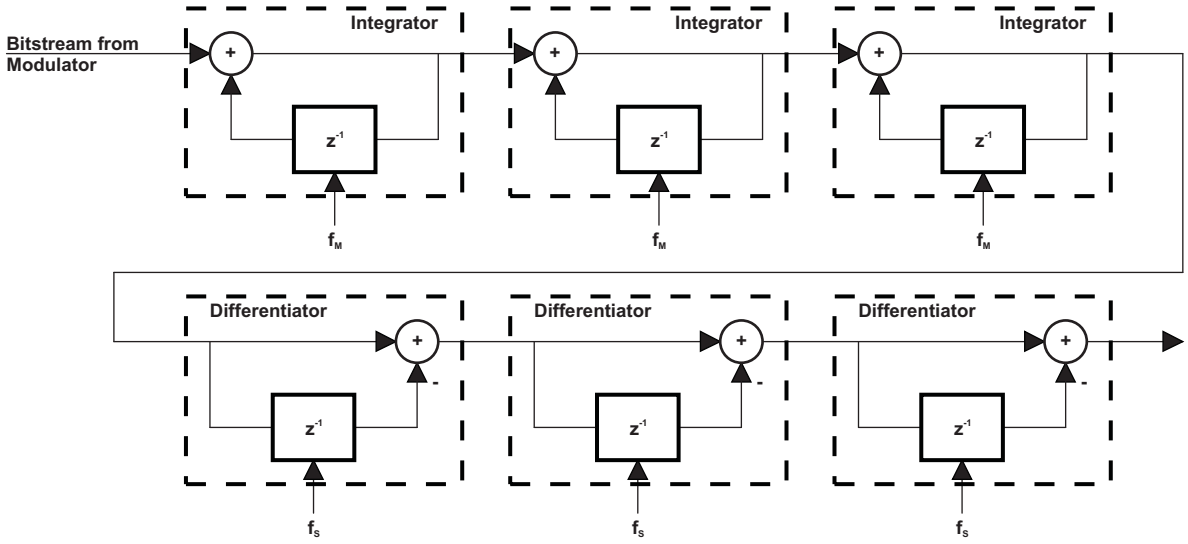

Figure 1-3. SINC^3 Filter Structure

The transfer function is described in the z-domain by:

$$H(z) = \left(\frac{1}{OSR} \times \frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3 \quad (1)$$

The transfer function is described in the frequency domain by:

$$H(f) = \left(\frac{\text{sinc}\left(OSR\pi \frac{f}{f_M} \right)}{\text{sinc}\left(\pi \frac{f}{f_M} \right)} \right)^3 = \left(\frac{1}{OSR} \times \frac{\sin\left(OSR \times \pi \times \frac{f}{f_M} \right)}{\sin\left(\pi \times \frac{f}{f_M} \right)} \right)^3 \quad (2)$$

Where the oversampling rate, OSR, is the ratio of the modulator frequency f_M to the sample frequency f_S. Figure 1-4 shows the filter's frequency response for an OSR of 32. The first filter notch is always at $f_S = f_M/OSR$. The notch's frequency can be adjusted by changing the oversampling rate using the CTSD16OSRx bits.

The digital filter for each enabled ADC channel completes the decimation of the digital bitstream and outputs new conversion results to the corresponding CTSD16MEMx register at the sample frequency f_S.

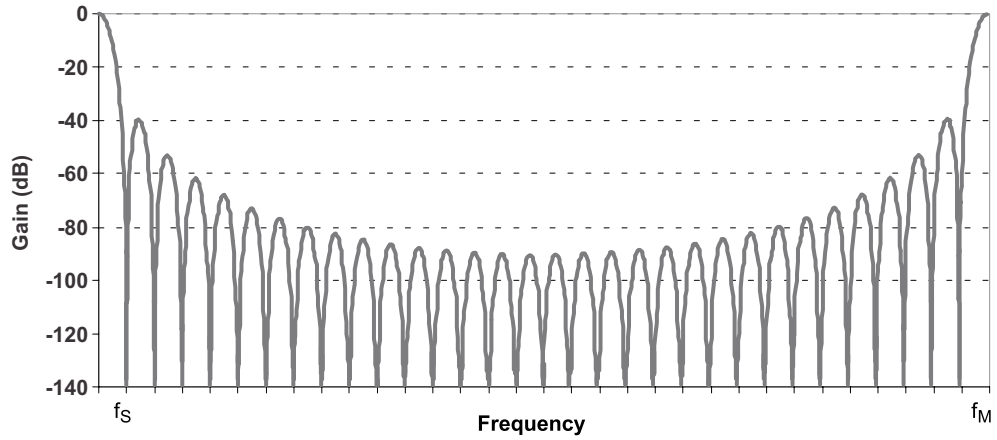

Figure 1-4. Comb Filter Frequency Response With OSR = 32

Figure 1-5 shows the digital filter step response and conversion points. For step changes at the input after start of conversion, a settling time must be allowed before a valid conversion result is available. The CTSD16INTDLY bit can provide sufficient filter settling time for a full-scale change at the ADC input. If the step occurs synchronously to the decimation of the digital filter, the valid data is available on the third conversion. An asynchronous step requires one additional conversion before valid data is available.

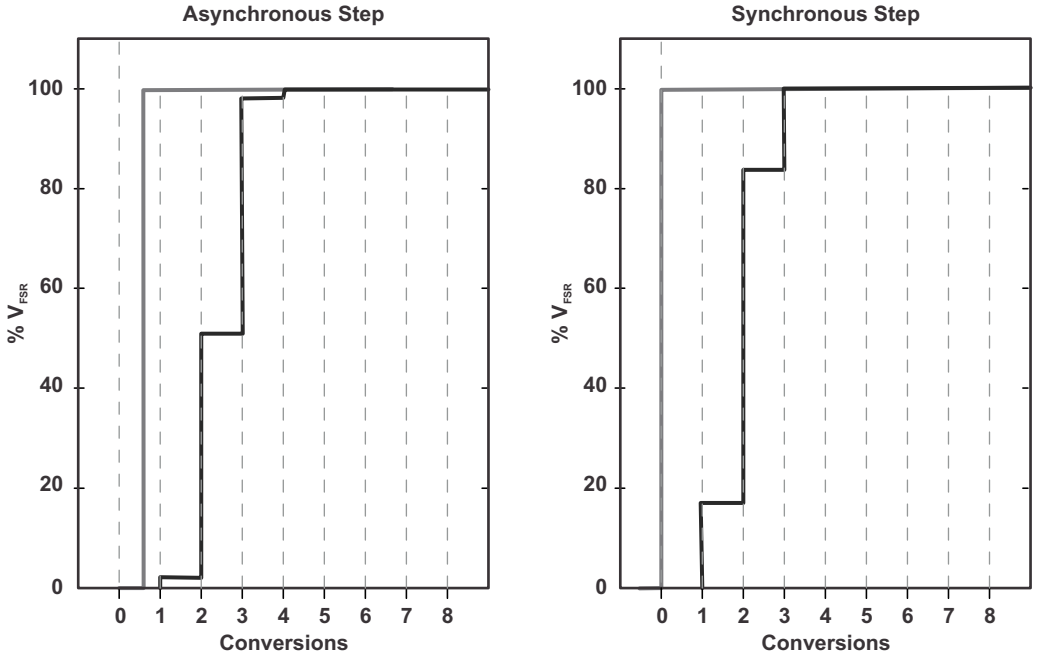

Figure 1-5. Digital Filter Step Response and Conversion Points Digital Filter Output

1.2.7.2 Digital Filter Output

The number of bits output by each digital filter is dependent on the oversampling ratio and ranges from 16 to 24 bits. Figure 1-6 shows the digital filter output bits and their relation to CTSD16MEMx for each OSR. For example, for OSR = 256 and LSBACC = 0, the CTSD16MEMx register contains bits 23-8 of the digital filter output. When OSR = 32, the CTSD16MEMx LSB is always zero.

The CTSD16LSBACC and CTSD16LSBTOG bits give access to the least significant bits of the digital filter output. When CTSD16LSBACC = 1 the 16 least significant bits of the digital filter's output are read from CTSD16MEMx using word instructions. The CTSD16MEMx register can also be accessed with byte instructions returning only the 8 least significant bits of the digital filter output.

When CTSD16LSBTOG = 1 the CTSD16LSBACC bit is automatically toggled each time the corresponding channel's CTSD16MEMx register is read. This allows the complete digital filter output result to be read with two read accesses of CTSD16MEMx. Setting or clearing CTSD16LSBTOG does not change CTSD16LSBACC until the next CTSD16MEMx access.

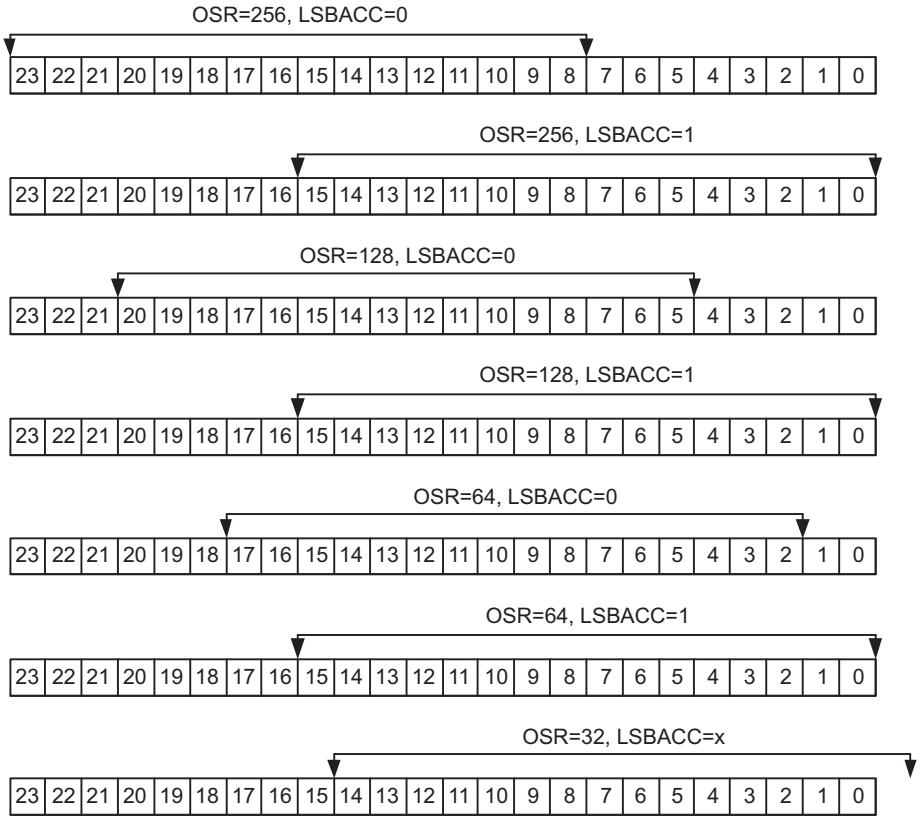

Figure 1-6. Used Bits of Digital Filter Output

1.2.8 Conversion Memory Registers: CTSD16MEMx

One CTSD16MEMx register is associated with each CTSD16 channel. Conversion results for each channel are moved to the corresponding CTSD16MEMx register with each decimation step of the digital filter. The CTSD16IFG bit for a given channel is set when new data is written to CTSD16MEMx. CTSD16IFG is automatically cleared when CTSD16MEMx is read by the CPU or may be cleared with software.

1.2.8.1 Output Data Format

The output data format is configurable in twos complement or offset binary as shown in Table 1-2. The data format is selected by the CTSD16DF bit.

Table 1-2. Data Format

CTSD16DF	Format	Analog Input	CTSD16MEMx(1)	Digital Filter Output (OSR = 256)
0	Offset binary	+FSR	FFFF	FFFFFF
		ZERO	8000	800000
		-FSR	0000	000000
1	Twos complement	+FSR	7FFF	7FFFFF
		ZERO	0000	000000
		-FSR	8000	800000

(1) Independent of SD24OSRx setting; SD24LSBACC = 0

Figure 1-7 shows the relationship between the full-scale input voltage range from $-V_{FSR}$ to $+V_{FSR}$ and the conversion result, including the digital values for both data formats.

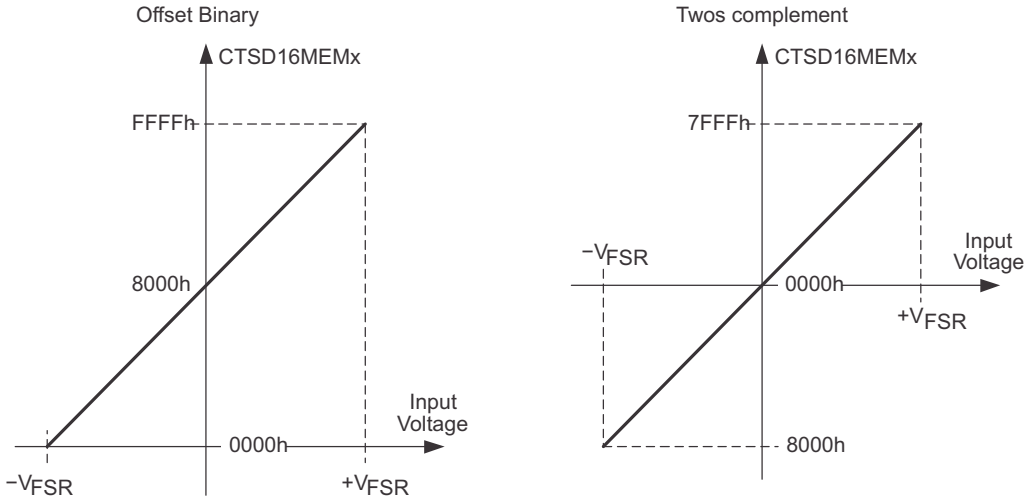

Figure 1-7. Input Voltage vs Digital Output

1.2.9 Conversion Modes

The CTSD16 module can be configured for four modes of operation (see Table 1-3). The CTSD16SNGL and CTSD16GRP bits for each channel select the conversion mode.

Table 1-3. Conversion Mode Summary

CTSD16SNGL	CTSD16GRP[(1)]	Mode	Operation
1	0	Single channel, single conversion	A single channel is converted once.
0	0	Single channel, continuous conversion	A single channel is converted continuously.
1	1	Group of channels, single conversion	A group of channels is converted once.
0	1	Group of channels, continuous conversion	A group of channels is converted continuously.

(1) A channel is grouped and is the master channel of the group when CTSD16GRP = 0 if CTSD16GRP for the prior channel is set.

1.2.9.1 Single Channel, Single Conversion

Setting the CTSD16SC bit of a channel initiates one conversion on that channel when CTSD16SNGL = 1 and it is not grouped with any other channels. The CTSD16SC bit is automatically cleared after conversion is complete.

Clearing CTSD16SC before the conversion is completed immediately stops conversion of the selected channel, powers down the channel, and turns off the corresponding digital filter. The value in CTSD16MEMx can change when CTSD16SC is cleared. TI recommends reading the conversion data in CTSD16MEMx before clearing CTSD16SC to avoid reading an invalid result.

1.2.9.2 Single Channel, Continuous Conversion

When CTSD16SNGL = 0, continuous conversion mode is selected. Conversion of the selected channel begins when CTSD16SC is set and continues until the CTSD16SC bit is cleared by software when the channel is not grouped with any other channel.

Clearing CTSD16SC immediately stops conversion of the selected channel, powers down the channel, and turns off the corresponding digital filter. The value in CTSD16MEMx can change when CTSD16SC is cleared. TI recommends reading the conversion data in CTSD16MEMx before clearing CTSD16SC to avoid reading an invalid result.

Figure 1-8 shows single channel operation for single conversion mode and continuous conversion mode.

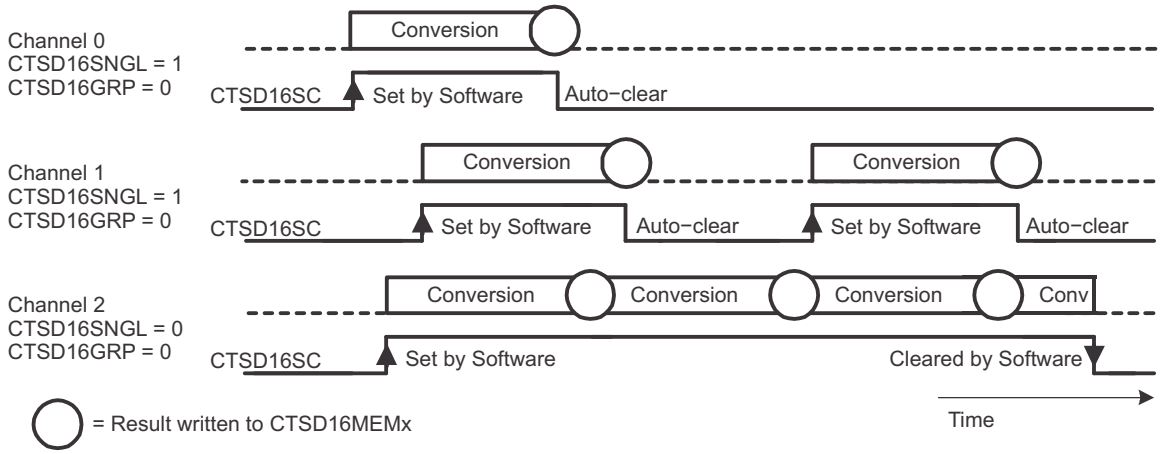

Figure 1-8. Single Channel Operation Example

1.2.9.3 Group of Channels, Single Conversion

Consecutive CTSD16 channels can be grouped together with the CTSD16GRP bit to synchronize conversions. Setting CTSD16GRP for a channel groups that channel with the next channel in the module. For example, setting CTSD16GRP for channel 0 groups that channel with channel 1. In this case, channel 1 is the master channel, enabling and disabling conversion of all channels in the group with its CTSD16SC bit. The CTSD16GRP bit of the master channel is always 0. The CTSD16GRP bit of last channel in CTSD16 has no function and is always 0.

When CTSD16SNGL = 1 for a channel in a group, single conversion mode is selected. A single conversion of that channel will occur synchronously when the master channel CTSD16SC bit is set. The CTSD16SC bit of all channels in the group will automatically be set and cleared by CTSD16SC of the master channel. CTSD16SC for each channel can also be cleared in software independently.

Clearing CTSD16SC of the master channel before the conversions are completed immediately stops conversions of all channels in the group, powers down the channels, and turns off the corresponding digital filters. Values in CTSD16MEMx can change when CTSD16SC is cleared. TI recommends reading the conversion data in CTSD16MEMx before clearing CTSD16SC to avoid reading an invalid result.

1.2.9.4 Group of Channels, Continuous Conversion

When CTSD16SNGL = 0 for a channel in a group, continuous conversion mode is selected. Continuous conversion of that channel occurs synchronously when the master channel CTSD16SC bit is set. CTSD16SC bits for all grouped channels are automatically set and cleared with the master channel's CTSD16SC bit. CTSD16SC for each channel in the group can also be cleared in software independently.

When CTSD16SC of a grouped channel is set by software independently of the master, conversion of that channel automatically synchronizes to conversions of the master channel. This ensures that conversions for grouped channels are always synchronous to the master.

Clearing CTSD16SC of the master channel immediately stops conversions of all channels in the group, powers down the channels, and turns off the corresponding digital filters. Values in CTSD16MEMx can change when CTSD16SC is cleared. TI recommends reading the conversion data in CTSD16MEMx before clearing CTSD16SC to avoid reading an invalid result.

Figure 1-9 shows grouped channel operation for three CTSD16 channels. Channel 0 is configured for single conversion mode, CTSD16SNGL = 1, and channels 1 and 2 are in continuous conversion mode, CTSD16SNGL = 0. Channel two, the last channel in the group, is the master channel. Conversions of all channels in the group occur synchronously to the master channel regardless of when each CTSD16SC bit is set using software.

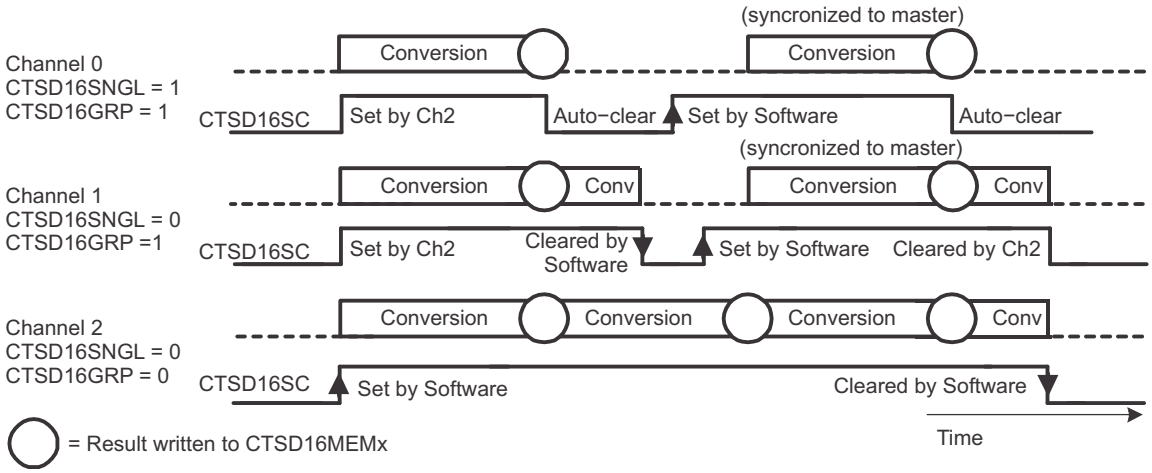

Figure 1-9. Grouped Channel Operation Example

1.2.10 Conversion Operation Using Preload

The CTSD16PREx register is used to determine a delay based on start-up time requirements and, when multiple channels are grouped, the CTSD16PREx registers can be used to delay the conversion time frame for each channel. Using CTSD16PREx, the decimation time of the digital filter is delayed by the specified number of f_M clock cycles and can range from 0 to 1023. Figure 1-10 shows an example using CTSD16PREx.

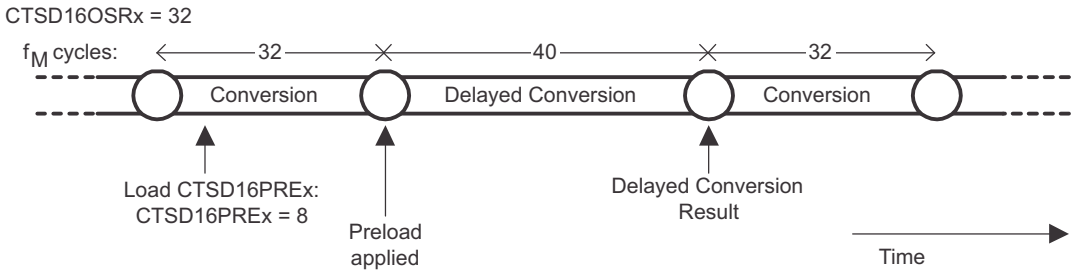

Figure 1-10. Conversion Delay Using Preload Example

The CTSD16PREx delay is applied to the beginning of the next conversion cycle after being written. The delay is used on the first conversion after CTSD16SC is set and on the conversion cycle following each write to CTSD16PREx. Following conversions are not delayed. After modifying CTSD16PREx, the next write to CTSD16PREx should not occur until the next conversion cycle is completed, otherwise the conversion results may be incorrect.

The accuracy of the result for the delayed conversion cycle using CTSD16PREx is dependent on the length of the delay and the frequency of the analog signal being sampled. For example, when measuring a DC signal, if there is no start-up time required (see the CTSD16PREx register PreloadValue bit description for details), CTSD16PREx delay has no effect on the conversion result regardless of the duration. The user must determine when the delayed conversion result is useful in their application.

Figure 1-11 shows the operation of grouped channels 0 and 1. The preload register of channel 1 is loaded with zero, resulting in immediate conversion. The conversion cycle of channel 0 is delayed by setting CTSD16PRE0 = 8. The first channel 0 conversion uses CTSD16PREx = 8, shifting all subsequent conversions by 8 f_M clock cycles.

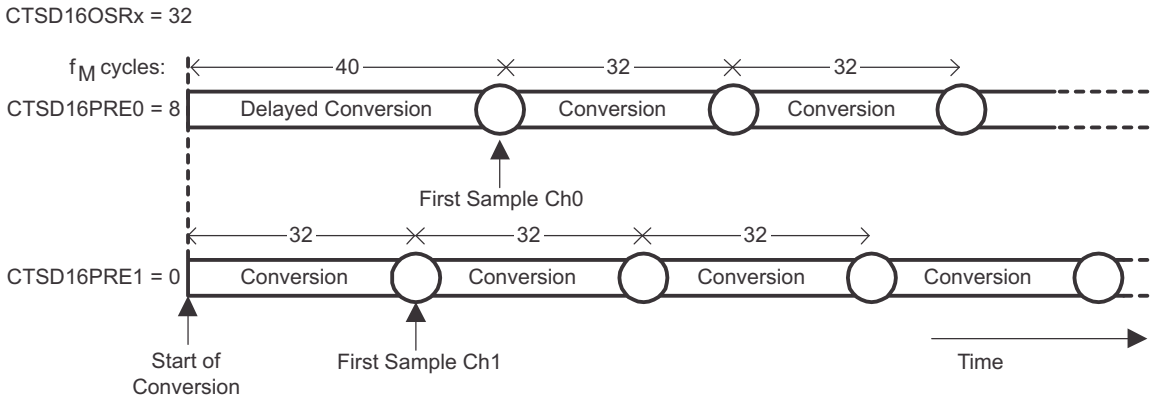

Figure 1-11. Start of Conversion Using Preload Example

When channels are grouped, care must be taken when a channel or channels operate in single conversion mode or are disabled in software while the master channel remains active. Each time channels in the group are re-enabled and resynchronized with the master channel, the preload delay for that channel is reintroduced. Figure 1-12 shows the resynchronization and preload delays for channels in a group. It is recommended that CTSD16PREx = 0 for the master channel to maintain a consistent delay between the master and remaining channels in the group when they are re-enabled.

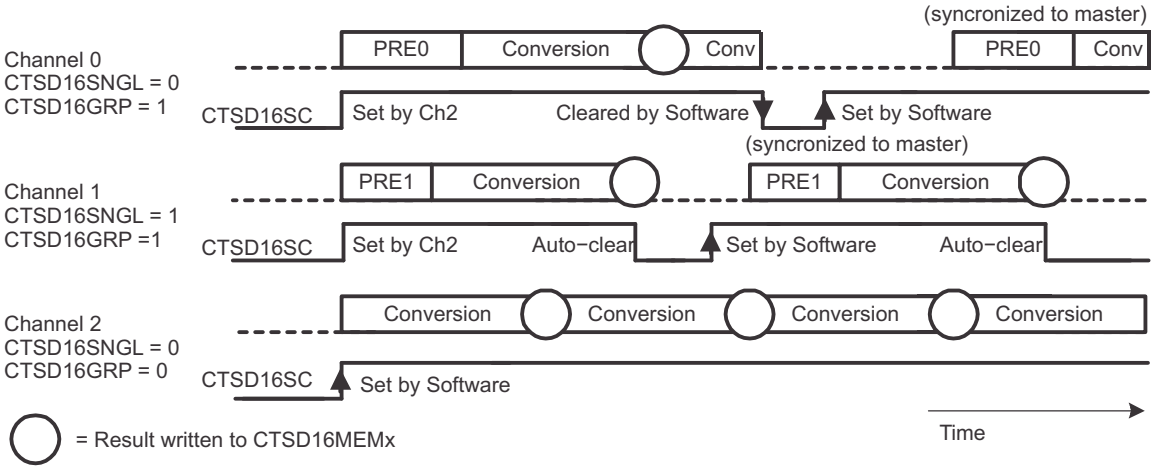

Figure 1-12. Preload and Channel Synchronization

1.2.11 Using the Integrated Temperature Sensor

To use the on-chip temperature sensor, select the analog input pair CTSD16INCHx = 0x6 and set REFTCOFF = 0 in REFCTL0 (REF module). This connects the temperature sensor to the positive CTSD16 input and connects the negative input to V_{REFBG}/V_{eREF+}, as for any single-ended input selection. Any other configuration is done as if an external analog input pair was selected, including CTSD16INTDLYx and CTSD16GAINx settings. The temperature sensor is part of the reference. It is possible to use the temperature sensor together with any of the available CTSD16 channels. However, it is not possible to use the temperature sensor with more than one CTSD16 channel at a time. The temperature measurement results will not be correct if more than one CTSD16 channel selects temperature sensor for conversion. CTSD16 can operate with either internal or external reference while using the temperature sensor.

Figure 1-13 shows the typical temperature sensor transfer function. When switching inputs of an CTSD16 channel to the temperature sensor, adequate delay must be provided using CTSD16INTDLYx to allow the digital filter to settle and make sure that conversion results are valid. The temperature sensor offset error can be large. TLV temperature sensor calibration values can be used as described in , *Device Descriptor Table*.

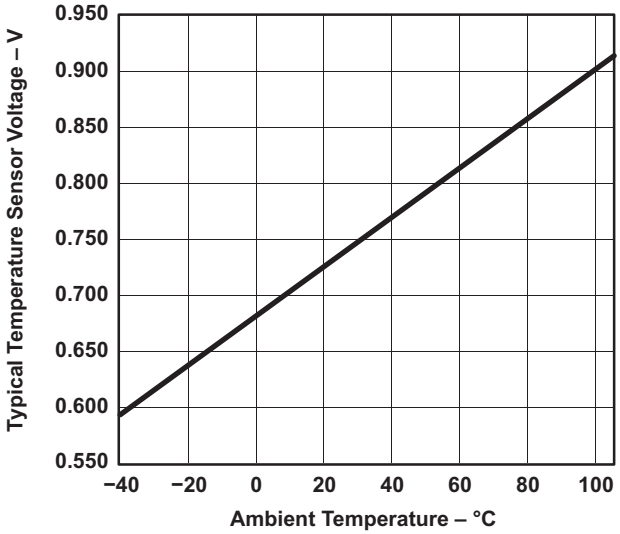

Figure 1-13. Typical Temperature Sensor Transfer Function

1.2.12 Using the Integrated AVCC Sense

To use the on-chip AVCC measurement, select the analog input pair CTSD16INCHx = 0x7. This connects AVCC sense to the positive CTSD16 input and connects the negative input to V_{REFBG}/V_{eREF+}, as for any single-ended input selection. Any other configuration is done as if an external analog input pair was selected, including CTSD16INTDLYx and CTSD16GAINx settings. It is possible to use the AVCC sense together with any of the available CTSD16 channels. However, it is not possible to use the AVCC sense with more than one CTSD16 channel at a time. The AVCC measurement results will not be correct if more than one CTSD16 channel selects AVCC sense for conversion. CTSD16 can operate with either internal or external reference while using the AVCC sense. AVCC sense measures the AVCC voltage divided by 2.

1.2.13 Grounding and Noise Considerations

As with any high-resolution ADC, appropriate printed circuit board layout and grounding techniques must be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. Therefore, solid decoupling on both the digital and analog supply is required (best with two capacitors, one 10 µF and one 100 nF, per supply).

In addition to grounding, ripple and noise spikes on the power-supply lines due to digital switching or switching power supplies can corrupt the conversion result. To achieve high accuracy, TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection.

If the internal reference is used, the reference voltage should be buffered externally by connecting a small capacitor as defined in the device-specific data sheet (C_{VREFBG}) to the VREFBG pin to reduce the noise on the reference.

1.2.14 Interrupt Handling

The CTSD16 has two interrupt sources for each channel:

- CTSD16IFGx: conversion ready
- CTSD16OVIFGx: conversion memory overflow

The CTSD16IFGx bits are set when their corresponding CTSD16MEMx memory register is written with a conversion result. An interrupt request is generated if the corresponding CTSD16IEx bit and the GIE bit are set. The CTSD16 overflow condition occurs when a conversion result is written to any CTSD16MEMx location before the previous conversion result was read.

The CTSD16 also has the CTSD16OFFG bit (the CTSD16 clock fault bit) which sets the OFIFG bit in SFRIFG1 register. OFIFG is shared with the system oscillators fault conditions.

1.2.14.1 CTSD16IV, Interrupt Vector Generator

All CTSD16 interrupt sources are prioritized and combined to source a single interrupt vector. CTSD16IV is used to determine which enabled CTSD16 interrupt source requested an interrupt. The highest priority CTSD16 interrupt request that is enabled generates a number in the CTSD16IV register (see Section 1.3.8). This number can be evaluated or added to the program counter to automatically enter the appropriate software routine. Disabled CTSD16 interrupts do not affect the CTSD16IV value.

Any read access of the CTSD16IV register has no affect on the CTSD16OVIFGx or CTSD16IFGx. The CTSD16IFGx flags are reset by reading the associated CTSD16MEMx register or by clearing the flags in software. CTSD16OVIFGx bits can only be reset with software. A write access to CTSD16IV clears all interrupt flags. If another interrupt is pending after servicing of an interrupt, another interrupt is generated. For example, if the CTSD16OVIFG0 and one or more CTSD16IFGx interrupts are pending when the interrupt service routine accesses the CTSD16IV register, the CTSD16OVIFG0 interrupt condition is serviced first and the corresponding flags must be cleared in software. After the RETI instruction of the interrupt service routine is executed, the highest priority CTSD16IFG pending generates another interrupt request.

1.2.14.2 Interrupt Delay Operation

The CTSD16INTDLY bit controls the timing for the first interrupt service request for the corresponding channel. This feature delays the interrupt request for a completed conversion by up to four conversion cycles to allow the digital filter to settle before generating an interrupt request. The delay is applied each time the CTSD16SC bit is set or when the CTSD16GAINx or CTSD16INCHx bits for the channel are modified. CTSD16INTDLY disables overflow interrupt generation for the channel for the selected number of delay cycles. Interrupt requests for the delayed conversions are not generated during the delay.

Example 1-1 shows the recommended use of CTSD16IV and the handling overhead. The CTSD16IV value is added to the PC to automatically jump to the appropriate routine.

Example 1-1. CTSD16 Interrupt Handling Software Example

The numbers at the right margin show the necessary CPU cycles for each instruction. The software overhead for different interrupt sources includes interrupt latency and return-from-interrupt cycles, but not the task handling itself. The latencies are:

- CTSD16OVIFG, CH0 CTSD16IFG, CH1 CTSD16IFG: 16 cycles
- CH2 CTSD16IFG: 14 cycles

The interrupt handler for channel 2 CTSD16IFG2 shows a way to check immediately if a higher prioritized interrupt occurred during the processing of the ISR. This saves nine cycles if another CTSD16 interrupt is pending.

```
; Interrupt handler for CTSD16.

INT_CTSD16                ; Enter Interrupt Service Routine   6
   ADD   &CTSD16IV,PC     ; Add offset to PC                  3
   RETI                   ; Vector 0: No interrupt            5
   JMP   ADOV             ; Vector 2: ADC overflow            2
   JMP   ADM0             ; Vector 4: CH_0 CTSD16IFG0         2
   JMP   ADM1             ; Vector 6: CH_1 CTSD16IFG1         2
;
; Handler for CH_2 CTSD16IFG2 starts here. No JMP required.
;
ADM2     MOV   &CTSD16MEM2,xxx   ; Move result, flag is reset
         ...                   ; Other instruction needed?
         JMP   INT_CTSD16        ; Check other int pending     2
;
; Remaining Handlers
;
ADM1     MOV   &CTSD16MEM1,xxx  ; Move result, flag is reset
         ...                  ; Other instruction needed?
         RETI                 ; Return                        5
;
ADM0     MOV   &CTSD16MEM0,xxx  ; Move result, flag is reset
         RETI                 ; Return                        5
;
ADOV     ...                  ; Handle CTSD16MEMx overflow
         RETI                 ; Return                        5
```

1.2.14.3 Using CTSD16 With DMA

Devices with an integrated DMA controller can automatically move data from any CTSD16MEMx to another location. DMA transfers are done without CPU intervention and are independent of any low-power modes.

If the respective interrupt enable bit CTSD16IEx is set, the selected CTSD16IFGx flag does not trigger a transfer. Any CTSD16IFGx is automatically cleared when the DMA controller accesses the corresponding CTSD16MEMx registers.

1.3 CTSD16 Registers

The CTSD16 registers are listed in Table 1-4. The base address can be found in the device-specific data sheet. The address offset is listed in Table 1-4.

Table 1-4. CTSD16 Registers

Offset	Acronym	Register Name	Type	Access	Reset	Section
00h	CTSD16CTL	CTSD16 Control	Read/write	Word	0000h	Section 1.3.1
02h	CTSD16CCTL0	CTSD16 Control Channel 0	Read/write	Word	0000h	Section 1.3.2
32h	CTSD16MEM0	CTSD16 Channel 0 Conversion Memory	Read	Word	0000h	Section 1.3.3
04h	CTSD16INCTL0	CTSD16 Channel 0 Input Control	Read/write	Word	0000h	Section 1.3.4
06h	CTSD16PRE0	CTSD16 Channel 0 Preload	Read/write	Word	0030h	Section 1.3.5
08h	CTSD16CCTL1	CTSD16 Channel 1 Control	Read/write	Word	0000h	Section 1.3.2
34h	CTSD16MEM1	CTSD16 Channel 1 Conversion Memory	Read	Word	0000h	Section 1.3.3
0Ah	CTSD16INCTL1	CTSD16 Channel 1 Input Control	Read/write	Word	0000h	Section 1.3.4
0Ch	CTSD16PRE1	CTSD16 Channel 1 Preload	Read/write	Word	00h	Section 1.3.5
0Eh	CTSD16CCTL2	CTSD16 Channel 2 Control	Read/write	Word	0000h	Section 1.3.2
36h	CTSD16MEM2	CTSD16 Channel 2 Conversion Memory	Read	Word	0000h	Section 1.3.3
10h	CTSD16INCTL2	CTSD16 Channel 2 Input Control	Read/write	Word	0000h	Section 1.3.4
12h	CTSD16PRE2	CTSD16 Channel 2 Preload	Read/write	Word	00h	Section 1.3.5
14h	CTSD16CCTL3	CTSD16 Channel 3 Control	Read/write	Word	0000h	Section 1.3.2
38h	CTSD16MEM3	CTSD16 Channel 3 Conversion Memory	Read	Word	0000h	Section 1.3.3
16h	CTSD16INCTL3	CTSD16 Channel 3 Input Control	Read/write	Word	0000h	Section 1.3.4
18h	CTSD16PRE3	CTSD16 Channel 3 Preload	Read/write	Word	00h	Section 1.3.5
1Ah	CTSD16CCTL4	CTSD16 Channel 4 Control	Read/write	Word	0000h	Section 1.3.2
3Ah	CTSD16MEM4	CTSD16 Channel 4 Conversion Memory	Read	Word	0000h	Section 1.3.3
1Ch	CTSD16INCTL4	CTSD16 Channel 4 Input Control	Read/write	Word	0000h	Section 1.3.4
1Eh	CTSD16PRE4	CTSD16 Channel 4 Preload	Read/write	Word	00h	Section 1.3.5
20h	CTSD16CCTL5	CTSD16 Channel 5 Control	Read/write	Word	0000h	Section 1.3.2
3Ch	CTSD16MEM5	CTSD16 Channel 5 Conversion Memory	Read	Word	0000h	Section 1.3.3
22h	CTSD16INCTL5	CTSD16 Channel 5 Input Control	Read/write	Word	0000h	Section 1.3.4
24h	CTSD16PRE5	CTSD16 Channel 5 Preload	Read/write	Word	00h	Section 1.3.5
26h	CTSD16CCTL6	CTSD16 Channel 6 Control	Read/write	Word	0000h	Section 1.3.2
3Eh	CTSD16MEM6	CTSD16 Channel 6 Conversion Memory	Read	Word	0000h	Section 1.3.3
28h	CTSD16INCTL6	CTSD16 Channel 6 Input Control	Read/write	Word	0000h	Section 1.3.4
2Ah	CTSD16PRE6	CTSD16 Channel 6 Preload	Read/write	Word	00h	Section 1.3.5
2C	CTSD16IFG	CTSD16 Interrupt Flag Register	Read/write	Word	0000h	Section 1.3.6
2E	CTSD16IE	CTSD16 Interrupt Enable Register	Read/write	Word	0000h	Section 1.3.7
30	CTSD16IV	CTSD16 Interrupt Vector	Read/write	Word	0000h	Section 1.3.8

1.3.1 CTSD16CTL Register

CTSD16 Control Register

Figure 1-14. CTSD16CTL Register

15	14	13	12	11	10	9	8
Reserved					CTSD16RRIERR	CTSD16RRIRDY	CTSD16RRIBURST
r0	r0	r0	r0	r0	r0	r0	rw-0
7	6	5	4	3	2	1	0
Reserved			CTSD16OFFG	Reserved	CTSD16REFS	Reserved	Reserved
r0	r0	r0	rw-0	rw-0	rw-0	r0	r0

Table 1-5. CTSD16CTL Register Description

Bit	Field	Type	Reset	Description
15-11	Reserved	R	0h	Reserved. Always reads as 0.
10	CTSD16RRIERR	R	0h	Rail-to-rail input error 0b = Rail-to-rail input no error (ready) 1b = Rail-to-rail input error (was ready but then not ready)
9	CTSD16RRIRDY	R	0	Rail-to-rail input ready 0b = Rail-to-rail input not ready 1b = Rail-to-rail input ready
8	CTSD16RRIBURST	RW	0h	Rail-to-rail input charge pump burst mode request from CTSD16 0b = Disables the rail-to-rail input charge pump burst mode request from CTSD16 1b = Enables the rail-to-rail input charge pump burst mode request from CTSD16, where charge pump is only enable when CTSD16 is converting to save power however the enable time of the charge pump must be considered. See the device specific OA data sheet section for the charge pump enable time.
7-5	Reserved	R	0h	Reserved. Always reads as 0.
4	CTSD16OFFG	RW	0h	CTSD16 clock fault flag. If this bit is set, the OFIFG flag is also set. CTSD16OFFG bit is set when a fault is detected with the CTSD16 clock (used by OA in rail-to-rail mode or CTSD16 module) 0b = No CTSD16 clock fault 1b = CTSD16 clock fault detected
3	Reserved	RW	0h	Reserved. Always write as 0.
2	CTSD16REFS	RW	0h	CTSD16 reference select. 0b = External reference selected. Internal reference voltage buffer disabled. 1b = Internal reference from shared REF selected and buffered internally to CTSD16
1	Reserved	R	0h	Reserved. Always reads as 0.
0	Reserved	R	0h	Reserved. Always reads as 0.

1.3.2 CTSD16CCTL0 to CTSD16CCTL6 Register

CTSD16 Channel x Control Register (x = 0 to 6)

Figure 1-15. CTSD16CCTL0 to CTSD16CCTL6 Register

15	14	13	12	11	10	9	8
Reserved					CTSD16SNGL	CTSD16OSRx	
r0	r0	r0	r0	r0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
CTSD16LSBTOG	CTSD16LSBACC	Reserved	CTSD16DF	Reserved		CTSD16SC	CTSD16GRP
rw-0	rw-0	r0	rw-0	r0	r0	rw-0	rw-0

Table 1-6. CTSD16CCTL0 to CTSD16CCTL6 Register Description

Bit	Field	Type	Reset	Description
15-11	Reserved	R	0h	Reserved. Always reads as 0.
10	CTSD16SNGL	RW	0h	Single conversion mode select 0b = Continuous conversion mode 1b = Single conversion mode
9-8	CTSD16OSRx	RW	0h	Oversampling ratio 00b = 256 01b = 128 10b = 64 11b = 32
7	CTSD16LSBTOG	RW	0h	LSB toggle. This bit, when set, causes CTSD16LSBACC to toggle each time the CTSD16MEMx register is read. 0b = CTSD16LSBACC does not toggle with each CTSD16MEMx read 1b = CTSD16LSBACC toggles with each CTSD16MEMx read
6	CTSD16LSBACC	RW	0h	LSB access. This bit allows access to the upper or lower 16-bits of the CTSD16 conversion result. 0b = CTSD16MEMx contains the most significant 16-bits of the conversion. 1b = CTSD16MEMx contains the least significant 16-bits of the conversion.
5	Reserved	R	0h	Reserved. Always reads as 0.
4	CTSD16DF	RW	0h	CTSD16 data format 0b = Offset binary 1b = Twos complement
3-2	Reserved	R	0h	Reserved. Always reads as 0.
1	CTSD16SC	RW	0h	CTSD16 start conversion 0b = No conversion start 1b = Start conversion
0	CTSD16GRP	RW	0h	CTSD16 group. Groups CTSD16 channel with next higher channel. Not used for the last channel. 0b = Not grouped 1b = Grouped

1.3.3 CTSD16MEM0 to CTSD16MEM6 Register

CTSD16 Channel x Conversion Memory Register (x = 0 to 6)

Figure 1-16. CTSD16MEM0 to CTSD16MEM6 Register

15	14	13	12	11	10	9	8
Conversion Results							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0
7	6	5	4	3	2	1	0
Conversion Results							
r-0	r-0	r-0	r-0	r-0	r-0	r-0	r-0

Table 1-7. CTSD16MEM0 to CTSD16MEM6 Register Description

Bit	Field	Type	Reset	Description
15-0	Conversion Results	R	0h	Conversion results. This register holds the upper or lower 16-bits of the digital filter output, depending on the CTSD16LSBACC bit.

1.3.4 CTSD16INCTL0 to CTSD16INCTL6 Register

CTSD16 Channel x Input Control Register (x = 0 to 6)

Figure 1-17. CTSD16INCTL0 to CTSD16INCTL6 Register

15	14	13	12	11	10	9	8
Reserved				CTSD16RRI	Reserved	Reserved	CTSD16INTDLY
r0	r0	r0	r0	rw-0	rw-0	r0	rw-0
7	6	5	4	3	2	1	0
CTSD16GAINx			CTSD16INCHx				
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-8. CTSD16INCTL0 to CTSD16INCTL6 Register Description

Bit	Field	Type	Reset	Description
15-12	Reserved	R	0h	Reserved. Always reads as 0.
11	CTSD16RRI	RW	0h	Rail-to-rail input enable. 0b = Rail-to-rail input disabled 1b = Rail-to-rail input enabled
10	Reserved	RW	0h	Reserved. Always write as 0.
9	Reserved	R	0h	Reserved. Always reads as 0.
8	CTSD16INTDLY	RW	0h	Interrupt delay generation after conversion start. This bit selects the delay for the first interrupt after conversion start. 0b = Fourth sample causes interrupt 1b = First sample causes interrupt
7-5	CTSD16GAINx	RW	0h	CTSD16 preamplifier gain 000b = x1 001b = x2 010b = x4 011b = x8 100b = x16 101b = Reserved 110b = Reserved 111b = Reserved
4-0	CTSD16INCHx	RW	0h	CTSD16 channel input 00000b = in+ = A0, in- = V_{REFBG}/V_{eREF+} 00001b = in+ = A1, in- = V_{REFBG}/V_{eREF+} 00010b = in+ = A2, in- = V_{REFBG}/V_{eREF+} 00011b = in+ = A3, in- = V_{REFBG}/V_{eREF+} 00100b = in+ = A4, in- = V_{REFBG}/V_{eREF+} 00101b = in+ = A5, in- = V_{REFBG}/V_{eREF+} 00110b = int+ = internal temperature sensor in- = V_{REFBG}/V_{eREF+} 00111b = in+ = internal VCC sense in- = V_{REFBG}/V_{eREF+} 01000b = in+ = internal VBAT sense in- = V_{REFBG}/V_{eREF+} 01001b = in+ = AD0+, in- = AD0- 01010b = in+ = AD0+, in- = V_{REFBG}/V_{eREF+} 01011b = in+ = AD1+, in- = AD1- 01100b = in+ = AD1+, in- = V_{REFBG}/V_{eREF+} 01101b = in+ = AD2+, in- = AD2- 01110b = in+ = AD2+, in- = V_{REFBG}/V_{eREF+} 01111b = in+ = AD3+, in- = AD3- 10000b = in+ = AD3+, in- = V_{REFBG}/V_{eREF+} 10001b = AD4x, shorted differential inputs to V_{REFBG}/V_{eREF+} 10010b = AD4x, shorted differential inputs to DAC0 output

1.3.5 CTSD16PRE0 to CTSD16PRE6 Register

CTSD16 Channel x Preload Register (x = 0 to 6)

Figure 1-18. CTSD16PRE0 to CTSD16PRE6 Register

15	14	13	12	11	10	9	8
Reserved						PreloadValue	
r0	r0	r0	r0	r0	r0	rw-0	rw-0
7	6	5	4	3	2	1	0
PreloadValue							
rw-0	rw-0	rw-1	rw-1	rw-0	rw-0	rw-0	rw-0

Table 1-9. CTSD16PRE0 to CTSD16PRE6 Register Description

Bit	Field	Type	Reset	Description
15-10	Reserved	R	0h	Reserved. Always reads as 0.
9-0	PreloadValue	RW	30h	CTSD16 digital filter preload value. Value represents number of CTSD16 clock cycles. • If internal reference is used and but not already on and settle when CTSD16 starts a conversion, refer to device-specific data sheet for V_{REFBG} settle time to determine preload minimum value. Note V_{REFBG} can be turned on with REFON = 1 and REFOUT = 1. Else, if CTSD16RRI = 1 need to use the charge pump startup time if not already on (OARRI = 1 or CTSD16RRIBURST = 0). Refer to the device data sheet OA section for charge pump enable time t_{CP_EN}. If charge pump is already on there is no minimum preload value • If internal reference is already settled or not used and CTSD16RRI = 0 and OARRI = 1 there is no preload minimum value required. • If internal reference is already settled or not used and CTSD16RRI = 0 and OARRI = 0 then the minimum preload value is the default one.

1.3.6 CTSD16IFG Register

CTSD16 Interrupt Flag Register

Figure 1-19. CTSD16IFG Register

15	14	13	12	11	10	9	8
Reserved	CTSD16OVIFG6	CTSD16OVIFG5	CTSD16OVIFG4	CTSD16OVIFG3	CTSD16OVIFG2	CTSD16OVIFG1	CTSD16OVIFG0
r0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
Reserved	CTSD16IFG6	CTSD16IFG5	CTSD16IFG4	CTSD16IFG3	CTSD16IFG2	CTSD16IFG1	CTSD16IFG0
r0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-10. CTSD16IFG Register Description

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads as 0.
14	CTSD16OVIFG6	RW	0h	CTSD16 converter 6 overflow interrupt flag 0b = No interrupt pending 1b = Interrupt pending
13	CTSD16OVIFG5	RW	0h	CTSD16 converter 5 overflow interrupt flag 0b = No interrupt pending 1b = Interrupt pending
12	CTSD16OVIFG4	RW	0h	CTSD16 converter 4 overflow interrupt flag 0b = No interrupt pending 1b = Interrupt pending
11	CTSD16OVIFG3	RW	0h	CTSD16 converter 3 overflow interrupt flag 0b = No interrupt pending 1b = Interrupt pending
10	CTSD16OVIFG2	RW	0h	CTSD16 converter 2 overflow interrupt flag 0b = No interrupt pending 1b = Interrupt pending
9	CTSD16OVIFG1	RW	0h	CTSD16 converter 1 overflow interrupt flag 0b = No interrupt pending 1b = Interrupt pending
8	CTSD16OVIFG0	RW	0h	CTSD16 converter 0 overflow interrupt flag 0b = No interrupt pending 1b = Interrupt pending
7	Reserved	R	0h	Reserved. Always reads as 0.
6	CTSD16IFG6	RW	0h	CTSD16 converter 6 interrupt flag. CTSD16IFG6 is set when new conversion results are available. CTSD16IFG6 is automatically reset when the CTSD16MEM6 register is read, or may be cleared with software. 0b = No interrupt pending 1b = Interrupt pending
5	CTSD16IFG5	RW	0h	CTSD16 converter 5 interrupt flag. CTSD16IFG5 is set when new conversion results are available. CTSD16IFG5 is automatically reset when the CTSD16MEM5 register is read, or may be cleared with software. 0b = No interrupt pending 1b = Interrupt pending
4	CTSD16IFG4	RW	0h	CTSD16 converter 4 interrupt flag. CTSD16IFG4 is set when new conversion results are available. CTSD16IFG4 is automatically reset when the CTSD16MEM4 register is read, or may be cleared with software. 0b = No interrupt pending 1b = Interrupt pending

Table 1-10. CTSD16IFG Register Description (continued)

Bit	Field	Type	Reset	Description
3	CTSD16IFG3	RW	0h	CTSD16 converter 3 interrupt flag. CTSD16IFG3 is set when new conversion results are available. CTSD16IFG3 is automatically reset when the CTSD16MEM3 register is read, or may be cleared with software. 0b = No interrupt pending 1b = Interrupt pending
2	CTSD16IFG2	RW	0h	CTSD16 converter 2 interrupt flag. CTSD16IFG2 is set when new conversion results are available. CTSD16IFG2 is automatically reset when the CTSD16MEM2 register is read, or may be cleared with software. 0b = No interrupt pending 1b = Interrupt pending
1	CTSD16IFG1	RW	0h	CTSD16 converter 1 interrupt flag. CTSD16IFG1 is set when new conversion results are available. CTSD16IFG1 is automatically reset when the CTSD16MEM1 register is read, or may be cleared with software 0b = No interrupt pending 1b = Interrupt pending
0	CTSD16IFG0	RW	0h	CTSD16 converter 0 interrupt flag. CTSD16IFG0 is set when new conversion results are available. CTSD16IFG0 is automatically reset when the CTSD16MEM0 register is read, or may be cleared with software 0b = No interrupt pending 1b = Interrupt pending

1.3.7 CTSD16IE Register

CTSD16 Interrupt Enable Register

Figure 1-20. CTSD16IE Register

15	14	13	12	11	10	9	8
Reserved	CTSD16OVIE6	CTSD16OVIE5	CTSD16OVIE4	CTSD16OVIE3	CTSD16OVIE2	CTSD16OVIE1	CTSD16OVIE0
r0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
Reserved	CTSD16IE6	CTSD16IE5	CTSD16IE4	CTSD16IE3	CTSD16IE2	CTSD16IE1	CTSD16IE0
r0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-11. CTSD16IE Register Description

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads as 0.
14	CTSD16OVIE6	RW	0h	CTSD16 converter 6 overflow interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
13	CTSD16OVIE5	RW	0h	CTSD16 converter 5 overflow interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
12	CTSD16OVIE4	RW	0h	CTSD16 converter 4 overflow interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
11	CTSD16OVIE3	RW	0h	CTSD16 converter 3 overflow interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
10	CTSD16OVIE2	RW	0h	CTSD16 converter 2 overflow interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
9	CTSD16OVIE1	RW	0h	CTSD16 converter 1 overflow interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
8	CTSD16OVIE0	RW	0h	CTSD16 converter 0 overflow interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
7	Reserved	R	0h	Reserved. Always reads as 0.
6	CTSD16IE6	RW	0h	CTSD16 converter 6 interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
5	CTSD16IE5	RW	0h	CTSD16 converter 5 interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
4	CTSD16IE4	RW	0h	CTSD16 converter 4 interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
3	CTSD16IE3	RW	0h	CTSD16 converter 3 interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
2	CTSD16IE2	RW	0h	CTSD16 converter 2 interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled

Table 1-11. CTSD16IE Register Description (continued)

Bit	Field	Type	Reset	Description
1	CTSD16IE1	RW	0h	CTSD16 converter 1 interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
0	CTSD16IE0	RW	0h	CTSD16 converter 0 interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled

1.3.8 CTSD16IV Register

CTSD16 Interrupt Vector Register

Figure 1-21. CTSD16IV Register

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
0	0	0	CTSD16IVx				
r0	r0	r0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 1-12. CTSD16IV Register Description

Bit	Field	Type	Reset	Description
15-5	Reserved	R	0h	Reserved. Always reads as 0.
4-0	CTSD16IVx	RW	0h	CTSD16 interrupt vector value. Writing to this register clears all pending interrupt flags. 00h = No interrupt pending 02h = Interrupt Source: CTSD16MEMx overflow; Interrupt Flag: CTSD16OVIFG (1); Interrupt Priority = Highest. 04h = Interrupt Source: CTSD16_0 Interrupt; Interrupt Flag: CTSD16IFG0 06h = Interrupt Source: CTSD16_1 Interrupt; Interrupt Flag: CTSD16IFG1 08h = Interrupt Source: CTSD16_2 Interrupt; Interrupt Flag: CTSD16IFG2 0Ah = Interrupt Source: CTSD16_3 Interrupt; Interrupt Flag: CTSD16IFG3 0Ch = Interrupt Source: CTSD16_4 Interrupt; Interrupt Flag: CTSD16IFG4 0Eh = Interrupt Source: CTSD16_5 Interrupt; Interrupt Flag: CTSD16IFG5 10h = Interrupt Source: CTSD16_6 Interrupt; Interrupt Flag: CTSD16IFG6; Interrupt Priority = Lowest

(1) When an CTSD16 overflow occurs, the user must check all CTSD16CCTLx CTSD16OVIFG flags to determine which channel overflowed.

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