TPIC7710EVM Evaluation Module

This user's guide describes the hardware platform containing a sample TPIC7710 and the relevant graphical user interface (GUI) software. The evaluation module (EVM) provides users with a quick and trouble-free way to evaluate the functionality of TPIC7710. The EVM board also is capable of connecting with a customer-supplied microprocessor board to evaluate the TPIC7710 at a higher system level.

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- Evaluation hardware
- GUI software
- Texas Instruments General Equipment Resource (TI GER) USB interface module
- USB cable

2 EVM Features

- Computer control of all digital Inputs
- Real-time monitor of all reporting register addresses (fault flags, etc.)
- Watchdog clock and 5-V supply generated by TI GER Module
- Potentiometers to set voltage thresholds
- Direct connection to external motors through banana-jack connections
- Header for easy connection to customer-specific microprocessor.

Windows is a trademark of Microsoft Corporation.

3 Equipment Needed for Product Evaluation

- Single-power supply capable of 14-V, 1-A operation.
- Computer with Windows™ XP and .net Framework 2.0 or later
- Screwdriver, slotted 1.2 mm
- DMM, oscilloscope
- Motor, microprocessor board (*customer supplied)

4 Introduction

The TPIC7710EVM provides a platform to demonstrate the functionality of the Electronic Park Brake ASIC available from the Mixed Signal Automotive Group within Texas Instruments. The circuit board is laid out in organized blocks that are analogous to the functional blocks within the product. This EVM is not a complete reference design of an actual park brake system. However, it is capable of interfacing the ASIC with a system, as well as stand-alone evaluation. The GUI software is organized similar to the EVM hardware, such that similar product functionality is grouped within separate tabs. Functional control bits are accessible using an editable grid view of all memory, as well as direct control via checkboxes. For a compete description, see the schematic and software sections .

5 Initial EVM Setup

5.1 Installing GUI Software

Before the TPIC7710 can be evaluated, the GUI software must be available on a host computer. Place the executable file in a convenient location (Desktop or c:\Texas Instruments EVM\) and double-click to run the application.

NOTE: Some computer networks have strong virus filtering that may cause the GUI to be deleted or replaced with a warning text file. If this happens, then it may be necessary to rename the extension part of the program to successfully pass through the network. For example, EVM_GUI_program.exe can be changed to EVM_GUI_program.rename. Once the file is on the host computer, the file name must be renamed to include .exe. Some networks may also require that executables be compressed (in a ZIP file) to be transferred.

5.2 Installing USB Resources for TI GER Communication Module

This EVM requires a separate interface module to allow the GUI program to communicate with the EVM hardware. The Texas Instruments General Equipment Resource (TI GER) is included in the EVM kit for this purpose. Connect the TI GER to the computer using the supplied USB cable to be detected by the Windows operating system. Once this is done, Windows identifies it as an HID device and it is immediately ready for use. The TI GER does not require the installation of any additional USB drivers.

5.3 Preparing the EVM Hardware

To complete the EVM setup, the EVM hardware (TPIC7710 PCB and TI GER) must be connected.

WARNING

This EVM contains components that are sensitive to electrostatic discharge (ESD). Use proper laboratory techniques and equipment to minimize the chance of an ESD or EOS event.

Power must be supplied to the TPIC7710 for basic operation. When connecting the supply be sure to connect the power supply's case ground with the negative terminal. All future reference to this *case ground + negative terminal* is referred to as GND. After this is done, the negative terminal must be connected to the EVM to provide a ground before power is applied.

The TI GER must be connected to the EVM board face up. The reset button on the TI GER and the TPIC7710 IC must both face in the same direction. A recommended connection procedure is follows.

Connection Procedure for the TPIC7710:

- Connect all power supply grounds to the AGND and PGND (KL31) banana jacks.
- Connect the TI GER to the computer using the supplied USB cable; then connect the TI GER to the EVM 30-pin header.
- Set the voltage and compliance current on the power supplies.
  - VBATT (KL30) must be set to a nominal voltage of 13.8 V. Compliance current must be 200 mA – 500 mA. This provides power to the TPIC7710
  - VMOT (KL30) must be set to a nominal voltage of 13.8 V. Compliance must be set appropriately to drive the dc motor. The EVM is designed to handle a maximum of 20 A. This provides power to the FET1/2/3 and motor drive relays.
- Plug in the positive terminal of the power supply to the appropriate banana jacks; then enable the power supply outputs.

  Note: Use a high-quality supply to provide power to this EVM. The power supply must be able to source current fast enough to prevent a voltage dip at the EVM terminals. When the motor is started, it draws very large amounts of current for 10's or 100's of milliseconds; some power supplies can react faster than others.

Finally, open the GUI software. If the setup is correct, "DISCONNECT FROM TIGER" is displayed at the top of the window indicating the TI GER has been detected and enumerated. Connection to the TPIC7710 can be verified by the Report Flag Grid, at the bottom of the GUI, changing cell colors to display the report register contents (blue is 0; red is 1).

6 Understanding the EVM Hardware

The TPIC7710 has well-defined functional blocks. The EVM hardware is also organized into analogous functional blocks for easy reference. See the schematics and layout section at the end of this document for circuitry details. The following functional blocks are accessible on the EVM hardware, depicted in Figure 1 and described in the following schematic pages.

1. TPIC7710 pinout
2. Circuits pertaining to the power distribution
   (a) Battery voltage for TPIC7710
   (b) Battery voltage for drivers and motors
   (c) Internal regulation of V5 and V5A supplies (5 volts)
   (d) VADC
   (e) Charge Pump
   (f) External 5-V supply (5V_EXT) for collateral circuitry
3. Circuits pertaining to the driver pins (OUTP1/2/3 and OUTN1/2
4. Circuits pertaining to the FET pins (FET1/2/3)
5. Circuits pertaining to the current measurement functionality
6. Circuits pertaining to the comparator functionality
7. Circuits pertaining to the relay functionality
8. Circuits pertaining to the motor interface
9. Circuits pertaining to the external connection of a microprocessor
10. Circuits pertaining to the connection to the TI GER module
11. Circuits pertaining to the WDT clock signal generation
12. Circuits pertaining to the floating ground for all LED indicators

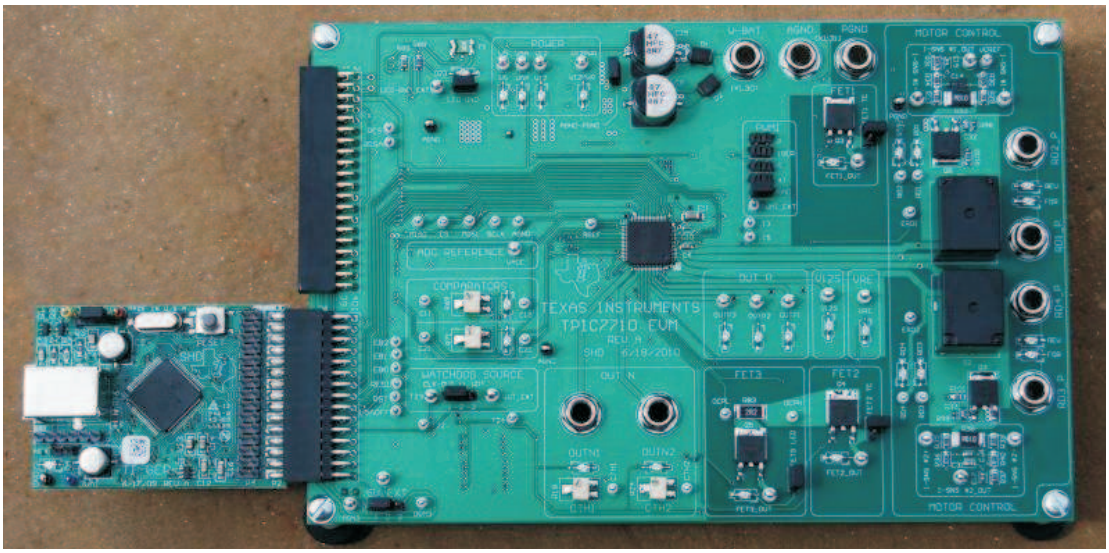


Figure 1. TPIC7710EVM Board

7 Headers, Test Points, and Banana Jacks

7.1 Headers

This EVM has two sets of horizontally mounted headers. The P6 header connects the TI GER module to the EVM printed-circuit board (PCB) for computer control using the supplied GUI. The TI GER must be connected with its RESET switch facing up.

The P5 header is a 2x40 pin, 100-mil female header. It is intended to provide all the connections that a customer-supplied microprocessor needs to more holistically evaluate the TPIC7710 as a system. Customers may design a small PCB with their system's microprocessor for this purpose. If this option is used, do not connect the TI GER module to the P6 header.

WARNING

If a customer-supplied external microprocessor is connected to the EVM (P6), do not simultaneously connect the TI GER module (P5). This may cause signal contention and may damage the TI GER module.

7.2 Test Points

Some terminals of the TPIC7710 are accessible by connection to a wire-loop test point. These connection points are intended for low-current source/sink or signal monitoring/driving. Many of these test points are connected in parallel with TI GER I/Os; for this reason, care must be taken not to overdrive any voltage that is output from the TI GER.

7.3 Banana Jacks

The TPIC7710 EVM has ten banana jacks. These jacks provide a convenient way to connect EVM circuitry to devices that may require high current. Four Jack are for general power supply connection, two jacks are for connection to the OUTN1/2 pins, and the remaining four jacks provide connection to a customer-supplied motor.

The V-BAT and AGND jacks supply power to the TPIC7218 as well as some of the attendant circuitry. The

V-MOT and PGND jacks provide power to the motor and FETs (FET1, FET2, and FET3). Power is supplied and distributed separately on the EVM to prevent any noise, flyback voltage, or voltage droop due to motor start/stop events from disrupting power to the TPIC7710. AGND and PGND exist on separate planes within the PCB; however, they can be connected together at two locations: the jumper AGND-PGND, and through a ferrite bead, L1.

The motor jacks: RD1_P, RD2_P, RD3_P, and RD4_P provide a high-current connections to the motor drive relays. Each banana jack directly connects to the pole of a SPDT relay. RD1_P and RD2_P work as a pair for motor #1, and RD3_P and RD4_P work as a pair for motor #2.

Finally, the OUTN1 and OUTN2 jacks provide connection to the TPIC7710 medium-current, low-side drivers.

7.4 Jumpers

The EVM has 11 jumpers that provide a simple way to reconfigure resources for some of the TPIC7710 functionality. See the Table 1 for jumper descriptions.

Table 1. Jumper Description

Jumper Annotation	Jumper Name	Description
JP1	AGND-PGND	Short AGND and PGND
JP2	5V_EXT : 5V TIGER	1:2 5V_EXT – 5V TIGER 2:3 5V_EXT – 5V_EXT TEST POINT
JP3	JP3	Link V12 to TIGER PWR-DWN pin
JP4	CLK-OUT :: WDT	1:2 WDT – TI GER clock signal 2:3 WDT – WDT Test Point (externally supplied watchdog signal)
JP5	V5	Short to couple PWMI to V5
JP6	PWMI_EXT	Short to couple PWMI to PWMI_EXT test point
JP7	PWMI_uP	Short to couple PWMI to J6
JP8	AGND	Short to couple PWMI to AGND
JP9	PWMI_TIG	Short to couple PWMI to TI GER
JP10	FET1 TC	Short to couple FET1 to motor for Test Current
JP11	FET2 TC	Short to couple FET2 to motor for Test Current
JP12	FET3 LED	Short to connect FET3 to LED ground
JP13	LED-GND	Short to connect all LED cathodes to the floating LED ground

7.5 Watchdog (WDT) Signal Generation

The TPIC7710 requires a steady clock signal at the WDT pin for full operation. The TI GER card is capable of generating frequencies down to 1 kHz, but this is not low enough to satisfy the watchdog requirements for the TPIC7710. To mitigate this problem, the EVM has a clock divider circuit built in which has a fixed-frequency divider value of 500. The WDT pin can also be driven from the WDT external test point.

7.6 LED Ground

The TPIC7710 has a normal operating voltage of 13.8 V and is variable over a very wide range of voltages. LEDs require a fixed current to illuminate which get power from the V-BATT supply. In order to keep the current through the LEDs stable with different V-BATT voltages, a circuit has been designed to track the V-BATT supply and provide the LED cathodes (and series resistance) with a voltage equal to V-BATT – 5. Therefore, high voltages on V-BATT do not affect the indicator LEDs .

WARNING

The LED ground circuit has been designed to accommodate a wide range of supply voltages; however, the TPIC7710 must not be operated at any voltage above its absolute maximum rating. Doing so may cause damage to the LED ground circuit.

The LED ground circuit is also sensitive to a particular condition where the V-BATT banana jack and the V-MOT banana jack are at different voltages. A self-resettable fuse has been placed in series with the LED ground path to prevent a large current from damaging the pass transistor.

7.7 Power Supply Link to TI GER PWR-DWN Pin

This EVM is also equipped to monitor the supply voltage on the TPIC7710 for the purpose of disabling the TI GER I/Os on supply power down. The TI GER supplies voltage/signals to the digital inputs of the TPIC7710; if the laboratory bench power supply is switched off, then it is possible that the TPIC7710 still has voltage on some pins. This condition may violate the absolute maximum ratings of the part, and can also parasitically power the part. To prevent this from occurring, the TI GER monitors V12 and disables all I/Os whenever V12 is less than 4 V. The TI GER's PWR-DWN I/O is capable of withstanding voltages up to 55 V.

8 Understanding the GUI Software

This EVM kit contains a GUI program necessary to control the TI GER, which in turn controls the TPIC7710. The software is designed to provide users with an uncomplicated platform to interface and evaluate the device (see Figure 2).

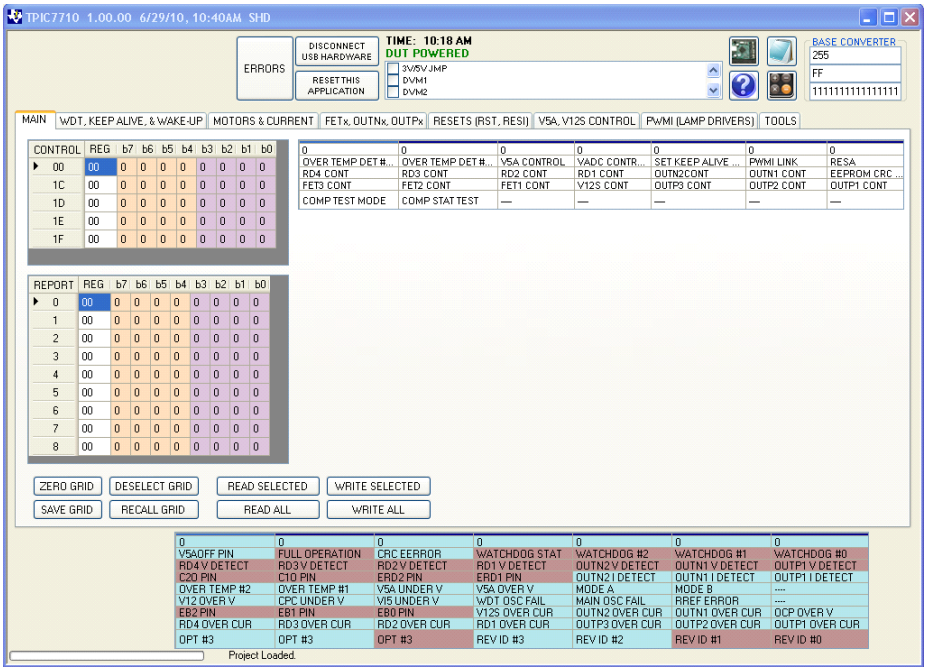
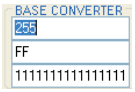


Figure 2. TPIC7710 Graphical User Interface

8.1 Standard Convenient Tools

For convenience, several useful tools are available at the top of the GUI.



- Base Converter – Type a hexadecimal, decimal, or binary number in the respective text box, then press ENTER to calculate the other two numerical values.

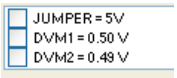
- Notepad (icon) – Click to open an empty Notepad window.

- Calculator (icon) – Click to open Windows Calculator.

- Question (icon) – Click to open a help window containing information about this GUI.

- Green TI GER (icon) – Click to open a window that directly controls all TI GER functions and I/O.

- TIME – System time
- MANUAL, DUT UNPOWERED, DUT POWERED – Indicates the state of the device power supply.
  - DUT UNPOWERED occurs when the TI GER detects that device power supply is turned off. In this state, the TI GER I/Os revert to a 0 V or high impedance.
  - DUT POWERED occurs when the TI GER detects the device power supply is turned on. In this state, the TI GER I/Os are in the normal operating state.
  - MANUAL occurs when the auto-power-down feature is disabled. This can be set by unchecking the Power-down TI GER with the chip power supply automatically checkbox.



- Checkbox list box – This scrollable box contains switches which enable or disable GUI features and control the device.

- DISCONNECT/CONNECT USB HARDWARE button – Indicates the state of the USB connection to TI GER. The TI GER can be manually connected or disconnected from the USB bus. If the TI GER is not found on the USB bus, then the button is always in the CONNECT TO USB HARDWARE state.

- RESET THIS APPLICATION button – Click this button to reset the GUI and the TI GER to the EVM/GUI's initial state. This may not reset all of the TPIC7710's functionality.

- ERRORS button – This button indicates if any user, GUI, or EVM errors occur. An error changes the button's color to red. Click on the button to view and clear any errors.

8.2 TPIC7710 GUI Specific Tools and Features

This GUI also contains TPIC7710 specific tools and features. The descriptions of these specialized functions follow.

- Report flags are displayed in a grid at the bottom of the GUI window. All bits in the report flag registers are displayed in individual cells. The color of the cell changes to indicate if the bit is a "1" or a "0". A 0 is depicted as light blue and a 1 is depicted as light red.

0	0	0	0	0	0	0
V5AOFF PIN	FULL OPERATION	CRC EERROR	WATCHDOG STAT	WATCHDOG #2	WATCHDOG #1	WATCHDOG #0
RD4 V DETECT	RD3 V DETECT	RD2 V DETECT	RD1 V DETECT	OUTN2 V DETECT	OUTN1 V DETECT	OUTP1 V DETECT
C20 PIN	C10 PIN	ERD2 PIN	ERD1 PIN	OUTN2 I DETECT	OUTN1 I DETECT	OUTP1 I DETECT
OVER TEMP #2	OVER TEMP #1	V5A UNDER V	V5A OVER V	MODE A	MODE B	----
V12 OVER V	CPC UNDER V	VI5 UNDER V	WDT OSC FAIL	MAIN OSC FAIL	RREF ERROR	----
EB2 PIN	EB1 PIN	EB0 PIN	V12S OVER CUR	OUTN2 OVER CUR	OUTN1 OVER CUR	OCP OVER V
RD4 OVER CUR	RD3 OVER CUR	RD2 OVER CUR	RD1 OVER CUR	OUTP3 OVER CUR	OUTP2 OVER CUR	OUTP1 OVER CUR
OPT #3	OPT #3	OPT #3	REV ID #3	REV ID #2	REV ID #1	REV ID #0

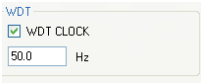
- An informational array (with white cells) lists the command bit names. This array is for informational purpose only, and does not serve any other function. To actually read or write data to the command registers, the address/data entry grid (on the left) must be used. It is important to note that the address/data entry grid contains all 8 bits of a SPI packet. Bit-0 is the parity bit; the GUI automatically calculates this bit regardless of the data entered in the grid.

0	0	0	0	0	0	0
OVER TEMP DET #...	OVER TEMP DET #...	V5A CONTROL	VADC CONTR...	SET KEEP ALIVE ...	PWMI LINK	RESA
RD4 CONT	RD3 CONT	RD2 CONT	RD1 CONT	OUTN2CONT	OUTN1 CONT	EEPROM CRC ...
FET3 CONT	FET2 CONT	FET1 CONT	V12S CONT	OUTP3 CONT	OUTP2 CONT	OUTP1 CONT
COMP TEST MODE	COMP STAT TEST	—	—	—	—	—

- The checkbox list box contains several TPIC7710 switches. The description of switch functionality follows.

  - REAL TIME DISPLAY OF MOTOR CURRENT – Check this box for continuous monitor and display of the each motor's current as it is measured across the sense resistors.
  - REAL TIME MONITOR OF REPORT FLAGS – Check this box to repeatedly read all report flag registers (over SPI) and update the cell color in the report flag grid.
  - DISREGARD COMMUNICATION ERRORS – Check this box to prevent any SPI errors from opening a notification message box and/or cause the ERRORS button to display an error condition. A SPI error condition is displayed whenever a parity error or nonmatching mirror bytes occur.
  - ENABLE RELAY TOGGLE – Check this box to disable normal GUI/device function for the purpose of entering a relay energized/de-energized (toggle) loop.

- The TPIC7710 features "keep-alive" functionality. In order to keep the TPIC7710 out of a sleep state, a specific repetitive SPI transfer must occur. This keep-alive SPI transfer must reoccur in a particular amount of time to keep the device alive/awake. Users can enable/disable this signal, as well as control the time between keep-alive SPI transfers.



- The TPIC7710 requires a watchdog clock signal at the WDT pin. Users can enable/disable this signal, as well as control the frequency of operation.

NOTE: It is possible (and expected) that a USB/TI GER error can occur. These events are infrequent. If this happens during an SPI transfer, then an error is reported in the ERRORS window. This error is real (indicating a parity or mismatch mirror byte) and is properly reported by the TPIC7710.

8.3 Grid Interface to Device Address and Data Space

This EVM features an address and data grid allowing convenient reads/writes to and from device data space. Users can read or write any number of addresses by selecting or modifying cell contents, then clicking one of the grid control buttons shown in Figure 4.

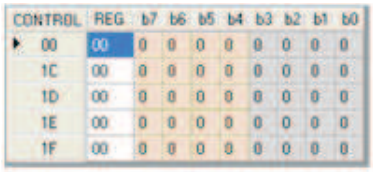


Figure 3. Example Grid

Figure 4. Grid Control Buttons

EVM software can contain more than one grid structure; however, all grids are controlled by the same control buttons. The GUI keeps track of the user's last selected or modified grid; it is this grid that is operated on when a grid control button is clicked. Following a grid operation, all cells contained within flash a particular and unique color to verify that the user's requested operation occurred on the intended grid. The color of the grid control button's text changes to the color flashed on the grid that was actually operated on. See Figure 5.

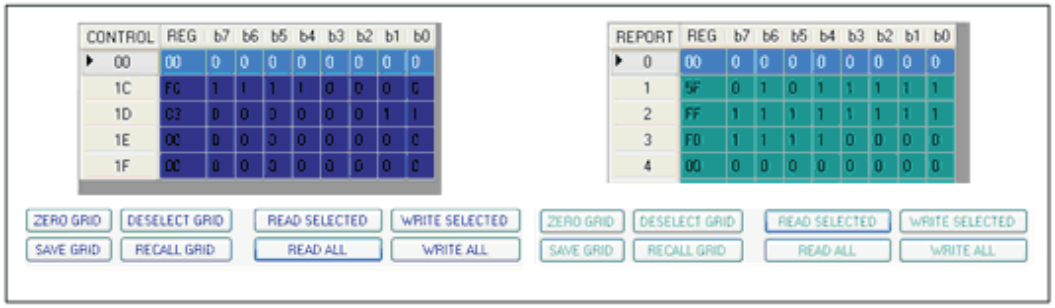


Figure 5. Grid and Button Flash Color

The READ SELECTED and READ ALL buttons initiate a read of the device data. Select one row/addresses by clicking on its left-most cell, or to select more than one row/address click on the left-most cell while holding the control key. This not only selects the address/row to read, but also selects the grid to be operated on when the READ SELECTED button is clicked. To read all rows/addresses, click on any left-most cell of the desired grid (to select the grid of interest), then click the READ ALL button. Returned data is displayed in the second column as a hexadecimal value and in the remaining bit cells as a binary number.

The WRITE SELECTED and WRITE ALL buttons initiate a write of the grid data to the device. Modify the data in the appropriate rows/addresses (the row changes to yellow or blue color); then click the WRITE SELECTED button. This not only modifies the data to write, but also selects the grid to be operated on when the WRITE SELECTED button is clicked. Data can be modified by directly entering a hexadecimal value in the second column, or by clicking the appropriate bits in the bit cells. Clicking a bit cell toggles the value from 1 to 0 or 0 to 1. All rows with modified data are written when the WRITE SELECTED button is clicked. To write all rows/addresses, click on any left-most cell of the desired grid (to select the grid of interest); then click the WRITE ALL button. This is especially useful to quickly populate all data at one time.

The SAVE GRID and RECALL GRID buttons provide a convenient way to store and recall grid contents to and from a text file. As with reads and writes, the grid of interest must be selected by clicking on any cell in the left-most column. Whenever a RECALL GRID command populates file data into the grid of interest, the user must click WRITE ALL (or select particular rows/addresses) to actually transfer the data into the device.

The remaining grid control buttons, ZERO GRID and DESELECT GRID, are used to force all data cells to zero and unhighlight any selected rows/addresses. Clicking ZERO GRID does not change the device data; it only changes the data displayed in the grid. If the user also wants to write zeros to the device, then WRITE ALL must also be clicked.

8.4 TPIC7710 Functions in Tabs

Figure 6. Organization of TPIC7710 GUI Controls

All GUI controls are organized by device function in separate tabs. Each tab contains a small number of controls pertaining to a particular functional block within the TPIC7710. The MAIN tab contains the address/data registers which directly interface TPIC7710 registers with the data displayed in the appropriate grid. For convenience, all functions of the TPIC7710 also can controlled by manipulating GUI graphical controls, which are broken out into separate tabs. Figure 6 depicts the tab organization, and the description of each tab is follows.

- WDT, KEEP ALIVE, & WAKE-UP – Contain controls for so-named device pins and bits
- MOTORS & CURRENT – Contain controls pertaining to motor drive
  - If motors are connected to the EVM, they can be controlled here.
  - Motor current can be (approximately) measured and displayed.
  - A Test Current feature also is included. To use this function, the FET1_TC and FET2_TC jumpers must be placed on the hardware. This feature connects FET1/2 to the motor circuitry through a 28-Ω resistance. In this mode, FET1/2 must not be controlled by any other tab to prevent resistors from overheating due to long FET on-times. The test current feature pulses the FET1/2 an adjustable amount of time which is small enough to prevent resistor overheating.

WARNING

If FET1 and/or FET2 are connected to the motor circuitry using the FET1_TC and FET2_TC jumpers, they must only be activated for a short time (10's – 100's of milliseconds). The resistor power rating is sized for pulsed-mode operation only. A sustained dc current may damage the resistors.

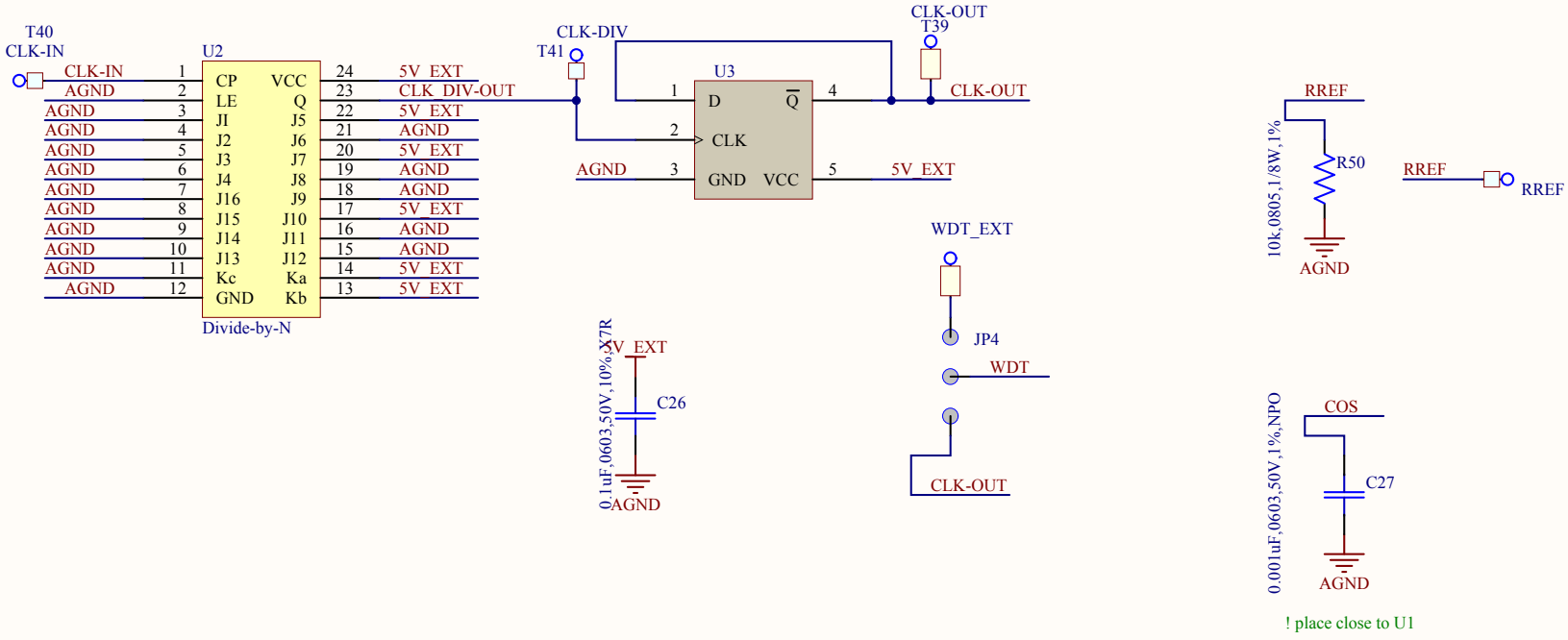
  - Continuous monitor of motor current can be enabled/disabled using the REAL TIME DISPLAY OF MOTOR CURRENT checkbox as previously described.
- FETx, OUTNx, OUTPx – Enable/Disable TPIC7710 internal and external drivers.
- RESETS (RST, RESI) – Control the TPIC7710's reset functionality.
- V5A, V12S CONTROL – Control bits and pins for V5A and V12S functionality.
- PWMI (LAMP DRIVERS) – Control PWMI bit and pin functionality.
- TOOLS – Contains a feature to continuously toggle relays. Pulse time can be modified by editing the time textboxes. As previously described, the ENABLE RELAY TOGGLE checkbox must be checked.

9 Schematics and PCB Artwork

The schematics and layered views of the printed-circuit board for the TPIC7710EVM appear on the following pages.

10 Related Documentation From Texas Instruments

To obtain a copy of any TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. Updated documents also can be obtained through the TI Web site at http://www.ti.com.



DIV-BY-N

296-9221-1-ND
CD74HC4059M96

f(OUT) = f(IN)/N

Kx

Ka	Kb	Kc	
1	1	1	/2
0	1	1	/4
1	0	1	/5
0	0	1	/8
1	1	0	/10

N= Kx * (Y) + 1*D1

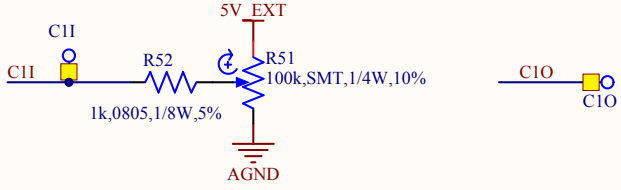
Y = (1000 * D5) +
(100 * D4) +
(10 * D3) +
(1 * D2)

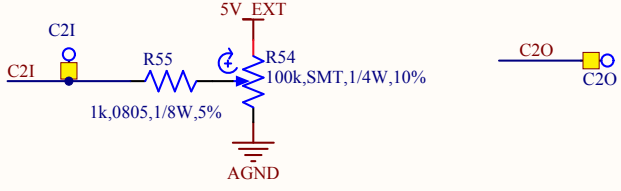
D5 = J4
D4 = J13,14,15,16
D3 = J9,10,11,12
D2 = J5,6,7,8
D1 = J1,2,3,4

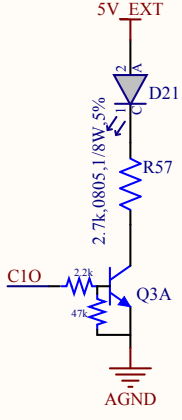
*divide by 500, set osc to 50kHz for f=100Hz (includes /2 from flip flop)

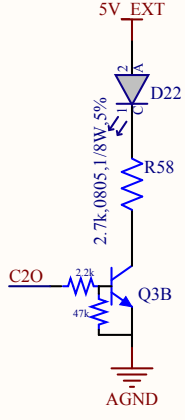
Title	CLOCKS AND WATCHDOG	
Size: A	Number:	Revision:
Date: 2/23/2011	Sheet of	
File: C:\Documents and Settings\..\clock div.SchDoc	Drawn By:	

Comparator thresholds

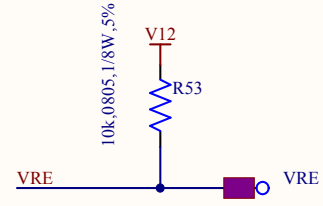


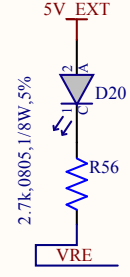




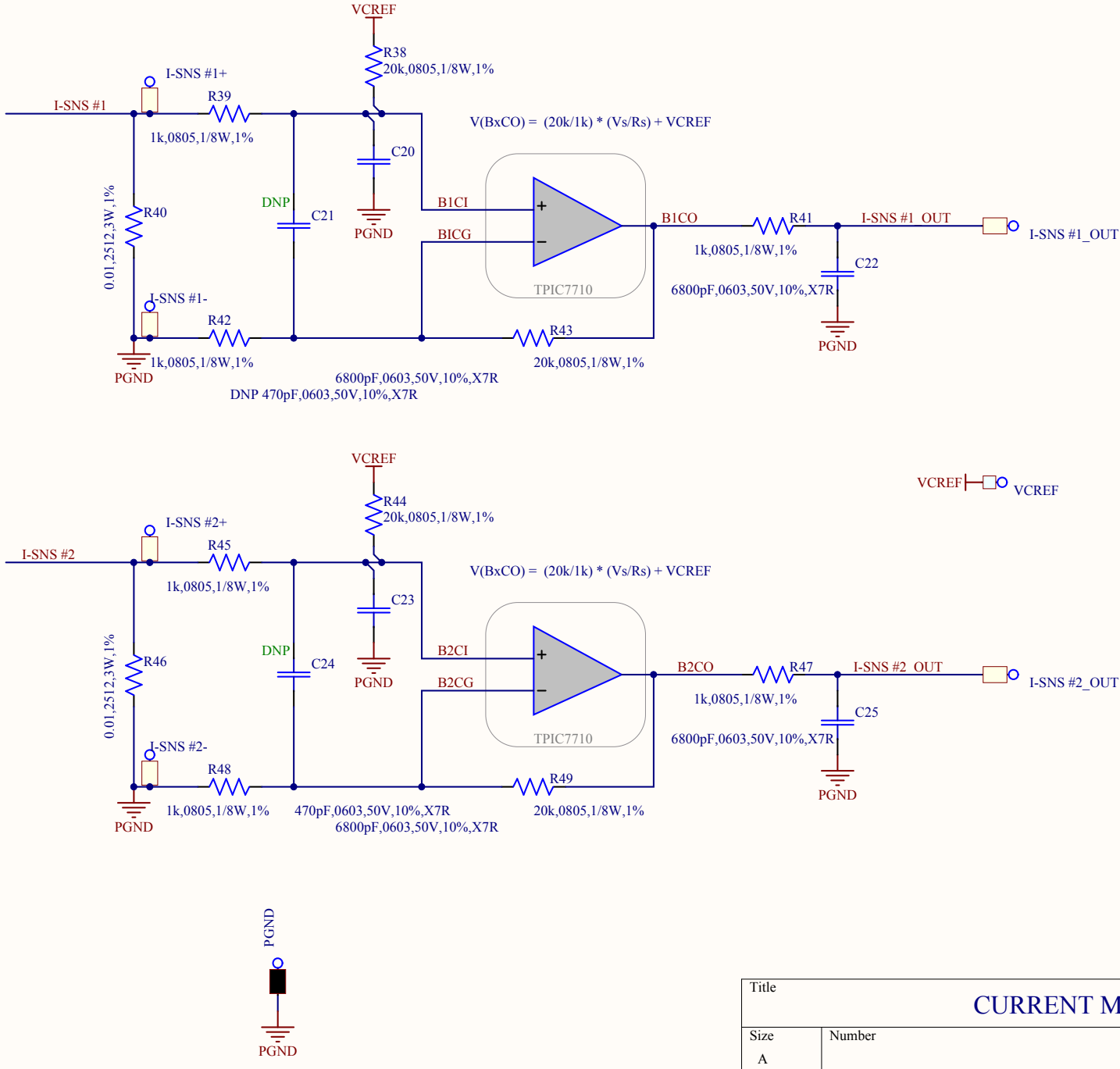


Control Signal for external Regulator



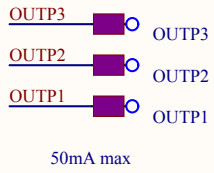


Title	COMPARATORS / VRE	
Size: A	Number:	Revision:
Date: 2/23/2011	Sheet of	
File: C:\Documents and Settings\..\comparators.SchDoc	Drawn By:	

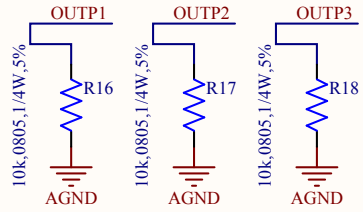


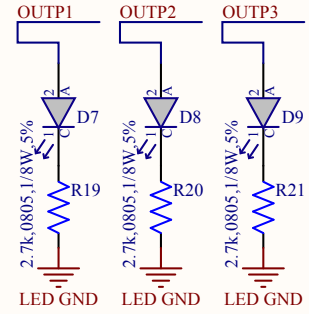
Title	CURRENT MEASURE	
Size: A	Number:	Revision:
Date: 2/23/2011	Sheet of	
File: C:\Documents and Settings\..\cur meas.SchDoc	Drawn By:	

external high-side drivers

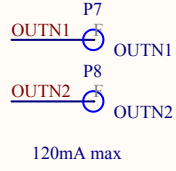


50mA max

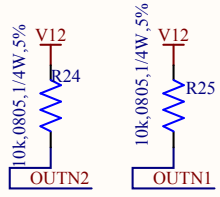




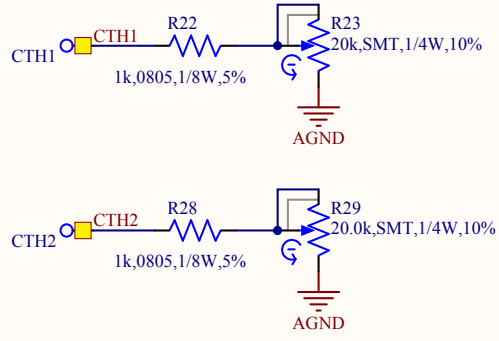
external low-side drivers



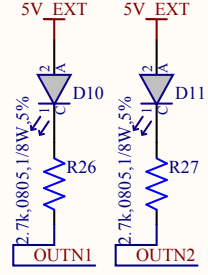
120mA max



current threshold for OUTN1/2

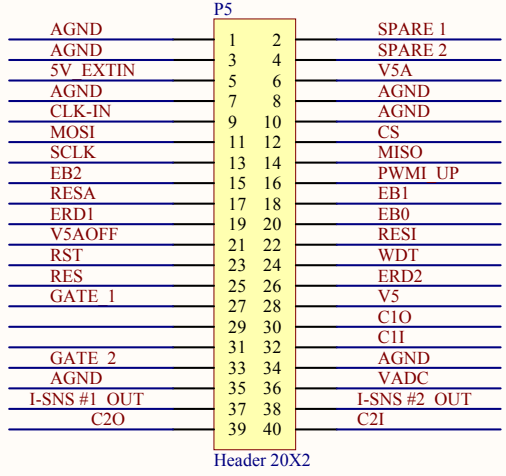


Ith = 160(Vcth/R)



Title: DRIVERS		
Size: A	Number:	Revision:
Date: 2/23/2011	Sheet of	
File: C:\Documents and Settings\..\drivers.SchDoc	Drawn By:	

Connection for external microprocessors



Title	External Primary/Secondary uP	
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Date: 2/23/2011	Sheet of	
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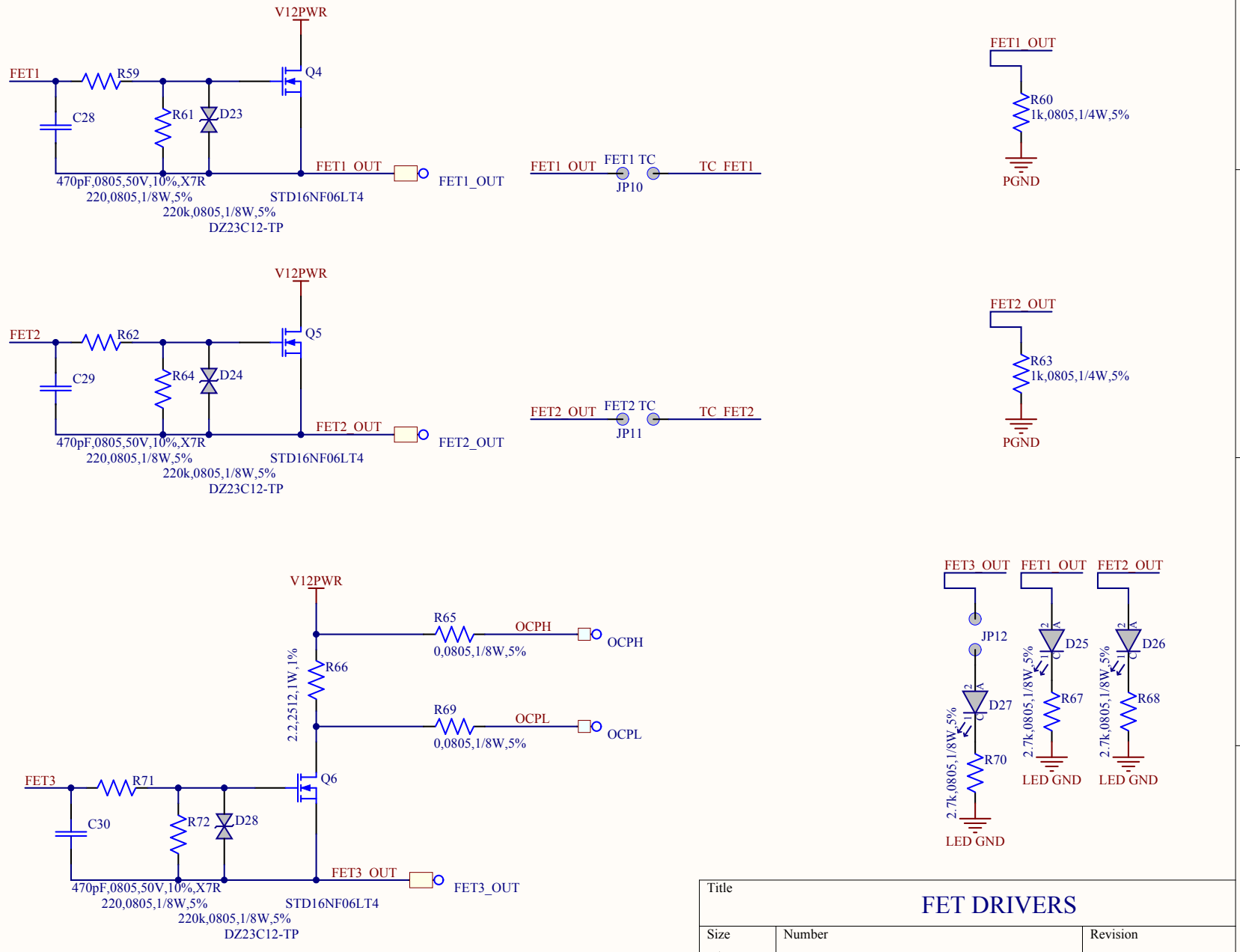
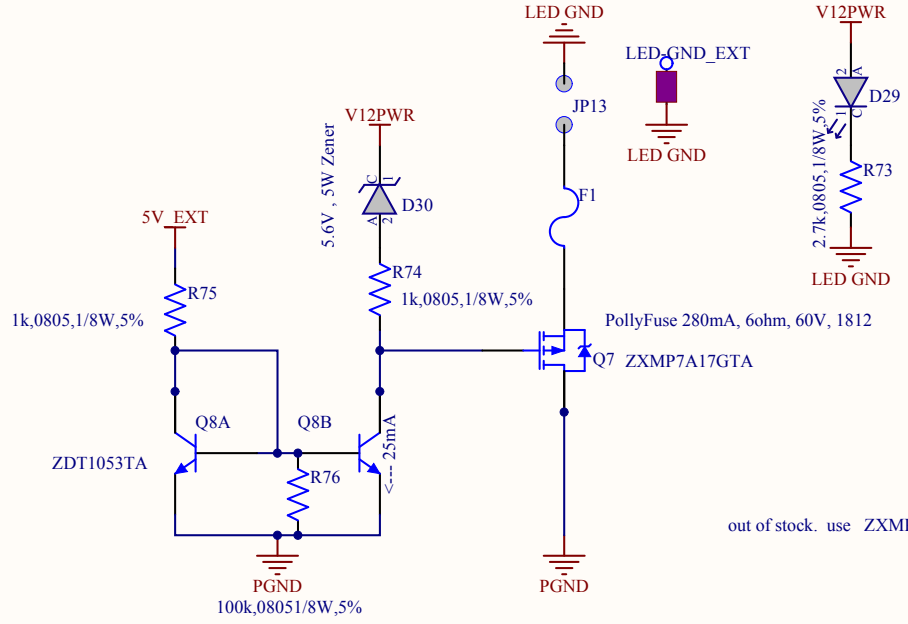


SUD15N06-90L-E3 ---> STD16NF06LT4

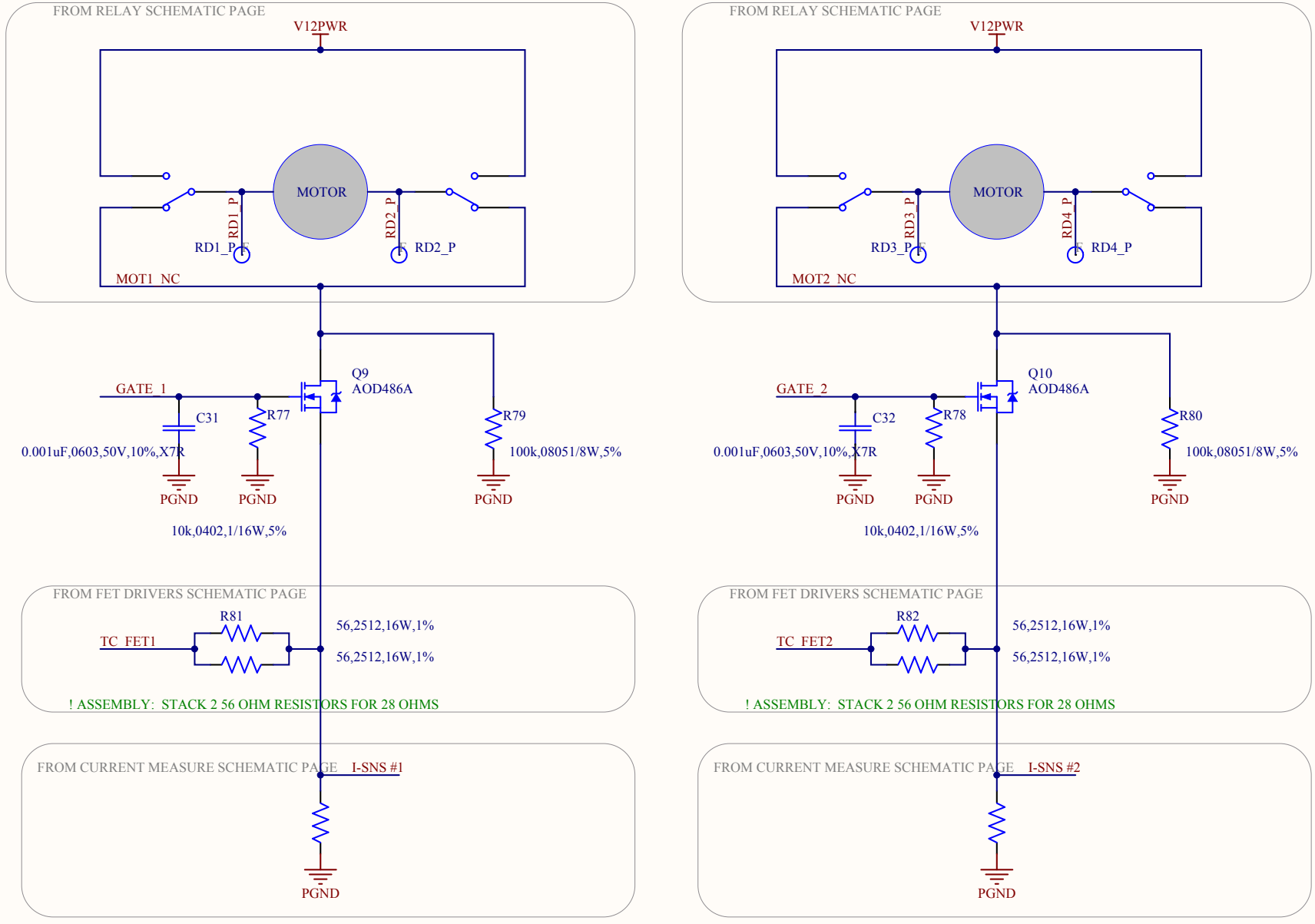
Title	FET DRIVERS	
Size: A	Number	Revision
Date: 2/23/2011	Sheet of	
File: C:\Documents and Settings\..\FET drivers.SchDoc	Drawn By:	

CIRCUIT TO CLAMP VOLTAGE TO LEDS TO 5V



out of stock. use ZXMP6A13GTA

Title	FLOATING GND (FOR LEDS)	
Size: A	Number:	Revision:
Date: 2/23/2011	Sheet of	
File: C:\Documents and Settings\..\LED GND.SchDoc	Drawn By:	



Title	MOTOR	
Size: A	Number:	Revision:
Date: 2/23/2011	Sheet of	
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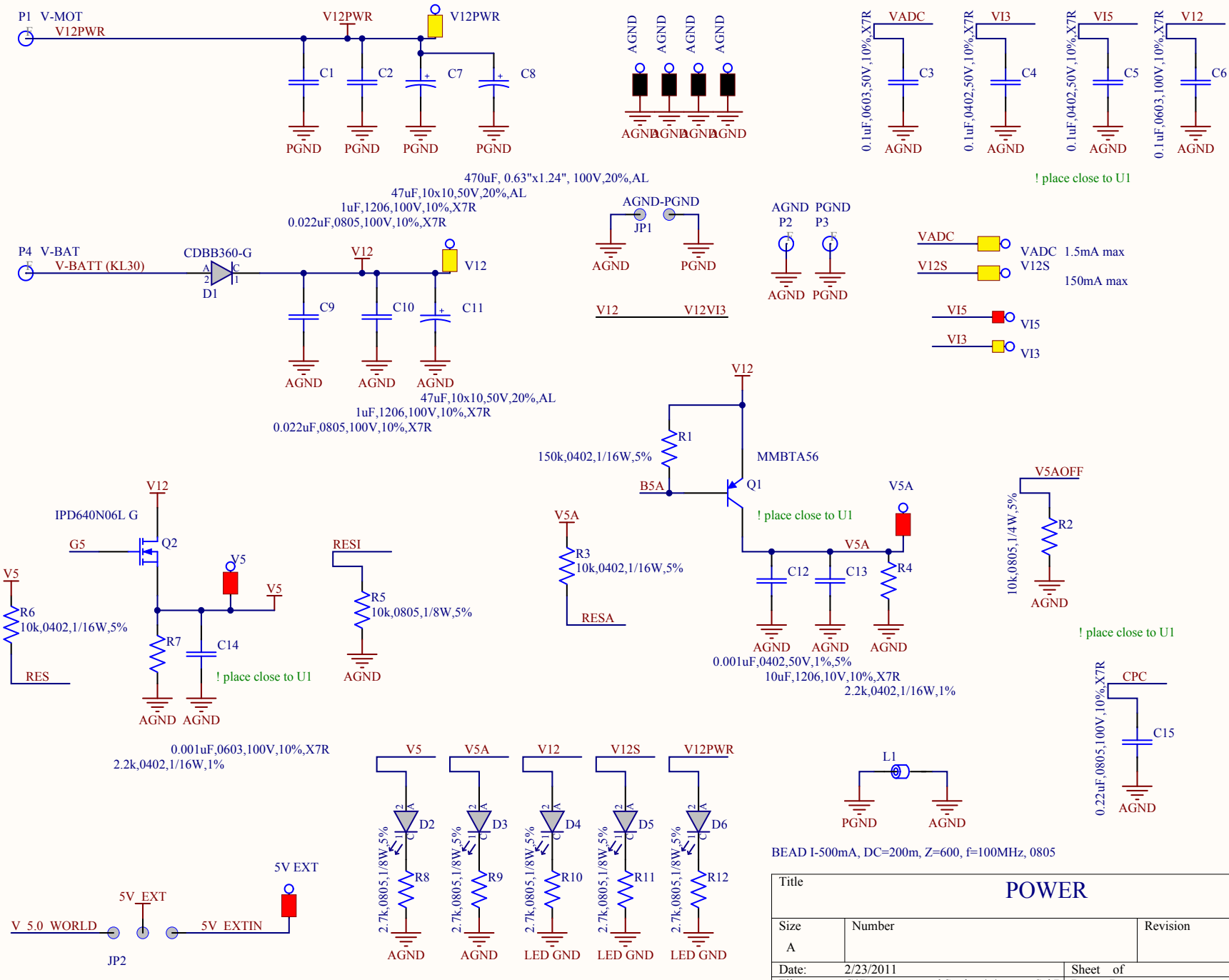
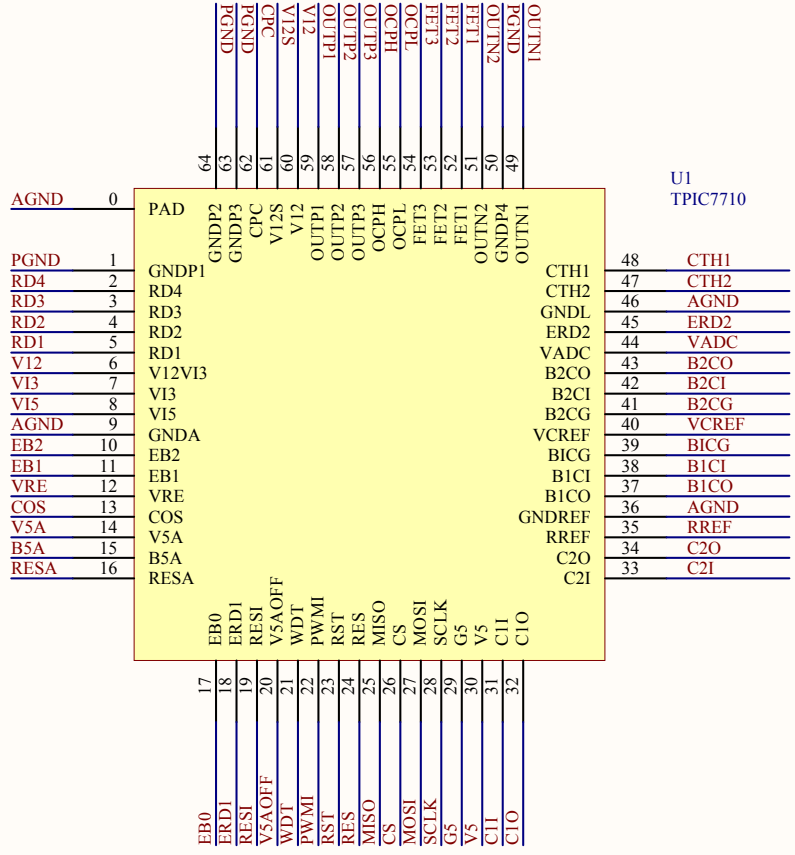
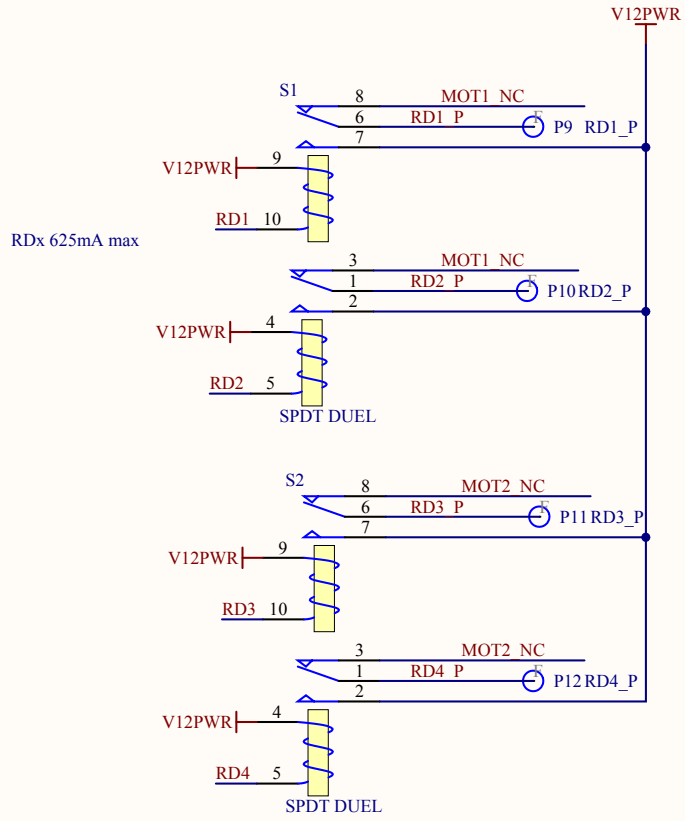
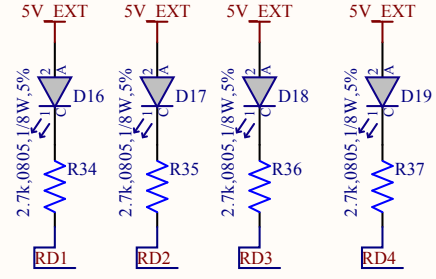

P1 V-MOT
V12PWR
V12PWR
V12PWR
C1
C2
C7
C8
PGND
PGND
PGND
PGND
AGND
AGND
AGND
AGND
AGND
AGND
AGND
AGND
VADC
VI3
VI5
V12
0.1uF,0603,50V,10%,X7R
0.1uF,0402,50V,10%,X7R
0.1uF,0402,50V,10%,X7R
0.1uF,0603,100V,10%,X7R
C3
C4
C5
C6
AGND
AGND
AGND
AGND
! place close to U1
470uF, 0.63"x1.24", 100V,20%,AL
47uF,10x10,50V,20%,AL
1uF,1206,100V,10%,X7R
0.022uF,0805,100V,10%,X7R
AGND-PGND
JP1
AGND
PGND
AGND PGND
P2 P3
AGND PGND
VADC
V12S
VADC 1.5mA max
V12S
150mA max
VI5
VI3
VI5
VI3
P4 V-BAT
V-BATT (KL30)
CDBB360-G
D1
V12
V12
C9
C10
C11
AGND
AGND
AGND
V12
V12VI3
47uF,10x10,50V,20%,AL
1uF,1206,100V,10%,X7R
0.022uF,0805,100V,10%,X7R
V12
R1
150k,0402,1/16W,5%
MMBTA56
B5A
Q1
V5A
V5A
R3
10k,0402,1/16W,5%
RESA
! place close to U1
V5AOFF
R2
10k,0805,1/4W,5%
AGND
V5A
R4
C12
C13
AGND
AGND
AGND
0.001uF,0402,50V,1%,5%
10uF,1206,10V,10%,X7R
2.2k,0402,1/16W,1%
! place close to U1
CPC
C15
0.22uF,0805,100V,10%,X7R
AGND
V12
IPD640N06L G
G5
Q2
V5
V5
V5
R6
10k,0402,1/16W,5%
RES
R7
C14
AGND
AGND
! place close to U1
RESI
R5
10k,0805,1/8W,5%
AGND
0.001uF,0603,100V,10%,X7R
2.2k,0402,1/16W,1%
V5
V5A
V12
V12S
V12PWR
D2
D3
D4
D5
D6
R8
R9
R10
R11
R12
2.7k,0805,1/8W,5%
AGND
AGND
LED GND
LED GND
LED GND
L1
PGND
AGND
BEAD I-500mA, DC=200m, Z=600, f=100MHz, 0805
5V EXT
5V_EXT
V_5.0_WORLD
5V_EXTIN
JP2
Title
POWER
Size
A
Number
Revision
Date: 2/23/2011
Sheet of
File: C:\Documents and Settings\..\power.SchDoc
Drawn By:

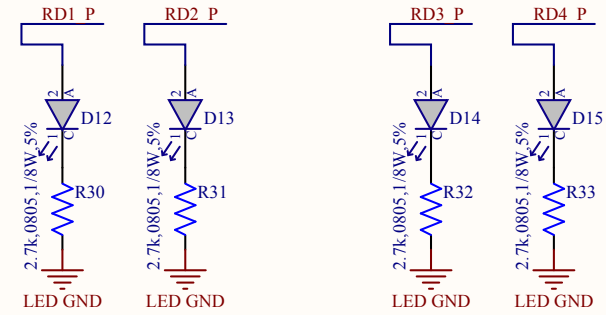


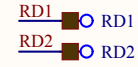
Title	**SN0805025QFP TPIC7710**	
Size: A	Number	Revision
Date: 2/23/2011	Sheet of	
File: C:\Documents and Settings\..\product.SchDoc	Drawn By:	

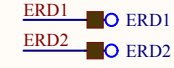
TI BUG

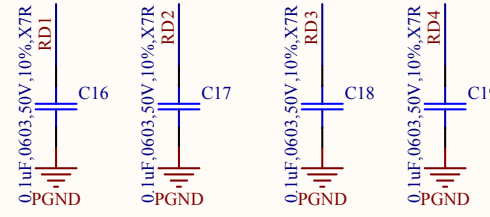












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Date: 2/23/2011	Sheet of	
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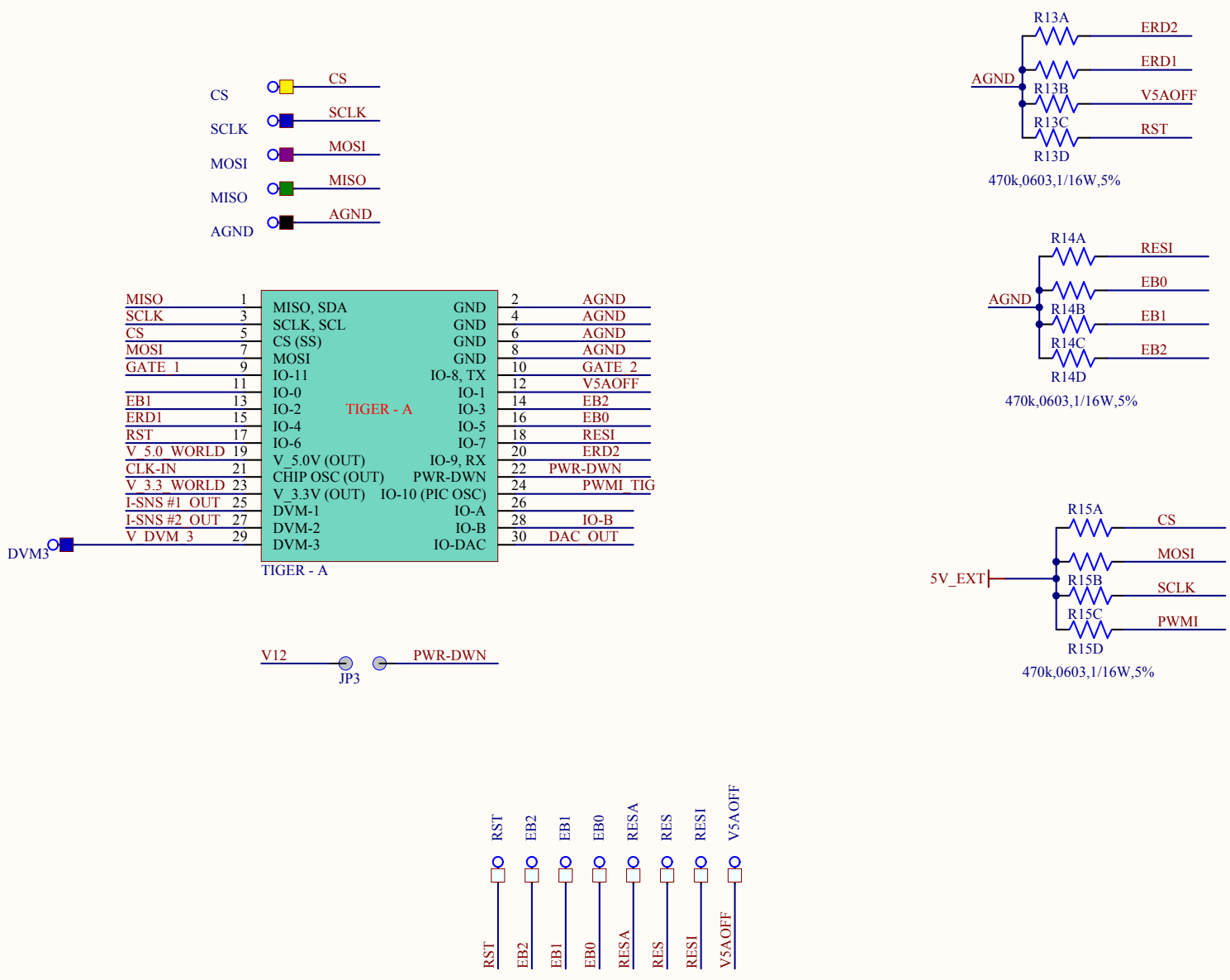
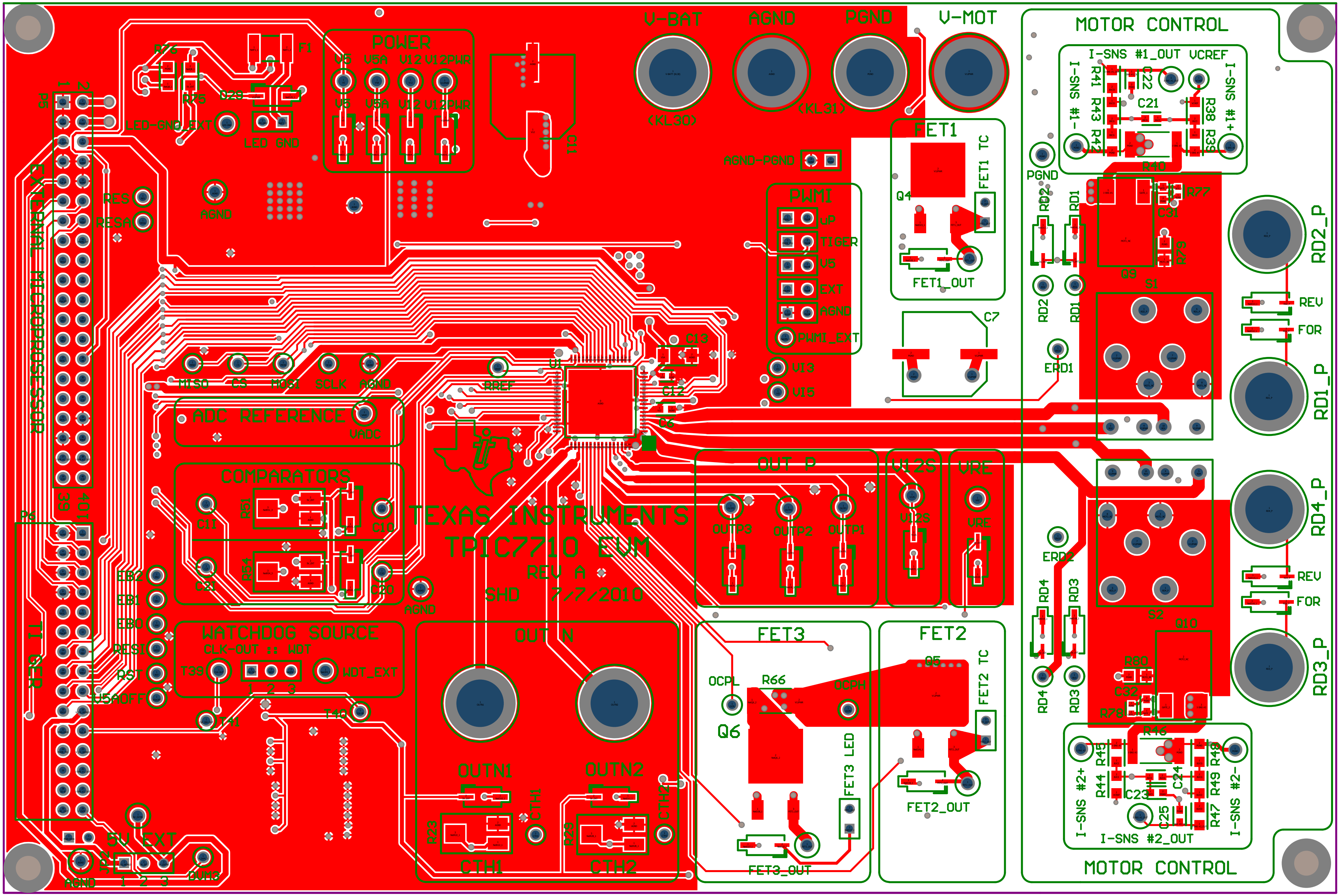
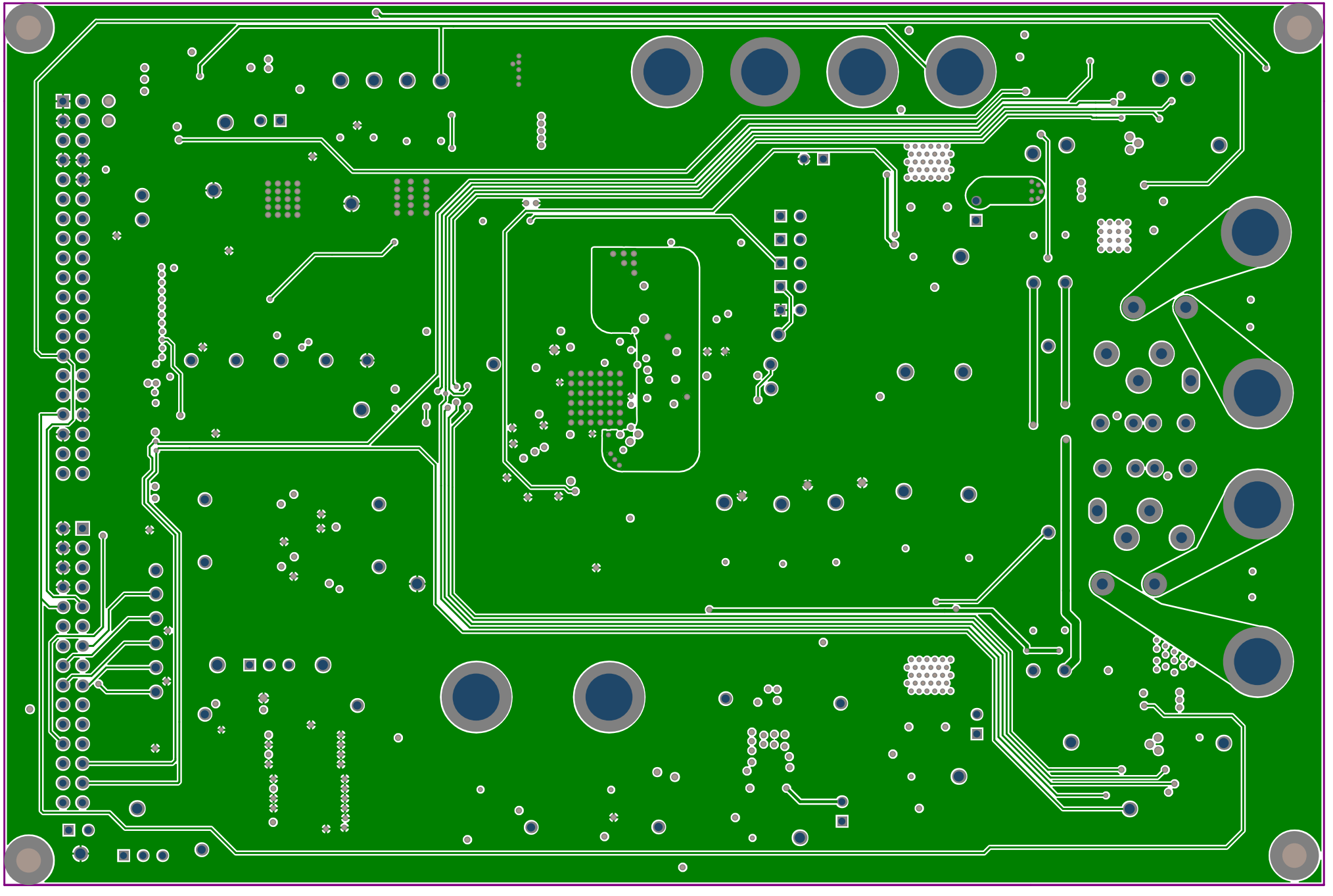
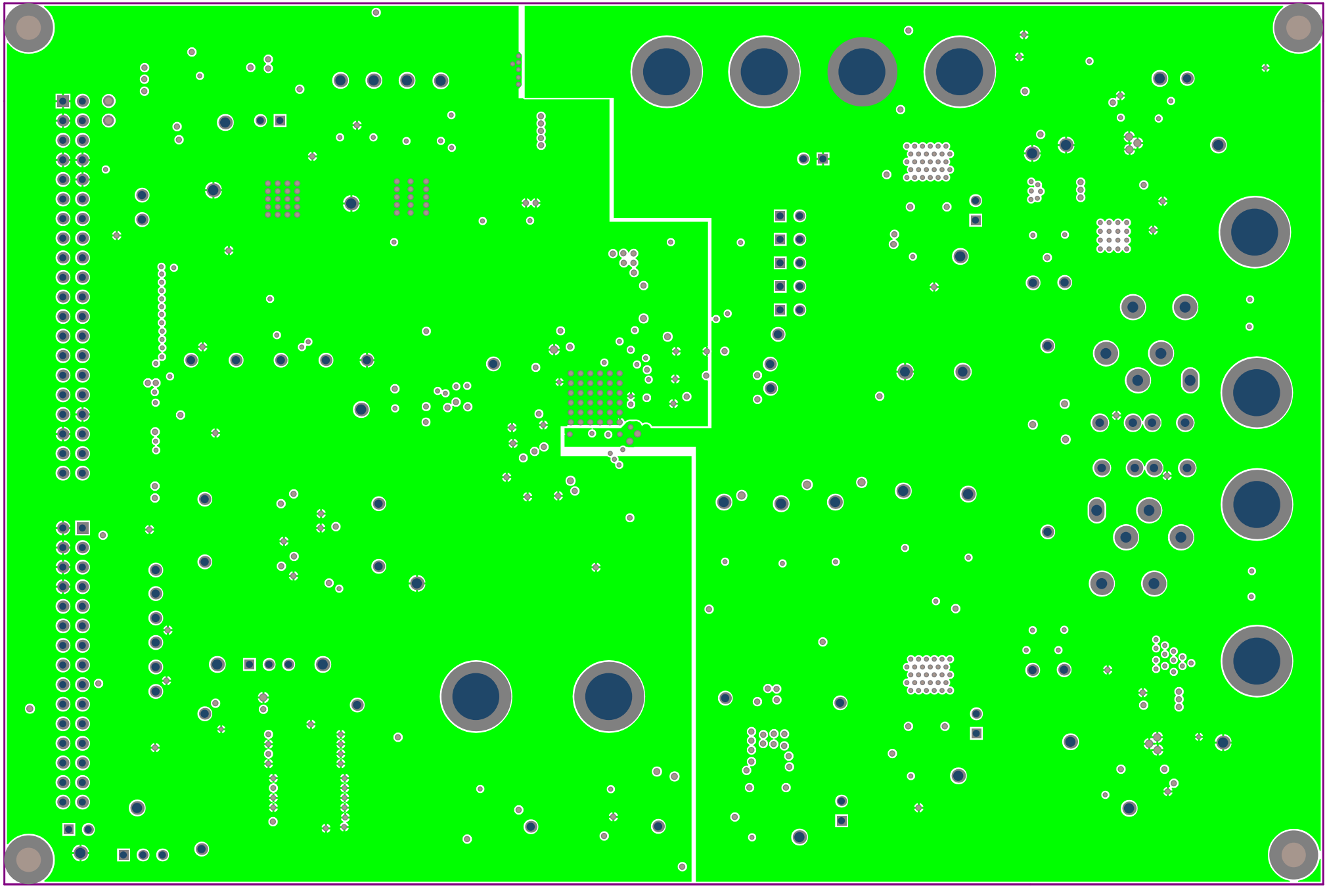
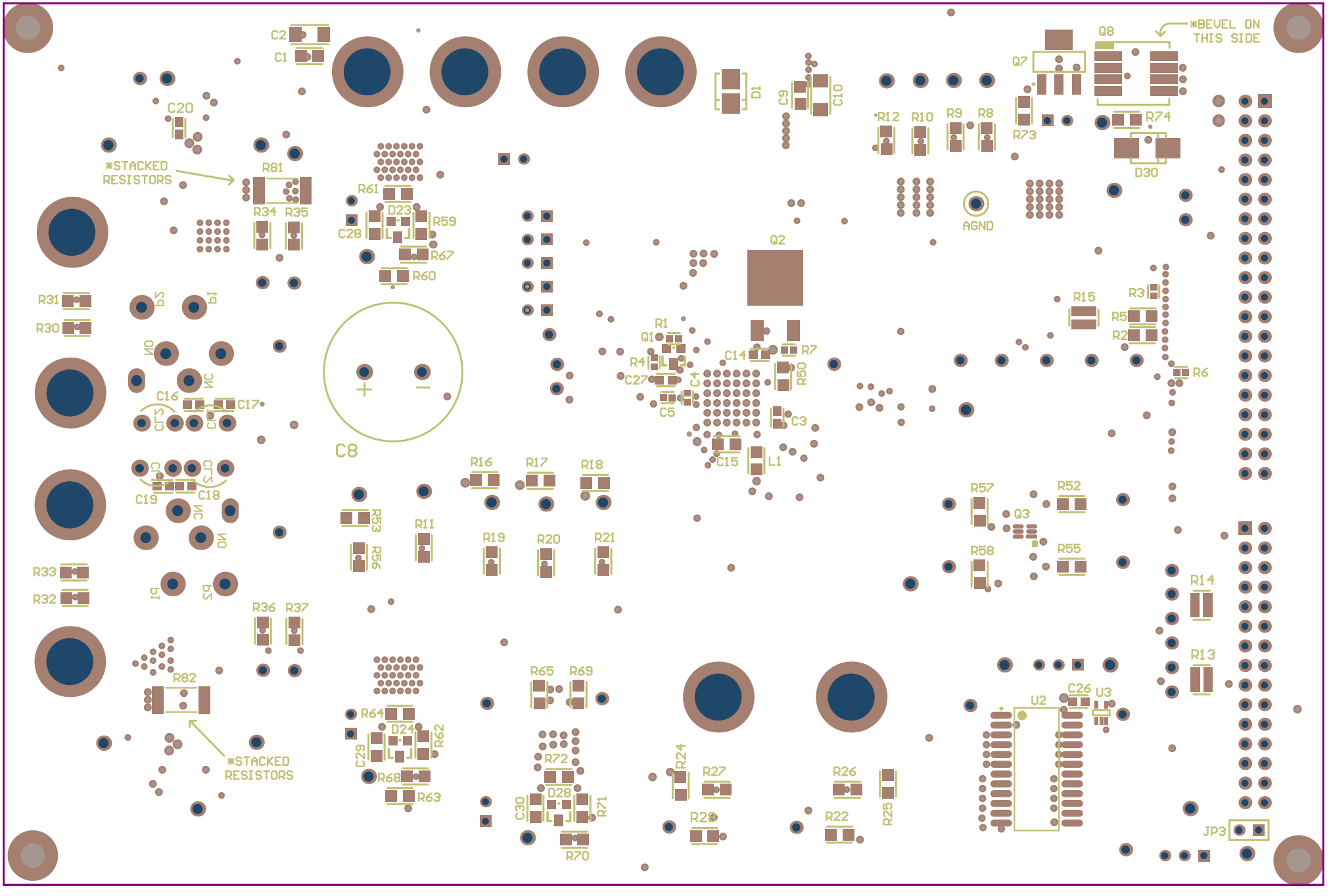


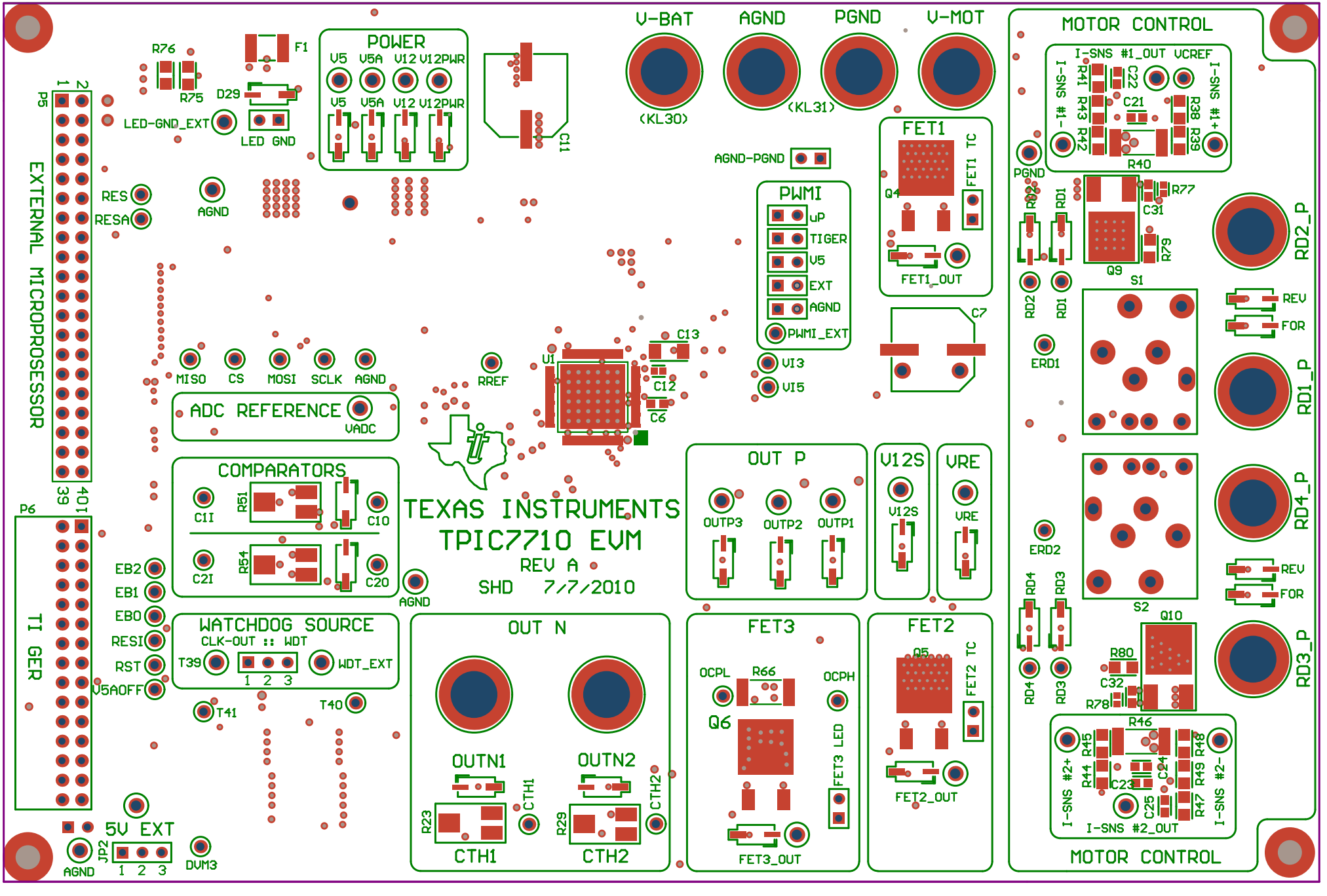
Title	TI GER	
Size: A	Number:	Revision:
Date: 2/23/2011	Sheet of	
File: C:\Documents and Settings\..\TI GER.SchDoc	Drawn By:	

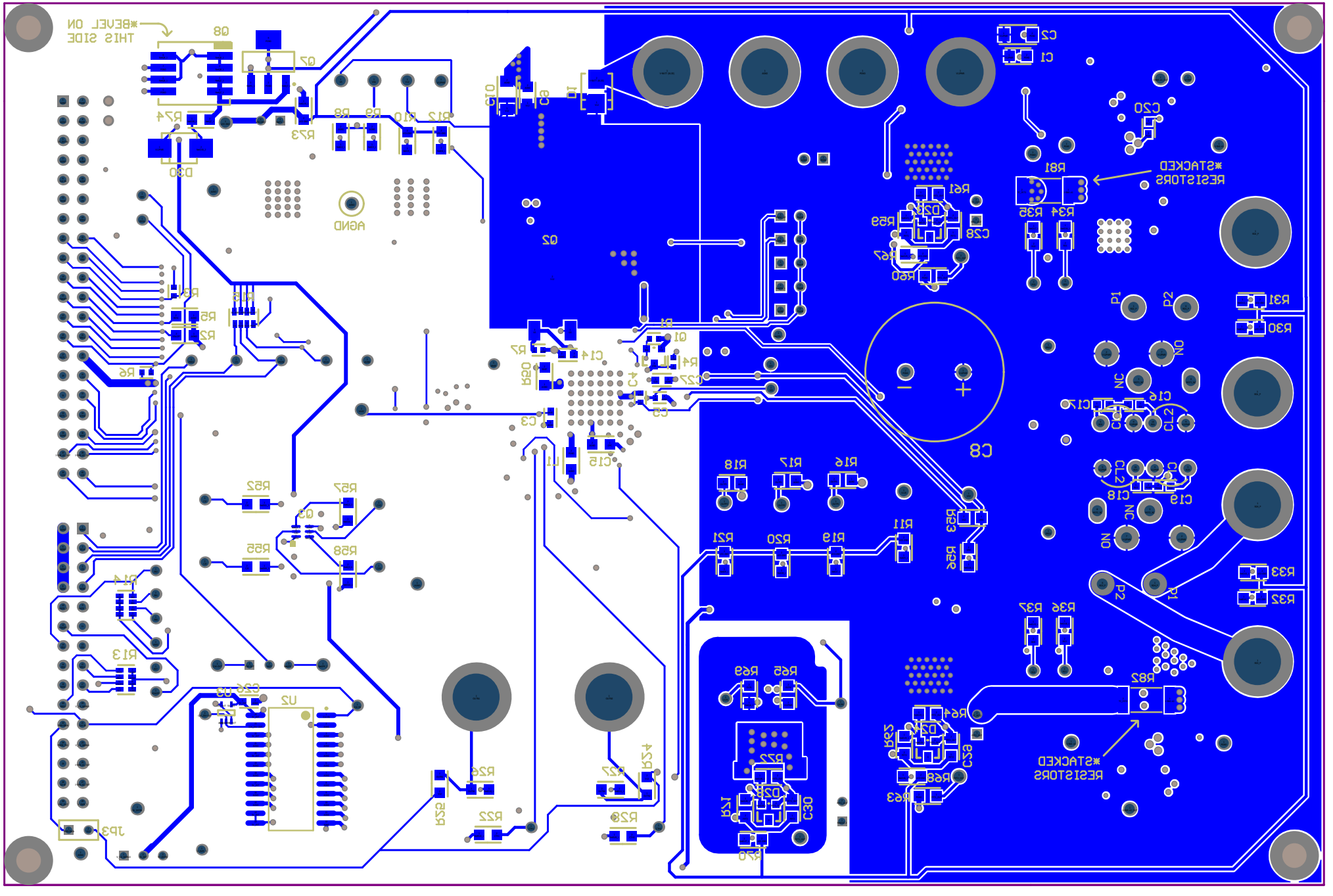

TEXAS INSTRUMENTS
TPIC7710 EVM
REV A
SHD 7/7/2010
POWER
V5 V5A V12 V12PWR
V-BAT
AGND
PGND
V-MOT
(KL30)
(KL31)
MOTOR CONTROL
I-SNS #1_OUT VCREF
FET1
FET1 TC
FET1_OUT
AGND-PGND
PWMI
UP
TIGER
V5
EXT
AGND
PWMI_EXT
V13
V15
C7
RD2_P
RD1_P
RD4_P
RD3_P
REV
FOR
S1
S2
Q9
Q10
ERD1
ERD2
EXTERNAL MICROPROCESSOR
LED-GND_EXT
LED GND
RES
RESA
AGND
MISO
CS
MOSI
SCLK
RREF
ADC REFERENCE
VADC
COMPARATORS
C11
C10
C21
C20
OUT P
OUTP3
OUTP2
OUTP1
V12S
VRE
WATCHDOG SOURCE
CLK-OUT :: WDT
T39
WDT_EXT
T41
T40
OUT N
OUTN1
OUTN2
CTH1
CTH2
FET3
OCPL
R66
OCPH
Q6
FET3 LED
FET3_OUT
FET2
FET2 TC
Q5
FET2_OUT
I-SNS #2_OUT
TI GER
5V EXT
AGND
OVMJ
RST
V5AOFF

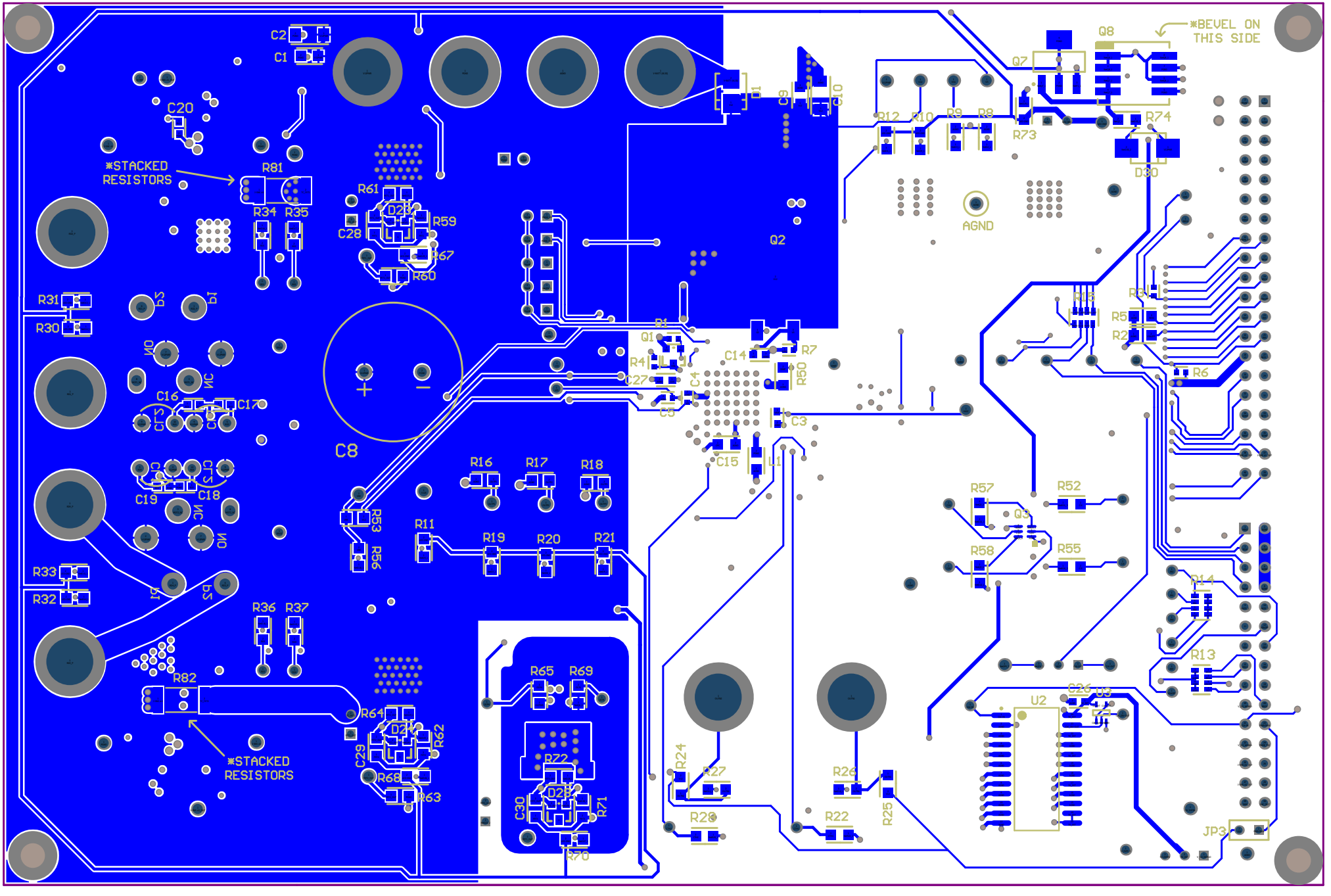


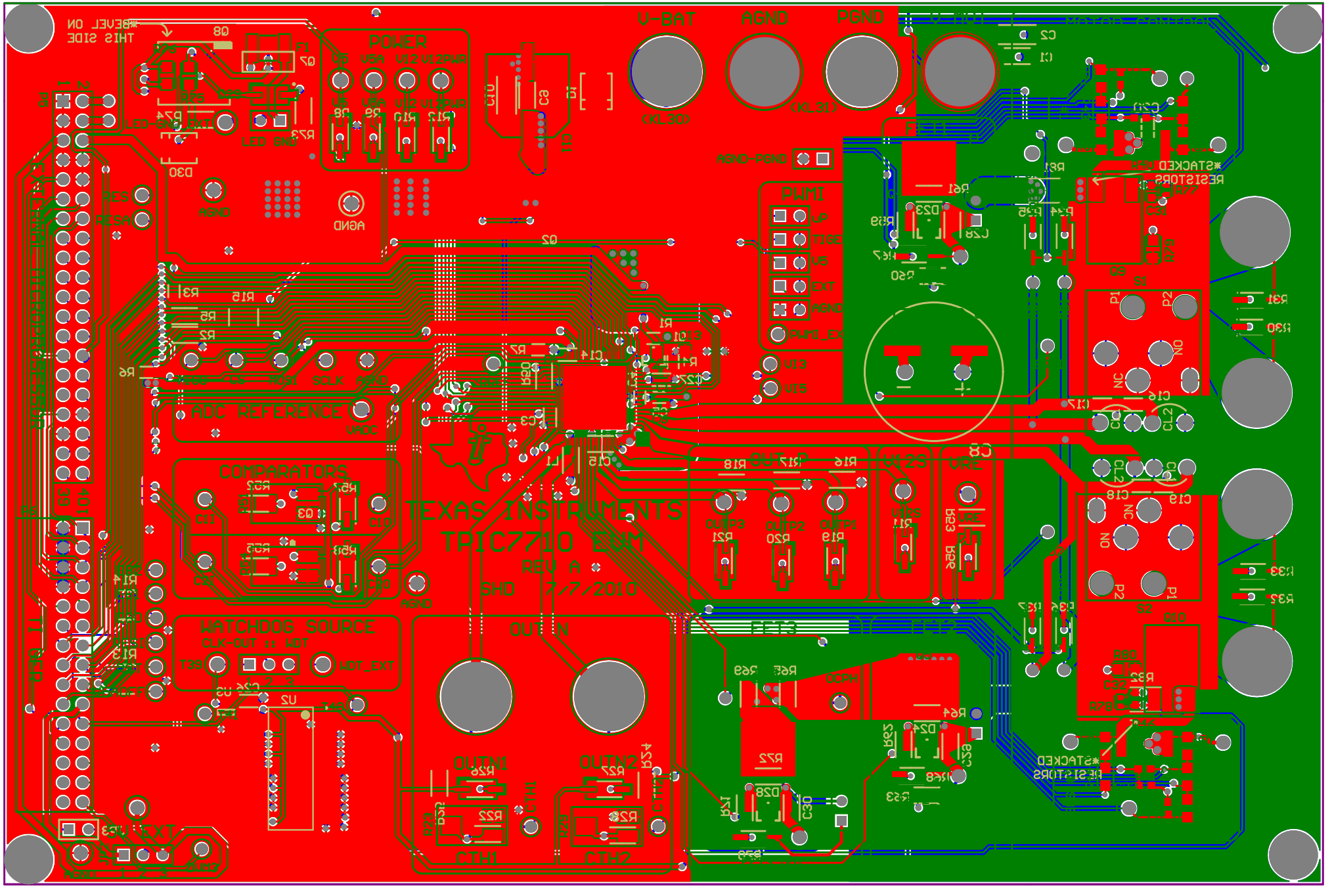



C2
C1
C20
*STACKED RESISTORS
R81
R34
R35
R61
D23
C28
R59
R67
R60
D1
C9
C10
*R12
R10
R9
R8
Q7
Q8
*BEVEL ON THIS SIDE
R73
R74
D30
AGND
Q2
R31
R30
R1
Q1
R4
C27
C14
R7
R50
C4
C5
C3
C15
L1
R15
R3
R5
R2
R6
C16
C17
C19
C18
C8
R16
R17
R18
R53
R56
R11
R19
R20
R21
R57
R52
Q3
R58
R55
R33
R32
R36
R37
R14
R13
R82
*STACKED RESISTORS
R64
D24
C29
R62
R68
R63
R65
R69
R72
D28
C30
R71
R70
R24
R27
R28
R26
R22
R25
U2
C26
U3
JP3


V-BAT
AGND
PGND
V-MOT
(KL30)
(KL31)
POWER
V5 V5A V12 V12PWR
V5 V5A V12 V12PWR
F1
R76
R75
D29
LED-GND_EXT
LED GND
C11
AGND-PGND
PWMI
uP
TIGER
V5
EXT
AGND
PWMI_EXT
VI3
VI5
FET1
Q4
FET1 TC
FET1_OUT
C7
MOTOR CONTROL
I-SNS #1_OUT VCREF
I-SNS -#1
I-SNS +#1
R41
R42
R43
C22
C21
R38
R39
R40
PGND
RD2_P
RD1_P
RD4_P
RD3_P
RD2
RD1
RD4
RD3
R77
C31
R79
Q9
Q10
S1
S2
REV
FOR
ERD1
ERD2
R80
C32
R78
R46
R45
R44
R48
R49
R47
C24
C23
C25
I-SNS #2+
I-SNS #2-
I-SNS #2_OUT
MOTOR CONTROL
EXTERNAL MICROPROSESSOR
P5
1
2
39
40
RES
RESA
AGND
MISO
CS
MOSI
SCLK
AGND
ADC REFERENCE
VADC
RREF
U1
C13
C12
C6
COMPARATORS
C1I
R51
C1O
C2I
R54
C2O
AGND
TEXAS INSTRUMENTS
TPIC7710 EVM
REV A
SHD 7/7/2010
OUT P
OUTP3
OUTP2
OUTP1
V12S
VRE
P6
TI GER
EB2
EB1
EB0
RESI
RST
V5AOFF
WATCHDOG SOURCE
CLK-OUT :: WDT
T39
WDT_EXT
1 2 3
T41
T40
OUT N
OUTN1
OUTN2
R23
CTH1
R29
CTH2
CTH1
CTH2
FET3
OCPL
R66
OCPH
Q6
FET3 LED
FET3_OUT
FET2
Q5
FET2 TC
FET2_OUT
5V EXT
JP2
1 2 3
AGND
DVM3


*BEVEL ON THIS SIDE
*STACKED RESISTORS
*STACKED RESISTORS
AGND
C8


*STACKED RESISTORS
*STACKED RESISTORS
*BEVEL ON THIS SIDE
AGND
C1
C2
C8
C20
R81
R34
R35
R61
C28
D28
R59
R67
R60
Q2
Q1
R4
C27
C5
C4
C14
R7
R50
C3
C15
L1
R16
R17
R18
R19
R20
R21
R11
R53
R56
R31
R30
R33
R32
R36
R37
R82
R64
C29
D29
R62
R68
R63
R65
R69
R72
D27
C30
R71
R70
R24
R27
R28
R26
R22
R25
Q8
Q7
R12
R10
R9
R8
R73
R74
D30
R54
R5
R2
R6
R57
R52
Q3
R58
R55
R14
R13
U2
C26
C25
JP3


U-BAT
AGND
PGND
POWER
PWMI
ADC REFERENCE
COMPARATORS
WATCHDOG SOURCE
TEXAS INSTRUMENTS
TPIC7710 EVM
REV A
SHD
7/7/2010
OUTP
OUTN
OUTN1
OUTN2
CTH1
CTH2
EXT

Evaluation Board/Kit Important Notice

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 0 V to xxx V and the output voltage range of 0 V to 14 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 145° C. The EVM is designed to operate properly with certain components above 145° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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