TEXAS INSTRUMENTS

DEM-DAI1803EVM

PCM1803 WITH DIGITAL AUDIO TRANSMITTER

User's Guide

April 2005 Audio Converter, Digital Audio (DCES Japan)

SLEU061

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Literature Number: SLEU061
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TEXAS INSTRUMENTS

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Description

The DEM-DAI1803 is an evaluation board for the PCM1803, a 96-kHz, 24-bit PCM audio A/D converter, with digital audio transmitter, mode-control switches and jumpers, onboard oscillator, –6-dB amplifier, and low-pass filter (LPF).

The DEM-DAI1803 operates from 5-V and ±15-V analog power supplies with 1-V rms or 2-V rms unbalanced analog signal input.

1.1 BLOCK DIAGRAM

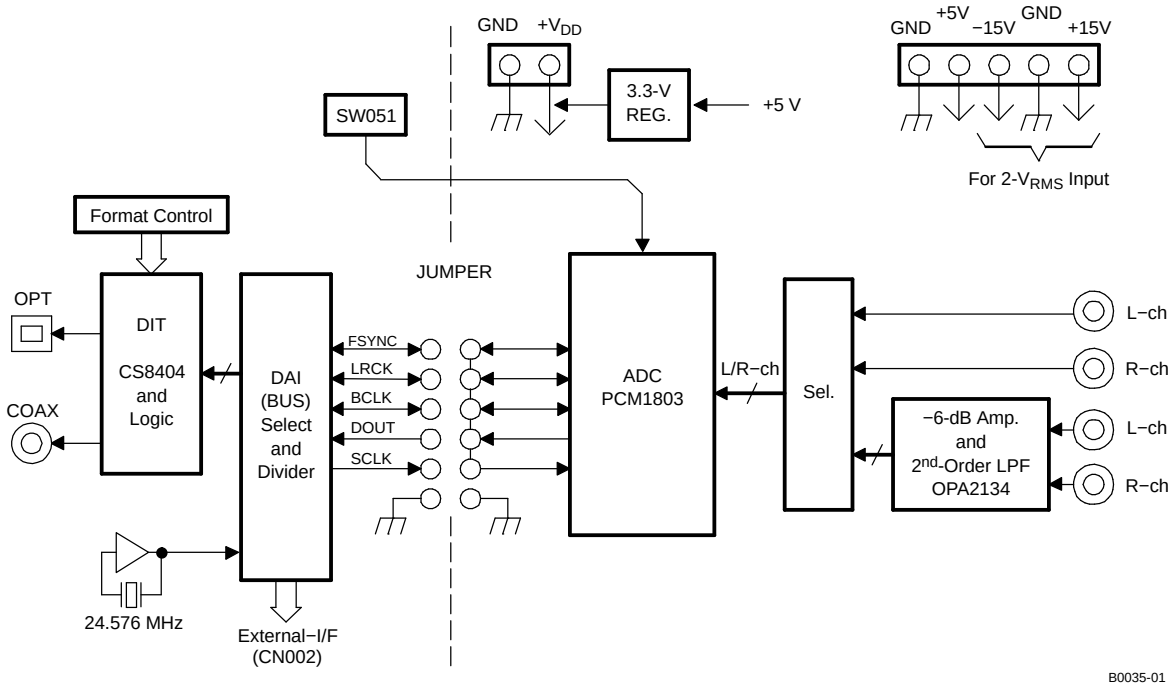


Figure 1-1. DEM-DAI1803 Block Diagram

1.2 DEM-DAI1803 BASIC CONNECTION AND OPERATION

1.2.1 BASIC CONNECTIONS

- Connect the 5-V and ±15-V power supplies to V_{CC}, AV_{CC}, $–AV_{CC}$, and GND on connectors CN051–CN055. The ±15-V supplies are required only for 2-V rms input.
- Connect the S/PDIF output to CN003 (coaxial) or U001 (optical).
- Ensure the presence of a system clock, supplied from the onboard oscillator or external input clock connector (CN001) through switch/jumper to the PCM1803.
- Set the data format using SW001, JP003, and SW051.
- Select the master or slave mode using SW002, SW051, JP002, JP004, and JP052.

1.2.2 CONFIGURATION CONTROLS

1.2.2.1 Analog Input Selection

Analog input up to 1 V rms is connected to CN103 and CN104. Analog input up to 2 V rms is connected to CN101 and CN102. The connector selection and corresponding jumper settings for JP101 and JP102 are shown in Table 1-1.

Table 1-1. Analog Input Selection (JP101 and JP102)

INPUT	JUMPER POSITION	INPUT CONNECTORS
1 V rms	Direct-IN	CN103 and CN104
2 V rms	–6dB/LPF	CN101 and CN102

1.2.2.2 HPF Bypass Control

The BYPAS section of SW051 is set to enable or disable (bypass) the high-pass filter of the PCM1803. Switch settings are shown in Table 1-2.

Table 1-2. PCM1803: HPF Bypass Control (SW051)

HPF BYPASS	BYPAS (SW051)
Enabled	H
Disabled	L

1.2.2.3 Oversampling Control

The oversampling rate of the PCM1803 can be selected using the OSR section of SW051, as shown in Table 1-3. The available oversampling rates are 64 f_S and 128 f_S.

Table 1-3. PCM1803: Oversampling Control (SW051)

OVERSAMPLING	OSR (SW051)
×128 f_S	H
×64 f_S	L

1.2.2.4 Master/Slave and System Clock Speed

The PCM1803 can be operated as a master or slave device, and when operating as a master, the system clock speed can be set. For each combination of master/slave operation mode and system clock speed in the two leftmost columns of Table 1-4, the remaining columns of the table show the mandatory and optional settings of the SW002 switch and SW051 MODE0 and MODE1 switches and of the JP002, JP004, and JP052 FSYNC jumpers.

Table 1-4. PCM1803: Master/Slave and Oversampling Rate Selection (JP002/004/052 and SW002/051)

MODE	SYSCLK	MODE1 (SW051)	MODE0 (SW051)	M/S select (SW002)	BCK sel (JP002)	LRCK sel (JP004)	FSYNC (JP052)
Master mode	512 f_S	L	H	Master	Remove jumper	Remove jumper	Master
	384 f_S	H	L				
	256 f_S	H	H				
Slave mode	Auto-detect	L	L	Slave	Select /2, /4, or /8 (See Table 1-6)	Select /128, /256, or /512 (See Table 1-7)	Install SLAVE jumper

1.2.2.5 System-Clock Dividing Ratio

Jumper JP001 settings and the corresponding system-clock dividing ratios are listed in Table 1-5. The MCK values in the table are based on using the internal 24.576-MHz oscillator or an external clock of equal frequency (see Section 1.2.2.9).

Table 1-5. System-Clock Dividing Ratio for MCK: 128 f_S-CS8404 (JP001)

DIVIDING RATIO	JUMPER POSITION	MCK VALUE
1/1	/1	–
1/2	/2	12.288 MHz (128 f_S for f_S = 96 kHz)
1/4	/4	6.144 MHz (128 f_S for f_S = 48 kHz)

1.2.2.6 Bit-Clock Dividing Ratio

Jumper JP002 settings and the corresponding bit-clock dividing ratios are listed in Table 1-6. The BCK values in the table are based on using the internal 24.576-MHz oscillator or an external clock of equal frequency (see Section 1.2.2.9).

Table 1-6. Bit-Clock Dividing Ratio (JP002)

DIVIDING RATIO	JUMPER POSITION	BCK VALUE
1/2 (Slave)	/2	12.288 MHz (64 f_S for f_S = 192 kHz)
1/4 (Slave)	/4	6.144 MHz (64 f_S for f_S = 96 kHz)
1/8 (Slave)	/8	3.072 MHz (64 f_S for f_S = 48 kHz)
– (Master)	Remove	–

1.2.2.7 LR-Clock Dividing Ratio

Jumper JP004 settings and the corresponding LR-clock dividing ratios are listed in Table 1-7. The BCK values in the table are based on using the internal 24.576-MHz oscillator or an external clock of equal frequency (see Section 1.2.2.9).

Table 1-7. LR-Clock Dividing Ratio (JP004)

DIVIDING RATIO	JUMPER POSITION	BCK VALUE
1/128 (Slave)	/128	192 kHz
1/256 (Slave)	/256	96 kHz
1/512 (Slave)	/512	48 kHz
– (Master)	Remove	–

1.2.2.8 Data Format Selection

Table 1-8 shows the data formats obtained by particular combinations of settings of jumper JP003 and the SW051 FMT0 and FMT1 switches.

Table 1-8. Data Format Selection (JP003 and SW051)

JP003	FMT1	FMT0	DATA FORMAT
L/J 24	L	L	PCM, left-justified, 24-bit
I^2S	L	H	PCM, I^2S, 24-bit

1.2.2.9 System-Clock Source Selection

Switch SW005 selects a clock source. The onboard (internal) clock is based on crystal X001 and operates at 24.576 MHz. The external clock is input on connector CN001. The jumper position to select each clock option is listed in Table 1-9.

Table 1-9. System-Clock Source Selection (SW005)

CLOCK SOURCE	JUMPER POSITION
Internal	INT
External	EXT

1.2.2.10 Manual Reset

The RESET switch, SW003, is a manually operated pushbutton switch. Pressing SW003 resets the CS8404.

1.2.2.11 Digital Signal Interface

The digital signals generated by the internal oscillator, divider, and PCM1803 are input to this jumper. For each pair of shorted pins, the corresponding digital signal is input to or output from the PCM1803. The layout of JP052 is shown in Figure 1-2.

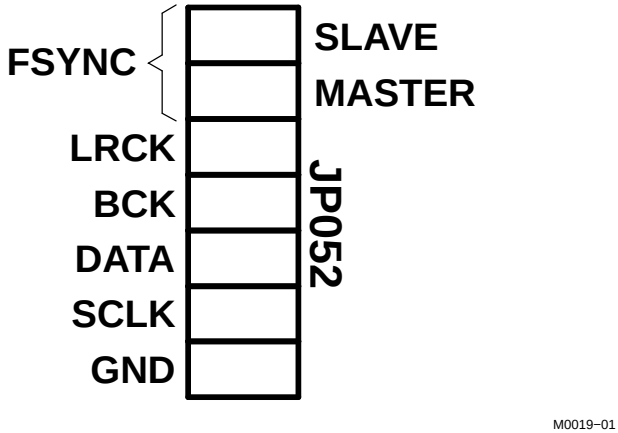


Figure 1-2. Digital Signal I/F to PCM1803 (JP052)

1.2.2.12 S/PDIF Transmitter Format

Operating configuration of the CS8404 digital audio interface transmitter can be set using the SW004 DIP switches. The individual switch settings and their functions are described in Table 1-10.

Table 1-10. S/PDIF Transmitter Format: CS8404 Configuration (SW004)

SWITCH	DESCRIPTION	SETTING (L = 0, H = 1)	FUNCTION
PROFESSIONAL MODE; PRO Switch = L (0)			
C9	C8,C9,C10,C11 – Channel mode (1 of 4)	1	0000 – Not indicated (default: 2-ch)
		0	0100 – Stereophonic
EM1, EM0	C2, C3, C4 – Emphasis (2 of 3)	11	Not indicated (default: none)
		10	No emphasis
		01	50/15Us
		00	CCITT J.17
C6, C7	C6, C7 – Sample frequency	11	Not indicated (default: 48 kHz)
		10	48 kHz
		01	44.1 kHz
		00	32 kHz
C1	C1 – Audio	1	0 – Normal audio
		0	1 – Nonaudio
TRNPT	Transparent mode	0	0 – Normal operation
		1	1 – Transparent mode
CONSUMER MODE; PRO Switch = H (1)			
C15	Generation status	1	0 – (see the S/PDIF standard)
		0	1 – (see the S/PDIF standard)
C8, C9	C8–C14 – Category code (2 of 7)	11	0000 0000 – General
		10	0100 0000 – PCM encoder/decoder
		01	1000 0000 – CD
		00	1100 0000 – DAT
C3	C3, C4, C5 – Emphasis (1 of 3)	1	000 – None
		0	100 – 50/15Us
C2	C2 – Copy/copyright	1	0 – Copy inhibited/copyright asserted
		0	1 – Copy permitted/copyright not asserted
FC1, FC0	C24, C25, C26, C27 – Sample frequency	11	44.1 kHz
		10	48 kHz
		01	32 kHz
		00	44.1 kHz, CD mode

SCHEMATICS AND PRINTED-CIRCUIT BOARD

This chapter presents the DEM-DAI1803 printed-circuit board and the DEM-DAI1803 schematics.

2.1 DEM-DAI1803 PRINTED-CIRCUIT BOARD

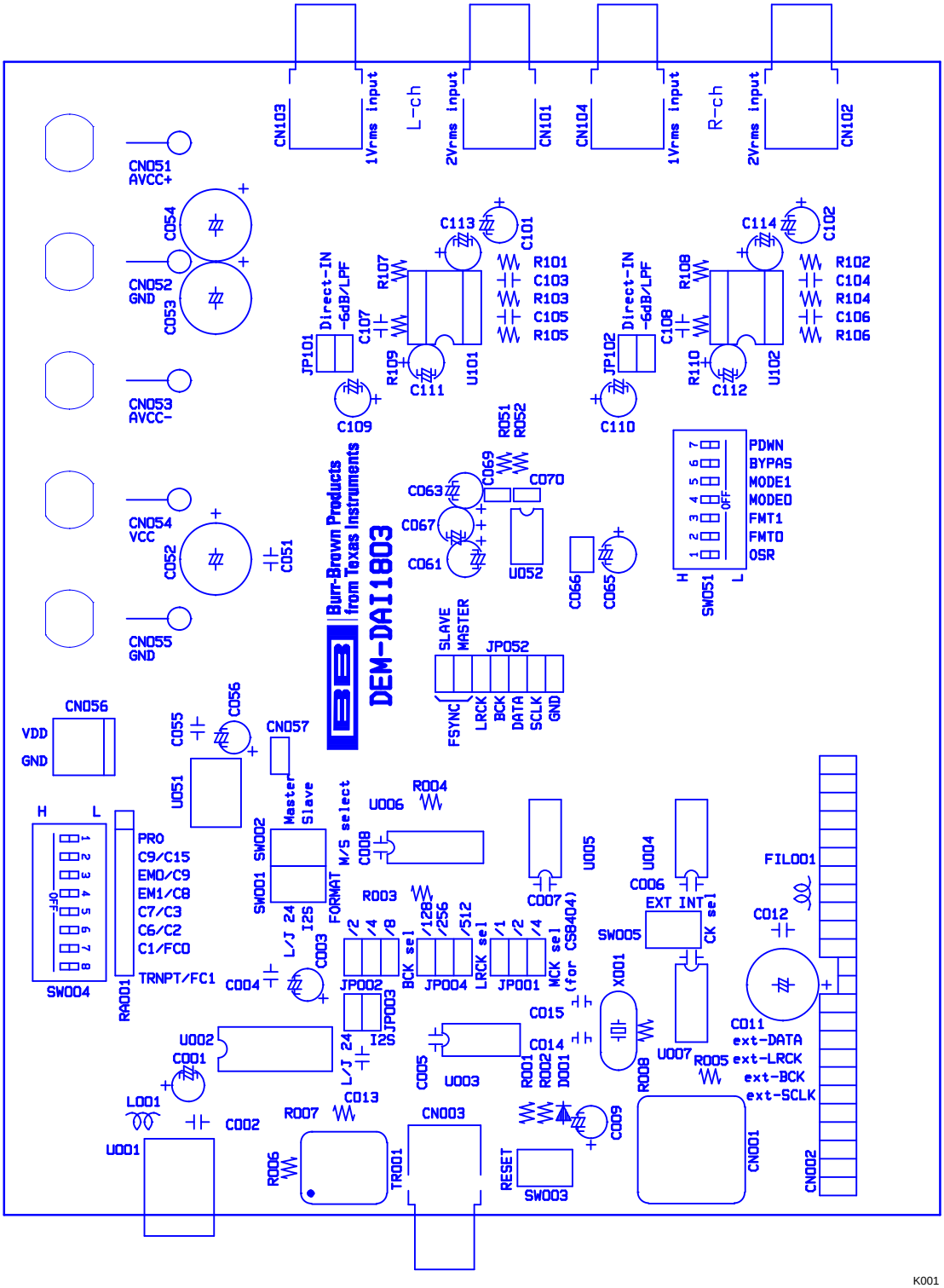
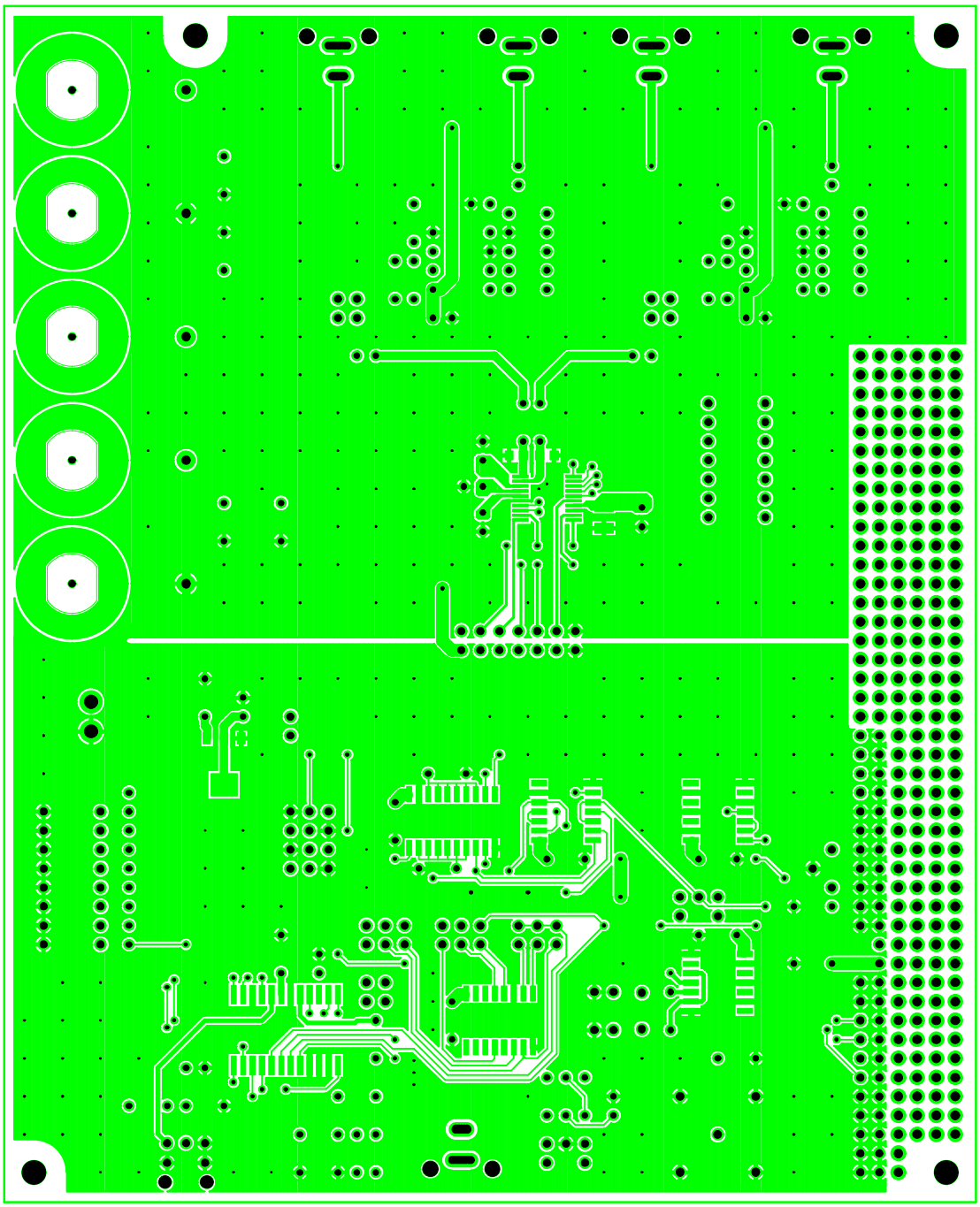


Figure 2-1. DEM-DAI1803 Silkscreen



K002

Figure 2-2. DEM-DAI1803 — Top View

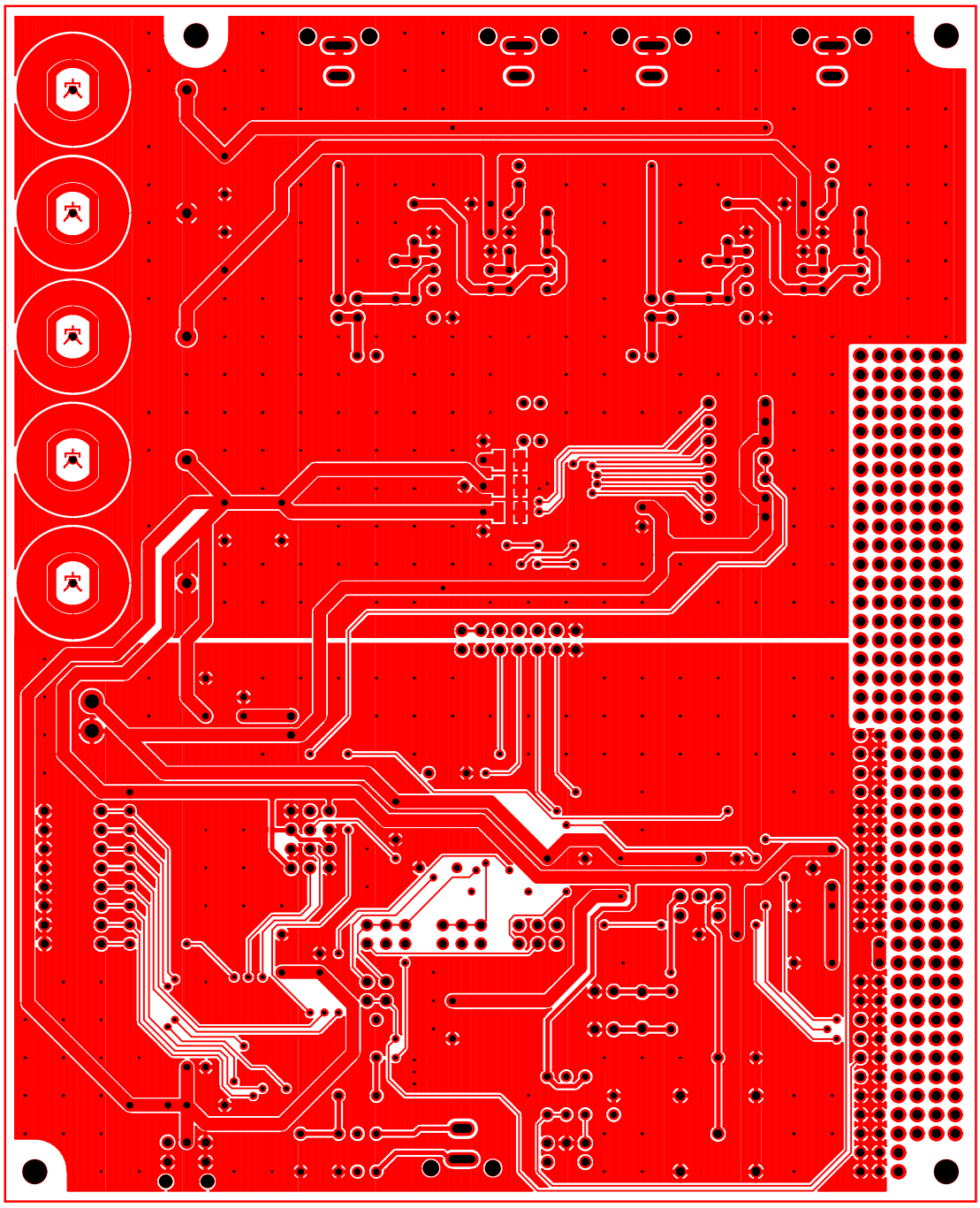


Figure 2-3. DEM-DAI1803 — Bottom View

2.2 DEM-DAI1803 SCHEMATICS

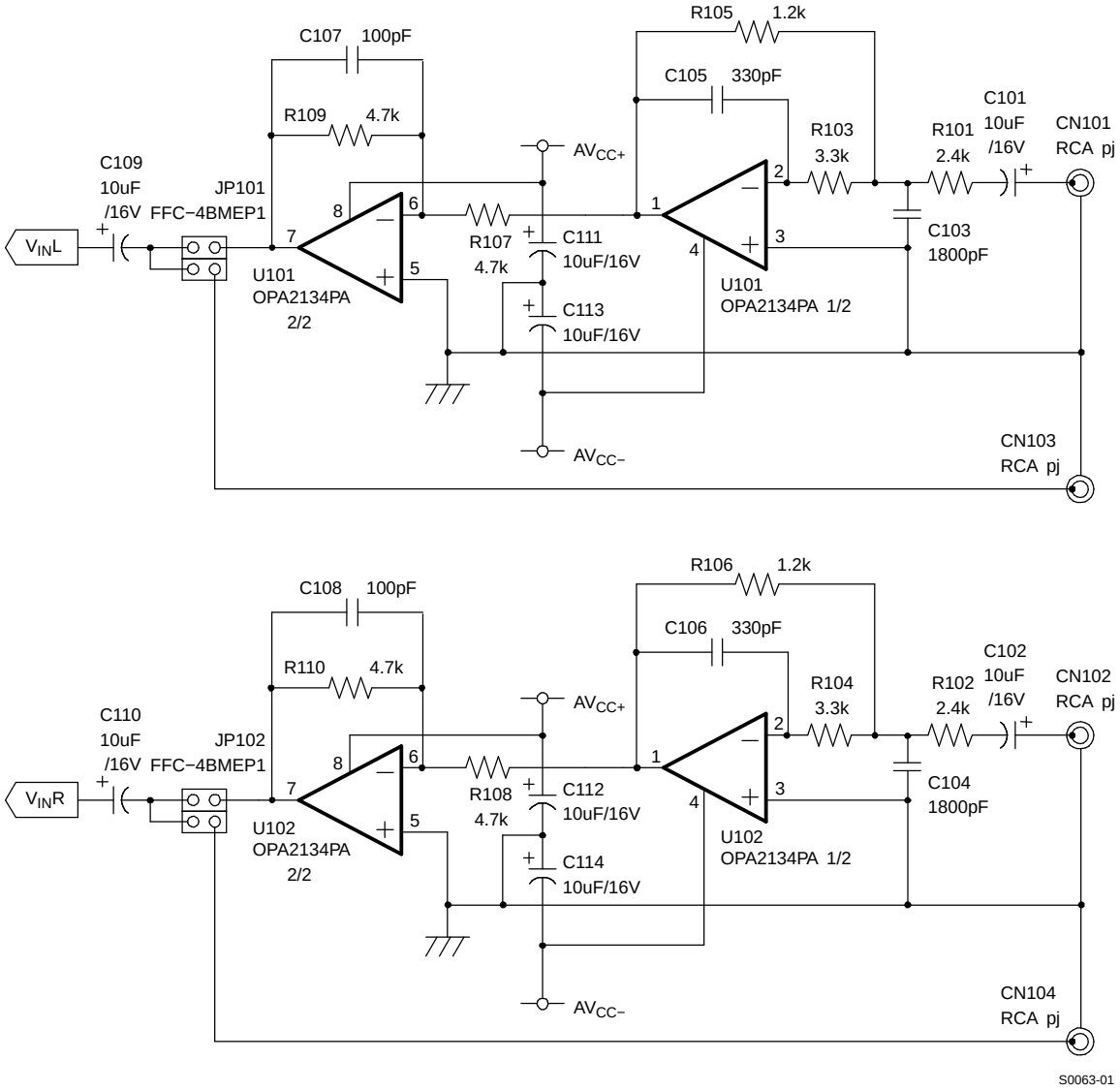


Figure 2-4. DEM-DAI1803 Analog Section Schematic Diagram

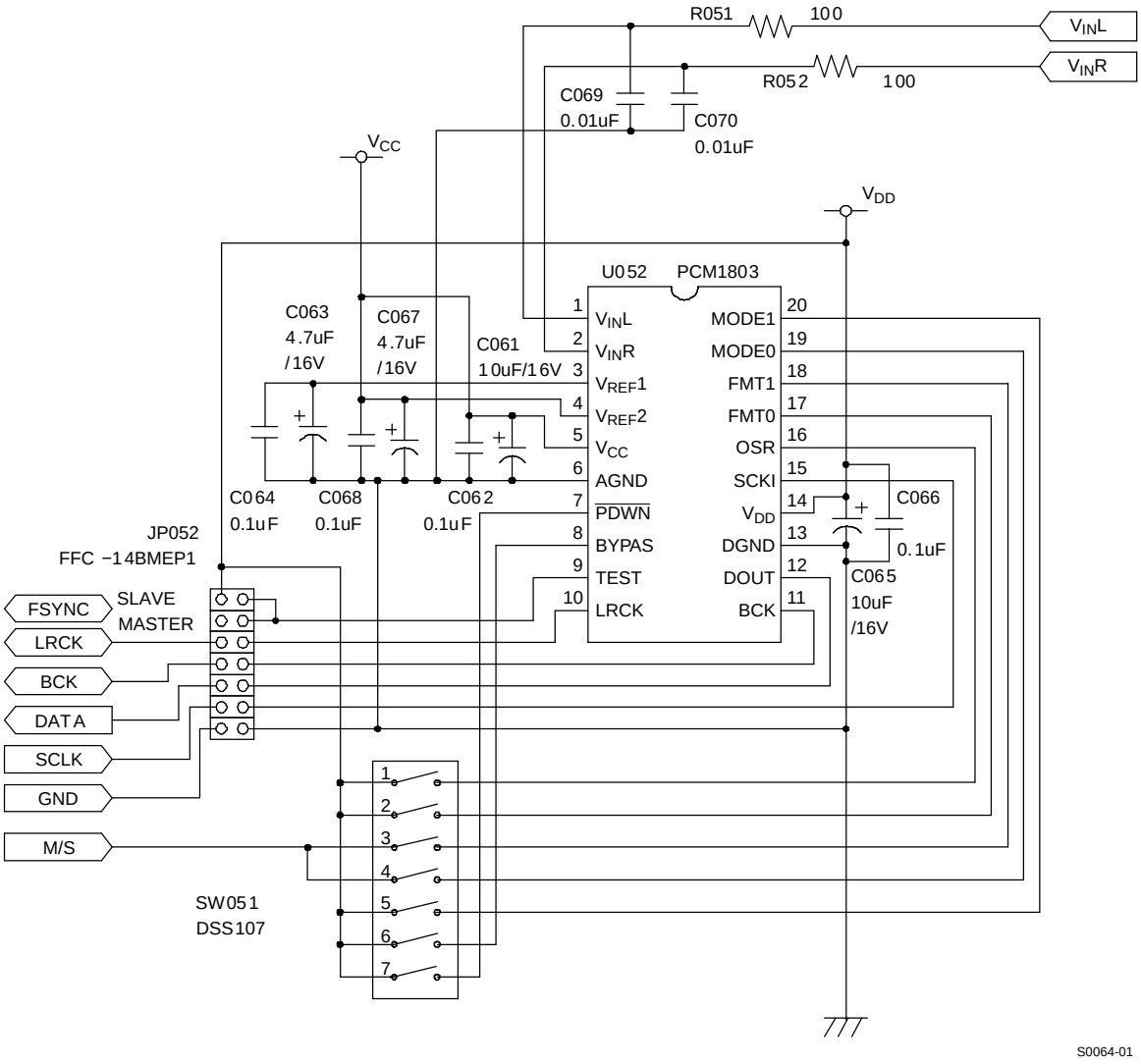


Figure 2-5. DEM-DAI1803 A/D Converter Section Schematic Diagram

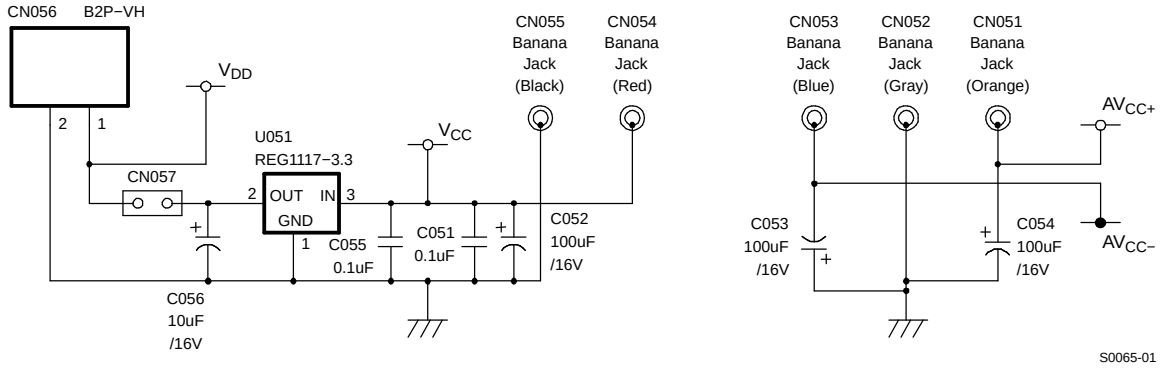


Figure 2-6. DEM-DAI1803 Regulator and Connector Schematic Diagram

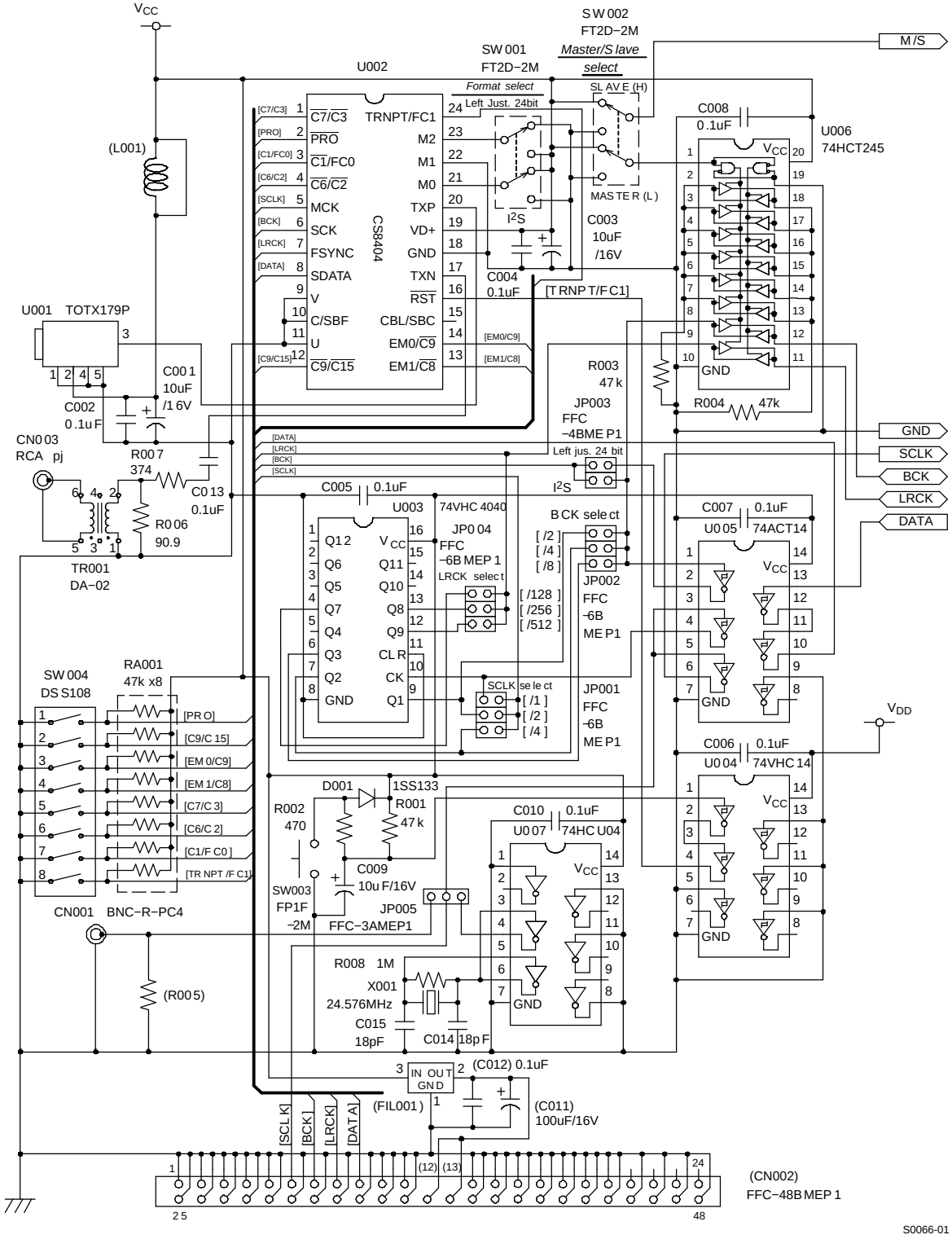


Figure 2-7. DEM-DAI1803 Digital Section (Digital Audio Interface) Schematic Diagram

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