TEXAS INSTRUMENTS

TPS54372EVM-215 3-Amp

SWIFT™ Regulator Evaluation Module

User's Guide

July 2002

PMP Systems Power

SLUU119

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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Chapter 1

Introduction

This chapter contains background information for the TPS54372, as well as support documentation for the TPS54372EVM-215 evaluation module (SLVP215). The SLVP215 performance specifications are provided with the schematic and bill of material.

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1.1 Background

The TPS54372EVM-215 evaluation module uses the TPS54372 tracking/termination synchronous buck regulator to provide an output voltage V_{TTQ} that is one half the voltage V_{DDQ} from a nominal 3.3-V or 5-V input. Rated input voltage and output current range is given in Table 1–1. These evaluation modules are designed to demonstrate the small PCB areas that may be achieved when designing with the TPS54372 regulator. The switching frequency is set at a nominal 700 kHz, allowing the use of a small footprint 1.0-µH output inductor. The MOSFETs of the TPS54372 are incorporated inside the TPS54372 package. This eliminates the need for external MOSFETs and their associated drivers. The low drain-to-source on resistance of the MOSFETs gives the TPS54372 high efficiency and helps to keep the junction temperature low at high output currents. The compensation components external to the IC allow flexibility in choosing output filter components voltage and a customizable loop response.

Table 1–1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Output Current Range
TPS54372EVM–215	3 V to 6 V	–3 A to 3 A

1.2 Performance Specification Summary

A summary of the TPS54372EVM-215 performance specifications is provided by Table 1–2. All specifications are given for an ambient temperature of 25°C, unless otherwise noted.

Table 1–2. TPS54372EVM-215 Performance Specification Summary

Specification	Test Conditions	Min	Typ	Max	Unit
Input voltage range		3	3.3 or 5	6	V
Output voltage set point		†	1.25	1.75	V
Output current range	V_I = 5 V	–3		3	A
Line regulation	I_O = 0 – 6 A		2.3		mV
Load regulation	V_I = 5 V		2.7		mV
Load transient response	I_O = 0 A to 2.25 A, t_r = 1 µs		–30		mV_{PK}
			50		µs
	I_O = 2.25 A to 0 A, t_f = 1 µs		30		mV_{PK}
			50		µs
Loop bandwidth	V_I = 3 V		85		kHz
Phase margin	V_I = 3 V		55		°
Loop bandwidth	V_I = 6 V		120		kHz
Phase margin	V_I = 6 V		40		°
Input ripple voltage‡			110	130	mV_{PP}
Output ripple voltage‡			18	20	mV_{PP}
Output rise time		4.7	8.4	15	ms
Operating frequency			700		kHz
Maximum efficiency	V_I = 5 V, I_O = 1.5 A		83.4%		–

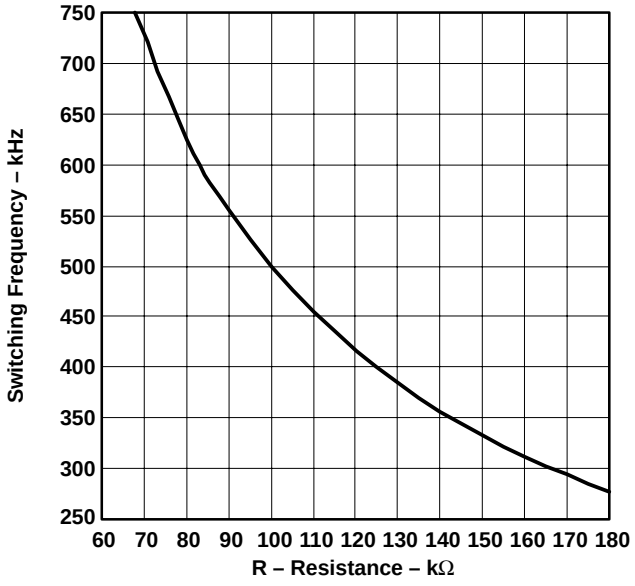
† 6% of V_I
‡ 20 MHz bandwidth limit

1.3 Modifications

The TPS54372EVM-215 is designed to demonstrate the small size that can be attained when designing with the TPS54372. Many of the features that allow for extensive modifications have been omitted from this EVM. The output voltage $V_{(TTQ)}$ can be set in the range of 6% of V_I to 1.75 V by changing the $V_{(DDQ)}$ voltage input at J3. The output $V_{(TTQ)}$ will track at one half the $V_{(DDQ)}$ voltage. The lower voltage limit is set by the minimum on time of the TPS54372. The upper voltage limit is set by the internal voltage reference. Larger output voltages up to 90% of V_I are possible in designs using the TPS54372, but are not supported on this evaluation module.

The switching frequency may be trimmed to any value between 280 kHz and 700 kHz by changing the value of R5. Decreasing the switching frequency results in increased output ripple unless the value of L1 is increased. A plot of the value of RT versus the switching frequency is given in Figure 1–1.

Figure 1–1. Frequency Trimming Resistor Selection Graph



Chapter 2

Test Setup and Results

This chapter describes how to properly connect, set up, and use the SLVP215 evaluation module. The chapter also includes test results typical for the SLVP215 and covers efficiency, output voltage regulation, load transients, loop response, output ripple, input ripple, and start-up.

The ambient temperature is 25°C for all test results unless otherwise noted.

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2.1 Input/Output Connections

The SLVP215 has the following six input/output connections: input, input return, output $V_{(TTQ)}$, output return, tracking input $V_{(DDQ)}$, and tracking input return. A diagram showing the connection points is shown in Figure 2–1. A power supply capable of supplying 5 A should be connected to J1 through a pair of 20 AWG wires. The load should be connected to J2 through a pair of 20 AWG wires. The maximum load current is ±3 A (current may be source or sink). Wire lengths should be minimized to reduce losses in the wires. Test point TP7 provides a place to easily connect an oscilloscope voltage probe to monitor the output voltage.

Figure 2–1. Connection Diagram

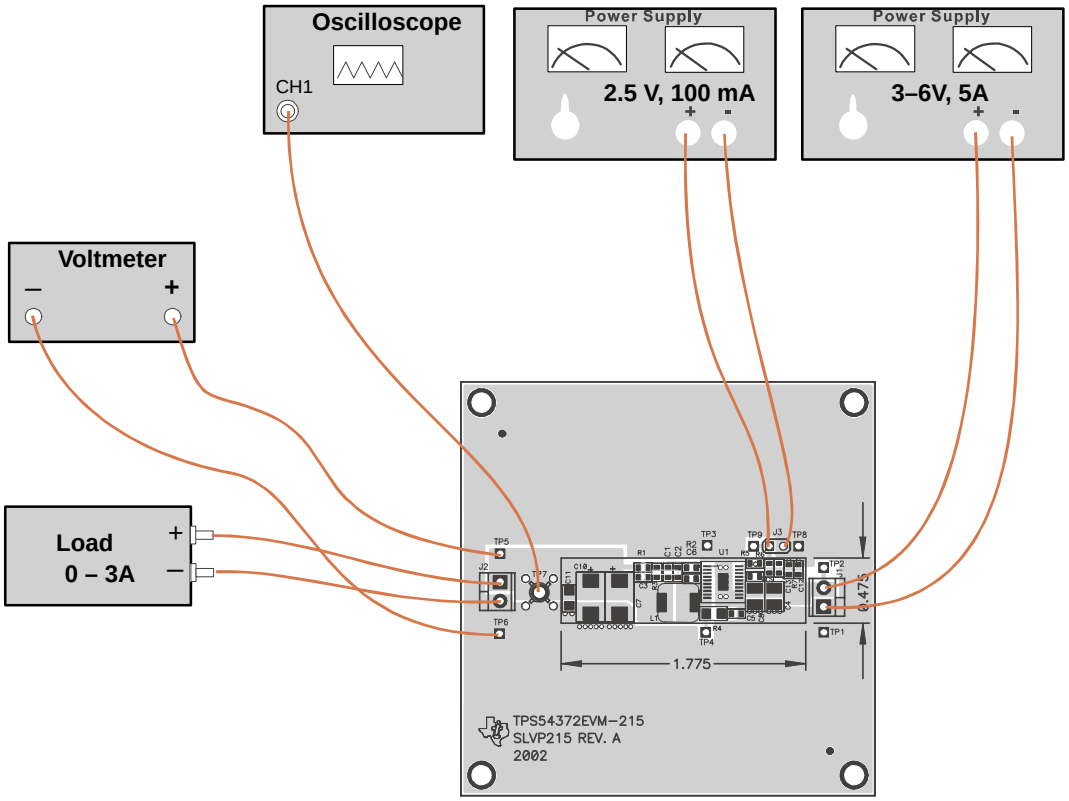


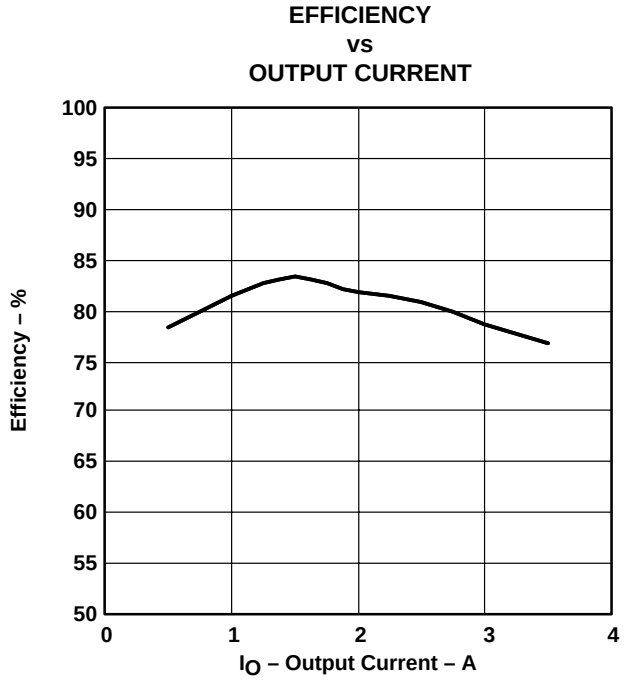
Table 2–1. Test Points

Test Point	Description
TP1	GND at V_I
TP2	V_I
TP3	AGND
TP4	Phase pin
TP5	V_O (V_{TTQ})
TP6	GND at V_O
TP7	V_O connection for oscilloscope probe
TP8	$V_{(DDQ)}$
TP9	GND at $V_{(DDQ)}$

2.2 Efficiency

The SLVP215 efficiency peaks at load current of about 1.5 A, and then decreases as the load current increases towards full load. The efficiency shown in Figure 2–2 is for 5-V input at an ambient temperature of 25°C. The efficiency is lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the MOSFETs. The efficiency is slightly lower at 700 kHz than at lower switching frequencies due to the gate and switching losses in the MOSFETs.

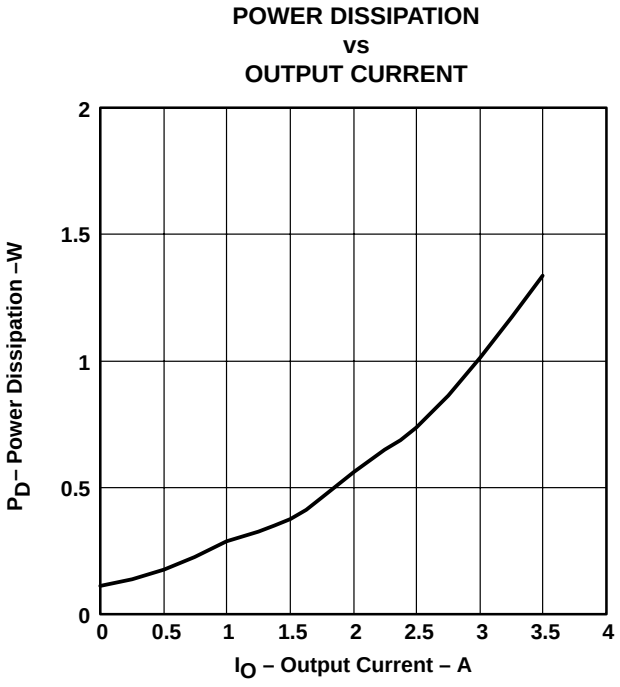
Figure 2–2. Measured Efficiency



2.3 Power Dissipation

The low junction-to-case thermal resistance of the PWP package, along with a good board layout, allows the SLVP215 EVMs to output full rated load current while maintaining safe junction temperatures. With a 5-V input source and a 3-A load, the junction temperature is approximately 60°C, while the case temperature is approximately 55°C. The total board losses at 25°C are shown in Figure 2–3.

Figure 2–3. Measured Board Losses



2.4 Output Voltage Regulation

The output voltage load regulation of the SLVP215 is shown in Figure 2–4, while the output voltage line regulation is shown in Figure 2–5. Measurements are given for an ambient temperature of 25°C.

Figure 2–4. Load Regulation

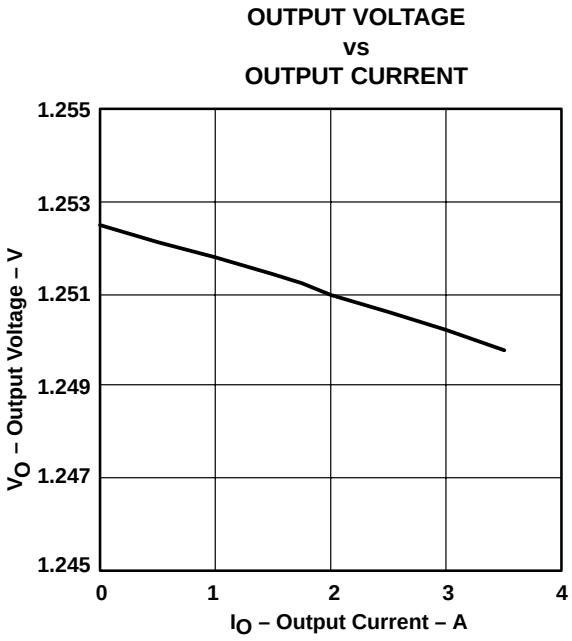
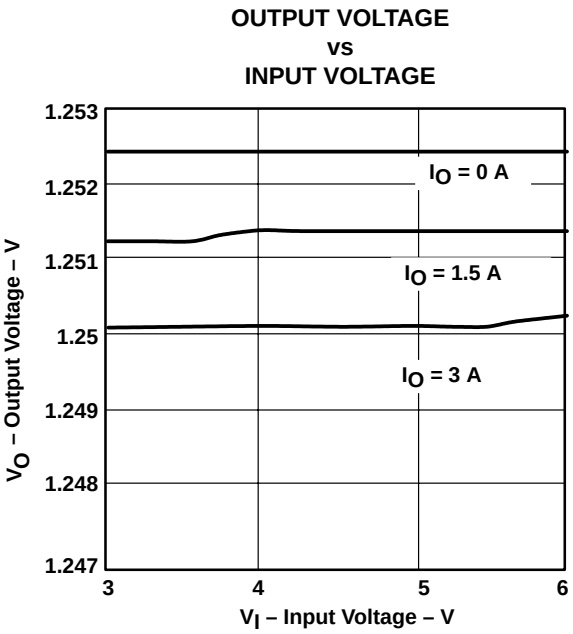


Figure 2–5. Line Regulation



2.5 Load Transients

The SLVP215 response to load transients is shown in Figure 2–6 and Figure 2–7. The current step in Figure 2–6 is 0 to 2.25 A, while the current step in Figure 2–7 is –1.5 A to 1.5 A (sinking to sourcing). Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

Figure 2–6. Source-Sink Current Transient Response

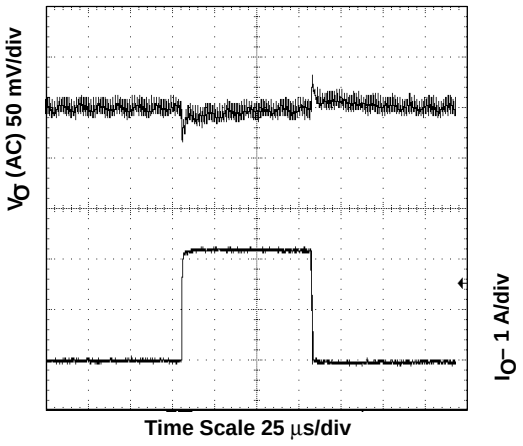
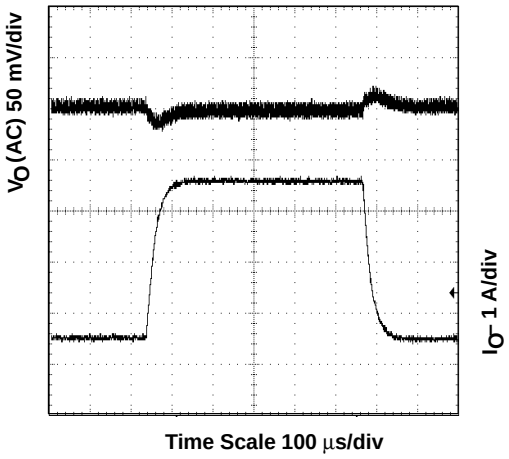


Figure 2–7. Load Transient Response



2.6 Loop Characteristics

The SLVP215 loop response characteristics are shown in Figure 2–8 and Figure 2–9. Gain and phase plots are shown at minimum and maximum operating voltage. The output current is 1.5 A.

Figure 2–8. Measured Loop Response, V_I = 3 V

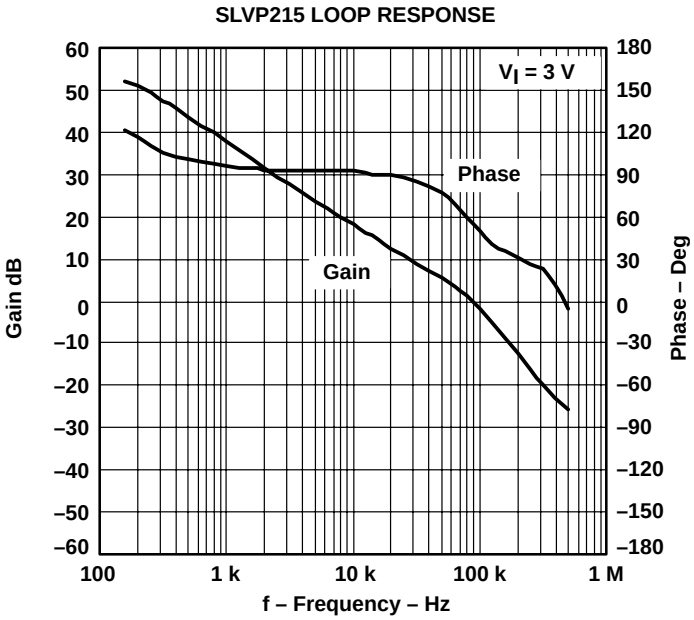
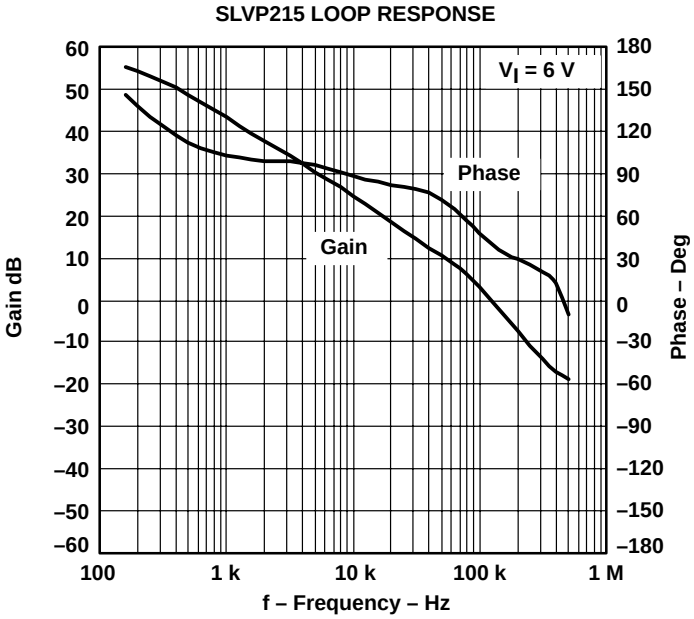


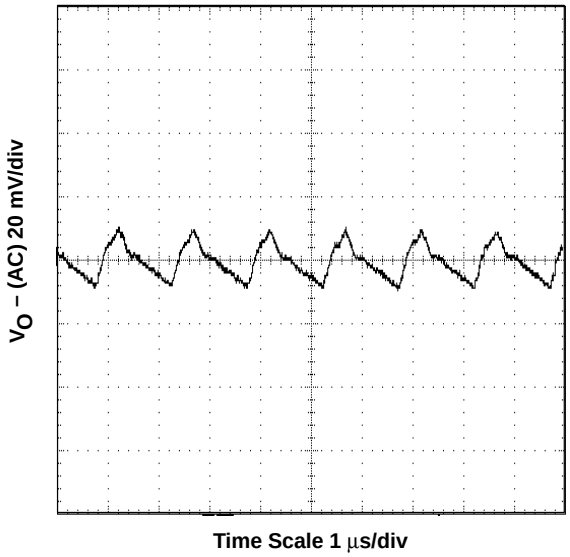
Figure 2–9. Measured Loop Response, V_I = 6 V



2.7 Output Voltage Ripple

The SLVP215 output voltage ripple is shown in Figure 2–10. The input voltage is 5 V for the TPS54372. Output current is the rated full-load current, 3 A.

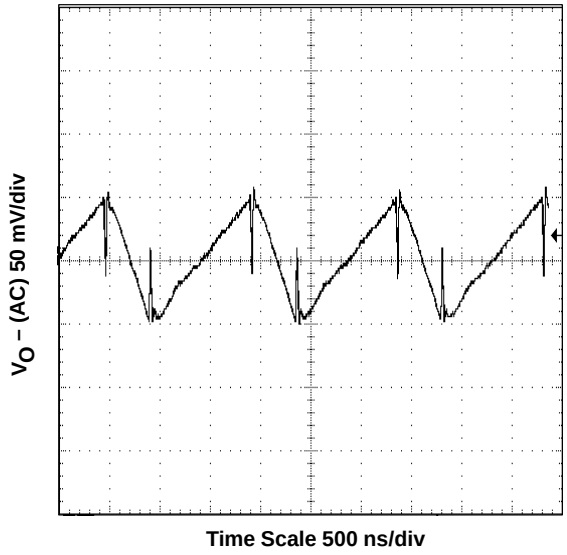
Figure 2–10. Measured Output Voltage Ripple



2.8 Input Voltage Ripple

The SLVP215 output voltage ripple is shown in Figure 2–11. The input voltage is 5 V for the TPS54372. Output current is the full-rated load current, 3 A.

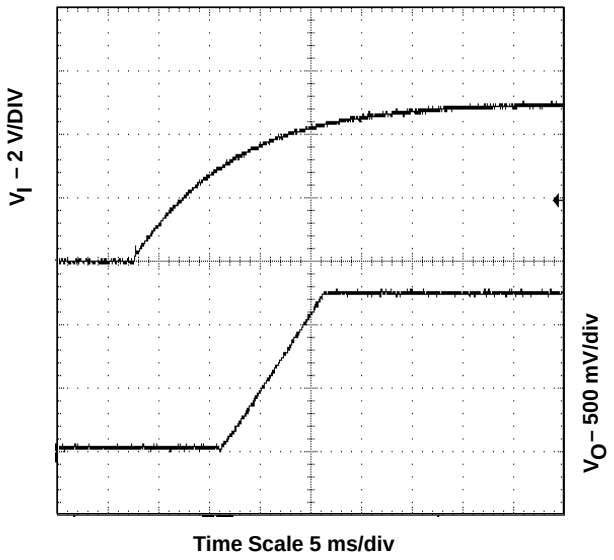
Figure 2–11. Input Voltage Ripple



2.9 Start-Up

The start-up voltage waveform of the SLVP215 is shown in Figure 2–12. There is approximately a 9-ms delay after the input voltage rises above the 2.9-V start-up voltage threshold until the output voltage begins to ramp up to the final value of 1.25 V. The output voltage tracks the greater of the internal and external slow-start voltages, accounting for the change in ramp rates .

Figure 2–12. Measured Start-Up Waveform



Chapter 3

Board Layout

This chapter provides a description of the SLVP215 board layout and layer illustrations.

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3.1 Layout

The board layout for the SLVP215 is shown in Figure 3–1 through Figure 3–3. The SLVP215 is laid out in a fashion to resemble a layer stack-up that may be encountered in a typical application. The top and bottom layers are 1.5 oz. copper. The top layer contains the main power traces for V_I, V_O, and $V_{(phase)}$. The top layer contains connections for the remaining pins of the TPS54372 and a large area filled with ground. The bottom layer consists entirely of a ground plane which is tied to the top layer ground are by means of vias including 10 directly under the TPS54372 device to provide a thermal path from the PowerPAD™ land to ground.

The input decoupling capacitors (C4 and C8), bias decoupling capacitor (C9), and bootstrap capacitor (C6) are all located as close to the IC as possible. In addition, the compensation components are kept close to the IC, minimizing noise pickup. The compensation circuit ties to the output voltage at the point of regulation, a wide trace to the output connector (J2).

Figure 3–1. Top-Side Layout

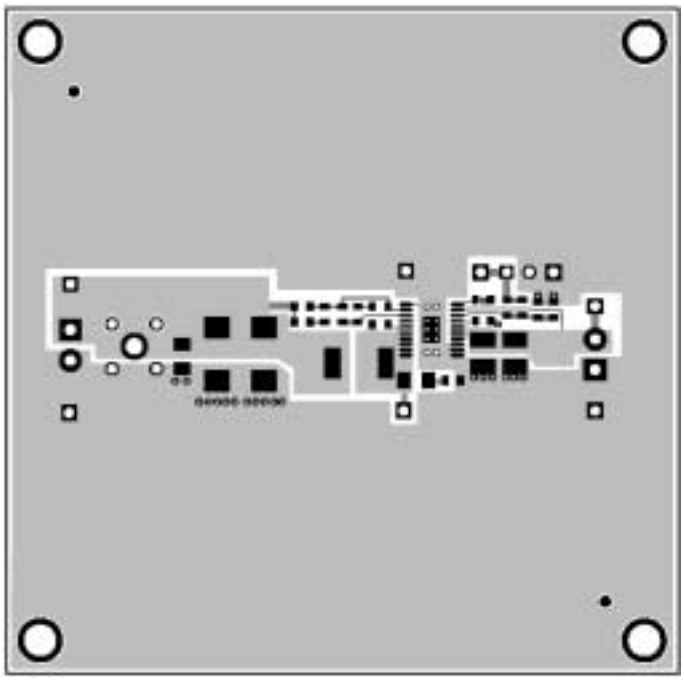

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Figure 3–2. Bottom-Side Layout (looking from top side)

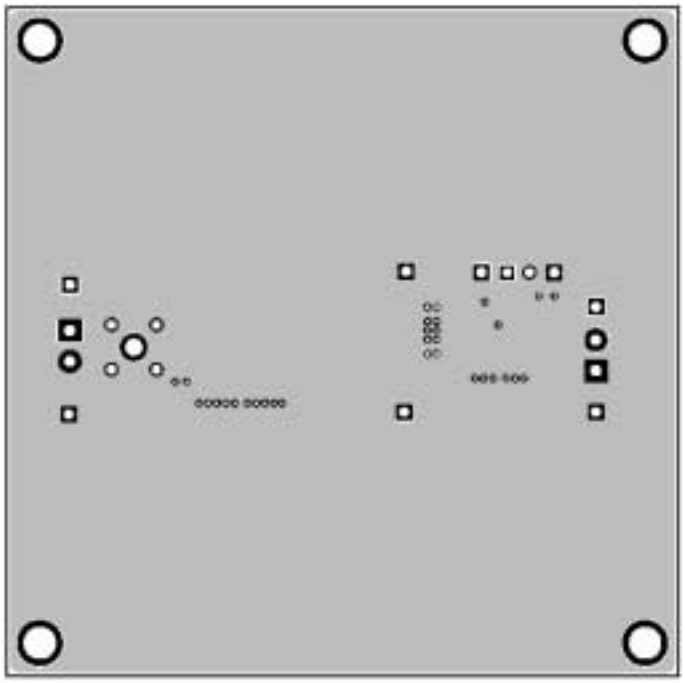
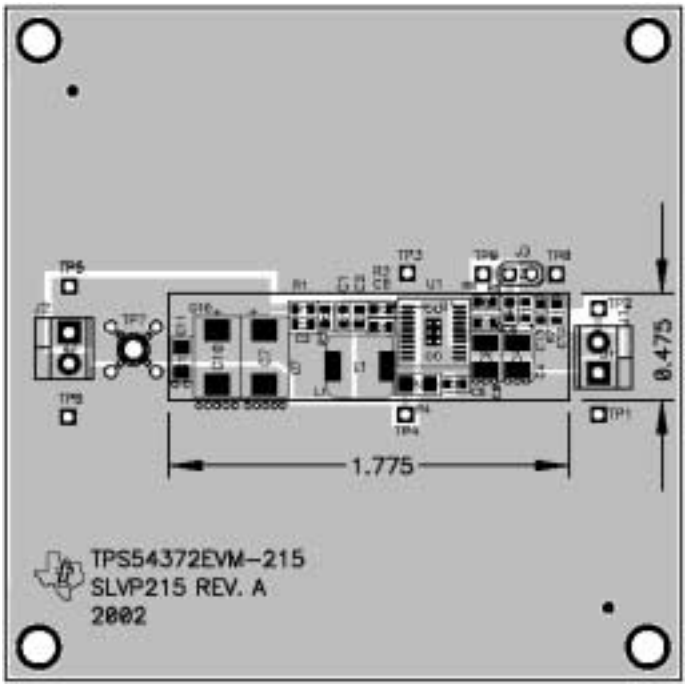


Figure 3–3. Top-Side Assembly



Chapter 4

Schematic and Bill of Materials

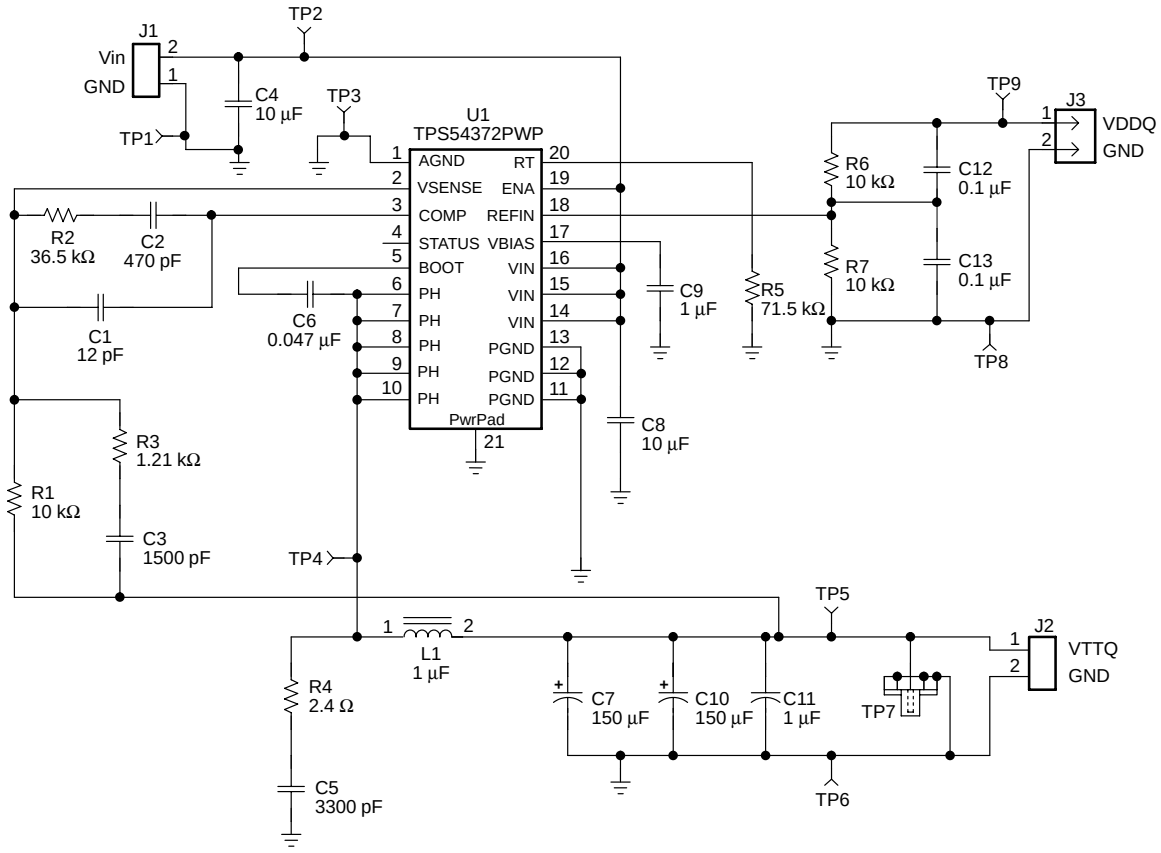
The SLVP215 schematic and bill of materials are presented in this chapter.

Topic **Page**

4.1 Schematic

The schematic for the SLVP215 is shown in Figure 4–1.

Figure 4–1. SLVP215 Schematic



4.2 Bill of Materials

The bill of materials for the SLVP215 is given by Table 4–1.

Table 4–1. SLVP215 Bill of Materials

Count	Ref Des	Description	Size	MFR	Part Number
1	C1	Capacitor, ceramic, 12 pF, 50 V, NPO, 5%	603	Panasonic	ECU-V1H120JCV
1	C11	Capacitor, ceramic, 1 μF, 16 V, X7R, 10%	1206	Panasonic	ECJ-3YB1C105K
2	C12, C13	Capacitor, ceramic, 0.1 μF, 25 V, X7R, 10%	603	Panasonic	ECJ-2VB1E104K
1	C2	Capacitor, ceramic, 470 pF, 50 V, X7R, 10%	603	Panasonic	ECU-V1H471KBV
1	C3	Capacitor, ceramic, 1500 pF, 50 V, X7R, 10%	603	Panasonic	ECJ-1VB1H152K
2	C4, C8	Capacitor, ceramic, 10 μF, 10 V, X5R, 20%	1210	Taiyo Yuden	LMK325BJ106MN
1	C5	Capacitor, ceramic, 3300 pF, 50 V, X7R, 10%	603	Panasonic	ECJ-1VB1H332K
1	C6	Capacitor, ceramic, 0.047 μF, 25 V, X7R, 10%	603	Panasonic	ECJ-2VB1E473K
2	C7, C10	Capacitor, polymer aluminum, 150 μF, 6.3 V	62100	Cornell Dubilier	ESRE151MO6R
1	C9	Capacitor, ceramic, 1 μF, 10 V, X5R, 20%	603	TDK	C1608X5R1A105K
2	J1, J2	Terminal block, 2 pin, 6 A, 3,5 mm	75525	OST	ED1514
1	J3	Header, 2 pin, 100 mil spacing, (36 pin strip)	23100	Sullins	PTC36SAAN
1	L1	Inductor, SMT, 1 μH, 8.5 A, 10 mΩ	0.270 sq	Vishay	IHLP-2525CZ-01
3	R1, R6, R7	Resistor, chip, 10 kΩ, 1/16 W, 1%	603	Std	Std
1	R2	Resistor, chip, 36.51 kΩ, 1/16 W, 1%	603	Std	Std
1	R3	Resistor, chip, 1.21 kΩ, 1/16 W, 1%	603	Std	Std
1	R4	Resistor, chip, 24 Ω, 1/8 W, 1%	1206	Std	Std
1	R5	Resistor, chip, 71.5 kΩ, 1/16 W, 1%	603	Std	Std
4	TP1, TP3, TP6 TP8	Test point, black, 1 mm	0.038″, 6400″	Farnell	240-333
4	TP1, TP3, TP5 TP9	Test point, red, 1 mm	0.038″, 6400″	Farnell	240-345
1	TP7	Adaptor, 3,5 mm probe clip (or 131-5031-00)	72900	Tektronix	131-4244-00
1	U1	IC	PWP20	TI	TPS54372PWP