Texas Instruments

UCC5696, 27-Line LVD-Only SCSI Terminator

Reference Design

UCC5696, 27-Line LVD-Only SCSI Terminator

James Garret *SCSI Termination Products*

Contents

1 Introduction 2
2 Features 2
3 Schematic 3
4 Layout 5
5 EVM Description 6
6 Software Requirements 6
7 Software Control 6
8 Performance Data 7
9 List of Material 8
10 References 13
11 List of Material 14
12 References 14

1 Introduction

The UCC5696, a LVD-only SCSI programmable terminator, terminates the next generation of SCSI parallel interfaces (SPI–5) and beyond. The UCC5696 makes use of an I^2C bus to program the differential impedance and the differential bias currents of the terminator. Using I^2C, the user can set the differential impedance in 5-Ω increments using 4 bits (16 steps), and the differential bias currents in 0.05-mA increments with 4 bits (16 steps). The UCC5696 also comes complete with a SPI–3 filter used for bus mode changes, and it is set to 200 ms typical.

2 Features

- Meets Ultra2 (SPI–2 LVD SCSI), Ultra3, Ultra160 (SPI–3), Ultra320 (SPI–4), and Ultra640 (SPI–5) Standards and considers options through to SPI–10.
- Compliant for Termpwr voltages of 2.7 V to 5.25 V.
- Contains differential fail-safe bias.
- Contains I^2C bus adjustable impedance and bias current.

3 Schematic

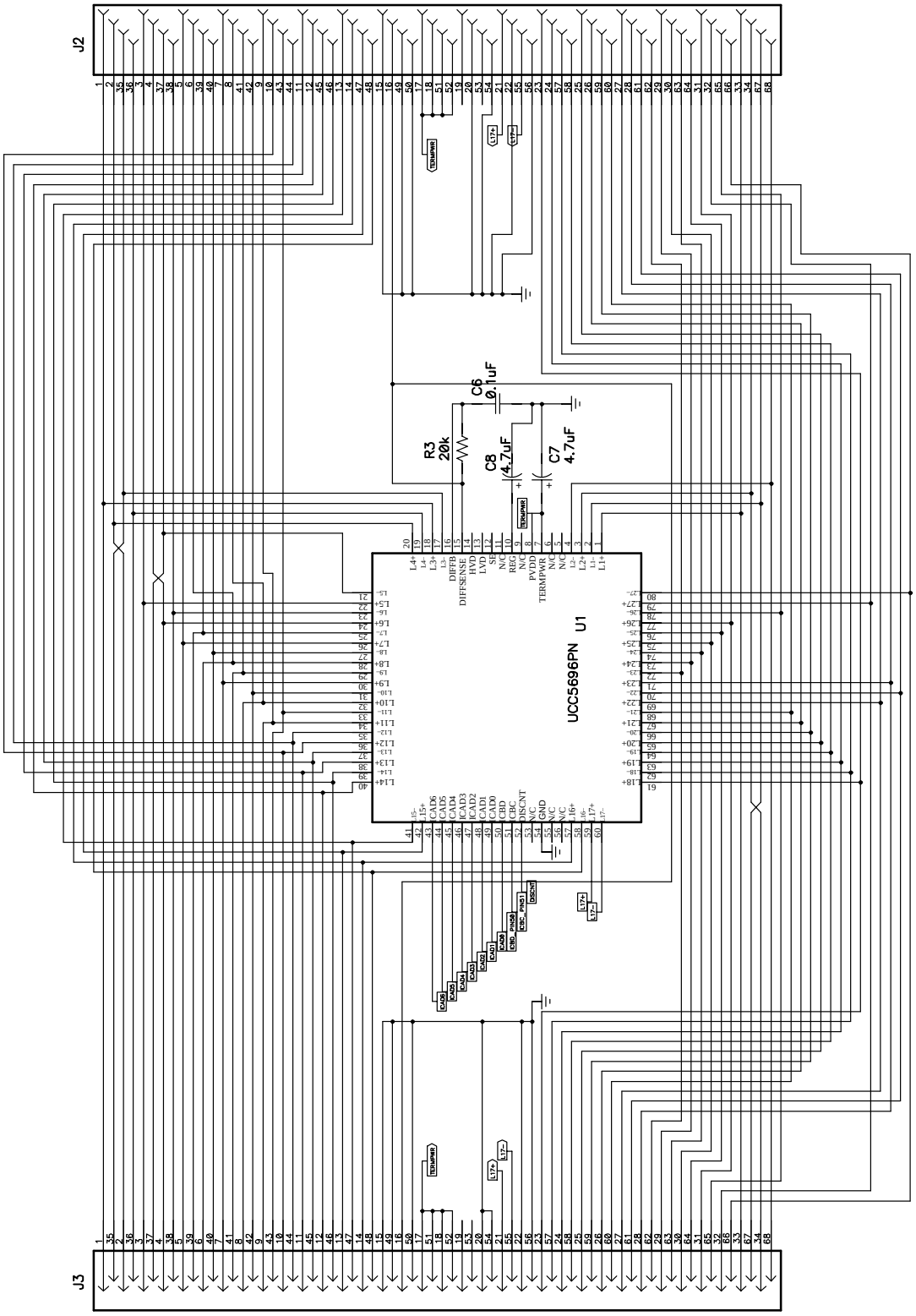


Figure 1. Schematic 1 SCSI Bus

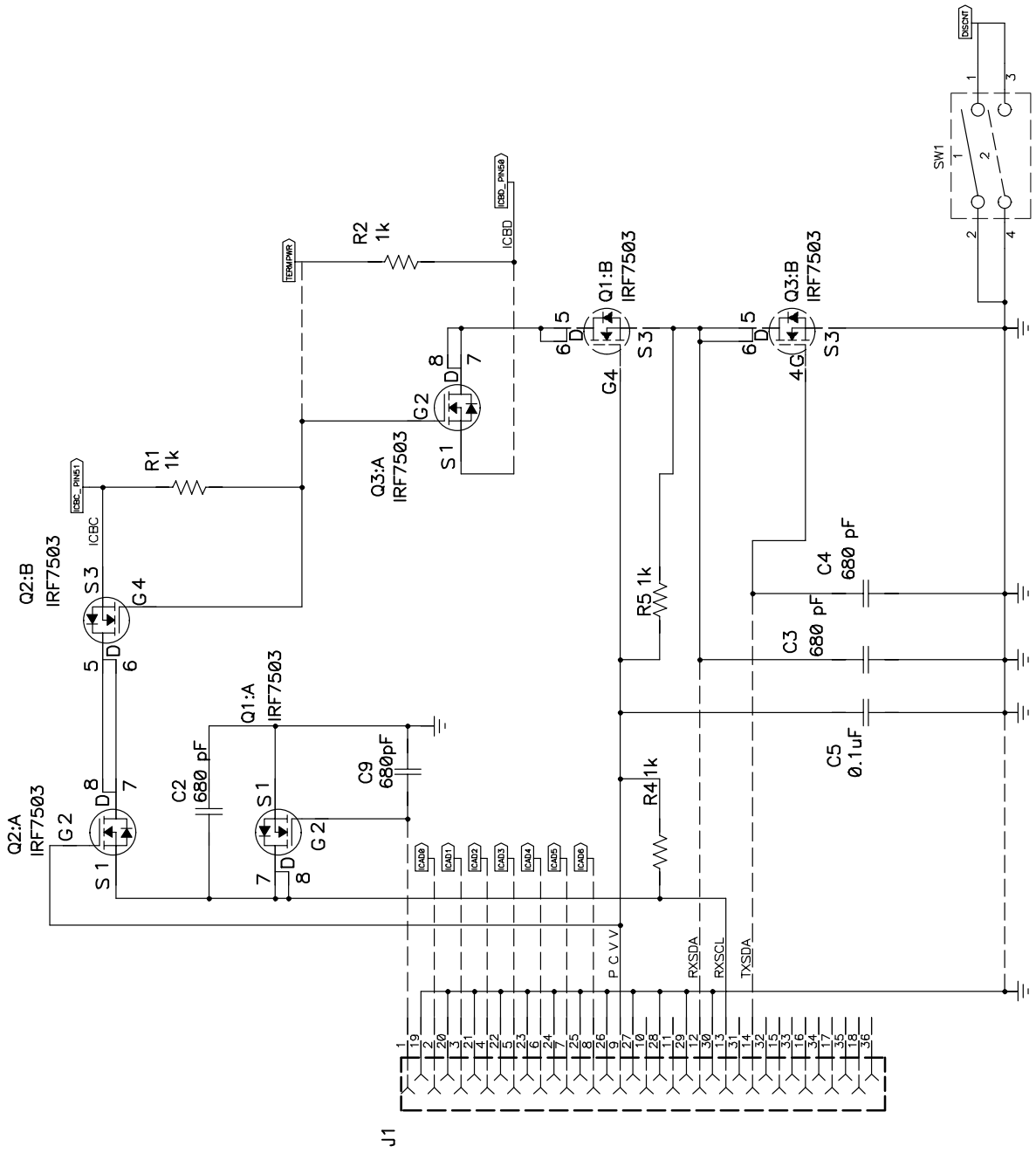


Figure 2. Schematic 2 I²C Parallel Port

4 Layout

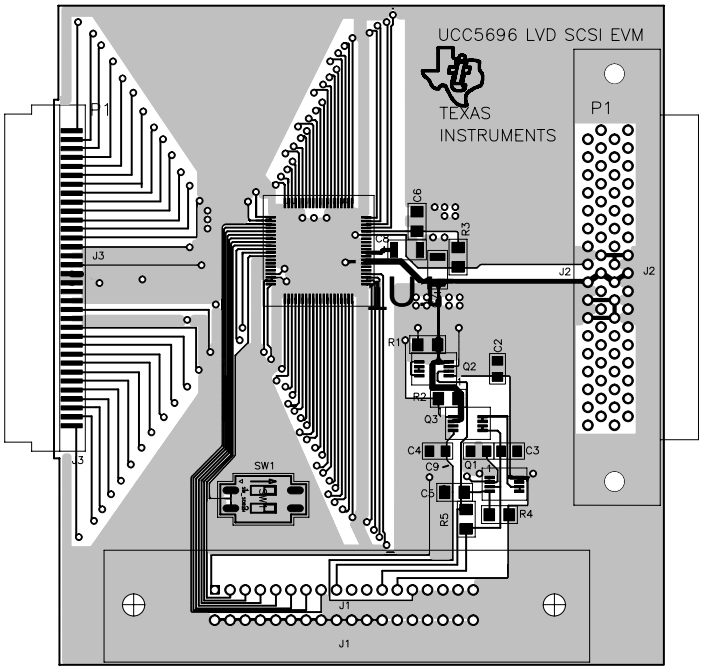


Figure 3. Top View

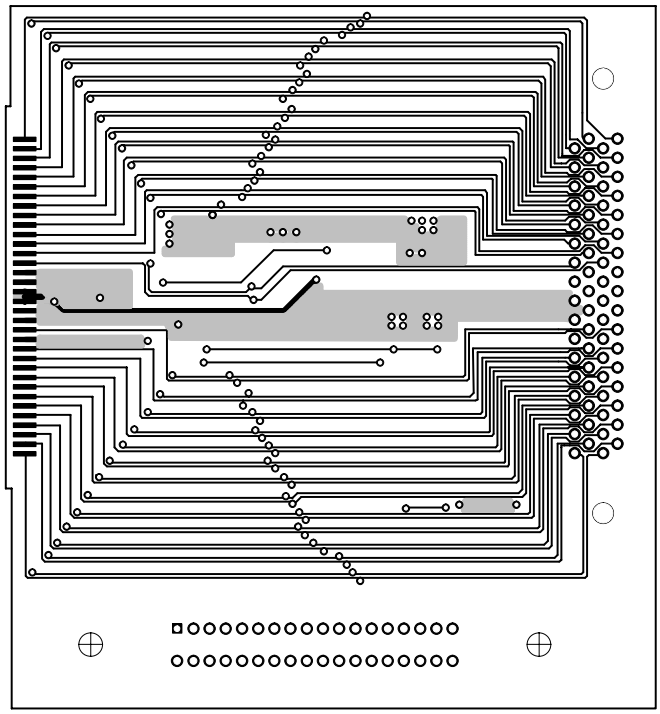


Figure 4. Bottom View

5 EVM Description

- Capacitors C2, C3, C4, C5, C7, C8, and C9 are bypass capacitors and intended to keep certain nodes *quiet*.
- Resistor R3 and capacitor C6 form a low pass filter for changes in DiffSense.
- Resistors R1, R2, R4, and R5 and MOSFETs Q1:A/B, Q2:A/B, and Q3:A/B form level shifting circuitry for level shifting the I^2C signals from PC_Vcc to TermPwr_Vcc. However, in a product, level-shifting may not be required.
- Switch SW1 is for disabling and enabling the UCC5696 through the DISConnect pin.
- Connector J1 can be connected to the parallel port of a PC to drive the I^2C signals. It should be noted that this connector is on the bottom side of the board.
- Connector J2 can be connected to a SCSI cable.
- Connector J3 can be connected to a SCSI device or a SCSI controller card.

6 Software Requirements

Software is required to run the I^2C bus, which allows for programming of differential impedance and differential bias currents. This software has been included as an 5696.EXE file which can be run on Windows 95/98 or MS–DOS. Later versions of Windows will not be able to run this file. It should be noted that one could use a separate PC to control the I^2C bus on the EVM if the use of Windows 95/98 is especially prohibitive to testing the SCSI drives.

7 I^2C Control Program Using the Parallel Port

The UCC5696 EVM uses a parallel port interface for programming the differential bias current and differential impedance. Provided is a program that is a basic DOS boot disk. The 5696.EXE program is best run from the boot disk as the operating systems limit the access to the parallel port.

The program automatically senses the speed of the processor and determines the correct I^2C speed. The processor range is from 100 MHz to 10 GHz, however the higher speeds have not been tested.

The program has 4 basic instructions as listed below and defined on the screen:

- A = Address, binary number – 7 bits
- W = Write the UCC5696 single register
- Z = Change the impedance [in Ohms] from 55 Ω to 130 Ω nominal value in steps of 5 Ω. Only valid numbers are accepted.
- I = Current in micro amps, 700 μA to 1450 μA in steps of 50 μA. Only valid numbers are accepted with no commas.

DUT (device under test) readings are continually scanned reflecting the values on the device. Error messages appear when the device can not be accessed and appear in the values when the device can not be accessed.

8 Screen (between the lines)

8.1 UCC5696 EVM setting program – DOS boot only – Parallel port

- A = Address binary number
- W = Write the I^2C register
- Z = Impedance in Ω, 55 Ω to 130 Ω in steps of 5 Ω
- I = Current in μA, 700 μA to 1450 μA in steps of 50 μA.

Power up values are 105 Ω and 1050 μA SPI–2 – SPI–4 default

The settings are not written to the UCC5696 until the write command is given.

All commands are executed with the enter key. ESCape to exit program.

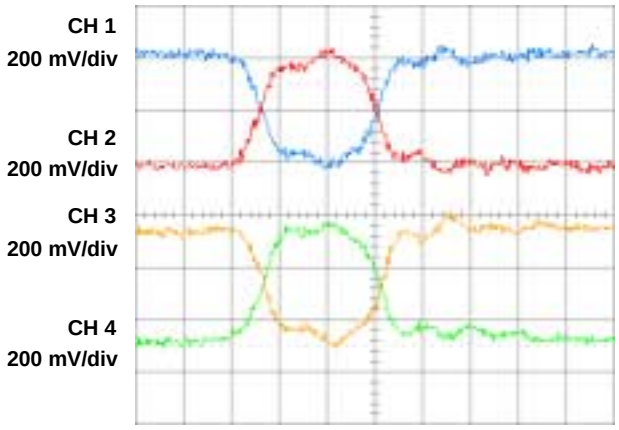
- DUT readings address (binary number), Z (Ω), I (μA)
- New Values address (binary number), Z (Ω), I (μA)
- Command
- Error messages will be displayed in red.

Type Z or I followed by the number in ohms or microamps and enter. Then type W to write to the device, the values change in the DUT readings.

The possible cause of the error messages are no Termpwr to the EVM, cable connection problem from the parallel port to the EVM or not able to access the printer port correctly.

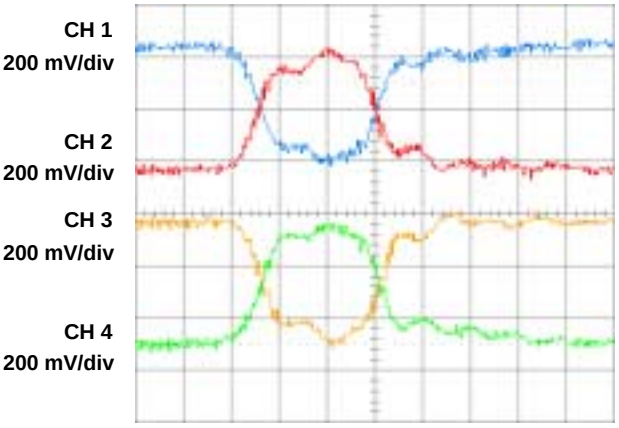
The impedance values should be adjusted to minimize the reflection. When looking at the reflections, the measurements should be done two or three devices away from the terminator. The round trip time from the device to the end of the system show the reflection point.

9 Examples



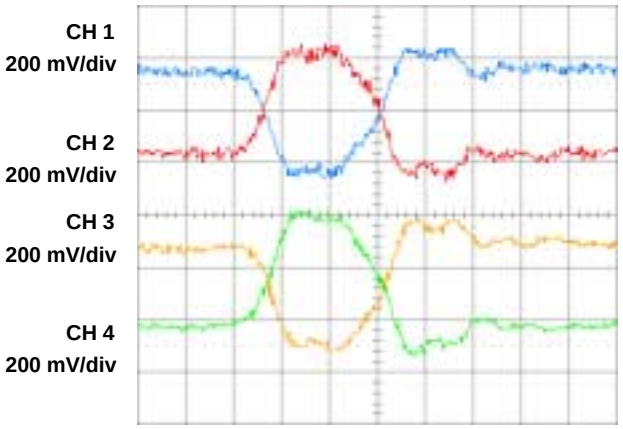
Example 1

Twist and flat cable with devices every 5 ¼ inches with three disk drives and nine disabled EVMs as simulated loads, this is the nominal setting of 105 Ω. The reflected impedance is higher than the incident wave, the measurement is 3 device slots from the terminator, 21 inches, the round trip time is approximately 4 ns. Note the lower trace is an outside pair (data line 13) on the twist and flat cable versus the upper trace is an inside pair (data line 8). The plus and minus lines are shown for each pair.



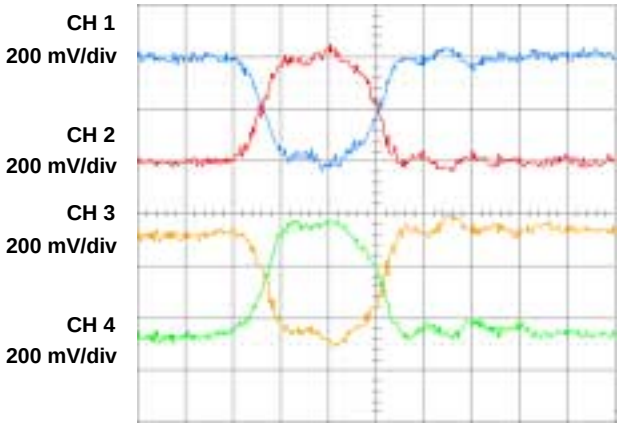
Example 2

Twist and flat cable with devices every 5 ¼ inches with three disk drives and nine disabled EVMs as simulated loads, this is the highest setting of 130 Ω. The reflected impedance is higher than the incident wave, the measurement is 3 device slots from the terminator, 21 inches, the round trip time is approximately 4 ns. Note the lower trace is an outside pair (data line 13) on the twist and flat cable versus the upper trace is an inside pair (data line 8).



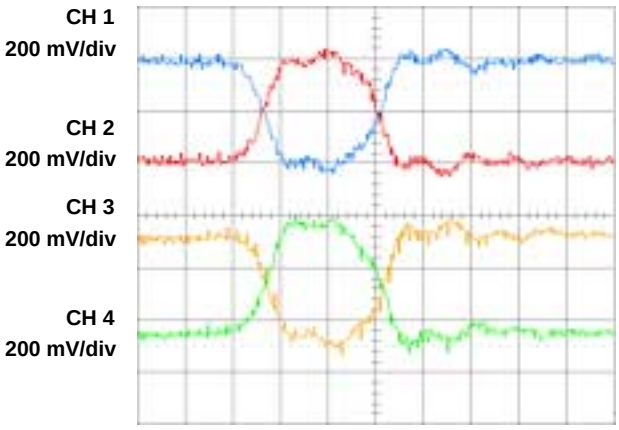
Example 3

Twist and flat cable with devices every 5 ¼ inches with three disk drives and nine disabled EVMs as simulated loads, this is the lowest setting of 55 Ω. The reflected impedance is lower than the incident wave, the measurement is 3 device slots from the terminator, 21 inches, the round trip time is approximately 4 ns. Note the lower trace is an outside pair (data line 13) on the twist and flat cable versus the upper trace is an inside pair (data line 8).



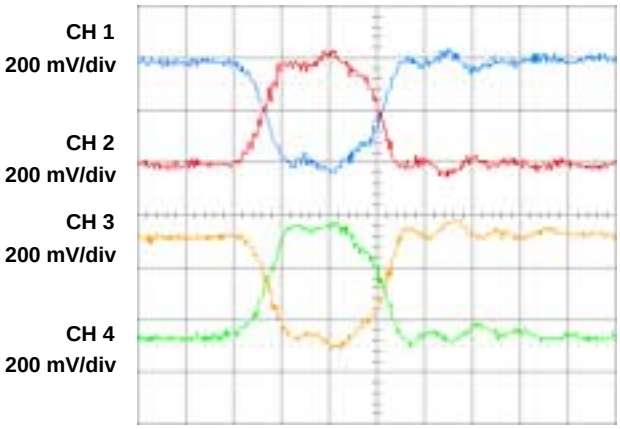
Example 4

Twist and flat cable with devices every 5 ¼ inches with three disk drives and nine disabled EVMs as simulated loads, this is the close setting of 90 Ω. The reflected impedance is about the same as the incident wave, the measurement is 3 device slots from the terminator, 21 inches, the round trip time is approximately 4 ns. Note the lower trace is an outside pair (data line 13) on the twist and flat cable versus the upper trace is an inside pair (data line 8).



Example 5

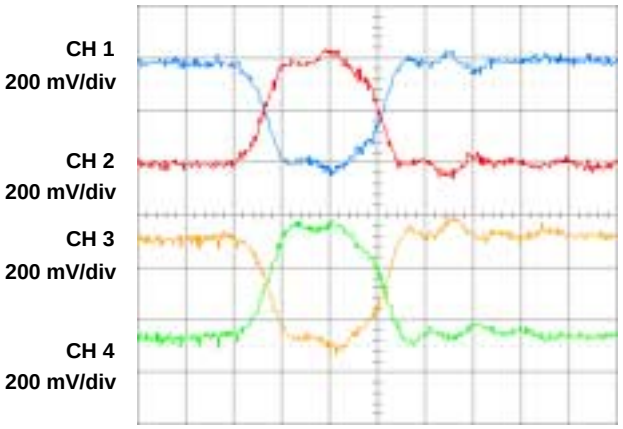
Twist and flat cable with devices every 5 ¼ inches with three disk drives and nine disabled EVMs as simulated loads, this is the slightly low setting of 80 Ω. The reflected impedance is lower than the incident wave, the measurement is 3 device slots from the terminator, 21 inches, the round trip time is approximately 4 ns. Note the lower trace is an outside pair (data line 13) on the twist and flat cable versus the upper trace is an inside pair (data line 8). The correct setting for this load condition is 85 Ω or 90 Ω.



Example 6

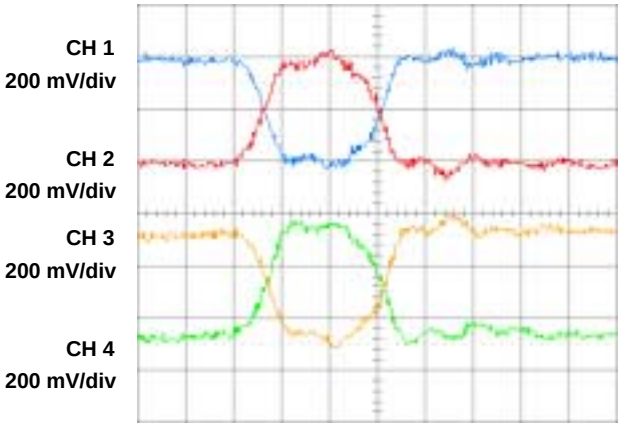
Twist and flat cable with devices every 5 ¼ inches with three disk drives and nine disabled EVMs as simulated loads, this is the correct setting of 85 Ω. The reflected impedance is about the same as the incident wave, the measurement is 3 device slots from the terminator, 21 inches, the round trip time is approximately 4 ns. Note the lower trace is an outside pair (data line 13) on the twist and flat cable versus the upper trace is an inside pair (data line 8).

Current adjustment was removed from SPI–5, but may be required in some case where crosstalk or system noise is a problem, but it has very little effect on the signal. Figures 1 to 6 are at the nominal bias of 1050 μA. See the examples below.



Example 7

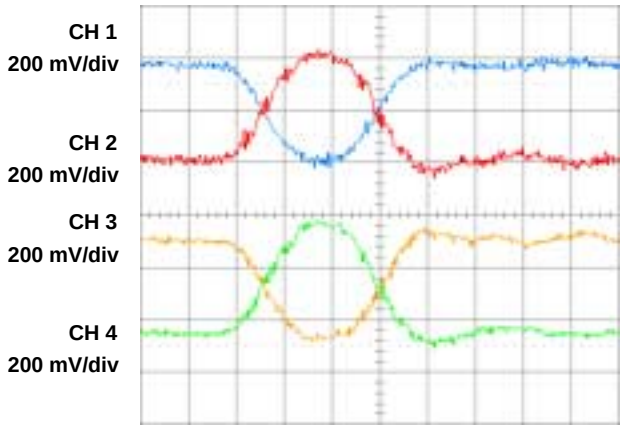
Twist and flat cable with devices every 5 ¼ inches with three disk drives and nine disabled EVMs as simulated loads, this is the correct setting of 85 Ω with the bias set to 1200 μA. The reflected impedance is about the same as the incident wave, the measurement is 3 device slots from the terminator, 21 inches, the round trip time is approximately 4 ns. Note the lower trace is an outside pair (data line 13) on the twist and flat cable versus the upper trace is an inside pair (data line 8).



Example 8

Twist and flat cable with devices every 5 ¼ inches with three disk drives and nine disabled EVMs as simulated loads, this is the correct setting of 85 Ω with the bias set to 900 μA. The reflected impedance is about the same as the incident wave, the measurement is 3 device slots from the terminator, 21 inches, the round trip time is approximately 4 ns. Note the lower trace is an outside pair (data line 13) on the twist and flat cable versus the upper trace is an inside pair (data line 8).

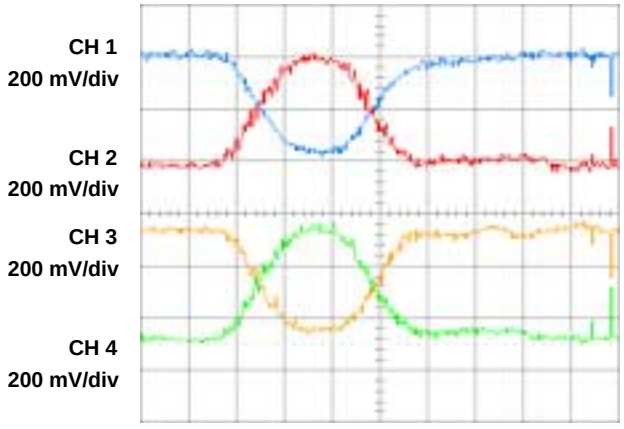
Increasing the loading, slows down the rise time. This was doubling the EVM loads on the last 4 slots on Examples 9 and 10.



t – Time – 5 ns/div

Example 9

Twist and flat cable with devices every 5 ¼ inches with three disk drives and fourteen disabled EVMs as simulated loads, this is the correct setting of 75 Ω. The reflected impedance is about the same as the incident wave, the measurement is 3 device slots from the terminator, 21 inches, the round trip time is approximately 4 ns. Note the lower trace is an outside pair (data line 13) on the twist and flat cable versus the upper trace is an inside pair (data line 8).



t – Time – 5 ns/div

Example 10

Twist and flat cable with devices every 5 ¼ inches with three disk drives and fourteen disabled EVMs as simulated loads, this is the nominal setting of 105 Ω. The reflected impedance is higher than the incident wave, the measurement is 3 device slots from the terminator, 21 inches, the round trip time is approximately 4 ns. Note the lower trace is an outside pair (data line 13) on the twist and flat cable versus the upper trace is an inside pair (data line 8).

10 Software Control

Table 1. Differential Bias Current Settings True

DIFFERENTIAL I_{BIAS} (mA)	BIT7 (MSB)	BIT6	BIT5	BIT4
0.70	0	0	0	0
0.75	0	0	0	1
0.80	0	0	1	0
0.85	0	0	1	1
0.90	0	1	0	0
0.95	0	1	0	1
1.00	0	1	1	0
1.05(1)	0	1	1	1
1.10	1	0	0	0
1.15	1	0	0	1
1.20	1	0	1	0
1.25	1	0	1	1
1.30	1	1	0	0
1.35	1	1	0	1
1.40	1	1	1	0
1.45	1	1	1	1

(1) Default settings

Table 2. Differential Impedance Settings True

DIFFERENTIAL IMP (Ω)	BIT3	BIT2	BIT1	BIT0
55	0	0	0	0
60	0	0	0	1
65	0	0	1	0
70	0	0	1	1
75	0	1	0	0
80	0	1	0	1
85	0	1	1	0
90	0	1	1	1
95	1	0	0	0
100	1	0	0	1
105(1)	1	0	1	0
110	1	0	1	1
115	1	1	0	0
120	1	1	0	1
125	1	1	1	0
130	1	1	1	1

(1) Default settings

11 List of Material

	Reference	Qty	Description	Manufacturer	Part Number
Capacitor	C6, C5	2	0.1 µF, 50 V, X7R, 1206, 10%	Panasonic	ECJ–3VB1H104K
	C7, C8	2	4.7 µF, 10 V, A Case, 10%	Panasonic	ECS–T1AY475R (TE series)
	C2, C3, C4, C9	4	680 pF, 50 V, NPO 0805, 5%	Panasonic	ECJ–2VC1H681J
Connectors	J2	1	68-pin right angle receptacle header	AMP (female)	787394–7 (Amplimite–SCSI–2)
	J3	1	68-pin straddle mount	Fujitsu (male)	FCN–238P068–G/E
	J1	1	36-pin parallel interface vertical mount	AMP (female)	552235–1
Resistor	R3	1	1/8 W, SMT, 1206, 1%	Panasonic	ERJ–8ENF–2002V
	R1, R2, R4, R5	4	1/8 W, SMT, 1206, 1%	Panasonic	ERJ–8ENF–1001V
MOSFETs	Q1:A/Q1:B, Q2:A/Q2:B, Q3:A/Q3:B	3	Micro-8 Dual NMOS	International Rectifier	IRF7503CT–ND
Switch	SW1	1	DIP Low Profile, SMT (SPST)	C&K	SD02HOSK Tape Sealed (SD Series)
IC	U1	1	SCSI LVD 27-line terminator	Unitrode/TI	UCC5696PN

12 References

UCC5696, *27-line LVD Only SCSI Terminator for SPI–5 and Beyond,* (TI Literature Number SLVS406)

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265