Texas Instruments

TPS2345 CompactPCI Hot Swap Power Manager Evaluation Module

User's Guide

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It is important to operate this EVM within the maximum input voltage ranges specified in Table 2.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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TPS2345 CompactPCI Hot Swap Power Manager Evaluation Module

Systems Power

Contents

1 Introduction

This User's Guide describes the use and features of the CompactPCI® Hot Swap Power Manager Evaluation Module (EVM). This EVM features the Texas Instruments (TI) TPS2345 CompactPCI® Hot Swap Power Manager integrated circuit (IC), a four-supply controller used to enable hot swap capability in boards or modules needing to meet the requirements of the CompactPCI® Hot Swap Specification, PICMG 2.1. The IC features programmable inrush current control, electronic circuit breakers, power-up and power-down sequencing, logic enable input, and load fault indicator. The CompactPCI® Hot Swap EVM is a PCB-based tool used to demonstrate the performance and operation of the TPS2345 IC in simulated live insertion and removal actions.

1.1 Features

The following list highlights some of the features of the TPS2345.

- Enables hot swap in CompactPCI® high availability systems
- Programmable current slew rate
- Power supply sequencing
- Peak current (IMAX) programmable via sense resistors
- Overcurrent circuit breaker at 2 × IMAX
- Precharge output
- HEALTHY# signal of board power good
- BD_SEL# signal for peripheral enable
- On-chip charge pump
- Low sleep mode current
- Undervoltage lockout (UVLO)
- 24-pin TSSOP package

1.2 Description

The TPS2345 CompactPCI® Hot Swap Power Manager (HSPM) provides highly integrated supply control of three positive (3.3 V, 5 V, and 12 V) and one negative (–12 V) supply rails with a minimum number of external components. A linear current amplifier (LCA) in each of the four device channels provides closed-loop control of load current during insertion and extraction events. This allows the designer to configure the plug-in card's maximum inrush slew rate and magnitude according to the requirements of the CompactPCI® hot swap specification.

After an add-in card insertion, once all input supplies are above undervoltage levels, and the BD_SEL# input is a logic low, the TPS2345 begins to apply power to the back-end power planes. Switching of the back–end power is achieved via four external N–Channel MOSFETs. Current to each supply plane is ramped at a programmed rate set by a capacitor on the current ramp pin (IRAMP), with supplies sequenced in the order 12 V, 5 V , 3.3 V and –12 V. The peak charging current on each channel is limited to an individually programmable value, or IMAX. If the IMAX level is achieved during insertion events, charging of the card's input bulk capacitance completes at that current level, as required.

As each back-end voltage is ramped in turn, its level is validated to ensure it is within the established tolerances. A timer, also derived from the current ramp capacitor, sets a time limit for ramping each channel, protecting systems from start-up into faulted loads. If all four supplies reach a known-good state, the HEALTHY# output is pulled low to allow enumeration of the add-in card. At this point, all four gate outputs are driving to an internal supply rail in order to fully enhance the external MOSFETs, producing a low-impedance power path for each load. An on-chip charge pump circuit boosts the Channel 1 input supply to provide sufficient gate overdrive to achieve minimum on-state resistance.

To further protect the backplane power bus, electronic circuit breakers provide continuous protection for the system supplies during plug-in operation. If any channel trips its circuit breaker, all supply outputs are rapidly turned off, and remain latched off. Also, the HEALTHY# output becomes high impedance. The TPS2345 can be reset by cycling either the BD_SEL# input or power to the device.

Controlled shutdown and power isolation of a plug-in is initiated by pulling the BD_SEL# pin high during a healthy supply state. The TPS2345 responds by ramping down each back-end voltage in the reverse order of the turn-on sequence.

The precharge output pin (PRECHG) provides a 1-V bias supply. This supply can be used for precharge of the CompactPCI® I/O lines during insertion (and extraction) events, to help minimize perturbations of the bus signals. The precharge circuitry is active whenever the 5-V supply is applied to the VIN2 input; thus the bias is available prior to mate, and after demate, of the bus connector pins.

2 The CompactPCI® Hot Swap EVM Kit

The CompactPCI® EVM kit is a two-board platform that enables designers to rapidly learn about the TPS2345 operation, and evaluate its performance during hot swap events. The main evaluation board is divided into two sections, one simulating the backplane side of a CompactPCI® system, and one containing the power interface section of a plug-in card as it may be implemented in a compliant hot swap system. On the main EVM PCB, the two subsections are essentially isolated. The EVM jumper card, when inserted into the main board's P1 connector, provides a mechanism for simulating hot swap events by abruptly applying power, ground and control signals on the backplane side to their corresponding inputs on the plug-in side. The supply and control signals correspond to those voltages found on the CompactPCI® P1 connector.

2.1 The CompactPCI® Hot Swap EVM Main Board

2.1.1 Module Description

The CompactPCI® EVM main board is divided into two separate circuits. When oriented such that the board nomenclature is upside right to the user, the left side of the board represents the backplane side of the hot swap interface; the right side represents the plug-in module side. This half contains the power isolation and control electronics comprising a hot swap interface that may be incorporated in a CompactPCI® full hot swap plug-in board. In addition, the right side of the main board contains some additional switches and components that can be used to facilitate device testing and for quick modifications of the plug-in characteristics. The two PCB sections connect to a 44-pin PCB edge connector (P1). Mate and demate of the plug-in is accomplished by inserting and removing the EVM jumper card.

The backplane side of the main board contains banana jacks and PCB headers for the connection of the user's power supplies for the four CompactPCI®-specified supply voltages: +12 V, 5 V, 3.3 V, and –12 V. Each input supply plane also contains the minimum amount of bulk capacitance specified to be provided at each backplane connector by the CompactPCI® base specification, PICMG 2.0.

The plug-in side of the EVM board contains the TPS2345 CompactPCI® HSPM IC, four power MOSFET switches, and some configuration capacitors. Two through-hole patterns are provided for each of the four back-end planes for the installation of large-value aluminum electrolytic capacitors. These capacitors simulate the input bulk capacitance that may be found on the target module's back-end supply nodes. Jumpers are provided for the quick connection or disconnection of these capacitors to the individual back-end nodes, for easy reconfiguration of the load characteristics. Table 9 lists the default capacitor values supplied with the EVM board.

In addition, banana jacks and PCB headers are provided on the back-end planes for easy hook-up of the user's resistive or electronic loads for simulation of the target application's load current levels, if desired.

The CompactPCI® Hot Swap EVM top assembly is shown in Figure 1.

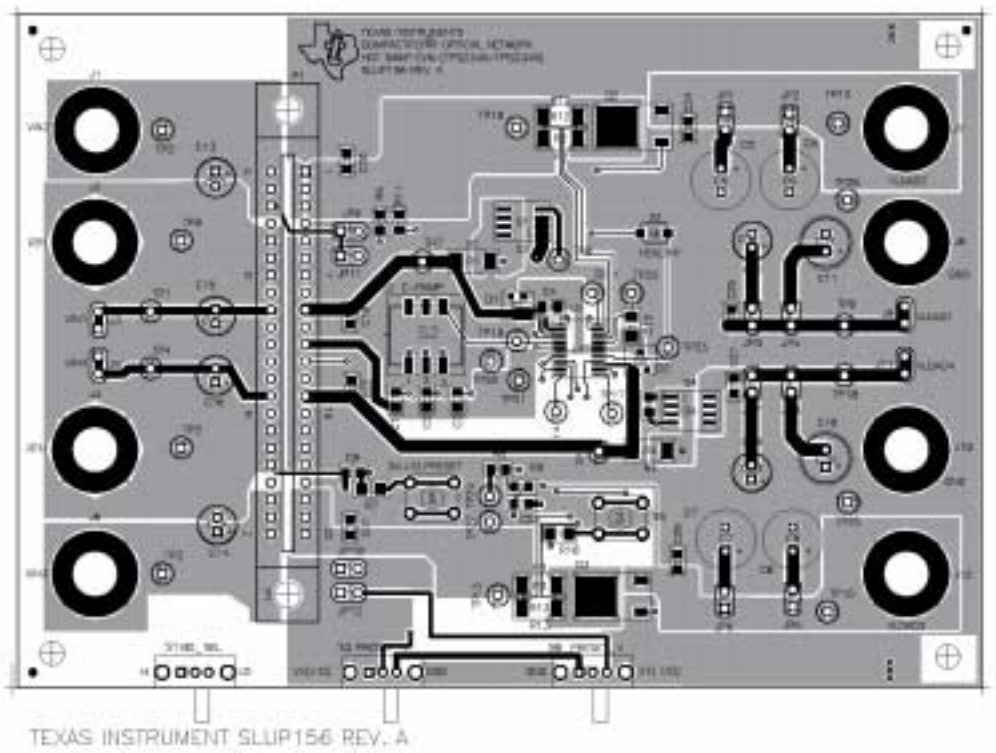

Figure 1. Evaluation Module Main Board Top Assembly

Load current slew rate programming of the TPS2345 device is programmed with a single external capacitor on the IRAMP pin. On the EVM, this is accomplished by selecting from among three pre-installed capacitors. The capacitors are easily selected or disconnected via the individual DIP switches of S2.

The TPS2345 contains an on-chip regulator which can be used as a bias supply for precharging the bus I/O lines if required. The EVM plug-in section contains circuitry to demonstrate the precharge output, including jumpers to select the V(I/O) level (5 V or 3.3 V), and components to simulate I/O line R-C characteristics.

Test points are provided throughout the EVM circuit for waveform monitoring. The test point connections are listed in Table 8.

2.1.2 EVM Schematic Diagram and List of Materials

The EVM main board schematic diagram is shown in Figures 2 and 3.

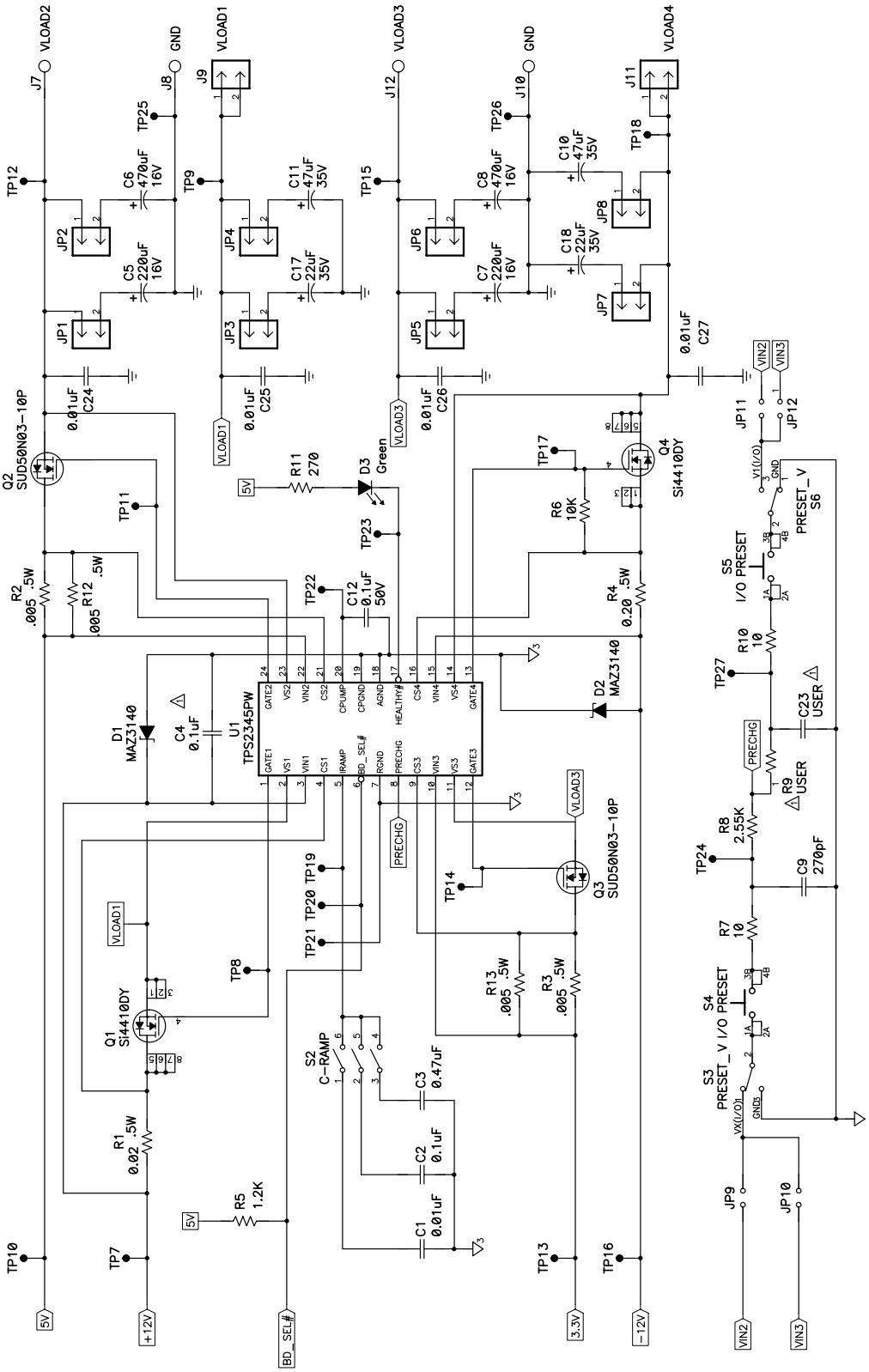

Figure 2. TPS2345EVM Schematic (Sheet 1)

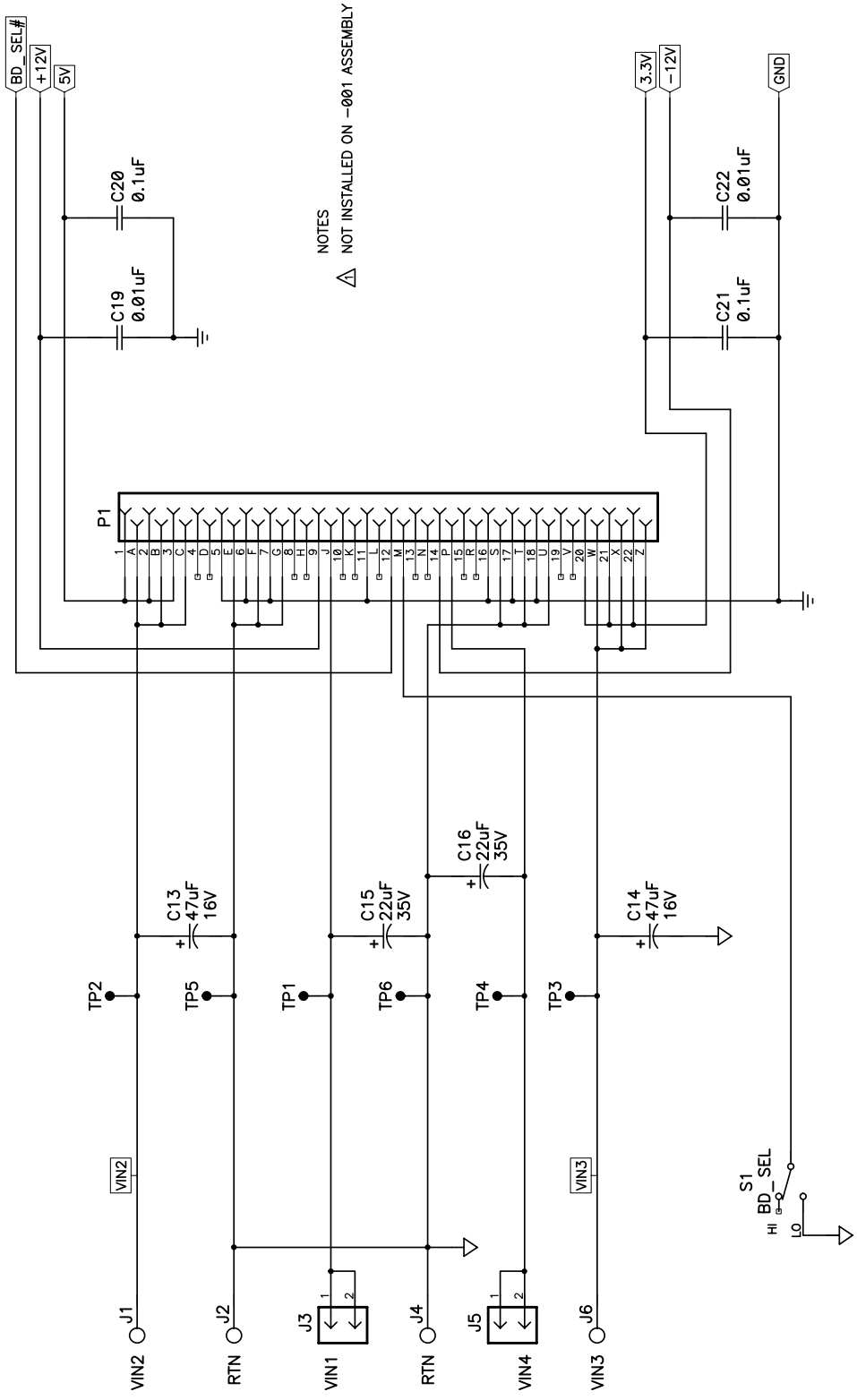

Figure 3. TPS2345EVM Schematic (Sheet 2)

Table 1. List of Materials (TPS2345EVM)

REF DES	QTY	DESCRIPTION	MANUF	PART NUMBER
C1	1	Capacitor, ceramic, 0.01 μF, 16 V, 10%, X7R	Vitramon	VJ0805Y103KXJA
C2	1	Capacitor, ceramic, 0.1 μF, 16 V, 10%, X7R	Vitramon	VJ0805Y104KXJA
C3	1	Capacitor, ceramic, 0.47 μF, 16 V, 10%, X7R	Panasonic	ECJ–2FB1C474K
C4	–	Capacitor, ceramic, 0.1 μF, 25 V, 20%, Z5U	Vitramon	VJ0805U104MXXA
C5, C7	2	Capacitor, aluminum electrolytic, 220 μF, 16V, 20%	Panasonic	EEU–FC1C221
C6, C8	2	Capacitor, aluminum electrolytic, 470 μF, 16V, 20%	Panasonic	ECA–1CM471
C9	1	Capacitor, ceramic, 270 pF, 50 V, 10%, C0G	Vitramon	VJ0805A271KXAA
C10, C11	2	Capacitor, aluminum electrolytic, 47 μF, 35 V, 20%	Panasonic	EEU–FC1V470
C12	1	Capacitor, ceramic, 0.1 μF, 50 V, 20%, Z5U	Vitramon	VJ1206U104MXAA
C13, C14	2	Capacitor, aluminum electrolytic, 47 μF, 16V, 20%	Panasonic	EEU–FC1C470
C15, C16, C17, C18	4	Capacitor, aluminum electrolytic, 22 μF, 35 V, 20%	Panasonic	EEU–FC1V220
C19, C22, C24, C25, C26, C27	6	Capacitor, ceramic, 0.01 μF, 25 V, 20%, Z5U	Vitramon	VJ0805U103MXXA
C20, C21	2	Capacitor, ceramic, 0.1 μF, 25 V, 20%, Z5U	Vitramon	VJ0805U104MXXA
C23	–	Capacitor, ceramic, 0805	Standard	Standard
D1, D2	2	Diode, zener, 14 V @ 5 mA, 0.2W, 2.5%	Panasonic	MAZ3140–M
D3	1	Diode, LED, green, GW type	Panasonic	LN1361C
J1, J2, J4, J6–J8, J10,J12	8	Jack, banana, non-insulated, PC mount	Pomona	3267
J3, J5, J9, J11, JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP8. JP9. JP10, JP11, JP12	16	Header, 2-pin, single row, 0.100 center, 0.025 sq., 0.230 head	Sullins	PTC36SAxN
P1	1	Connector, 44-pin, PCB vert., 0.100 centers	Tyco	530843–4
Q1, Q4	2	XSTR, MOSFET, N-channel, $V_{(BR)}$ > 30V	Vishay–Siliconix	Si4410DY
Q2, Q3	2	XSTR, MOSFET, N-channel, $V_{(BR)}$ > 30V	Vishay–Siliconix	SUD50N03–10P
R1	1	Resistor, 0.02 Ω, 0.5W, 1%	Vishay–Dale	WSL–2010 .020<1%
R2, R3, R12, R13	4	Resistor, 0.005 Ω, 0.5W, 1%	Vishay–Dale	WSL–2010 .005<1%
R4	1	Resistor, 0.20 Ω, 0.5W, 1%	Vishay–Dale	WSL–2010 .200<1%
R5	1	Resistor, 1.2 kΩ, 0.1W, 5%	Venkel	CR0805–10W122J
R6	1	Resistor, 10 kΩ, 0.1W, 5%	Venkel	CR0805–10W103J
R7, R10	2	Resistor, 10 Ω, 0.125W, 5%	Venkel	CR1206–8W100J
R8	1	Resistor, 2.55 kΩ, 0.1W, 1%	Venkel	CR0805–10W2551F
R9		Resistor, 0.1W, 5%, 0805	Standard	Standard
R11	1	Resistor, 270 Ω, 0.1W, 5%	Venkel	CR0805–10W271J
S1, S3, S6	3	Switch, slide, SPDT, right angle, 200mA	E–Switch	EG1213
S2	1	Switch, dip, 3-position, SPST	CTS	219–03MS
S4, S5	2	Switch, momentary, NO, 1.6N	Panasonic	EVQ–PAE0xy
TP5, TP6, TP21, TP25, TP26	5	Jack, test point, black	Farnell	240–333
TP1–TP4, TP7–TP20, TP27, TP22–TP24	22	Jack, test point, red	Farnell	240–345
U1	1	CompactPCI Hot Swap Power Manager	Texas Instruments	TPS2345PW

REF DES	QTY	DESCRIPTION	MANUF	PART NUMBER
N/A	1	Plug, keying, connector, intercontact	Tyco	650025–2
N/A	10	Jumper, 2-pin, 0.100 center	Sullins	STC02SYAN
N/A	4	Spacer, nylon, hexagonal, #6–32, 0.625 in.	Eagle	14HTSP020
N/A	4	Screw, nylon, round head, #6–32, 0.25 in.	Eagle	010632R025
N/A	1	PCB, FR–4, 2–Layer, SMOBC, 5.6” x 3.9”, 0.062” thick	Texas Instruments	SLUP156
N/A	1	PCB, FR–4, 2–Layer, SMOBC, 2.33” x 2.30”	Texas Instruments	SLUP159

2.2 The CompactPCI® Hot Swap EVM Jumper Card

2.2.1 Description

The EVM jumper card is used to apply the four supply voltages, present at the input banana jacks, to the four supply inputs of the main board’s plug-in side. Inserting and removing the jumper card into and out of the main board P1 connector simulates hot swap events. There are no components mounted on the jumper card; it simply makes the point-to-point connections to apply input power to the plug-in electronics. This mechanism allows the EVM main board, which may have several scope probes and meter leads connected to it during use, to remain stationary on the user’s bench.

The jumper card top layer is shown in Figure 4.

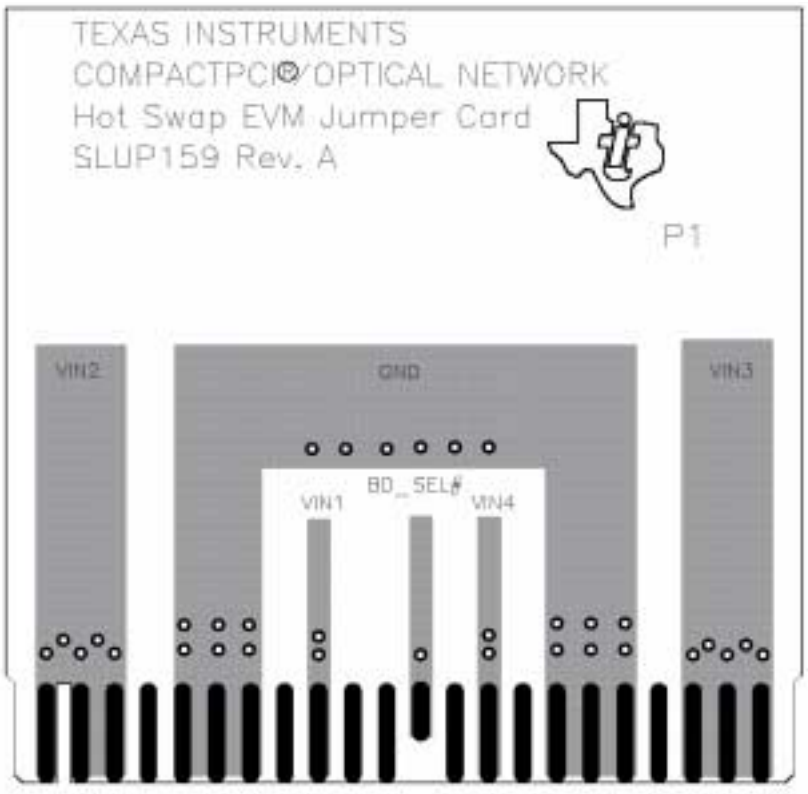

Figure 4. Jumper Card Top Aseembly

2.2.2 Jumper Card Schematic Diagram

The EVM jumper card schematic diagram is shown in Figure 5.

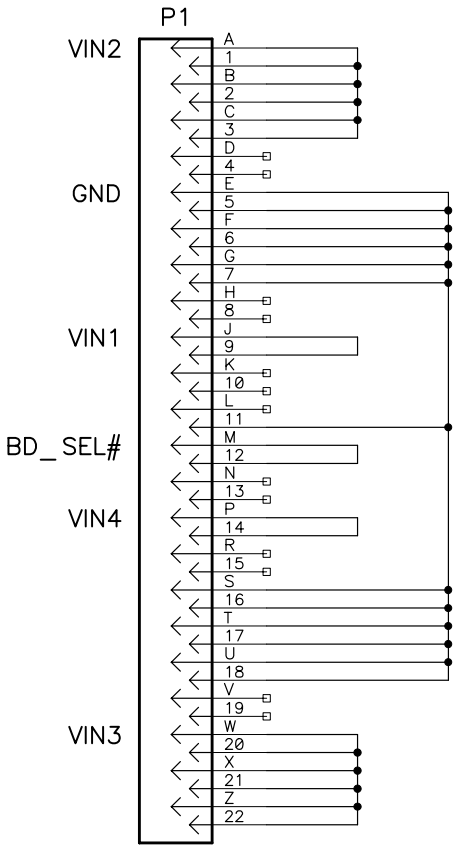

Figure 5. Jumper Card Schematic

There are no components installed on the jumper card, and consequently no list of materials required.

2.3 Operating Specifications

The EVM and jumper card are designed for some degree of user reconfiguration, as described later in Section 4, *Using the EVM Kit to Evaluate the TPS2345*. This includes modifications for different load current requirements. However, under no circumstances should the EVM be operated beyond the input supply and load currents specified in Table 2.

Table 2. Absolute Maximum Ratings (1)(2)

PARAMETER	MIN	MAX	UNITS
Channel 1 supply voltage range, VIN1(3)	–0.3	14	V
Channel 2 supply voltage range, VIN2	–0.3	15	
Channel 3 supply voltage range, VIN3	–0.3	15	
Channel 4 supply voltage range, VIN4(3)	–14	0.3	
Load current, VLOAD1		–3	A
Load current, VLOAD2		–9	
Load current, VLOAD3		–9	
Load current, VLOAD4		–1.9	
Load return current, J8, J10		12	
Supply return current, J2, J4		–12	
Ambient operating temperature range	–40	85	°C

(1) All voltages are with respect to the PCB RTN node at J2 or J4.
(2) Currents are positive into and negative out of the specified terminal.
(3) The EVM contains clamping circuitry to clamp the voltage of the TPS2345 VIN1 and VIN4 inputs below ±15 V. The EVM survives transient voltage excursions at J3 and J5 beyond the DC limits specified in Table 2.

Component selection for the EVM was done to configure the circuit for a typical CompactPCI® application. As such, the target operating conditions, for the factory-installed component values, are as shown in Table 3.

Table 3. EVM Recommended Operating Conditions (1)(2)

PARAMETER	MIN	TYP	MAX	UNITS
Nominal supply voltage, VIN1		12		V
Nominal supply voltage, VIN2		5		
Nominal supply voltage, VIN3		3.3		
Nominal supply voltage, VIN4		–12		
Load current, VLOAD1			–0.7	A
Load current, VLOAD2			–6.5	
Load current, VLOAD3			–6.5	
Load current, VLOAD4			–0.3	

(1) All voltages are with respect to the PCB RTN node at J2 or J4.
(2) Currents are positive into and negative out of the specified terminal.

3 Getting Started

3.1 Equipment Requirements

The following test equipment is required to use the EVM:

- Power supply, 15 Vdc at 2 A minimum, quantity of 2
- Power supply, 6 Vdc at 10 A minimum, quantity of 2
- Oscilloscope, 4-channel preferred
- Digital voltmeter (DVM)

3.2 Verifying the EVM Operation

The following procedure steps may be used to verify functional operation of the EVM after receipt.

3.2.1 Equipment Setup

CAUTION:

Under no circumstances should the shorting jumpers be installed across both headers JP9 and JP10, or both JP11 and JP12 at the same time. Doing so may cause damage to the EVM board or test equipment.

If installed, remove the jumper card from the main board P1 connector. Connect the supplied jumpers across headers JP1 through JP8, inclusive.

Connect the EVM and test equipment as shown in Figure 6. Turn on and adjust the power supplies to the nominal voltages shown in Table 4. On each supply, verify the current limit control is set to allow sourcing of the minimum current indicated in the table.

NOTE: During a power down event, the TPS2345 HSPM IC sequences the loads off in a prescribed order. For each load disable, the back-end plane voltage is monitored for decay below 1 V prior to advancing to and turning off the next load (except for the negative voltage channel). Because of the large amount of capacitance on the EVM back-end planes, this sequence can take a long time if no discharge load other than the device sense pins is provided. Consequently, the user may wish to connect discharge resistors at each voltage plane, shown as R_{LOAD} in Figure 6. This function works for even light loads; for example, 510-Ω, 1-W resistors are sufficient.

Table 4. Power Supply Setup Parameters

POWER SUPPLY	NOMINAL OUTPUT (V)	MINIMUM CURRENT (A)
1	12.0	2
2	5.0	10
3	3.3	10
4	–12.0	2

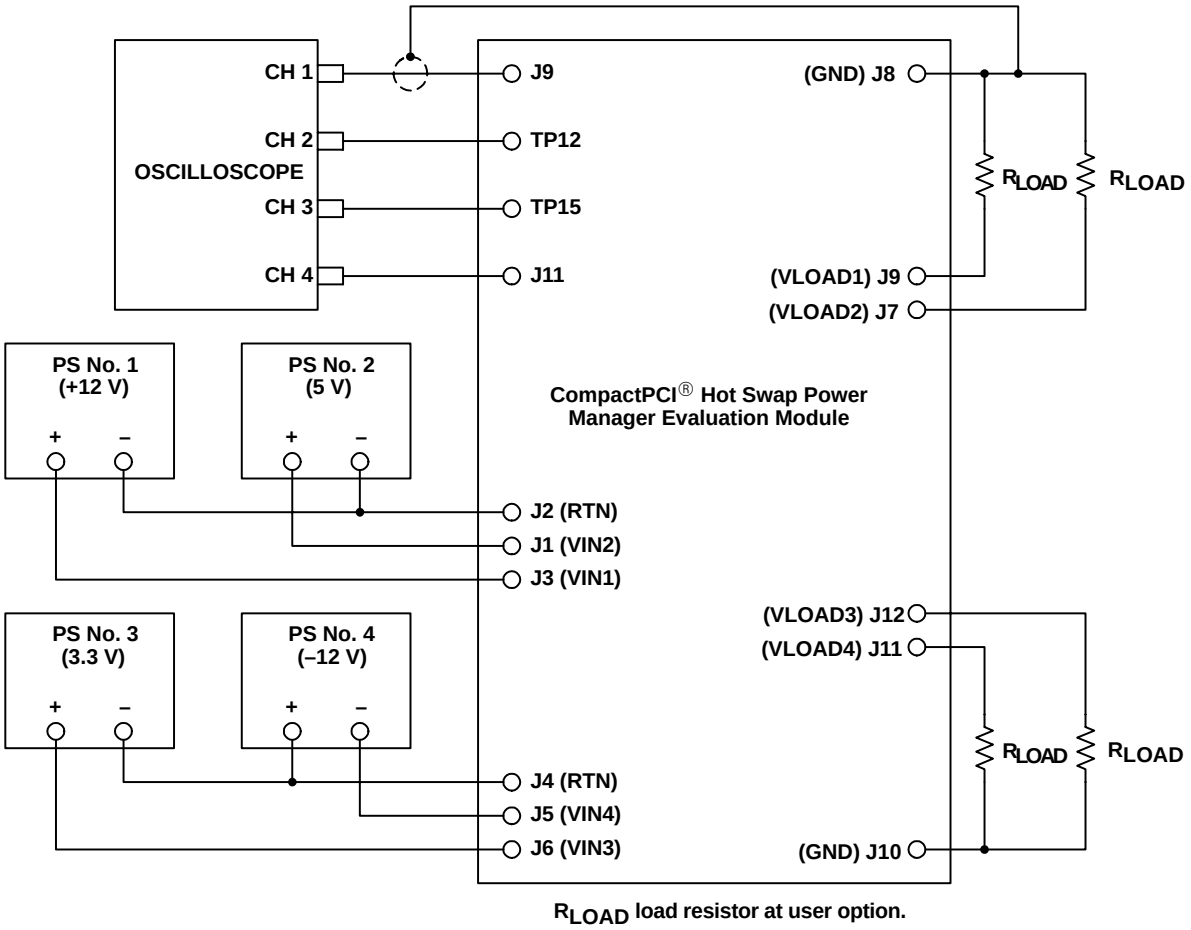

Figure 6. EVM Setup

On the EVM main board, set the switches to the initial positions indicated in Table 5.

Table 5. EVM Switch Initlal Positions

SWITCH	REFERENCE DESIGNATOR	POSITION
BD_SEL	S1	HI
C–RAMP	S2–1	ON
	S2–2	OFF
	S2–3	OFF
PRESET_V	S3	GND
	S6	GND

3.2.2 Functionality Test

Insert the jumper card into the P1 connector, observing the proper insertion keying. On the EVM main board, verify the HEALTHY LED is OFF. Verify the voltage readings indicated in Table 6 are obtained at the corresponding test points. All voltages are referenced to the PCB ground at TP25 or TP26.

Table 6. Test Point Voltages – Outputs OFF

TEST POINT	VOLTAGE READING
TP9	0 ±10 mVdc
TP12	0 ±10 mVdc
TP15	0 ±10 mVdc
TP18	0 ±10 mVdc
TP20	4.8 Vdc minimum
TP24	1.0 ± 0.1 Vdc

On the oscilloscope, set the channel amplifiers to the following scales:

- CH1: 5 V/div
- CH2: 2 V/div
- CH3: 2 V/div
- CH4: 5 V/div

Set the scope time base to 5 ms/div. Set the scope to trigger on the rising edge of Channel 1, at about a 5-V level. Set the trigger mode to NORMAL.

On the EVM main board, set the BD_SEL switch to the LO position. Verify that the green HEALTHY LED is illuminated. On the oscilloscope, a sweep should have been obtained similar to that shown in Figure 7. The total ramp-up time of all four back-end voltages, t_{START} in Figure 7, should be about 27 ms. To verify that all four back-end planes are powered up, a DVM can be used to verify the Table 7 voltages are present at the test points indicated. All voltages are referenced to the PCB ground at TP25 or TP26.

Table 7. Test Point Voltages – Outputs ON

TEST POINT	VOLTAGE READING
TP9	12 Vdc
TP12	5 Vdc
TP15	3.3 Vdc
TP18	–12 Vdc
TP24	1.0 ± 0.1 Vdc

Place the BD_SEL switch in the HI position.

Reconnect the Channel 1 scope probe to test point TP19. Set the Channel 1 vertical amplifier to 500 mV/div. Set the scope time base to 100 ms/div. Set the scope to trigger on the rising edge of Channel 1 at about 500 mV, single sequence.

Verify all four back-end planes have decayed to approximately 0 volts. On the EVM main board, set switches S2–2 and S2–3 to the ON position.

Place the BD_SEL switch in the LO position. After a slight delay, the HEALTHY LED is illuminated and a scope sweep similar to the one shown in Figure 8 is seen.

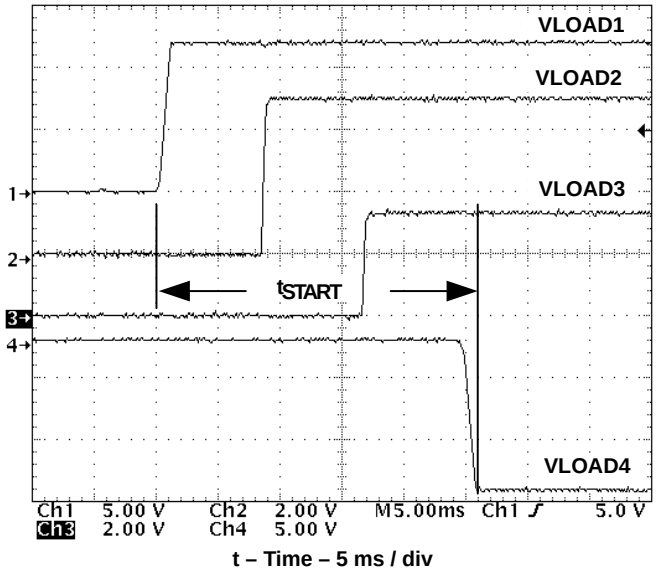

Figure 7. Load Power-Up Sequence

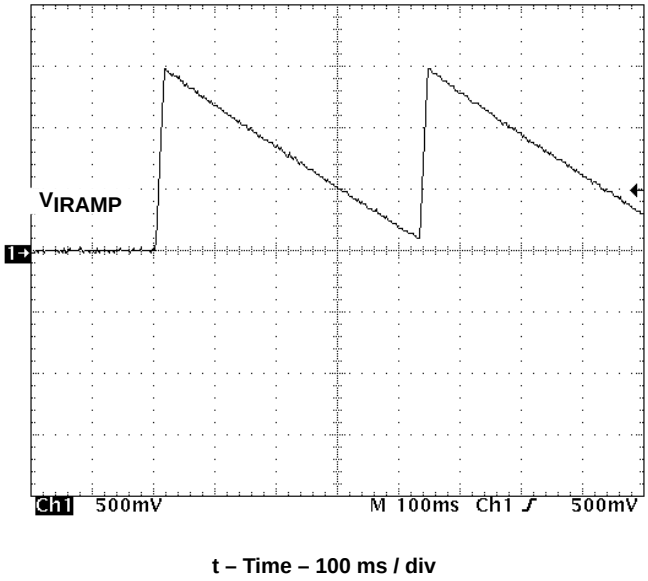

Figure 8. IRAMP Waveform Pulse

4 Using the EVM Kit to Evaluate the TPS2345

Procedures similar to the steps of Section 3.2.2 *Functionality Test*, for functional test of the EVM can also be used to continue evaluation of the TPS2345 controller. Additional details about the EVM features are provided in this section.

4.1 Test Points

The EVM contains numerous test points located throughout the circuit for waveform monitoring. A list of the EVM test points and their associated signals is given in Table 8.

Table 8. EVM Test Points

TEST POINT	SIGNAL NAME	DESCRIPTION
TP1	VIN1	Channel 1 (+12 V) supply input
TP2	VIN2	Channel 2 (5 V) supply input
TP3	VIN3	Channel 3 (3.3 V) supply input
TP4	VIN4	Channel 4 (–12V) supply input
TP5	RTN	Supply return
TP6	RTN	Supply return
TP7	VIN1	Channel 1 (+12V) power, plug–in side
TP8	GATE1	Gate drive for Channel 1 pass FET
TP9	VLOAD1	Channel 1 load (back-end plane) voltage
TP10	VIN2	Channel 2 (5 V) power, plug-in side
TP11	GATE2	Gate drive for Channel 2 pass FET
TP12	VLOAD2	Channel 2 load (back-end plane) voltage
TP13	VIN3	Channel 3 (3.3 V) power, plug-in side
TP14	GATE3	Gate drive for Channel 3 pass FET
TP15	VLOAD3	Channel 3 load (back-end plane) voltage
TP16	VIN4	Channel 4 (–12 V) power, plug–in side
TP17	GATE4	Gate drive for Channel 4 pass FET
TP18	VLOAD4	Channel 4 load (back-end plane) voltage
TP19	IRAMP	TPS2345 IRAMP pin
TP20	BD_SEL#	BD_SEL# signal
TP21	GND	Circuit common (ground) node
TP22	CPUMP	TPS2345 charge pump output
TP23	HEALTHY#	HEALTHY# signal
TP24	V(P)	Test network, precharge circuit
TP25	GND	Load common
TP26	GND	Load common
TP27	V(P)	Test network, precharge circuit

4.2 Load Capacitors

Capacitors are available on-board for connection into the four switched load-side planes. These capacitors can be used to model the bulk capacitance that the target hot swap plug-in presents to the supply planes. Table 9 lists the load capacitors installed for each back-end node.

The jumpers shown for each plane can be used for quick connect into or disconnect from the circuit.

Table 9. EVM Load Capacitors

BACK-END NODE	JUMPER NAME	VALUE	MINIMUM VOLTAGE RATING
12V (VLOAD1)	JP3	22 µF	35 V
	JP4	47 µF	35 V
5V (VLOAD2)	JP1	220 µF	16 V
	JP2	470 µF	16 V
3.3V (VLOAD3)	JP5	220 µF	16 V
	JP6	470 µF	16 V
–12V (VLOAD4)	JP7	22 µF	35 V
	JP8	47 µF	35 V

To closer approximate the user's application, these capacitors can be removed from the PCB and replaced.

CAUTION:

When replacing any of the large aluminum electrolytic load capacitors, select only those capacitors with an appropriate voltage rating, and observe the polarity marking on the PCB silkscreen.

4.3 CompactPCI® BD_SEL# Signal

The BD_SEL# signal is used in a hot swap CompactPCI® system to detect board presence and for platform control of the hardware connection process. On the EVM, this signal is controlled with the BD_SEL switch, located towards the left end of the main board. Also, in a typical implementation, the BD_SEL# signal is carried via one of the shortest connector pins in the staged connector. The EVM jumper card has only two levels of contact staging; however, BD_SEL# is on shorter contacts such that it mates only after all power and ground pins connect.

4.4 Changing the Current Limit Thresholds

During power-up of a plug-in card, the TPS2345 limits the peak current sourced to each back-end plane for charging of bulk capacitance. The LCA in each of the device's four channels (one per controlled supply) senses load current as the drop across an external sense resistor. Current is regulated by slewing the gate of the pass FET to maintain the voltage drop at a preset level. Therefore, peak current can be established by selecting the appropriate sense resistor value. As supplied from the factory, the CompactPCI® Hot Swap EVM has the following sense resistor values installed, with the corresponding nominal current limits shown.

Table 10. Default Current Limit Thresholds

DEVICE CHANNEL	SUPPLY CONTROLLED	SENSE RESISTOR		CURRENT LIMIT (A)	
		REFERENCE DESIGNATOR	VALUE (mΩ)	MINIMUM	NOMIMAL
1	+12V	R1	20	0.8	1.0
2	5V	R2 || R12	2.5 (1)	6.8	8.0
3	3.3V	R3 || R13	2.5 (1)	6.8	8.0
4	–12V	R4	200	0.375	0.75

(1) The parallel combination of these two resistors.

To modify the current limit for any of the EVM channels, the appropriate resistor can be determined from equation (1).

$$R_{SNSx} = \frac{VMAXx}{IMAXx} \quad (1)$$

where

- R_{SNSx} is the sense resistor value for channel x
- VMAXx is the sense voltage limit
- IMAXx is the desired current limit threshold

Using the device minimum values for VMAXx along with the required minimum current limit ensures that minimum amount of current can always be supplied to the load. For information on the specified sense voltage values, please refer to the TPS2345 data sheet.

4.5 Changing the Inrush Slew Rate

During a turn-on sequence, the TPS2345 power manager IC also controls the slew rate at which charging current is ramped to the back-end power planes. The slew rate is user-programmable as a function of sense resistor and a single capacitor connected between the IRAMP and GND pins. The EVM provides three preset capacitor values, selectable via the individual DIP switches of S2. These default values and the resultant nominal slew rates are given in Table 11

Table 11. EVM Default Slew Rates (Amperes/Second)

S2 DIP CLOSED	SUPPLY NAME		
	12 V	5 V	3.3 V
1	4300	34,400	34,400
2	430	3440	3440
3	91	730	730

The slew rate of the three positive supplies can be changed by replacing any capacitor C1, C2 or C3 on the main board. The PCB component patterns are sized for standard 0805 ceramic chip capacitors. To configure the EVM for a different slew rate, the recommended procedure is to select the supply with the most stringent (slowest) requirement, and calculate a new capacitor value from equation (2). Then, verify that the new value satisfies the requirements of the remaining supplies using equation (3).

$$C_{RAMPx} = \frac{58}{67,500 \times R_{SNSx} \times \left(\frac{di}{dt}\right)_x} \quad (2)$$

where

- C_{RAMPx} is the capacitor value (in microfarads) indicated by the Channel x slew rate requirement
- R_{SNSx} is the Channel x sense resistor value, in ohms
- $(di/dt)_x$ is the slew rate in amperes/milliseconds

Once a value for C_{RAMP} has been selected, the slew rates of the other channels (in A/ms) can be determined by rewriting equation (2) as equation (3), and substituting the appropriate values.

$$\left(\frac{di}{dt}\right)_x = \frac{58}{67,500 \times R_{SNSx} \times C_{RAMP}} \quad (3)$$

- C_{RAMP} is given in microfarads

4.6 Using the Precharge Circuitry

The CompactPCI® Hot Swap EVM contains two test points, TP24 and TP27, either of which can be used to observe the operation of the PRECHG output of the TPS2345. The internal precharge regulator provides a 1-V bias supply at the PRECHG pin whenever 5-V power (VIN2 input) is applied.

Test point TP24 can be used to monitor the voltage that might be seen at any of the plug-in module's I/O pins during an insertion. TP24 connects to the output (pin side) of an R-C network driven by the PRECHG output. The network is intended to represent the equivalent load on PRECHG of 20 CompactPCI® I/O lines, all pulled simultaneously in the same direction. (This assumes 51-kΩ precharge resistors are used.) The network at TP24 is charged to either V(I/O) or ground potential whenever momentary switch S4 (I/O PRESET) is depressed and held. Place switch S3 (PRESET_V) in either the VX(I/O) or GND position for a V(I/O) or ground bias value, respectively. The TPS2345 precharge circuit brings the network back to the nominal 1.0-V precharge voltage when S4 is released. This can help the user simulate bus precharge at long power pin mating, or during medium pin contact bounce. The VX(I/O) potential can be set to either 5 V by installing a jumper across header JP9, or 3.3 V by installing jumper JP10.

CAUTION:

Do NOT install jumpers across both headers JP9 and JP10 at the same time. Doing so shorts the 5-V and 3.3-V input supplies together, possibly damaging either the supplies or the EVM board. It is recommended to use a single jumper for both JP9 and JP10, such that it must always be removed from one header to be installed across the other.

As an alternative, test point TP27 is provided, with a separate set of component patterns, for monitoring the precharge function with the user's selection of R-C network. Use 0805 resistor R9 and 0805 chip capacitor C23 for this. TP27 connects to the output (pin side) of this network. The network at TP27 is charged to either V(I/O) or ground potential whenever momentary switch S5 (I/O PRESET) is depressed and held. Place switch S6 (PRESET_V) in either the V1(I/O) or GND position for a V(I/O) or ground bias value, respectively. The TPS2345 precharge circuit brings the network back to the nominal 1.0-V precharge voltage when S5 is released. The V1(I/O) potential can be set to either 5 V by installing a jumper across header JP11, or 3.3 V by installing jumper JP12.

CAUTION:

Do NOT install jumpers across both headers JP11 and JP12 at the same time. Doing so will short the 5-V and 3.3-V input supplies together, possibly damaging either the supplies or the EVM board. It is recommended to use a single jumper for both JP11and JP12, such that it must always be removed from one header to be installed across the other.

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