TEXAS INSTRUMENTS

48-V to 3.3-V Forward Converter with Active Clamp Reset Using the UCC2891 Active Clamp Current Mode PWM Controller

User's Guide

December 2006 *Power Supply MAN*

SLUU178A

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Literature Number: SLUU178A
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Using the UCC2891 Active Clamp Current Mode PWM Controller

1 Introduction

The UCC2891EVM evaluation module (EVM) is a forward converter providing a 3.3-V regulated output at 30 A of load current, operating from a 48-V input. The EVM operates over the full 36 V to 72 V telecom input range, and is able to fully regulate down to zero load current. The module uses the UCC2891 current mode active clamp PWM controller for effectively demonstrating the active clamp transformer reset technique.

Benefits of the active clamp include a control driven transformer reset scheme allowing zero voltage switching (ZVS) to increase overall efficiency, lower drain-to-source voltage stress, extended duty cycle beyond 50% and reduced electromagnetic radiated emissions. Combined with synchronous rectification, this EVM is configured to operate at 300 kHz and exhibits a peak efficiency of just over 92%, with a full load efficiency of 89%. The EVM displays many features that might be typical of a more complex design, yet its compact board layout and low component count make it elegantly simple.

2 Description

The UCC2891 controller family provides advanced active clamp control features such as programmable maximum duty cycle clamp, programmable dead time between the two primary switches and the ability to drive either a P-channel, or N-channel MOSFET in either a high-side or low-side active clamp configuration. The UCC2891 also allows the ability to start-up directly from the 48-V telecom bus voltage, eliminating the need for external start-up circuitry. It includes programmable soft start, internal slope compensation for peak current mode control, internal low-line voltage sensing, internal syncronizable clock input, cycle-by-cycle current limiting, and a robust 2-A sink/source TrueDrive™ internal gate drive circuit. The result is a highly efficient design loaded with features, requiring very few external components.

The TrueDrive™ hybrid output architecture used in the UCC2891 uses TI's unique TrueDrive™ Bipolar/CMOS output. To the user, this simply means ultra-fast rise and fall times by providing the highest possible drive current where it is needed most, at the MOSFET Miller plateau region.

The UCC2891/2/3/4 is available in either a 16-pin SOIC or 16-pin TSSOP package for applications where absolute minimal board space is required.

The UCC2891EVM highlights the many benefits of using the UCC2891 active clamp current mode PWM controller. This user's guide provides the schematic, component list, assembly drawing, artwork and test set up necessary to evaluate the UCC2891 in a typical telecom application. More detailed design information can be found listed in the References section.

2.1 Applications

The UCC2891 is suited for use in isolated telecom 48-V input systems requiring high-efficiency and high-power density for very low-output voltage, high-current converter applications, including:

- Server Systems
- Datacom
- Telecom
- DSP's, ASIC's, FPGA's

2.2 Features

The UCC2891EVM features include:

- ZVS transformer reset using active clamp technique in forward converter
- All surface mount components, double sided half brick ($2.2 \times 2.28 \times 0.5$) inches
- Complementary auxilliary drive for active clamp with programmable dead time for ZVS
- Current mode control with synchronization function
- Internal PWM slope compensation
- Start-up directly from telecom input voltage
- Synchronous rectifier output stage allows high-efficiency operation
- Programmable soft-start
- Up to 30-A dc output current
- Regulation to zero load current
- Non-latching, output overcurrent and short circuit protection
- Non-latching, Input undervoltage protection
- 1500-V isolation primary to secondary

3 UCC2891EVM Electrical Performance Specifications

The UCC2891EVM electrical performance specifications are listed in Table 1.

Table 1. UCC2891EVM Performance Summary

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristics					
Input voltage range		36	48	72	V
No load intput current	V_{IN} = 36 V, I_{OUT} = 0 A		75	100	mA
Maximum input current	V_{IN} = 36 V, I_{OUT} = 30 A		3.00	3.25	A
Input voltage ripple	V_{IN} = 72 V, I_{OUT} = 30 A		1.50	1.75	V_{P-P}
Input voltage ripple					
Output voltage	36 V ≤ V_{IN} ≤ 72 V, 0 A ≤ I_{OUT} ≤ 30 A	3.25	3.30	3.35	V
Output voltage regulation	Line regulation (36 V ≤ V_{IN} ≤ 72 V, I_{OUT} = 0 A)		0.003%		
	Load regulation (0 A ≤ I_{OUT} ≤ 30 A, V_{IN} = 48 V)		0.060%		
Output voltage ripple	V_{IN} = 48 V, I_{OUT} = 30 A		30	35	mV_{P-P}
Output load current	V_{IN} = 48 V, I_{OUT} = 30 A	0		30	A
Output current limit	36 V ≤ V_{IN}≤ 72 V			32	
Output current limit					
Switching frequency		275		325	kHz
Control loop bandwidth	36 V ≤ V_{IN} ≤ 72 V, I_{OUT} = 10 A	5		8	
Control loop bandwidth	36 V ≤ V_{IN} ≤ 72 V, 2 A ≤ I_{OUT} ≤ 30 A	30		50	°C
Peak efficiency			92%		
Full load efficiency	V_{IN} = 48 V, I_{OUT} = 30 A		89%		

4 Schematic

A schematic of the UCC2891EVM is shown in Figure 1. Terminal block J1 is the 48-V input voltage source connector and J8 is the output and return for the 3.3-V output voltage.

On the primary side, U1 is the UCC2891 shown with the necessary discrete circuitry for configuring the controller to operate at 300 kHz with the maximum duty clamp set for 0.65. The EVM is programmed to start at VIN=36 V, as determined by R11 and R12. To minimize power dissipation in the current sense, a current sense transformer, T1 is used, as opposed to simply using a sense resistor between the source of Q2 and power ground. Q2 is the primary switching MOSFET and is selected based upon VDS and low RDS(on). Q1 is the AUX (active reset) MOSFET and is selected based upon preferred package only, with only minor consideration given for $R_{DS(on)}$ and Qg. Since the active clamp used in this design is low-side referenced, Q1 must be a P-channel type MOSFET. The reason for this is further explained in application note SLUA299[2]. C9 is the clamp capacitor used to maintain a constant dc voltage. The input voltage is subtracted from the clamp voltage to allow transformer reset during the active clamp period.

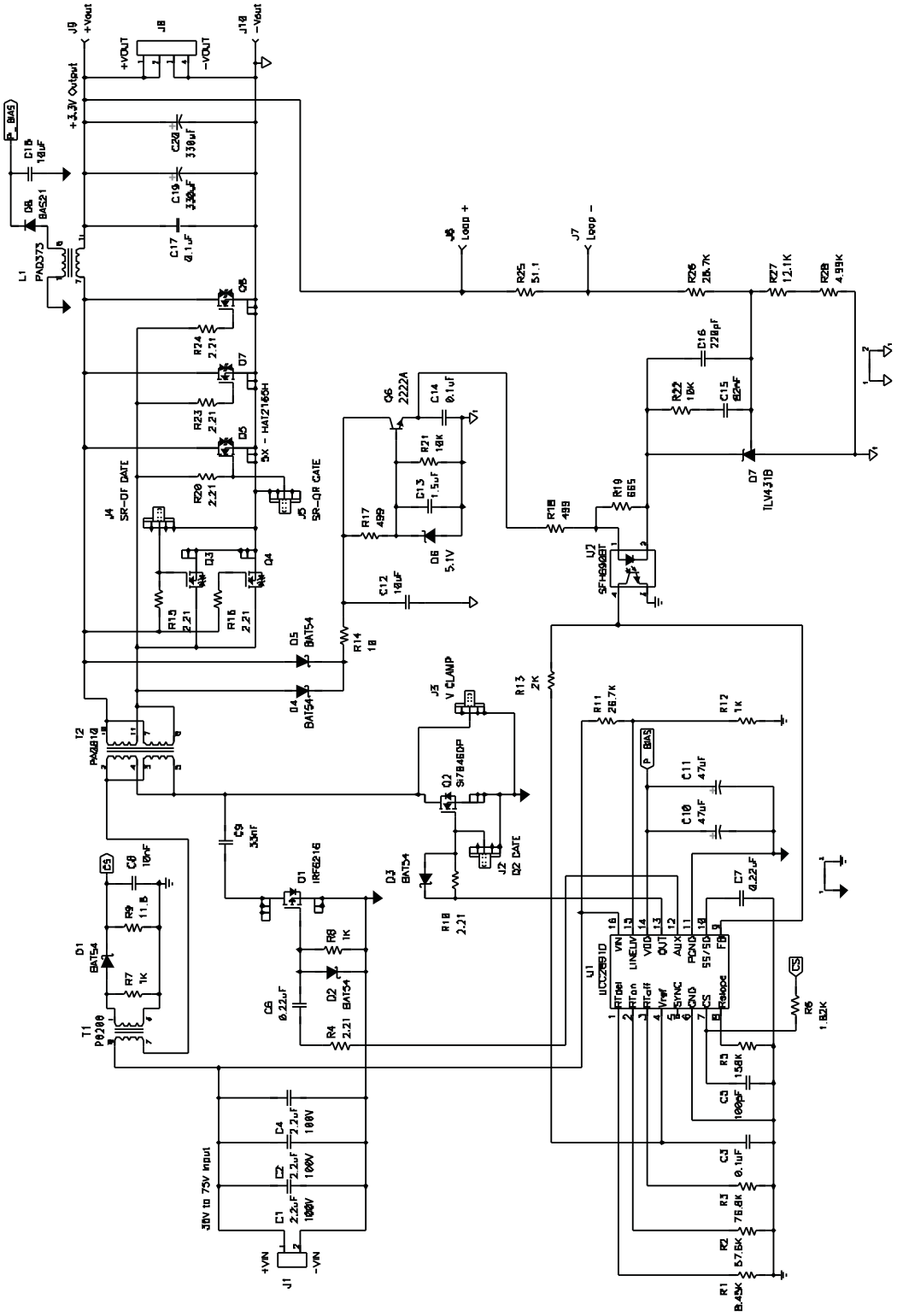

Figure 1. UCC2891EVM Schematic

High efficiency is achieved using self-driven synchronous rectification on the secondary side. Q3 and Q4 are placed in parallel and make up the forward synchronous rectifier (SR), while the reverse SR is made up of the parallel combination of Q5, Q7 and Q8. If the duty cycle were limited to 50% then the reverse SR could be reduced to only two parallel MOSFETs, but since these devices are operating near 60% duty cycle during the freewheel mode, they carry a higher average current than seen by Q3 and Q4. The output inductor L1 has a coupled secondary, referenced to the primary side, used to provide bootstrapping voltage to U1. A stable bias for the optocoupler, U2 is provided by the series pass regulator made up of D6, Q6 and some associated filtering.

Scope jacks J2 and J3 allow the user to measure the gate-to-source and drain-to-source signals for Q2, the primary MOSFET. J4 and J5 allow convenient access to the gate drive signals of each SR on the secondary side. J6 and J7 are available allowing the option of using a network analyzer to non-invasively measure the control to output loop gain and phase.

5 EVM Test Setup

Figure 2 shows the basic test set up recommended to evaluate the UCC2891EVM.

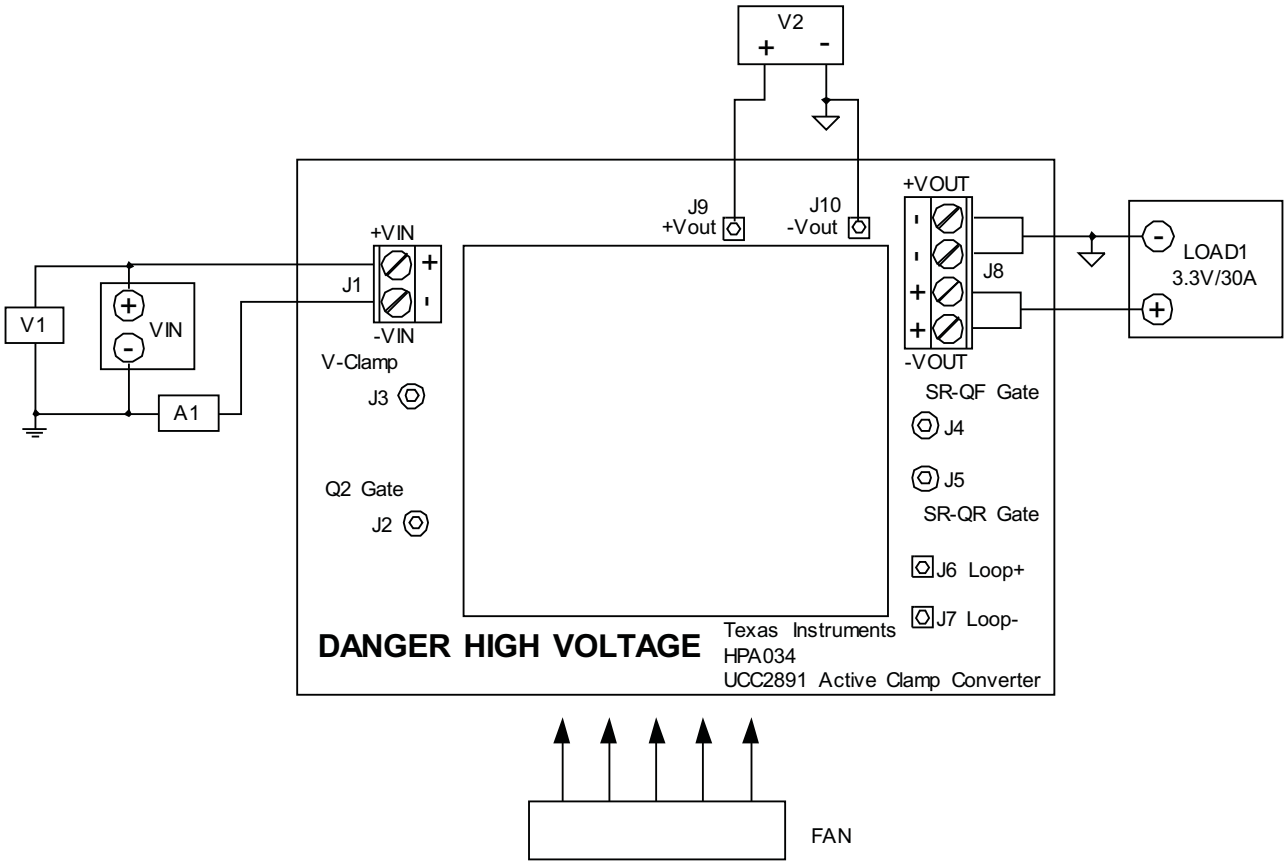

Figure 2. Recommended EVM Test Configuration

5.1 Output Load (LOAD1)

For the output load to VOUT, a programmable electronic load set to constant current mode and capable of sinking between $0A_{DC}$ and $30A_{DC}$, is used. Using a dc voltmeter, V2, it is also advised to make all output voltage measurements directly at J9 and J10 pins. Unless the load has remote sense capability, measuring VOUT at LOAD1 results in some voltage measurement error, especially at higher load current, due to finite voltage drops across the wires between J8 and the electronic load.

5.2 DC Input Source (VIN)

The input voltage is a variable DC source capable of supplying between 0 V_{DC} and 72 V_{DC} at no less than 3.5 A_{DC}, and connected to J1 and A1 as shown in Figure 2. For fault protection to the EVM, good common practice is to limit the source current to no more than 4 A_{DC} for a 36 V input. A dc ammeter, A1 should also be inserted between VIN and J1 as shown in Figure 2.

5.3 Network Analyzer

A network analyzer can be connected directly to J6 and J7. The UCC2891EVM provides a 51.1-Ω resistor (R25) between the output and the voltage feedback to allow easy non-invasive measurement of the control to output loop response.

5.4 Recommended Wire Guage

The connection between the source voltage, VIN and J1 of the EVM can carry as much as $3.25A_{DC}$. The minimum recommended wire size is AWG #20 with the total length of wire less than 8 feet (4 feet input, 4 feet return). The connection between J8 of the EVM and LOAD1 can carry as much as $30A_{DC}$. The minimum recommended wire size is AWG #16, with the total length of wire less than 8 feet (4 feet output, 4 feet return).

5.5 Fan

Most power converters include components that can be hot to the touch when approaching temperatures of 605C. Because this EVM is not enclosed to allow probing of circuit nodes, a small fan capable of 200-400 LFM is recommended to reduce component temperatures when operating at or above 50% maximum rated load current.

6 Power Up/Down Test Procedures

The following test procedure is recommended primarily for power up and shutting down the EVM. Whenever the EVM is running above an output load of 15 A_{DC}, the fan should be turned on. Also, never walk away from a powered EVM for extended periods of time.

1. Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before power is applied to the EVM. Electrostatic smock and safety glasses should also be worn.
2. Prior to connecting the DC input source, VIN, it is advisable to limit the source current from VIN to 3.5-A maximum. Make sure VIN is initially set to 0 V and connected to J1 as shown in Figure 2.
3. Connect the ammeter A1 (0A to10A range) between VIN and J1 as shown in Figure 2.
4. Connect voltmeter (can optionally use voltmeter from VIN source if available), V1 across VIN as shown in Figure 2.
5. Connect LOAD1 to J8 as shown in Figure 2. Set LOAD1 to constant current mode to sink 0 A_{DC} before VIN is applied.
6. Connect voltmeter, V2 across J9 and J10 as shown in Figure 2.
7. Increase VIN from 0 V to 36 V_{DC}.
8. Observe that VOUT is regulating when VIN is at 36 V.
9. Increase VIN to 48 V.
10. Increase LOAD1 from 0 A to 15 A_{DC}.
11. Turn on fan making sure to blow air directly on the EVM.
12. Increase LOAD1 from 15 A_{DC} to 30 A_{DC}.
13. Decrease LOAD1 to 0 A.
14. Decrease VIN from 48 V_{DC} to 0 V.
15. Shut down VIN.

7 Power Up/Down Test Procedures

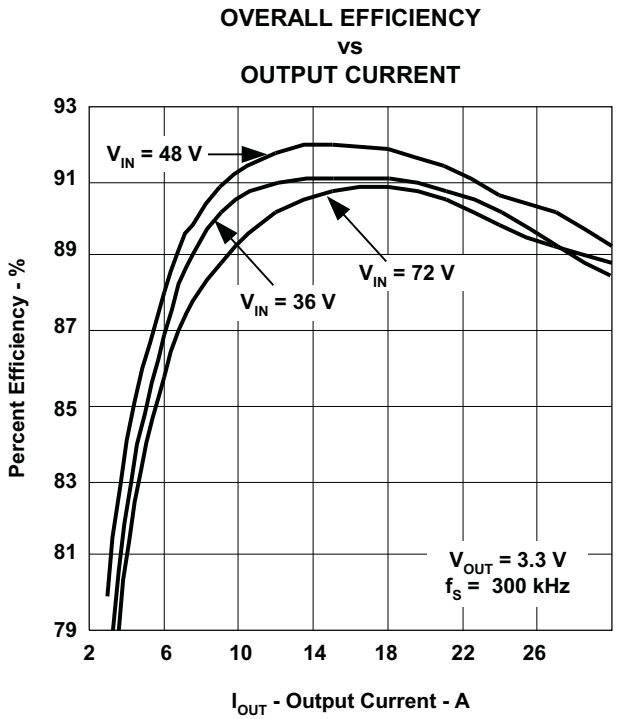

Figure 3.

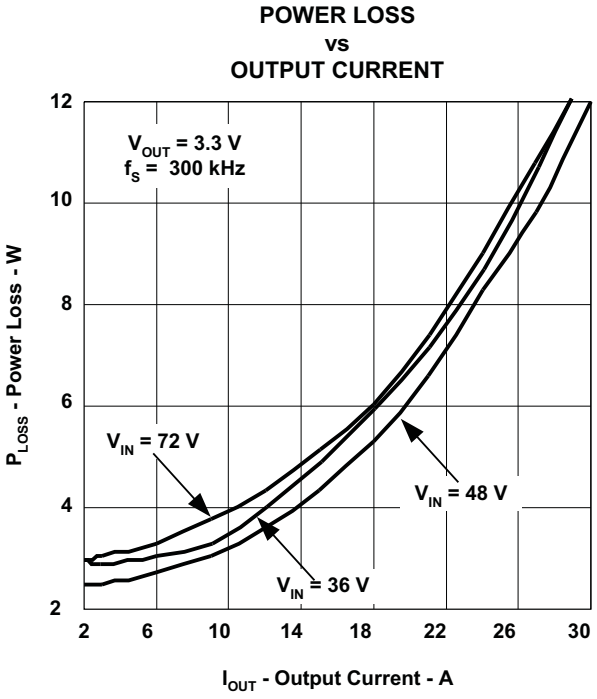

Figure 4.

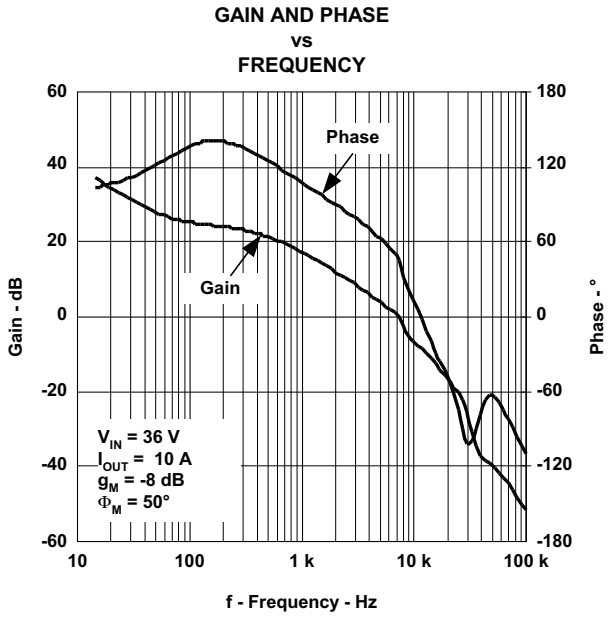

Figure 5.

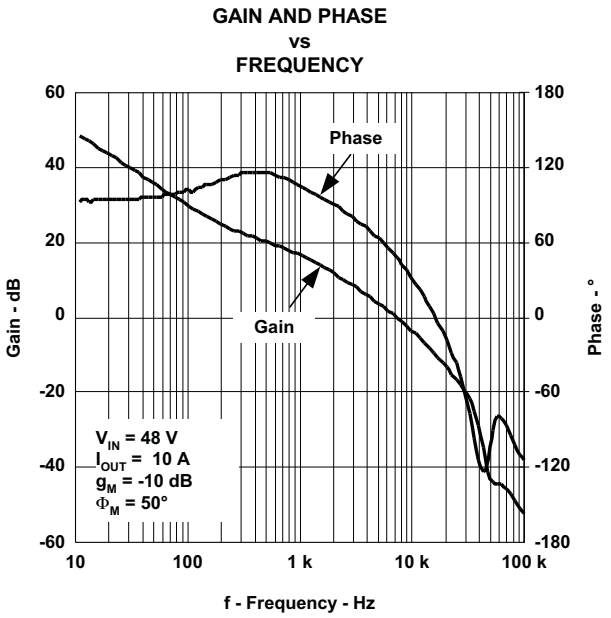

Figure 6.

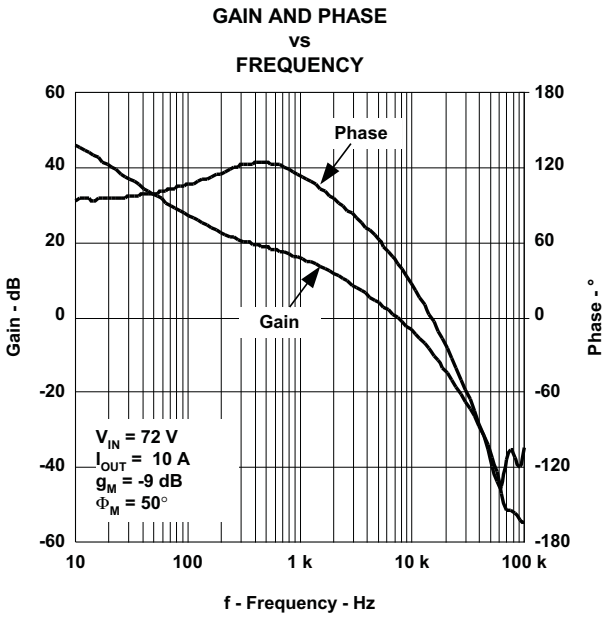

Figure 7.

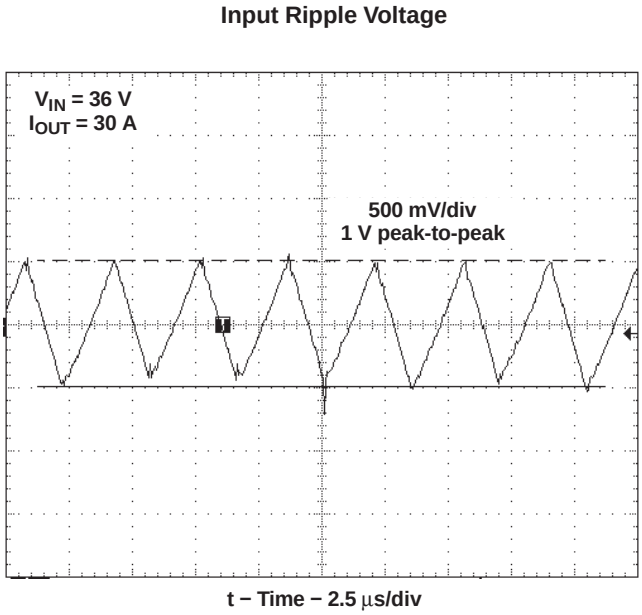

Figure 8.

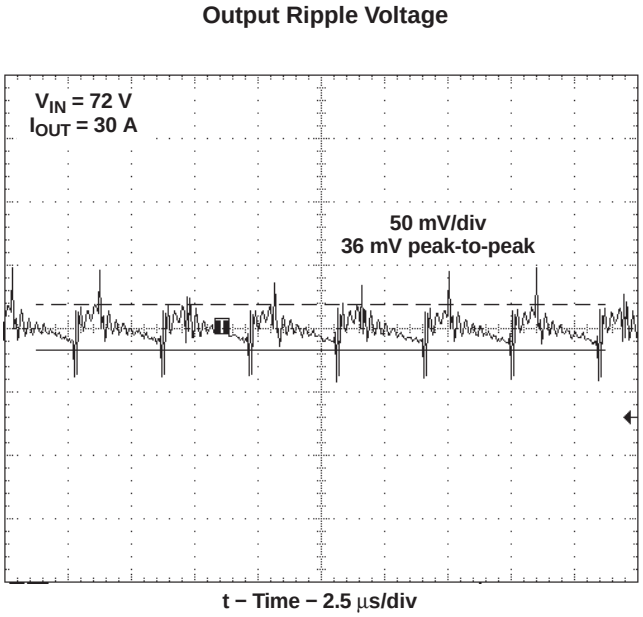

Figure 9.

Output Ripple Voltage

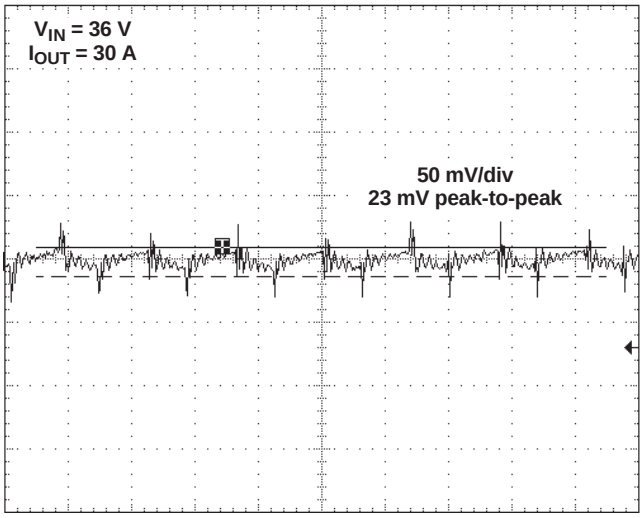

Figure 10.

SR Gate Drive

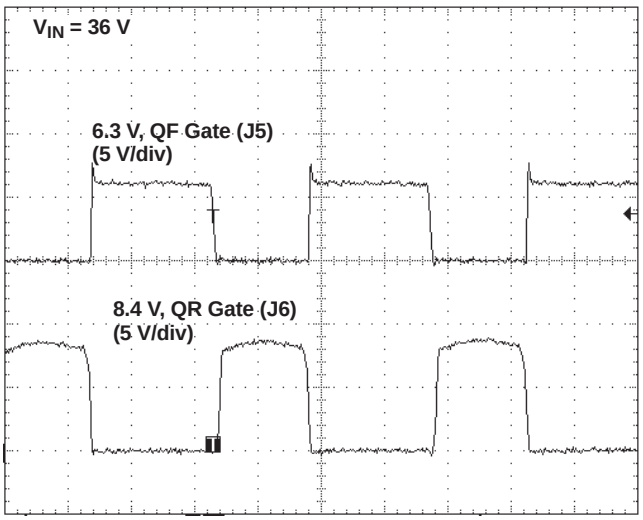

Figure 12.

Transformer Primary

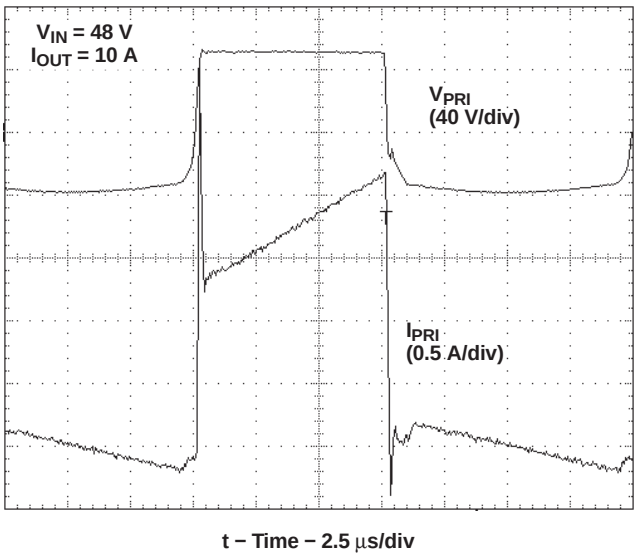

Figure 11.

SR Gate Drive

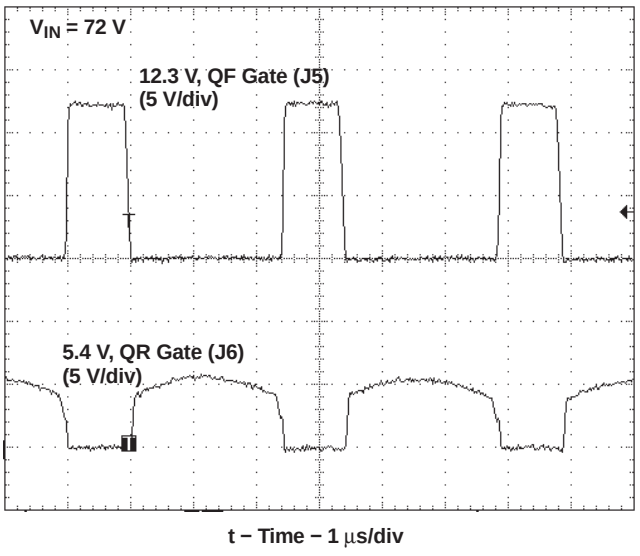

Figure 13.

8 EVM Assembly Drawing and Layout

Figure 14 through Figure 20 show the top-side and bottom-side component placement for the EVM, as well as device pin numbers where necessary. A four layer PCB was designed using the top and bottom layers for signal traces and component placement along with an internal ground plane. The PCB dimensions are 3.6" x 2.7" with a design goal of fitting all components within the industry standard half-brick format, as outlined by the box dimensions 2.28" x 2.20" shown in Figure 15. All components are standard OTS surface mount components placed on the both sides of the PCB. The copper-etch for each layer is also shown.

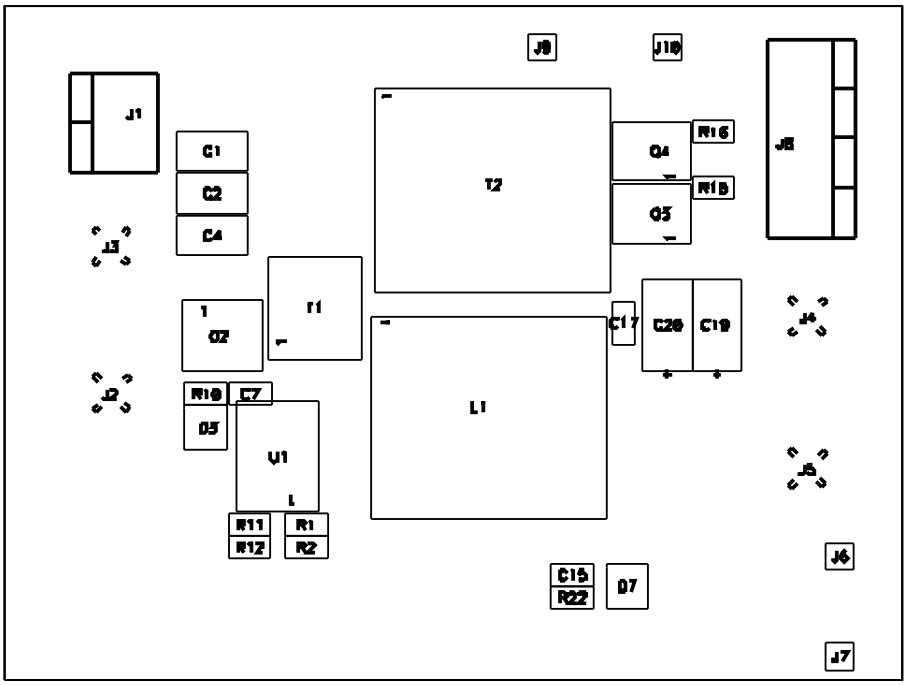

Figure 14. Top Side Component Assembly

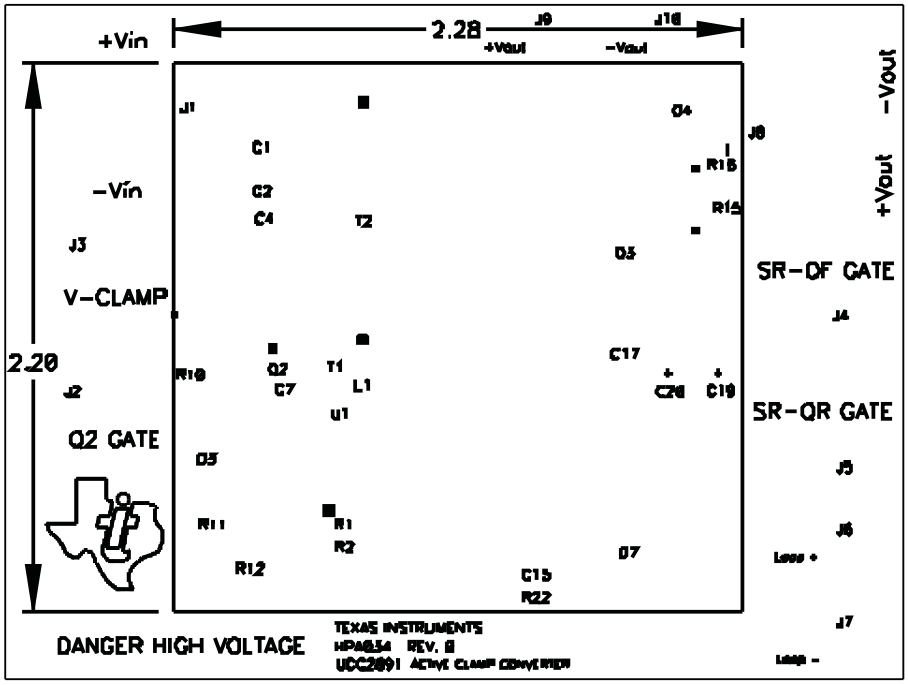

Figure 15. Top Side Silk Screen

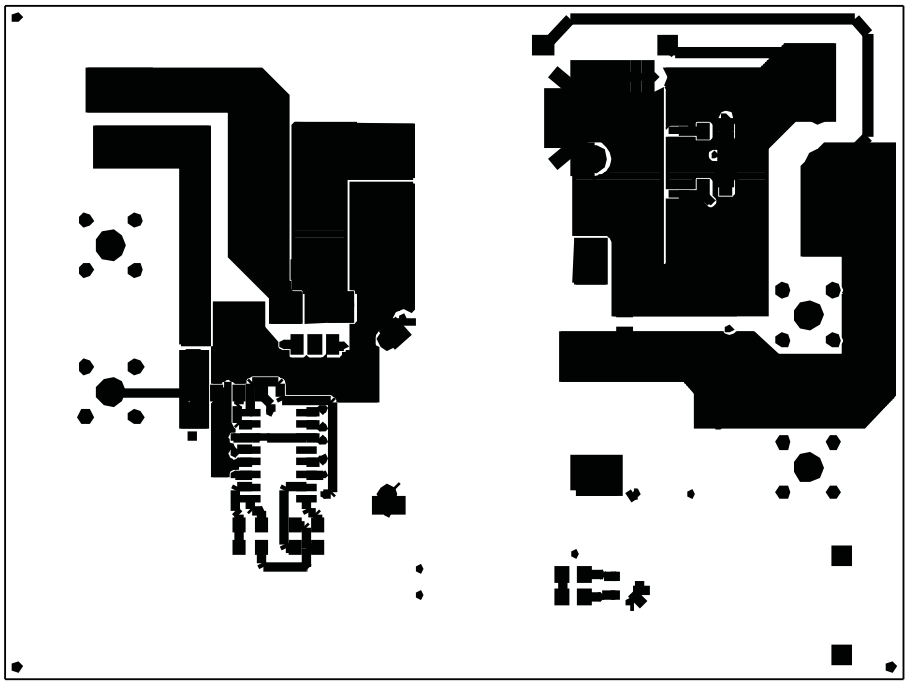

Figure 16. Top Signal Trace Layer

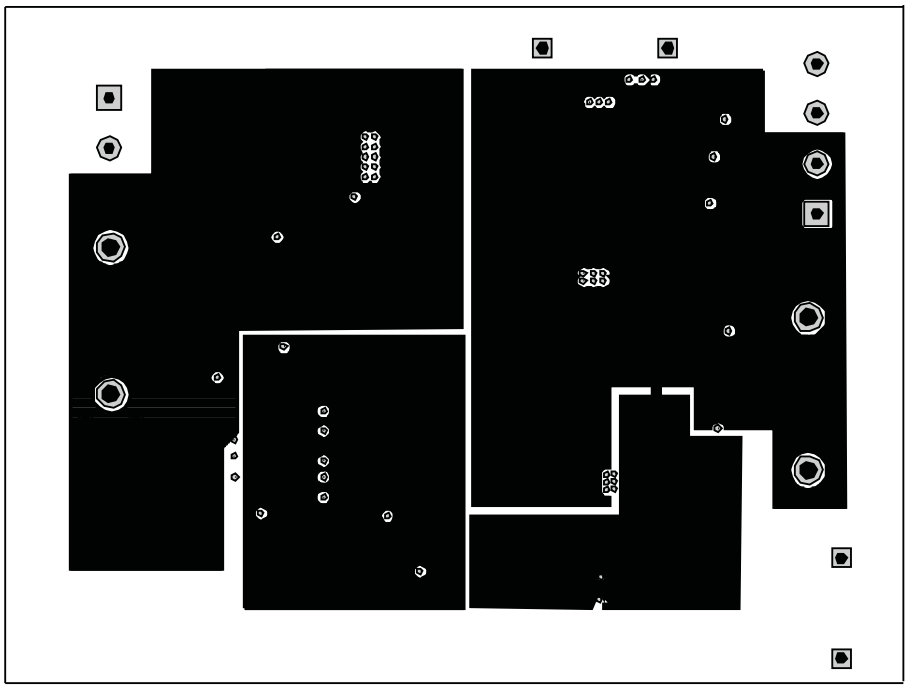

Figure 17. Internal Split Ground Plane

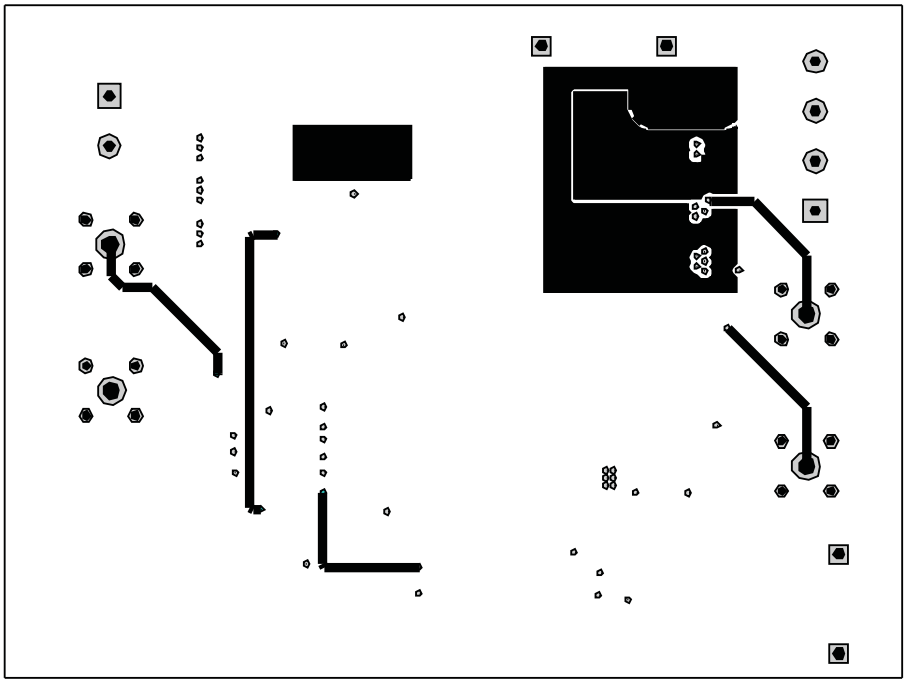

Figure 18. Internal Signal Trace Layer

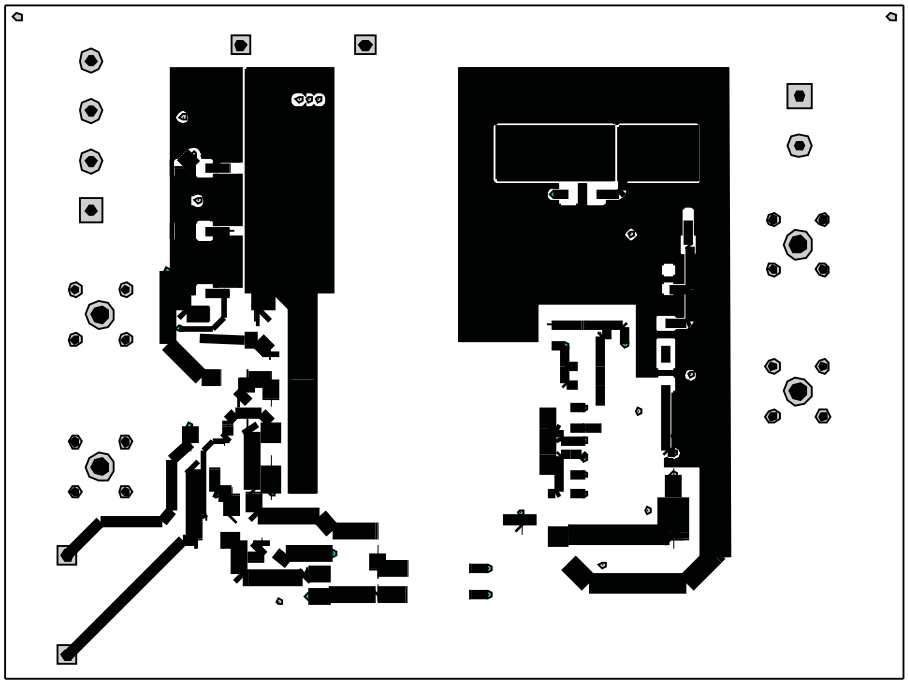

Figure 19. Bottom Signal Trace Layer

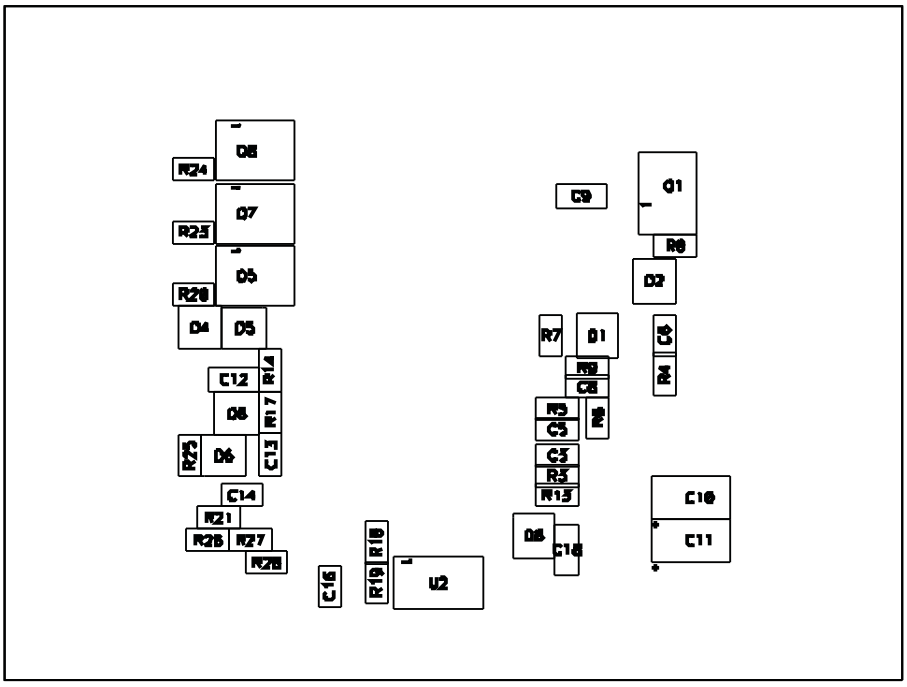

Figure 20. Bottom Side Component Assembly

9 List of Materials

The following table lists the UCC2891EVM components corresponding to the schematic shown in Figure 1.

Table 2. List of Materials

REF	QTY	DESCRIPTION	MFR	PART NUMBER
C1, C2, C4	3	Capacitor, ceramic, 2.2 μF, 100 V, X7R, 20%, 1812	TDK	C4532X7R2A225M
C3, C14, C17	3	Capacitor, ceramic, 0.1 μF, 50 V, X7R, 20%, 805	Vishay	VJ0805Y104MXAA
C5	1	Capacitor, ceramic, 100 pF, 50 V, NPO, 10%, 805	Vishay	VJ0805A101KXAA
C6, C7	2	Capacitor, ceramic, 0.22 μF, 50 V, X7R, 20%, 805	TDK	C2012X7R1H224M
C8	1	Capacitor, ceramic, 10 nF, 50 V, X7R, 20%, 805	Vishay	VJ0805Y103MXAA
C9	1	Capacitor, ceramic, 33 nF, 250 V, X7R, 10%, 1206	MuRata	GRM31CR72E333KW03L
C10, C11	2	Capacitor, tantalum chip, 47 μF, 16 V, C	Vishay	595D476X9016C2T
C12, C18	2	Capacitor, ceramic, 10 μF, 16 V, X5R, 20%, 1206	TDK	C3216X5R1C106M
C13	1	Capacitor, ceramic, 1.5 μF, 10 V, X5R, 20%, 805	TDK	C2012X5R1A155M
C15	1	Capacitor, ceramic, 82 nF, 50 V, X7R, 10%, 805	Vishay	VJ0805Y823KXAA
C16	1	Capacitor, ceramic, 220 pF, 50 V, NPO, 10%, 805	Vishay	VJ0805A221KXAA
C19, C20	2	Capacitor, POSCAP, 330 μF, 6.3 V, 20%, 7343 (D)	Sanyo	6TPD330M
D1, D2, D3, D4, D5	5	Diode, schottky, 200 mA, 30 V, SOT23	Vishay	BAT54
D8	1	Diode, switching, 200 mA, 200 V, SOT23	Philips/NXP	BAS21
D6	1	Diode, zener, 5.1 V, 350 mW, SOT23	Vishay	BZX84C5V1
D7	1	Adjustable precision shunt regulator, 0.5%, SOT23	TI	TLV431BCDBZ
J1	1	Terminal block, 2 pin, 15 A, 5.1 mm, 0.40 × 0.35	OST	ED500/2DS
J2, J3, J4, J5	4	Adaptor, 3.5 mm probe clip (or 131-5031-00), 3.5 mm	Tektronix	131 4244 00
J6, J7, J9, J10	4	Printed circuit pin, 0.043 hole, 0.3 length, 0.043	Mill Max	3103-1-00-15-00-00-0X-0
J8	1	Terminal block, 4 pin, 15 A, 5.1mm, 0.80 × 0.35	OST	ED500/4DS
L1	1	Inductor, 2 μH, 1 pri, 1 sec, 0.920 × 0.780	Pulse	PA0373
Q1	1	MOSFET, P-channel, 150 V, 2.2 A, 240 mΩ, SO-8	IR	IRF6216
Q2	1	MOSFET, N-channel, 150 V, 6.7 A, 50 mΩ, PowerPak SO-8	Vishay	Si7846DP
Q3, Q4, Q5, Q7, Q8	5	MOSFET, N-channel, 30 V, 55 A, 2.5 mΩ, LFPAK	Renesas	HAT2165H
Q6	1	Bipolar, NPN, 40 V, 600 mA, 225 mW, SOT23	Vishay	MMBT2222A

Table 2. List of Materials (continued)

REF	QTY	DESCRIPTION	MFR	PART NUMBER
R1	1	Resistor, chip, 8.45 kΩ, 1/10 W, 1%, 805	Vishay	CRCW0805-8451-F
R2	1	Resistor, chip, 57.6 kΩ, 1/10 W, 1%, 805	Vishay	CRCW0805-5762-F
R3	1	Resistor, chip, 76.8 kΩ, 1/10 W, 1%, 805	Vishay	CRCW0805-7682-F
R4, R10, R15, R16, R20, R23, R24	7	Resistor, chip, 2.21 Ω, 1/10 W, 1%, 805	Vishay	CRCW0805-2R21-F
R5	1	Resistor, chip, 158 kΩ, 1/10 W, 1%, 805	Vishay	CRCW0805-1583-F
R6	1	Resistor, chip, 1.82 kΩ, 1/10 W, 1%, 805	Vishay	CRCW0805-1821-F
R7, R8, R12	3	Resistor, chip, 1 kΩ, 1/10 W, 1%, 805	Vishay	CRCW0805-1001-F
R9	1	Resistor, chip, 11.8 Ω, 1/10 W, 1%, 805	Vishay	CRCW0805-11R8-F
R11	1	Resistor, chip, 26.7 kΩ, 1/10 W, 1%, 805	Vishay	CRCW0805-2672-F
R13	1	Resistor, chip, 2 kΩ, 1/10 W, 1%, 805	Vishay	CRCW0805-2001-F
R14	1	Resistor, chip, 10 Ω, 1/10 W, 1%, 805	Vishay	CRCW0805-10R0-F
R17, R18	2	Resistor, chip, 499 Ω, 1/10 W, 1%, 805	Vishay	CRCW0805-4990-F
R19	1	Resistor, chip, 665 Ω, 1/10 W, 1%, 805	Vishay	CRCW0805-6650-F
R21, R22	2	Resistor, chip, 10 kΩ, 1/10 W, 1%, 805	Vishay	CRCW0805-1002-F
R25	1	Resistor, chip, 51.1 Ω, 1/10 W, 1%, 805	Vishay	CRCW0805-51R1-F
R26	1	Resistor, chip, 28.7 kΩ, 1/10 W, 1%, 805	Vishay	CRCW0805-2872-F
R27	1	Resistor, chip, 12.1 kΩ, 1/10 W, 1%, 805	Vishay	CRCW0805-1212-F
R28	1	Resistor, chip, 4.99 kΩ, 1/10 W, 1%, 805	Vishay	CRCW0805-4991-F
T1	1	Transformer, current sense, 10-A, 1:100, SMD	Pulse	P8208
T2	1	Transformer, high-frequency planar, planar	Pulse	PA0810
U1	1	IC, current mode active clamp PWM controller, SO-16	TI	UCC2891D
U2	1	IC, phototransistor, CTR 100%-300%, SOP-4	Vishay	SFH690BT

10 References

1. UCC2891 Current Mode Active Clamp PWM Controller, Datasheet, (SLUS542)
2. Designing for High Efficiency with the UCC2891 Active Clamp PWM Controller, by Steve Mappus, Application Note (SLUA299)

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