

# TPS51125 Buck Controller Evaluation Module User's Guide



## Table of Contents

<b>1 Introduction</b> .....	2
<b>2 Performance Specification Summary</b> .....	2
<b>3 Schematic</b> .....	3
<b>4 Test Setup and Results</b> .....	4
<b>5 Configuration</b> .....	6
<b>6 Physical Layouts</b> .....	7
<b>7 List of Materials</b> .....	10
<b>8 References</b> .....	11
<b>9 Revision History</b> .....	11

### Trademarks

Out-of-Audio™ and D-CAP™ are trademarks of Texas Instruments.  
All trademarks are the property of their respective owners.

## 1 Introduction

The TPS51125 is a cost-effective, dual-synchronous buck controller targeted for notebook system power supply solutions. It provides 5-V and 3.3-V LDOs and requires few external components. The 270-kHz VCLK output can be used to drive an external charge pump, generating gate drive voltage for the load switches without reducing the efficiency of the main converter. The TPS51125 supports high-efficiency, fast transient response and provides a combined power-good signal. Out-of-Audio™ mode light-load operation enables low acoustic noise at much higher efficiency than conventional forced PWM operation. Adaptive on-time D-CAP™ control provides convenient and efficient operation. The part operates with supply input voltages ranging from 5.5 V to 28 V and supports output voltages from 2 V to 5.5 V.

The TPS51125EVM evaluation module is a high-efficiency, dual synchronous buck converter providing 5 V at 8 A and 3.3 V at 8 A from 8-V to 25-V input.

## 2 Performance Specification Summary

Table 2-1 gives the EVM performance specifications and qualifications.

**Table 2-1. Performance Specification Summary**

SPECIFICATION		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V <sub>IN</sub>	Input voltage range	Voltage applied to VBAT	8		25	V
<b>CHANNEL 1</b>						
V <sub>OUT</sub>	Output voltage			5		V
f	Operating frequency	V <sub>TONSEL</sub> = V <sub>VREF</sub> , V <sub>VIN</sub> = 12 V, I <sub>OUT</sub> = 6 A		245		kHz
I <sub>OUT</sub>	Output current	8 V ≤ V <sub>VIN</sub> ≤ 25 V	8			A
I <sub>OC</sub>	Overcurrent limit	V <sub>VIN</sub> = 12 V		10		
<b>CHANNEL 2</b>						
V <sub>OUT</sub>	Output voltage			3.3		V
f	Operating frequency	V <sub>TONSEL</sub> = V <sub>VREF</sub> , V <sub>VIN</sub> = 12 V, I <sub>OUT</sub> = 6 A		305		kHz
I <sub>OUT</sub>	Output current	8 V ≤ V <sub>VIN</sub> ≤ 25 V	8			A
I <sub>OC</sub>	Overcurrent limit	V <sub>VIN</sub> = 12 V		10		

### 3 Schematic

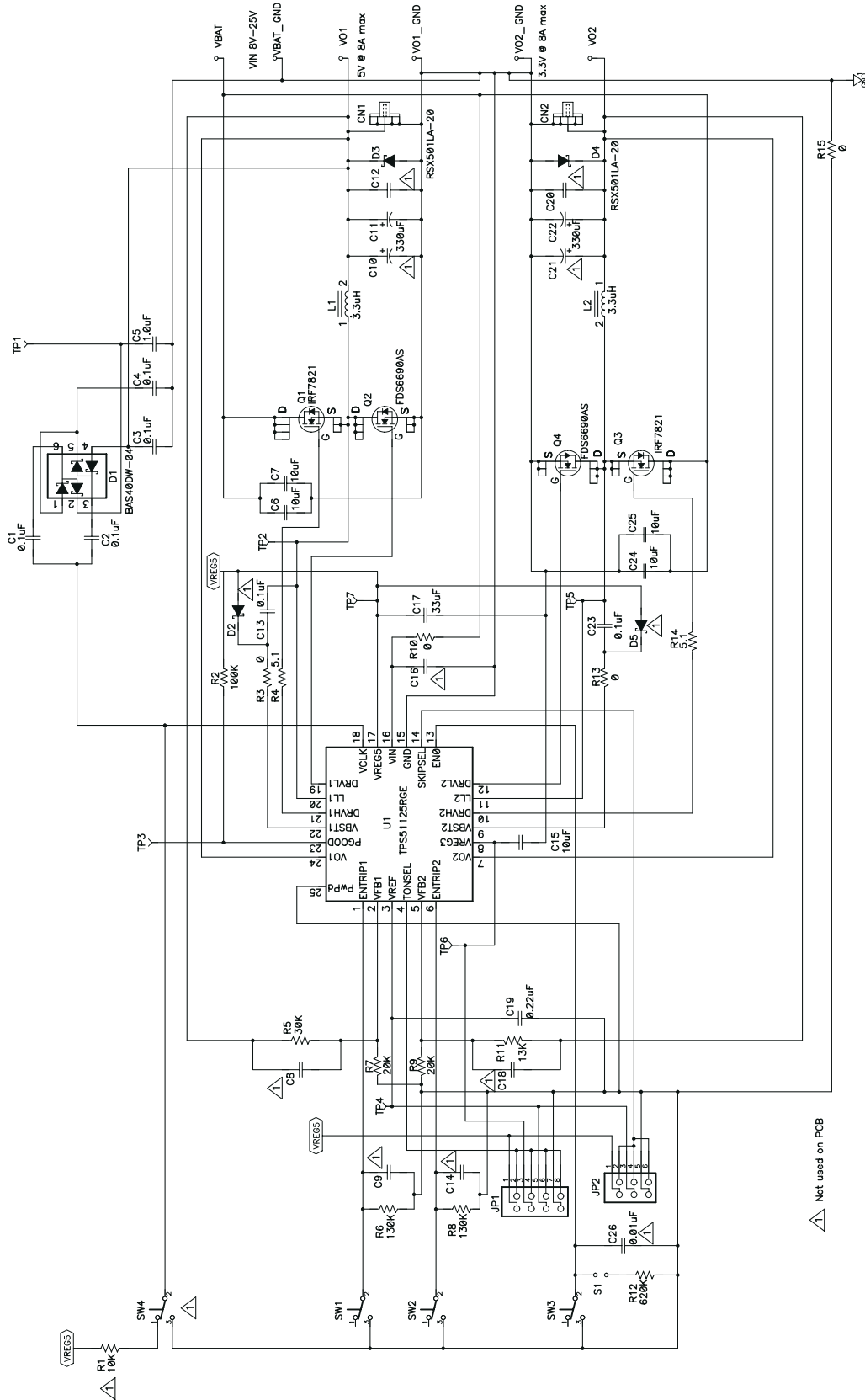


Figure 3-1. TPS51125-EVM Schematic Diagram

## 4 Test Setup and Results

### 4.1 Test Setup

Connect the test equipment and TPS51125EVM board as shown in Figure 4-1.

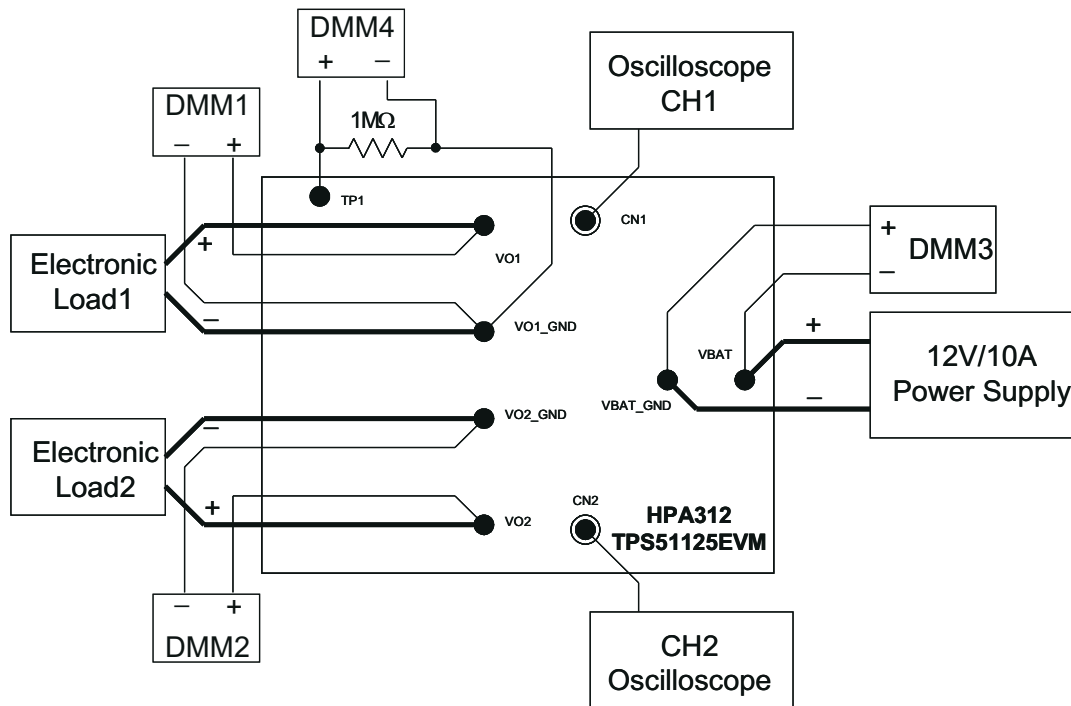


Figure 4-1. Equipment Setup for TPS51125EVM Board

### 4.2 Test Procedure

1. Ensure the switches SW1 (ENTRIP1), SW2 (ENTRIP2), and SW3 (EN0) are in the “OFF” position.
2. Ensure the shunt jumper for JP1 is set to 5-pin to 6-pin (Med1), and shunt jumper for JP2 is set to 3-pin to 4-pin (Auto-skip).
3. Apply appropriate VBAT voltage to VBAT and VBAT\_GND terminals.
4. Turn on SW3 (EN0), and both VREG5 (5V-LDO) and VREG3 (3.3V-LDO) start up.
5. When SW3 stays on, VREF (2V-REF) is enabled.
6. When SW3 stays on and turn on SW1 (ENTRIP1), CH1-output starts up.
7. When SW3 stays on and turn on SW2 (ENTRIP2), CH2-output starts up.

### 4.3 Start-Up Performance

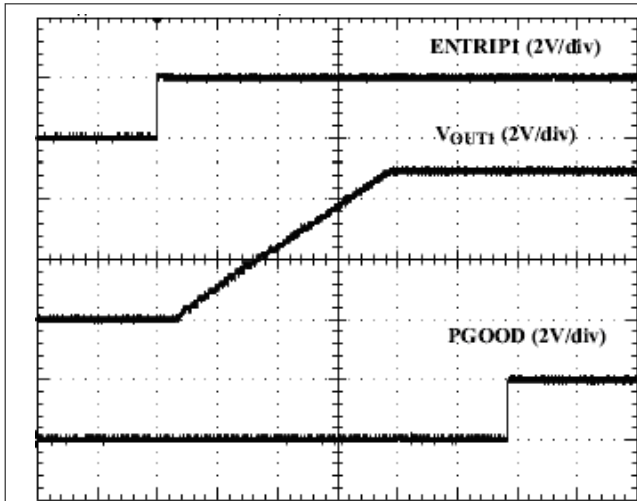


Figure 4-2. 5-V Start-Up Waveforms

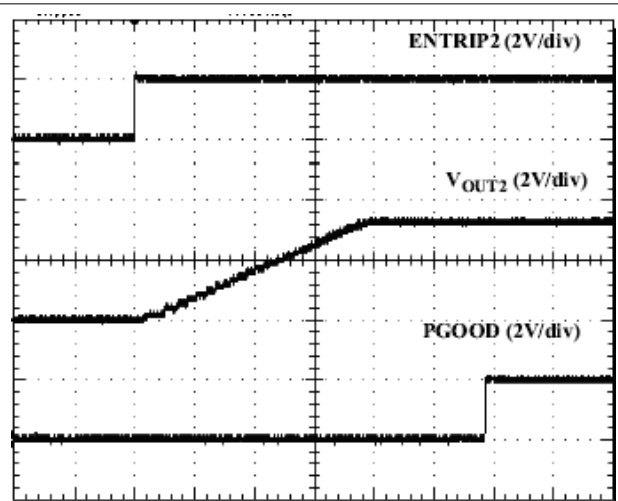


Figure 4-3. 3.3-V Start-Up Waveforms

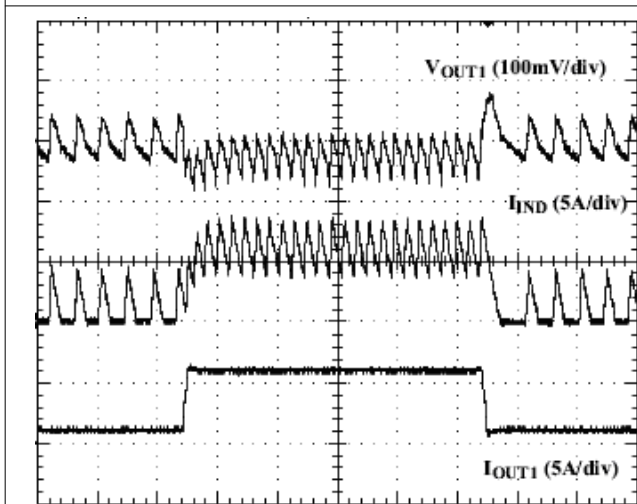


Figure 4-4. 5-V Load Transient Response

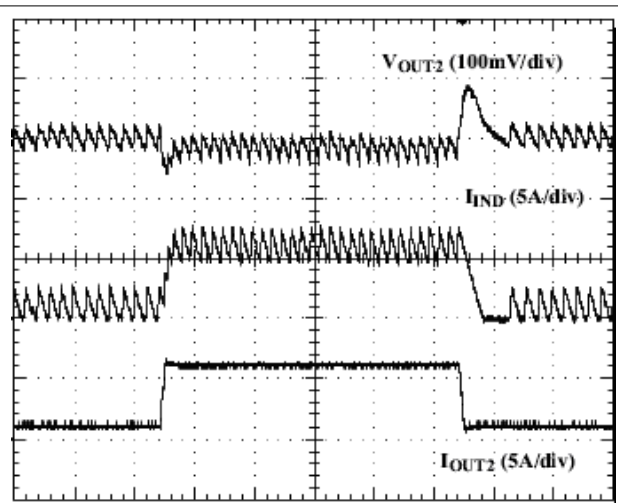


Figure 4-5. 3.3-V Load Transient Response

## 5 Configuration

This EVM can be set at a configuration of the user's choice. Please refer to the following specific configuration setting sections.

### 5.1 Switching Frequency Selection

The switching frequency can be set by the TONSEL pin using JP1 on the EVM. The default setting is 245 kHz for CH1 and 305 kHz for CH2.

**Table 5-1. Switching Frequency Selection**

TONSEL CONNECTION	SWITCHING FREQUENCY (kHz)	
	CH1	CH2
GND (SLOW)	200	250
VREF (MED1)	245	305
VREG3 (MED2)	300	375
VREG5 (FAST)	365	460

### 5.2 Operation Mode Selection

Operation mode can be set by the SKIPSEL pin using JP2 on the EVM. The default setting on the EVM is auto-skip mode.

**Table 5-2. Operation Mode Selection**

SKIPSEL CONNECTION	OPERATION MODE
GND	PWM only
VREF	Auto skip
VREG5	Out-of-Audio

### 5.3 VCLK ON/OFF Selection

The VCLK drive for the charge-pump can be disabled by pulling down EN0 with 620 k $\Omega$  of resistance using S1 on the EVM.

**Table 5-3. VLCK Control**

END CONNECTION	VCLK
OPEN	ENABLED
Pull down to GND with 620 k $\Omega$	DISABLED

## 6 Physical Layouts

This section provides the board layout and assembly drawings for the EVM, that include the top layer (Figure 6-1), the bottom layer (Figure 6-2), and inner layer views (Figure 6-3 and Figure 6-4) of the EVM.

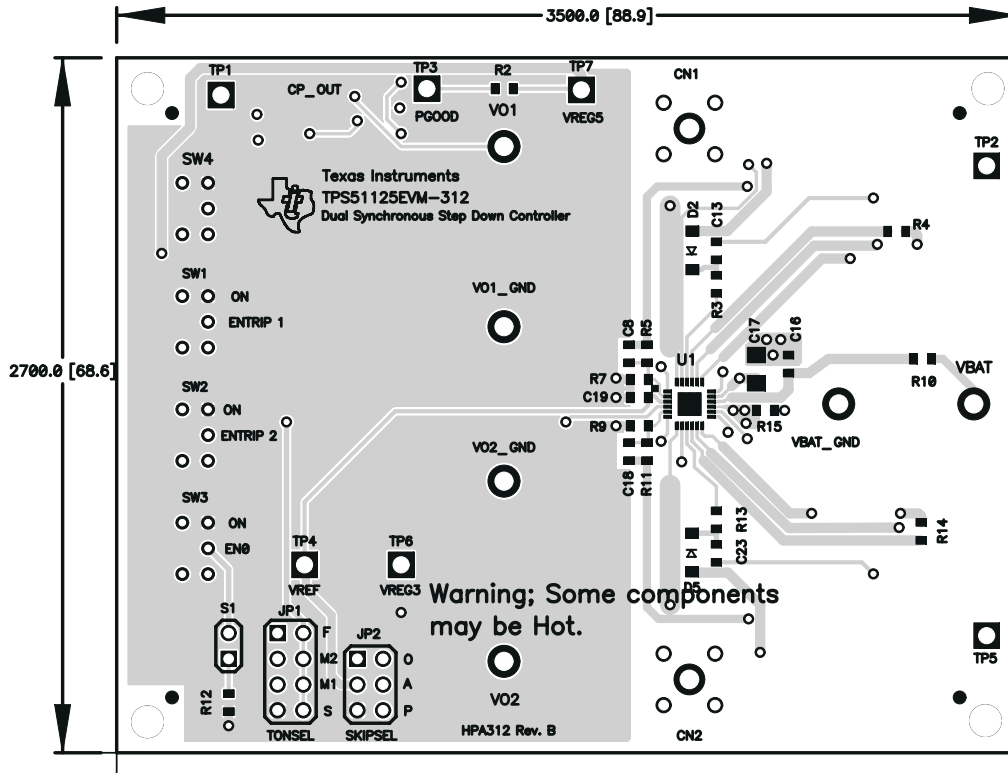


Figure 6-1. Top Layer Routing

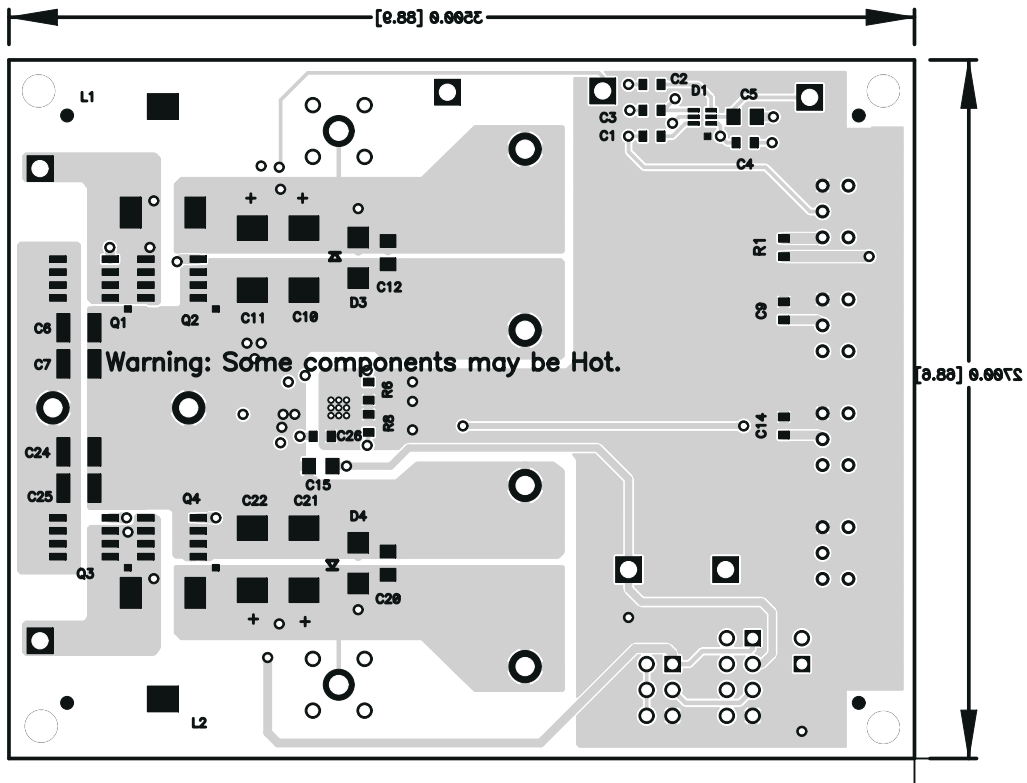


Figure 6-2. Bottom Layer Routing

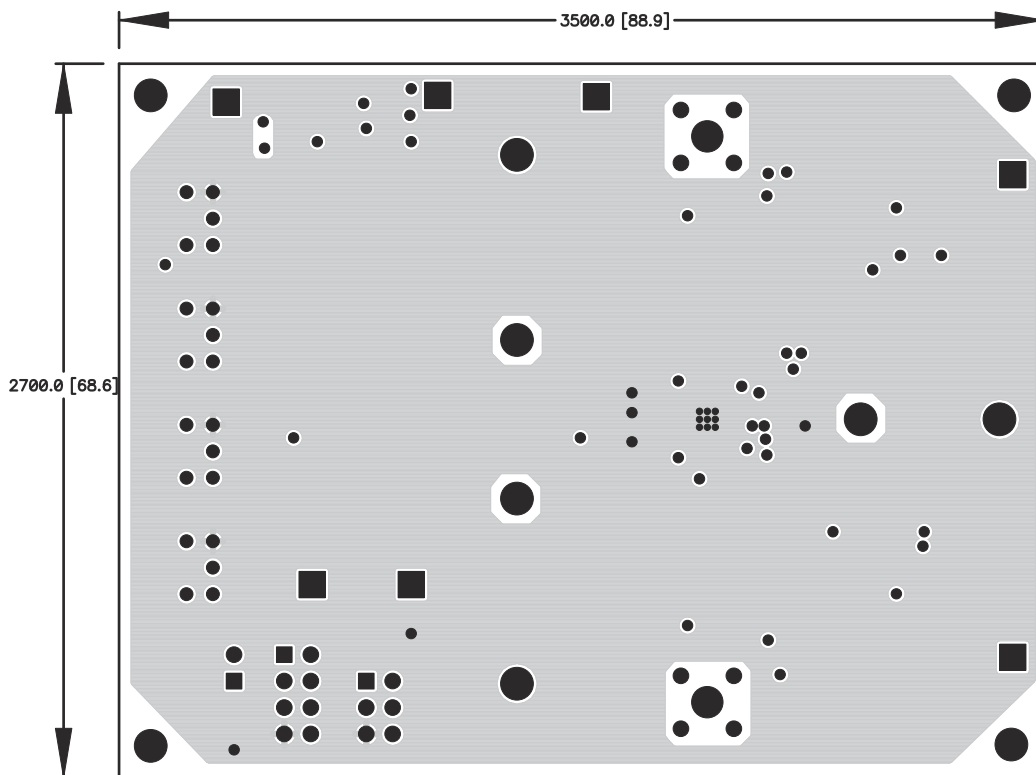
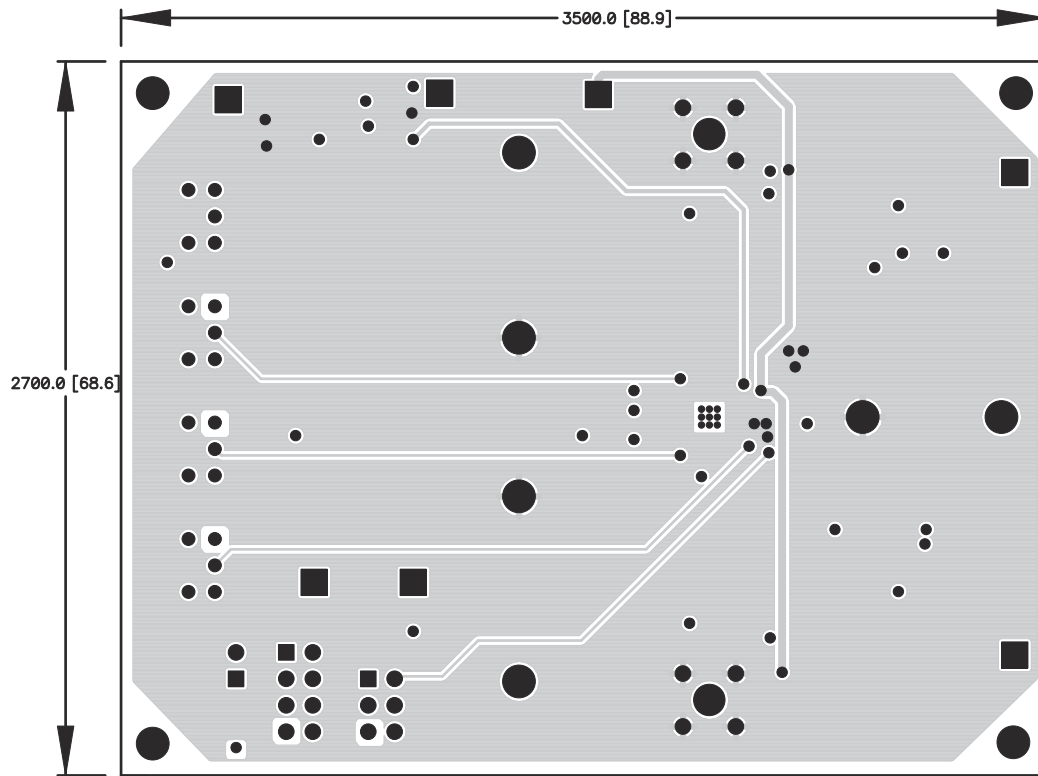


Figure 6-3. Inner Layer 1





**Figure 6-4. Inner Layer 2**

## 7 List of Materials

**Table 7-1. TPS51125 List of Materials**

RERERENCE DESIGNATOR	QTY	DESCRIPTION	SIZE	MFR	PART NUMBER
C1, C2, C3, C4, C13, C23	6	Capacitor, Ceramic, 100 nF, 50 V, X5R, 10%	0603	muRata	GRM188B31H104K
C5	1	Capacitor, Ceramic, 1 $\mu$ F, 25 V, X5R, 10%	0805	TDK	C2012X5R1E105K
C6, C7, C24, C25	4	Capacitor, Ceramic, 10 $\mu$ F, 25 V, BJ, M	1210	Taiyo Yuden	TMK325BJ106MM
C8, C9, C14, C16, C18, C26	0	Capacitor	0603	Any	Any
C10, C21	0	Capacitor	7343 (D)	Any	Any
C11, C22	2	Capacitor, POS, 330 $\mu$ F, 6.3 V, 25 m $\Omega$ , 20%	7343 (D)	SANYO	6TPE330ML
C12, C20	0	Capacitor	0805	Any	Any
C15	1	Capacitor, Ceramic, 10 $\mu$ F, 6.3 V, X5R, 10%	0805	TDK	C2012X5R0J106K
C17	1	Capacitor, Ceramic, 33 $\mu$ F, 6.3 V, X5R, 20%	1206	TDK	C3216JB0J336M
C19	1	Capacitor, Ceramic, 220 nF, 50 V, X5R, 10%	0603	muRata	GRM188B31C224K
CN1, CN2	2	Adaptor, 3.5-mm probe clip ( or 131-5031-00)	0.2	Tektronix	131-4244-00
D1	1	Diode, Schottky Barrier Array, 40 mA, 40 V	SOT363	Diodes	BAS40DW-04
D2, D5	0	Diode, Schottky, 0.5 A, 30 V	SOD123	Any	Any
D3, D4	2	Diode, Schottky, 3 A, 20 V	SMA	Rohm	RSX501LA-20 or RSX501L-20
JP1	1	Header, 2x4-pin, 100 mil spacing (36-pin strip)	0.20 x 0.40 in	Sullins	PTC36DAAN
JP2	1	Header, 2x3-pin, 100 mil spacing (36-pin strip)	0.20 x 0.30 in	Sullins	PTC36DAAN
L1, L2	2	Inductor, high-current, 7.3 m $\Omega$ , 14 A, SMT	0.425 x 0.45 in	Toko	FDA1055-3R3M
Q1, Q3	2	MOSFET, N-channel, 30 V, 11 A, 9.1 m $\Omega$	SO8	IR	IRF7821
Q2, Q4	2	MOSFET, N-channel, 30 V, 11 A, 12.5 m $\Omega$	SO8	Fairchild	FDS6690AS
R1	0	Resistor	0603	Any	Any
R2	1	Resistor, Chip, 100 k $\Omega$ , 1/16W, 1%	0603	Std	Std
R3, R10, R13, R15	4	Resistor, Chip, 0 $\Omega$ , 1/16 W, 1%	0603	Std	Std
R4, R14	2	Resistor, Chip, 5.1 $\Omega$ , 1/16W, 1%	0603	Std	Std
R5	1	Resistor, Chip, 30 k $\Omega$ , 1/16W, 1%	0603	Std	Std
R6, R8	2	Resistor, Chip, 130 k $\Omega$ , 1/16W, 1%	0603	Std	Std
R7, R9	2	Resistor, Chip, 20 k $\Omega$ , 1/16W, 1%	0603	Std	Std
R11	1	Resistor, Chip, 13 k $\Omega$ , 1/16W, 1%	0603	Std	Std
R12	1	Resistor, Chip, 620 k $\Omega$ , 1/16W, 1%	0603	Std	Std
S1	1	Header, 2-pin, 100 mil spacing, (36-pin strip)	0.2 x 0.2 in	Sullins	PTC36SAAN
SW1, SW2, SW3	3	Switch, ON-ON mini toggle	0.28 x 0.18 in	Nikkai	G-12AP
SW4	0	Switch, ON-ON mini toggle	0.28 x 0.18 in	Any	Any
TP1, TP2, TP3, TP4, TP5, TP6, TP7	7	Test point, yellow, through-hole	0.125 x 0.125 in	Keystone	5014
U1	1	Dual synchronous step-down controller with OOA operation and 100-mA LDO	QFN-24	TI	TPS51125RGE
VBAT, VBAT_GND, VO1, VO1_GND, VO2, VO2_GND	6	Pin, wiring terminal	0.12(D) x 0.4 in	Mill Max	3138-2-00-15-00-00-080
	1	Printed circuit board	3.5 x 2.7 x 0.062 in	Any	TPS51125EVM
	3	Shunt, 2POs, gold	0.100 x 0.200 inch	Molex	15-29-1025
	4	Standoff M/F hex 4-40 nylon	0.625 in	Keystone	4803

**Table 7-1. TPS51125 List of Materials (continued)**

REFERENCE DESIGNATOR	QTY	DESCRIPTION	SIZE	MFR	PART NUMBER
	4	Nut hex 4-40 nylon		Building Fasteners	NY HN 440

## 8 References

Texas Instruments, [TPS51125 Dual-Synchronous Buck Controller](#) data sheet

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2012) to Revision B (January 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document. ....	2
• Updated the user's guide title.....	2

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated