User's Guide

TPS51315 Step-Down Converter Evaluation Module User's Guide

ABSTRACT

The TPS51315-EVM evaluation module (EVM), is a D-CAP™ mode, 10-A synchronous buck controller with integrated MOSFETs providing a fixed 1.5-V output at up to 10 A from a 12-V input bus. The EVM uses the TPS51315 step down buck controller.

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Trademarks

1 Introduction

The TPS51315-EVM evaluation module (EVM), is a D-CAP™ mode, 10-A synchronous buck controller with integrated MOSFETs providing a fixed 1.5-V output at up to 10 A from a 12-V input bus. The EVM uses the TPS51315 step down buck controller.

2 Description

The TPS51315-EVM is designed to use a regulated 12-V bus to produce a regulated 1.5-V output at up to 10 A of the load current. The TPS51315-EVM is designed to demonstrate the TPS51315 in a typical low-voltage application while providing a number of test points to evaluate the performance of the TPS51315.

3 Typical Applications

- High current system converters for server and desktop power
- Point of load non-isolated DC-DC converters for telecom and datacom application

4 Features

The TPS51315-EVM features include

- 10-A DC Steady State Current
- Support pre-bias output voltage start-up
- 300-kHz switching frequency
- J4 for enable function
- Convenient test points for probing critical waveforms and loop response testing
- J5 for hiccup overcurrent protection option

5 Electrical Performance Specifications

Table 5-1 gives the EVM performance specifications.

Table 5-1. Performance Specification Summary

	SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
V_{IN}	Input voltage range		4.5	12	14	V
$I_{IN(max)}$	Maximum input current	V_{IN} = 4.5 V, I_O = 10 A			3.9	A
I_{IN}	No load input current	V_{IN} = 14 V, I_O = 0 A			30	mA
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage			1.5		V
V_{REG}	Output voltage regulation	Line regulation, 10 V ≤ V_{IN} ≤ 14 V			0.3%	
		Load regulation, V_{IN} = 12 V, 0 A ≤ I_O ≤ 10 A			0.5%	
V_{RIPPLE}	Output voltage ripple	V_{IN} = 12 V, I_O = 10 A			30	mVpp
	Ouptut load current		0		10	A
	Output overcurrent threshold			15		A
SYSTEMS CHARACTERISTICS						
f_{SW}	Switching frequency			300		kHz
η	Peak efficiency	V_{IN} = 12 V, V_{OUT} = 1.5 V, I_O = 4 A		90.29%		
η	Full load efficiency	V_{IN} = 12 V, V_{OUT} = 1.5 V, I_O = 10 A		87%		
T_A	Operating ambient temperature			25		°C

6 Schematic

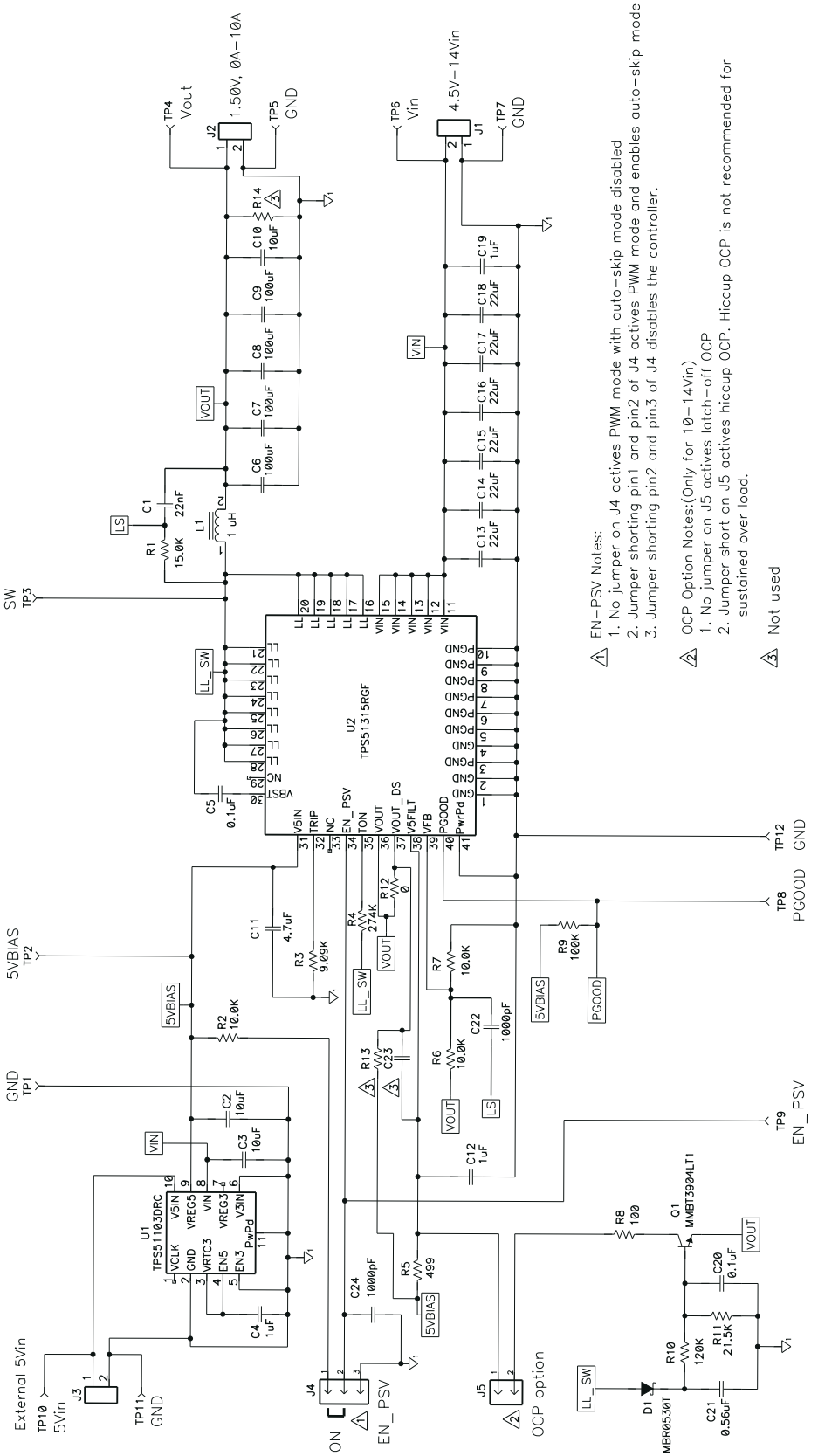

Figure 6-1. TPS51315-EVM Schematic Diagram

7 Test Setup

7.1 Test Equipment

7.1.1 Voltage Source

The input voltage source V_{IN} should be a variable DC source between 0 V and 14 V, capable of supplying 10 Adc. Connect V_{IN} to J1 as shown in Figure 7-2.

7.1.2 Multimeters

A voltmeter between 0 V and 15 V should be used to measure V_{IN} at TP6 (V_{IN}) and TP7 (GND). A voltmeter between 0 V and 5 V for output voltage measurement at TP4 (V_{OUT}) and TP5 (GND). A current meter between 0 A and 10 A (A1) as shown in Figure 7-2 is used for input current measurements.

7.1.3 Output Load

The output load should be an electronic constant resistance mode load capable of between 0 Adc and 20 Adc at 1.5 V.

7.1.4 Oscilloscope

A digital or analog oscilloscope can be used to measure the output ripple. The oscilloscope should be set for 1-MΩ impedance, 20-MHz bandwidth, AC coupling, 2-µs/division horizontal resolution, 20-mV/division vertical resolution. Test points TP4 and TP5 can be used to measure the output ripple voltage. Place the oscilloscope probe tip through TP4 and rest the ground barrel on TP5 as shown in Figure 7-1. Using a leaded ground connection may induce additional noise due to the large ground loop.

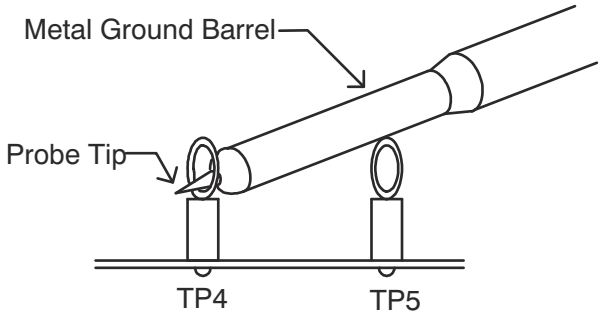

Figure 7-1. Tip and Barrel Measurement for V_{OUT} Ripple

7.1.5 Fan

Some of the components in this EVM may approach temperatures of 60°C during operating. A small fan capable of 200-400 LFM is recommended to reduce component temperatures while the EVM is operating. The EVM should not be probed while the fan is not running.

7.1.6 Recommended Wire Gauge

For V_{IN} to J1 (12-V input) the recommended wire size is 1 × AWG #14 per input connection, with the total length of wire less than 4 feet (2 feet input, 2 feet return). For J2 to LOAD the minimum recommended wire size is 1 × AWG #14, with the total length of wire less than 4 feet (2 feet output, 2 feet return).

7.2 Recommended Test Setup

Figure 7-2 is the recommended test set up to evaluate the TPS51315-EVM. Working at an ESD workstation, make sure that any wrist straps, bootstraps or mats are connected referencing the user to earth ground before power is applied to the EVM.

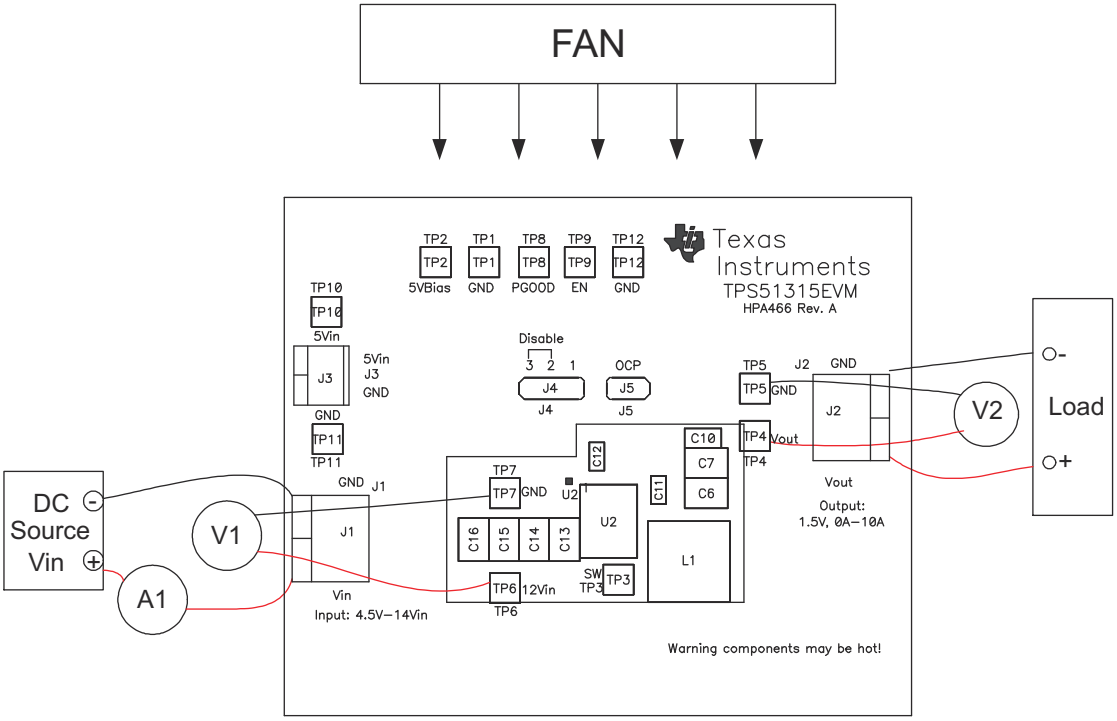

Figure 7-2. TPS51315-EVM Recommended Test Set Up

7.2.1 Configuration

1. EN-PSV J4 setting.
   a. No Jumper actives PWM mode only.
   b. Jumper on pin1 and pin2 actives auto-skip mode
   c. Jumper on pin2 and pin3 disables the controller. (Default setting)
2. OCP option J5 setting (only between 10 V_{IN} and 14 V_{IN})
   a. No Jumper actives latch-off OCP. (Default setting)
   b. Jumper on J5 actives hiccup OCP. Hiccup OCP is not recommended for sustained over load.

7.2.2 Input Connections

1. Prior to connecting the DC input source V_{IN}, it is advisable to limit the source current from V_{IN} to 10 A maximum. Make sure V_{IN} is initially set to 0 V and connected as shown in Figure 7-2.
2. Connect a voltmeter V1 at TP6(V_{IN}) and TP7 (GND) to measure the input voltage.

7.2.3 Output Connections

1. Connect Load to J2 and set the load to constant resistance mode to sink 0 Adc before V_{IN} is applied.
2. Connect a voltmeter V2 at TP4 (V_{OUT}) and TP5 (GND) to measure the output voltage.

7.2.4 Other Connections

Place a fan as shown in Figure 7-2 and turn on, making sure air is flowing across the EVM.

8 Test Procedure

8.1 Line/Load Regulation and Efficiency Measurement Procedure

1. Ensure that the load is set to constant resistance mode and to sink 0 Adc.
2. Ensure that the jumper provided in the EVM to short on pin 2 and pin 3 of J4 before V_{IN} is applied.
3. Increase V_{IN} from 0 V to 12 V, using V1 to measure input voltage.
4. Remove the jumper on J4 to enable the controller.
   a. No jumper on J4 to active PWM mode but disable auto-skip mode.
   b. Jumper short on pin 1 and pin 2 of J4 to active PWM mode and enable auto-skip mode.
5. Vary load from between 0 VAdc and 10Adc, V_{OUT} should remain in load regulation.
6. Vary V_{IN} from 10 V to 14 V. V_{OUT} should remain in line regulation.
7. Put the jumper on pin 2 and pin 3 of J4 to disable the controller.
8. Decrease the load to 0 A.
9. Decrease V_{IN} to 0 V.

8.2 List of Test Points

Table 8-1. Test Point Functions

TEST POINTS	NAME	DESCRIPTION
TP1	GND	GND for 5VBIAS
TP2	5VBIAS	5VBIAS
TP3	SW	Monitor switch node voltage
TP4	V_{OUT}	V_{OUT}
TP5	GND	GND for Vout
TP6	V_{IN}	V_{IN}
TP7	GND	GND for V_{IN}
TP8	PGOOD	Power Good
TP9	EN_PSV	Enable
TP10	5Vin	External 5VIN
TP11	GND	GND for external 5VIN
TP12	GND	GND

8.3 Equipment Shutown Procedure

1. Shut down load.
2. Shut down V_{IN}.
3. Shut down fan.

9 Performance Data and Typical Characteristic Curves

Figure 9-1 through Figure 9-10 present typical performance curves for the TPS51315-EVM

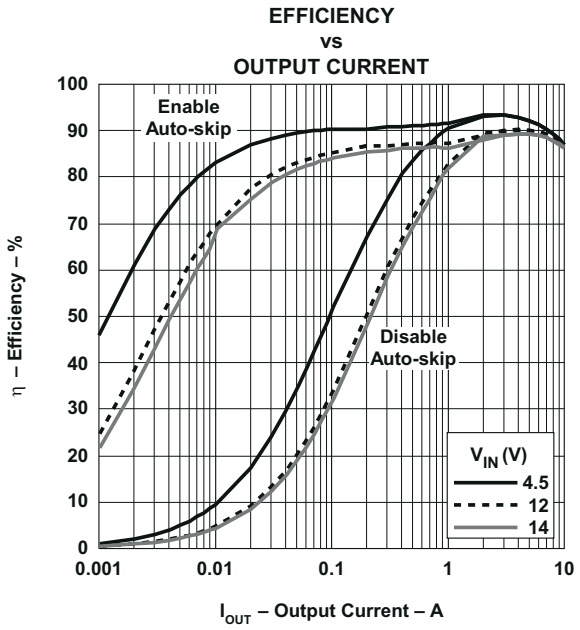

Figure 9-1. TPS51315-EVM Efficiency

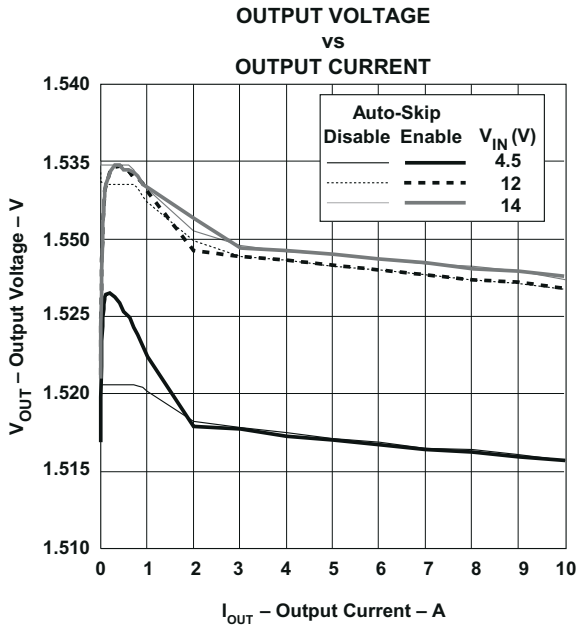

Figure 9-2. TPS51315-EVM Load Regulation

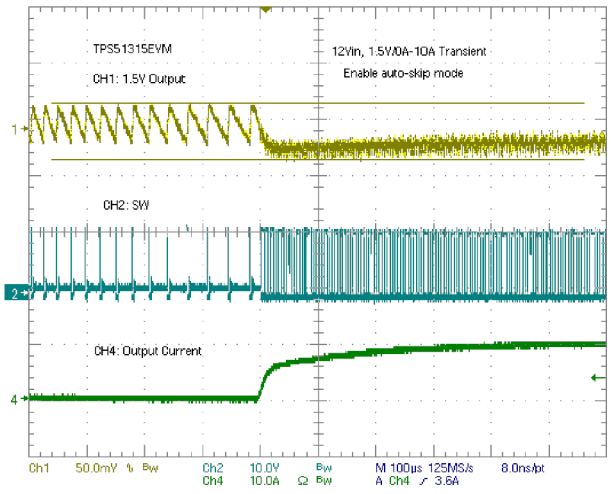

Figure 9-3. 0-A to 10-A Load Transient Rise

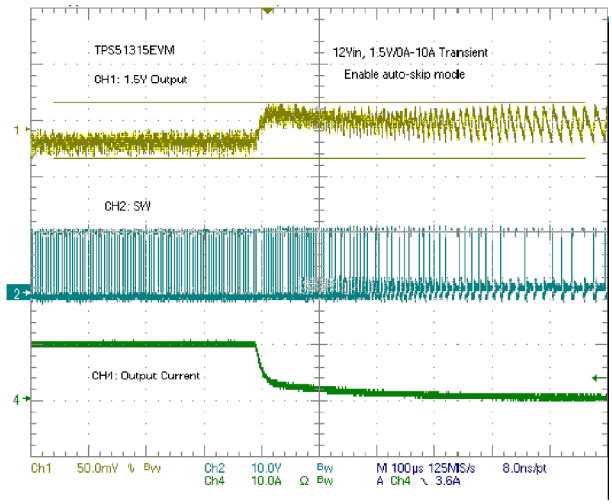

Figure 9-4. 0-A to 10-A Load Transient Fall

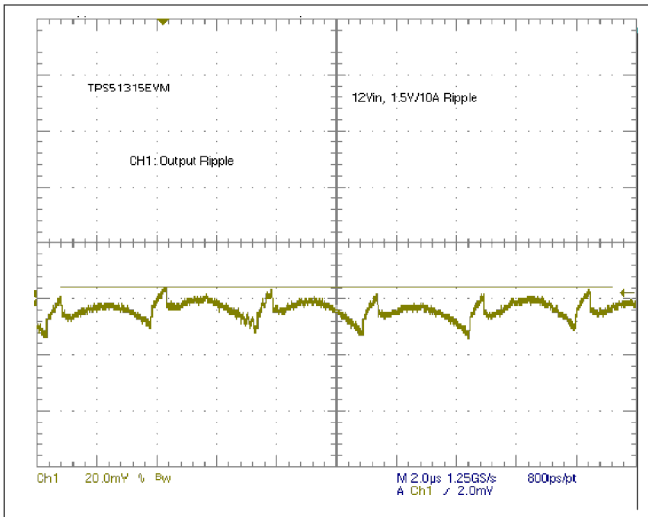

Figure 9-5. Output Ripple

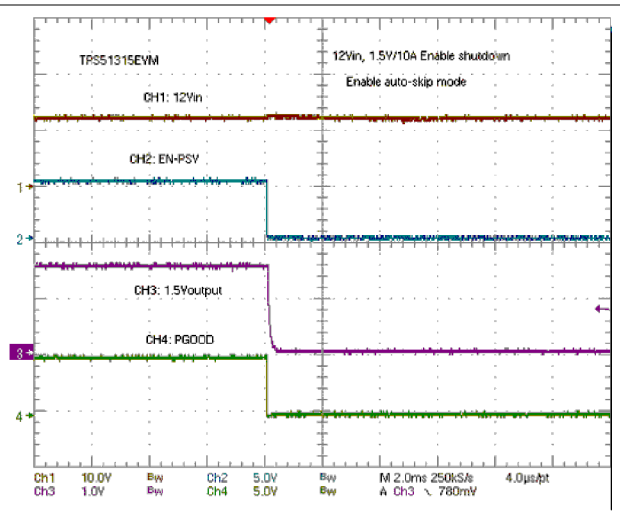

Figure 9-6. Enable Turn-Off

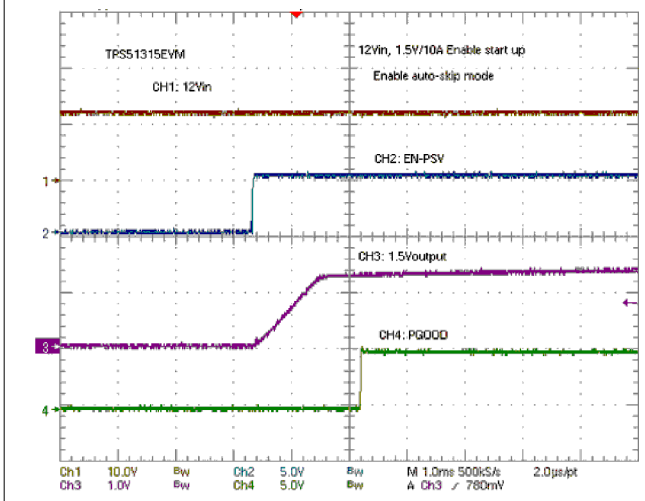

Figure 9-7. Enable Turn-On

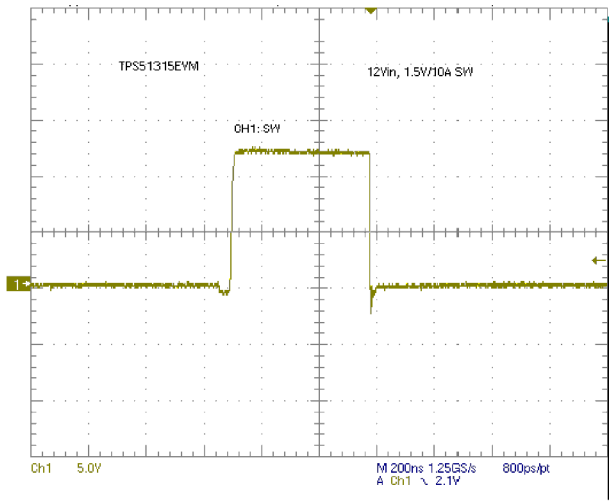

Figure 9-8. Switching Node

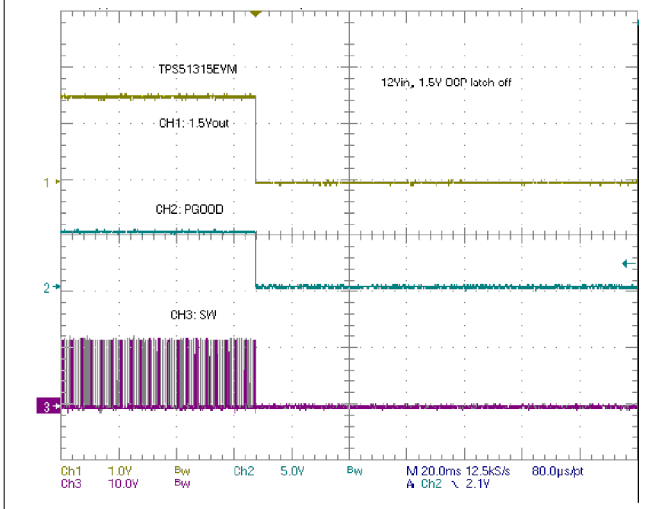

Figure 9-9. Overcurrent Protection (OCP) Latch-Off

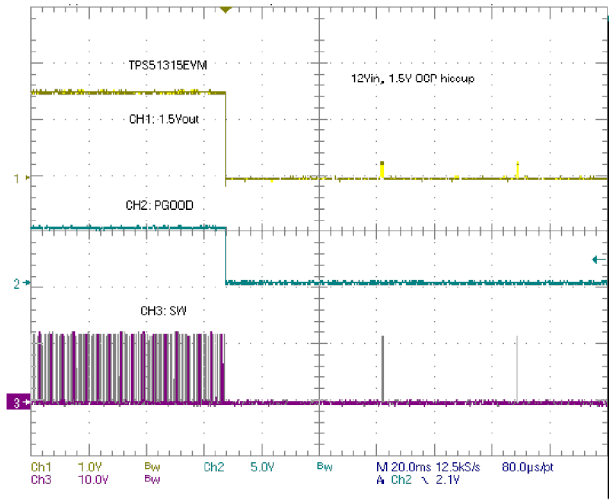

Figure 9-10. Overcurrent Protection (OCP) Hiccup

10 EVM Assembly Drawing and PCB layout

Figure 10-1 through Figure 10-8 show the design of the TPS51315-EVM printed circuit board. The EVM has been designed using 6 layers on a 2-oz. copper circuit board.

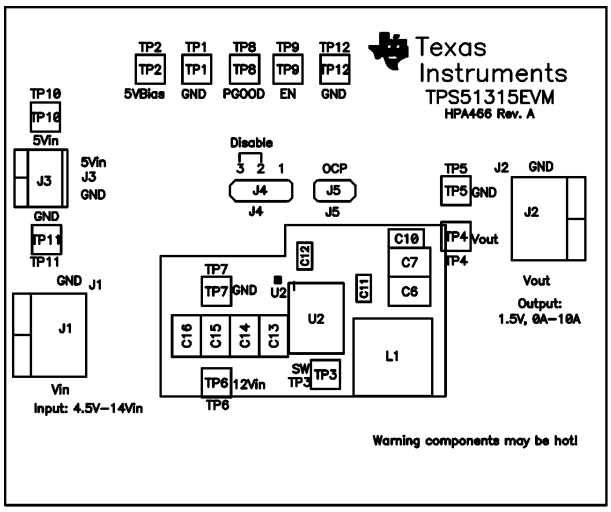

Figure 10-1. Top Layer Assembly Drawing (Top View)

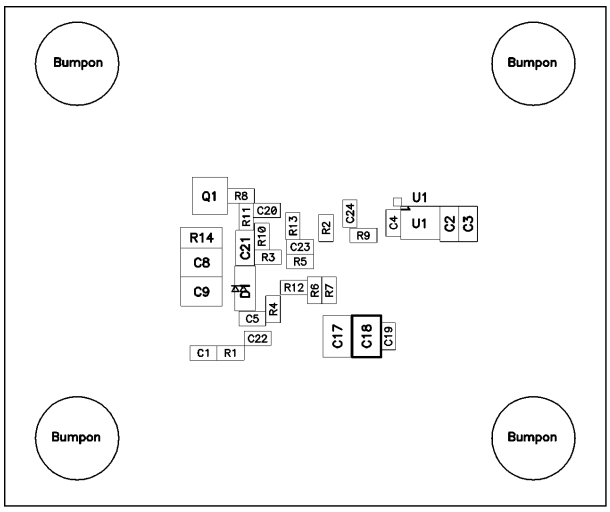

Figure 10-2. Bottom Assembly Drawing (Bottom View)

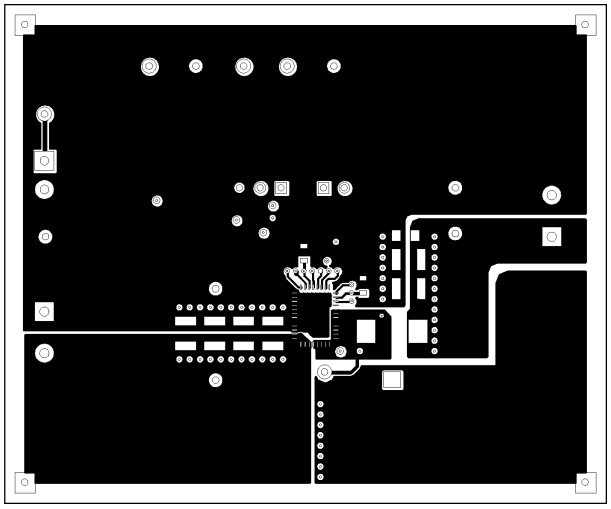

Figure 10-3. Top Copper (Top View)

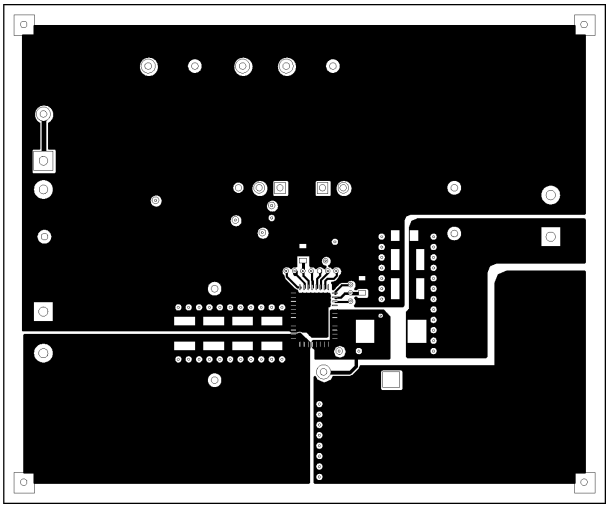

Figure 10-4. Internal Layer 1

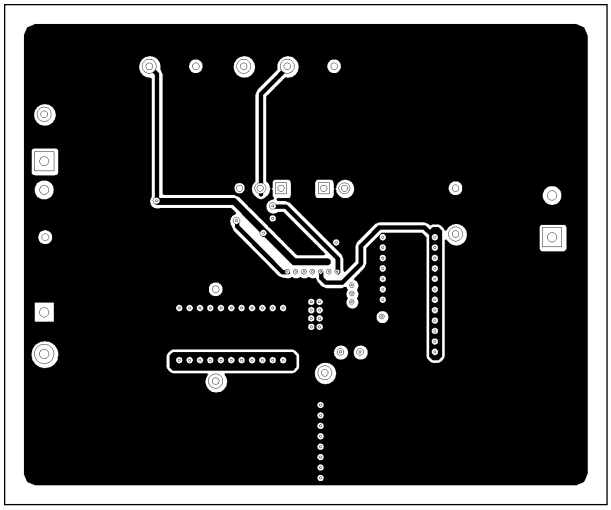

Figure 10-5. Internal Layer 2

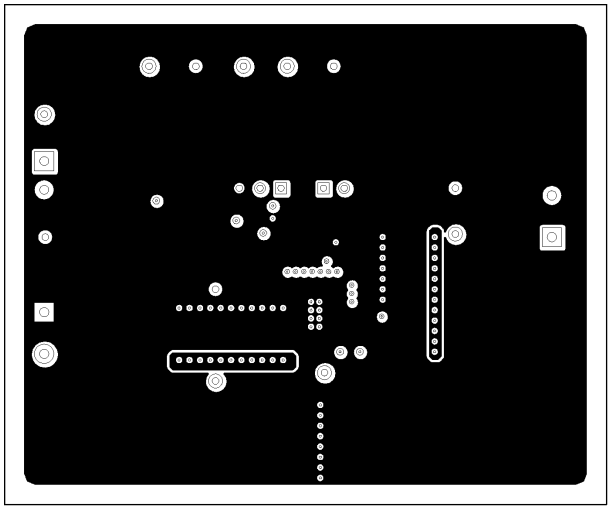

Figure 10-6. Internal Layer 3

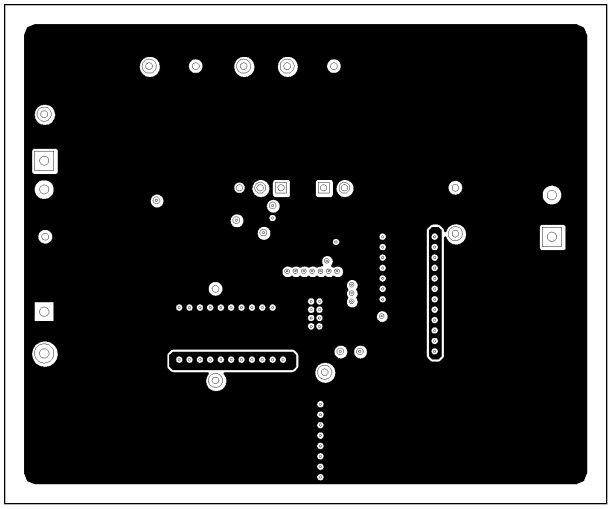

Figure 10-7. Internal Layer 4

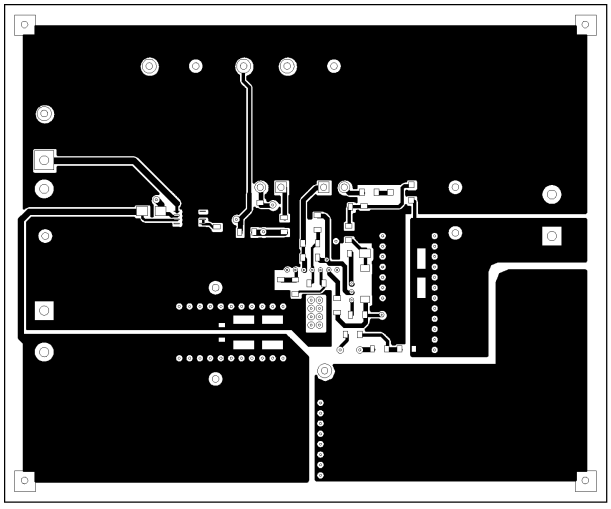

Figure 10-8. Bottom Copper (Top View)

11 List of Materials

List of materials for the TPS51315-EVM.

Table 11-1. TPS51315-EVM List of Materials

REFERENCE DESIGNATOR	QTY	DESCRIPTION	MFR	PART NUMBER
C13, C14, C15, C16, C17, C18	6	Capacitor, Ceramic, 22 µF, 16V, X5R, 20%, 1210	MuRata	GRM32ER61C226KE20L
C1	1	Capacitor, Ceramic, 22 nF, 50V, X7R, 10%, 0603	STD	STD
C10, C2, C3	3	Capacitor, Ceramic, 10 µF, 16V, X5R, 10%, 0805	STD	STD
C11	1	Capacitor, Ceramic, 4.7 µF, 10V, X5R, 10%, 0603	STD	STD
C19, C4, C12	3	Capacitor, Ceramic, 1 µF, 16V, X7R, 10%, 0603	STD	STD
C20, C5	2	Capacitor, Ceramic, 0.1 µF, 25V, X7R, 10%, 0603	STD	STD
C21	1	Capacitor, Ceramic, 0.56 µF, 25V, X7R, 10%, 0603	STD	STD
C22, C24	2	Capacitor, Ceramic, 1000 pF, 25V, X7R, 10%, 0603	STD	STD
C6, C7, C8, C9	4	Capacitor, Ceramic, 100 µF, 6.3V, X5R, 20%, 1210	MuRata	GRM32ER60J107ME20L
D1	1	Diode, Schottky, 0.5 A, 30 V	On Semiconductor	MBR0530T
L1	1	Inductor, SMT, 1.0 µH, 13 A, 0.0023 Ω	ICE Components	IN06155
Q1	1	Bipolar, N-channel, 40 V, 200 mA, 350 mW, SOT-23	On Semiconductor	MMBT3904LT1
R1	1	Resistor, Chip, 15 kΩ 1/16W, 1%, 0603	STD	STD
R10	1	Resistor, Chip, 120 kΩ, 1/16W, 1%, 0603	STD	STD
R11	1	Resistor, Chip, 21.5 kΩ, 1/16W, 1%, 0603	STD	STD
R12	1	Resistor, Chip, 0 Ω, 1/16W, 5%, 0603	STD	STD
R2, R6, R7	3	Resistor, Chip, 10 kΩ, 1/16W, 1%, 0603	STD	STD
R3	1	Resistor, Chip, 9.09 kΩ, 1/16W, 1%, 0603	STD	STD
R4	1	Resistor, Chip, 274 kΩ, 1/16W, 1%, 0603	STD	STD
R5	1	Resistor, Chip, 499 Ω, 1/16W, 1%, 0603	STD	STD
R8	1	Resistor, Chip, 100 Ω, 1/16W, 1%, 0603	STD	STD
R9	1	Resistor, Chip, 100 kΩ, 1/16W, 1%, 0603	STD	STD
U1	1	IC, Integrated LDO with switch-over circuit, DGS10	Texas Instruments	TPS51103DRC
U2	1	IC, Synchronous PWM controller with integrated switcher,QFN-40	Texas Instruments	TPS51315RGF

12 References

Texas Instruments, *TPS51315 10-A Step-Down Synchronous Switcher with Integrated MOSFETs* data sheet

13 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (February 2012) to Revision C (January 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	2
• Updated the user's guide title.	2

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