

Using the TPS23851 Reference Design

Reference Design



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TPS23851 Board Layout Guidelines

This manual provides best practices for the board layout of the TPS23851 PSE power controller.

1 Overview

The TPS23851 is a quad-power controller engineered to insert power onto Ethernet cable according to IEEE Std 802.3at-2009 for power sourcing equipment (PSE). The PSE controller can detect powered devices (PDs) that have a valid signature, determine the power requirements of the devices according to the classification, and apply power to the devices, limited per 802.3at standards. Based on an industry standard register set, the PSE controller is software compatible with other PSE controllers for basic functionality.

Beyond the industry standard operation, the TPS23851 operates with enhanced features. Port current trip point can be set to all classification thresholds of 802.3at and can be programmed up to 816 mA in excess of 802.3at. The TPS23851 supports AC and DC disconnection with a precision on-chip, 110-Hz oscillator for AC waveform generation. The PSE also contains four 14-bit A/D converters that constantly monitor voltage and current on each port. This information is available on the I²C bus for power management.

The basic general configuration of the device and a typical *port* component population is shown below in [Figure 1](#).

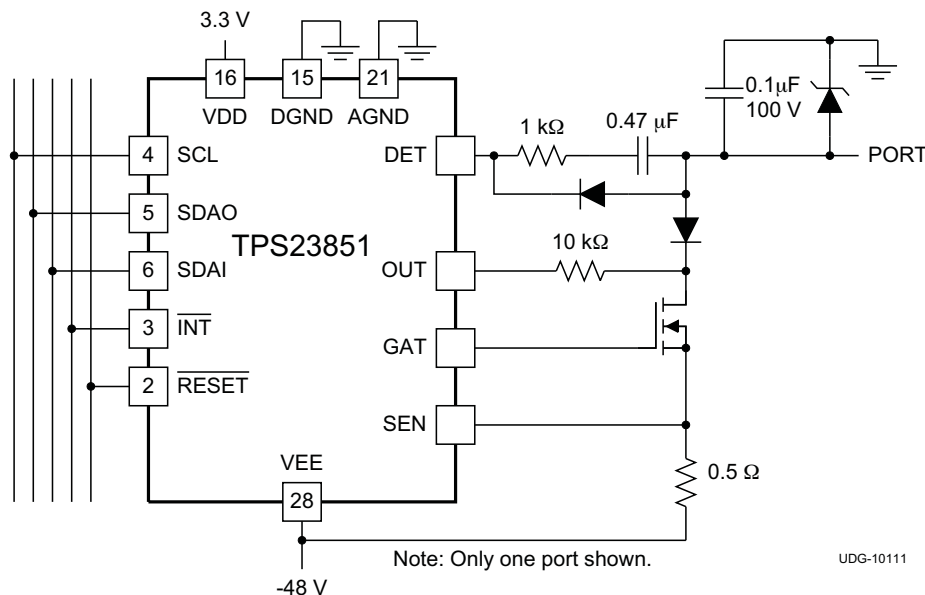


Figure 1.

1.1 Typical Application Schematic

Figure 2 below shows a typical application schematic for the TPS23851. This schematic highlights the typical component support for the chip and one of the four ports of the device.

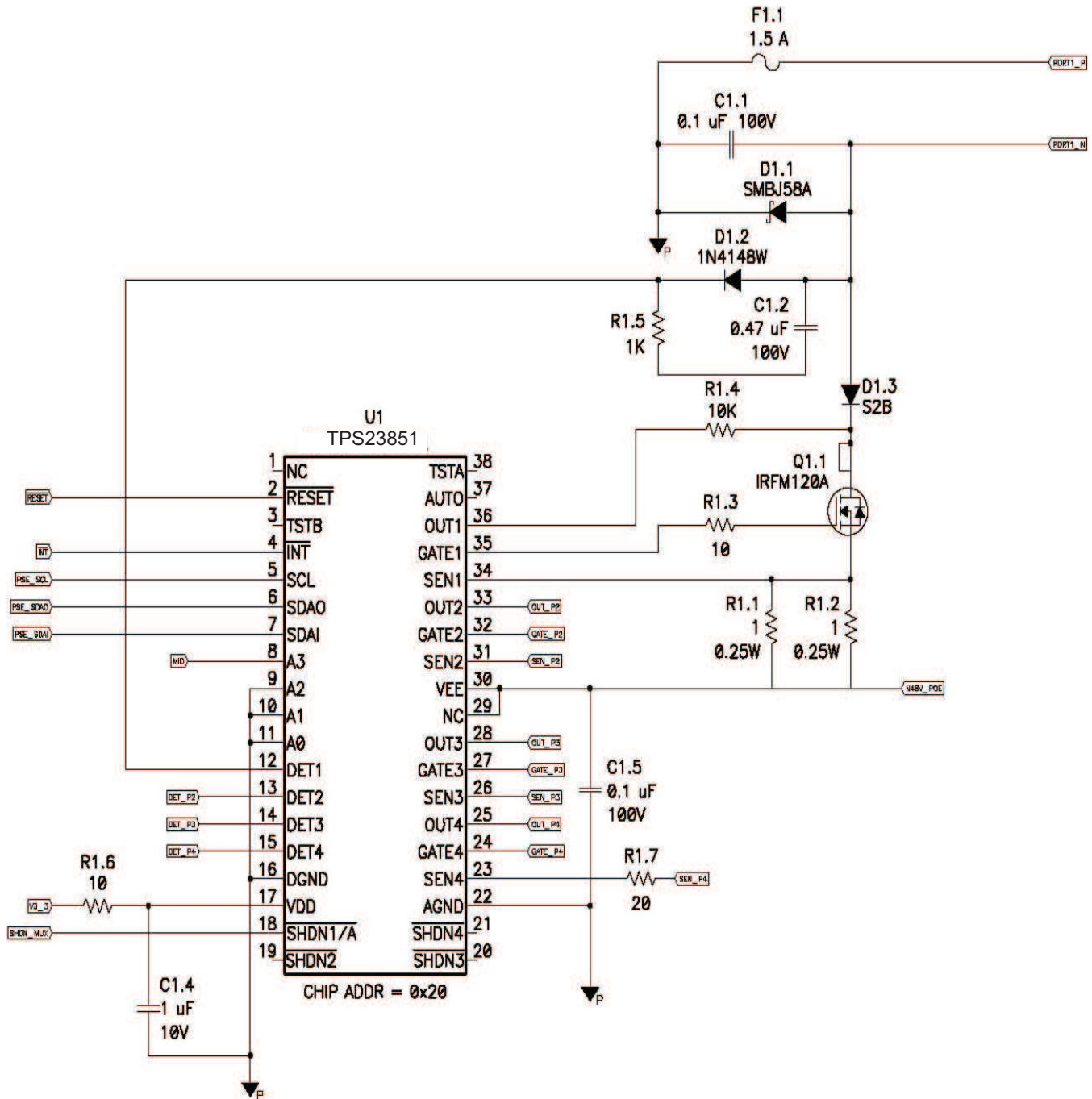


Figure 2. TPS23851 Typical Application

NOTE: The above schematic uses the TSSOP-36 package pinout. Pin numbers must be adjusted when the SSOP-36 package type is used.

2 Component Function, Selection and Placement

2.1 Supply Decoupling

Both the VDD and VEE pins of the device should be decoupled as shown. The decoupling caps (C1.4 and C1.5) should be as close to the corresponding VDD and VEE pins (TSSOP-38 VDD=17, VEE=29,30; SSOP-36 VDD=16, VEE=28) as possible. Power supply slew rate at power on and off should be kept below 1V/ μ S. Usually this is not an issue due to the magnitude of capacitance on these lines, however, in some cases where a small dedicated switching regulator is used for VDD that may not be the case. R1.6 is recommended to create an RC filter on the VDD pin to prevent an issue due to dv/dt and to remove the high level of hash/noise typically found on this rail.

2.2 Current Sensing

The parallel combination of R1.1 and R1.2 form the main 0.5- Ω current sense resistor of this device.

CAUTION

The layout of this component is very critical and the quality of that layout will determine the overall performance of the PSE controller. A poor layout will result in channel-to-channel crosstalk, erratic DC disconnect performance, errors in classification level reporting and errors in port current measurement.

A proper, high-performance layout relies on grouping the current sense resistors of all 4 ports in a cluster, close to the TPS23851 such that the -48-V return of these resistors forms a star connection. At the central point of that star, is the one and only connection point for the VEE pin of the TPS23851. The VEE power feed also branches off from that same star point to the supply. The four SENx pins should terminate right at the top side of each 0.5- Ω resistor with a separate path from that same end to the source of the corresponding power FET.

The figure below shows the *Kelvin* connection for the SENx trace to the sense resistors.

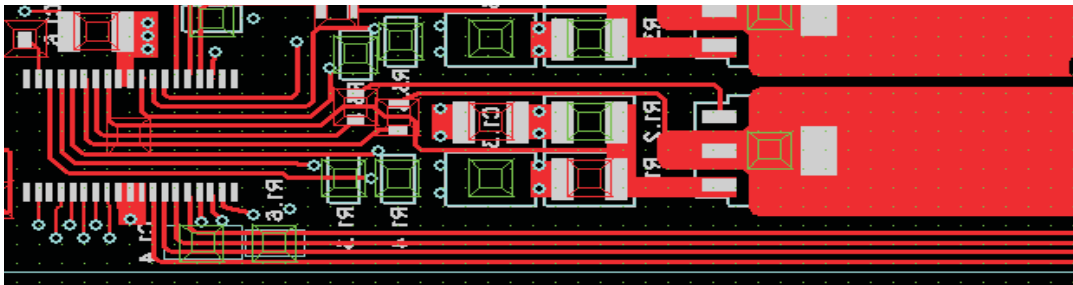


Figure 3. The *Kelvin* Connection

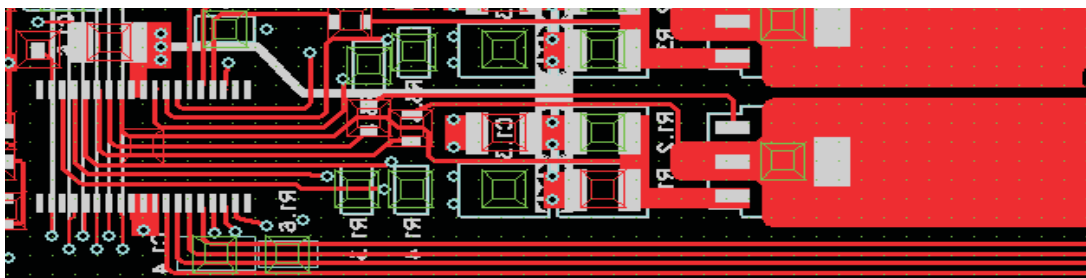


Figure 4. The *Kelvin* Connection

Two parallel resistors are used to get better tolerance due to statistical averaging and better heat spreading on the board. 1% or better tolerance resistors should always be used here.

The figure below shows how each cluster of eight sense resistors made of four parallel pairs are connected to a STAR VEE source on a multi-TPS23851 PSE board. (blue layer)

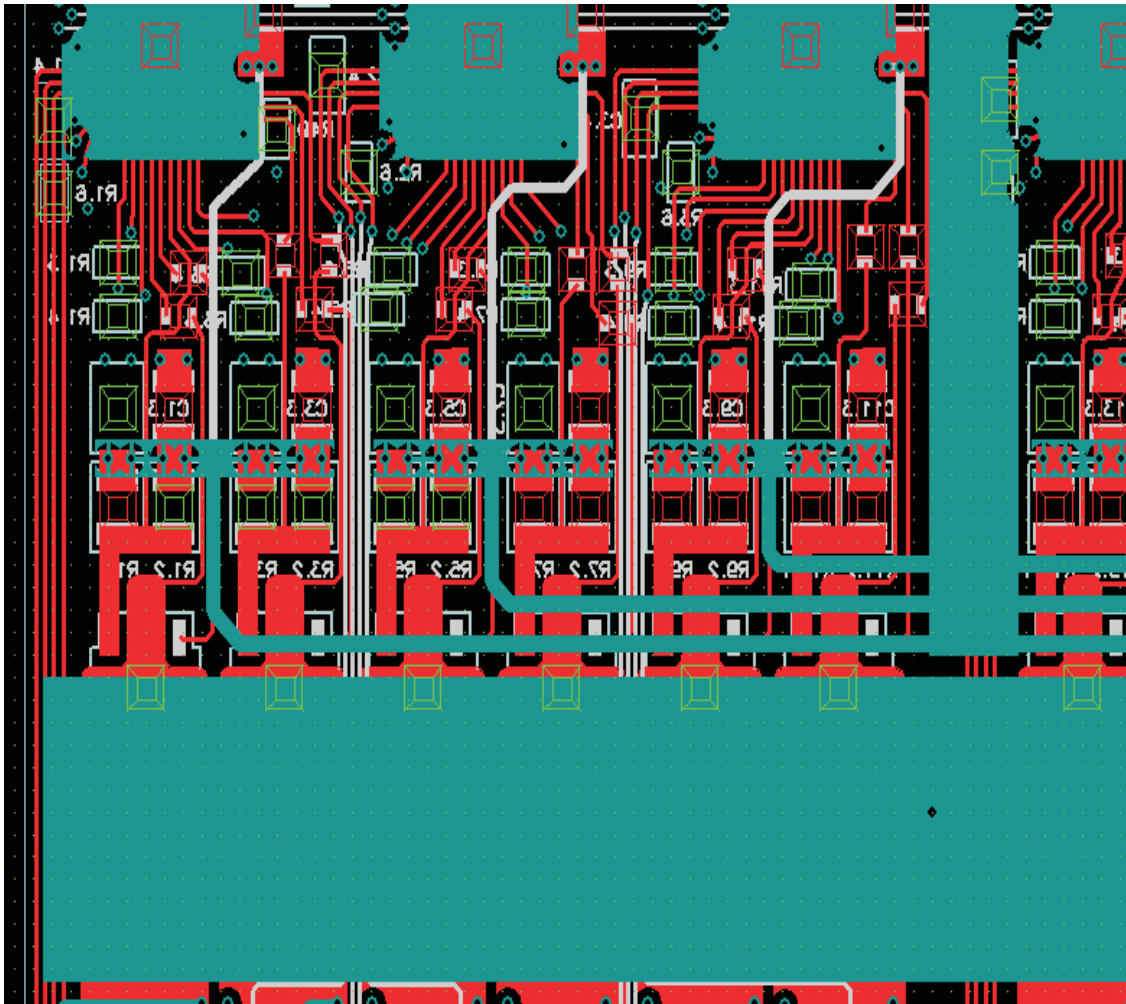


Figure 5. Four Parallel Pairs Made With Eight Sense Resistors

2.3 Port Components

C1.1 and D1.1 are port related components to protect against external voltage surges, reduce EMI and absorb ESD strikes to the port. It is preferable to locate these components closer to the corresponding port and port magnetics.

2.4 AC Disconnect Components

D1.2, R1.5, C1.2 and D1.3 are used for the AC disconnect function. When AC disconnect is enabled a 110-Hz sinewave is present on the DET pins and coupled to the port thru these components. The AC current flowing out of the DET pin is monitored by the TPS23851 and when it drops below a threshold due to a high-impedance load condition, the port is shutdown. Component value selection should not deviate from that shown as it will alter the AC disconnect threshold. C1.2 is a high-voltage ceramic cap (100 V or better) to minimize capacitance change due to voltage coefficient. D1.2, R1.5, and C1.2 should be clustered together whereas D1.3 should be located in the high current path and close to the drain of Q1.1

2.5 Power MOSFET

Careful thermal design should be considered for power MOSFET Q1.1. The power drain tab of this SOT223 should be soldered directly to a copper heat spreader under the device. The area of that heat spreader should be maximized. The spreader should be augmented with additional connections to thermal heat spreaders in the core of the circuit board or on the backside. The combined area of the heat spreaders should be at least 0.5 inches, but this is very dependent on the thermal characteristics of the specific application. Traces in the high current paths of the drain and source nodes should be at least 15-mils wide, leading to the magnetics and port RJ45 connectors.

Resistor R1.7 should be located as close as possible to the GATE node of this MOSFET whereas R1.4 should be located close to the corresponding OUT pin of the TPS23851.

The figure below shows the copper heat sink tabs for MOSFETs on the top and bottom side of a PSE board with heat spreaders on the internal layers. You will also note heat spreaders under the TPS23851 as well. The layer stack up goes from left to right as Top Layer, Internal1 Layer, Internal2 Layer, Internal3 Layer and Bottom Layer.

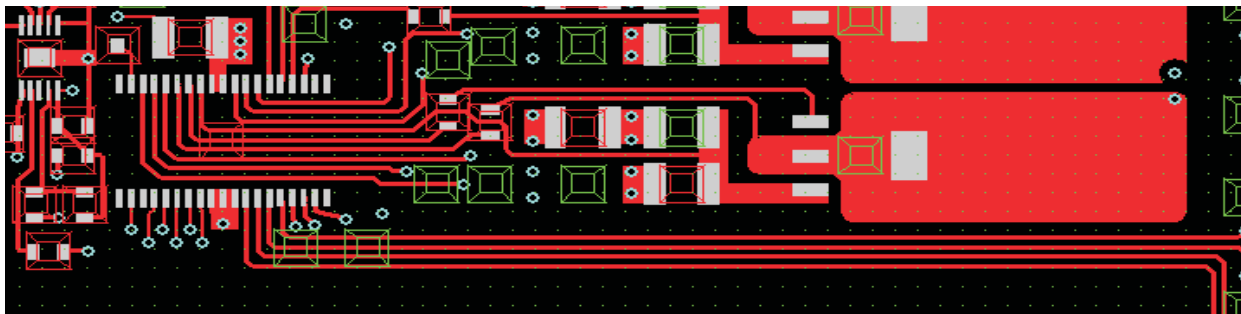


Figure 6. Top Layer

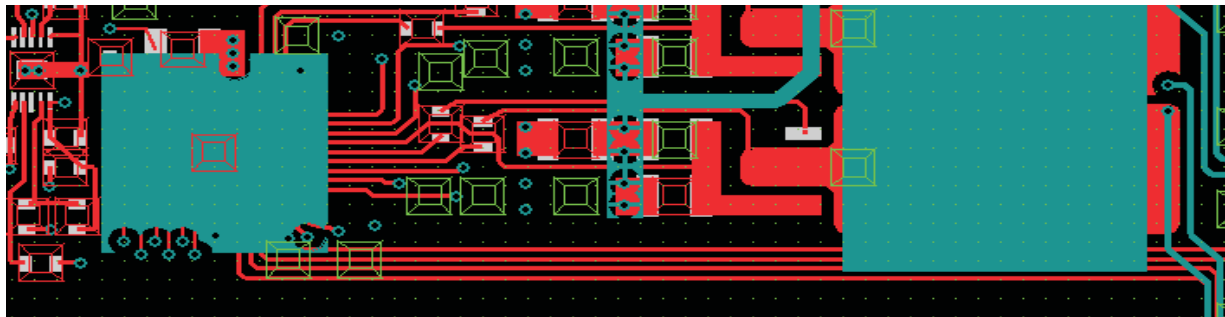


Figure 7. Internal 1 Layer

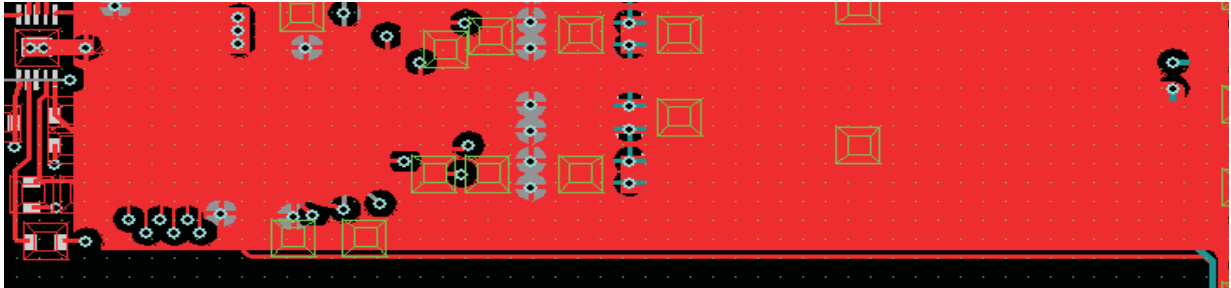


Figure 8. Internal 2 Layer

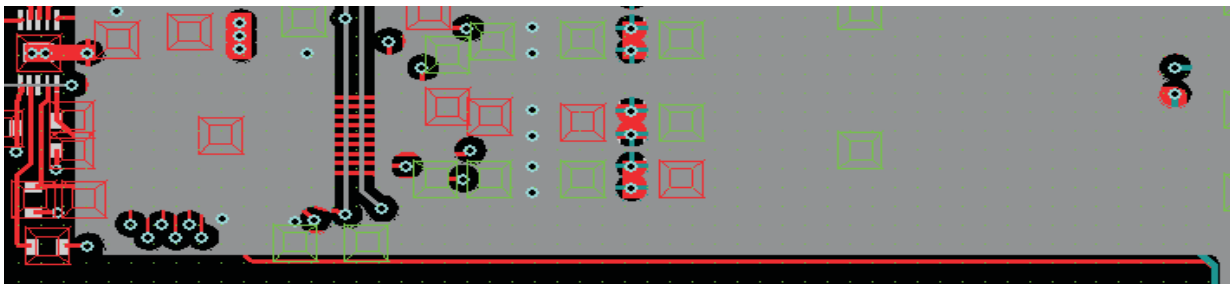


Figure 9. Internal 3 Layer

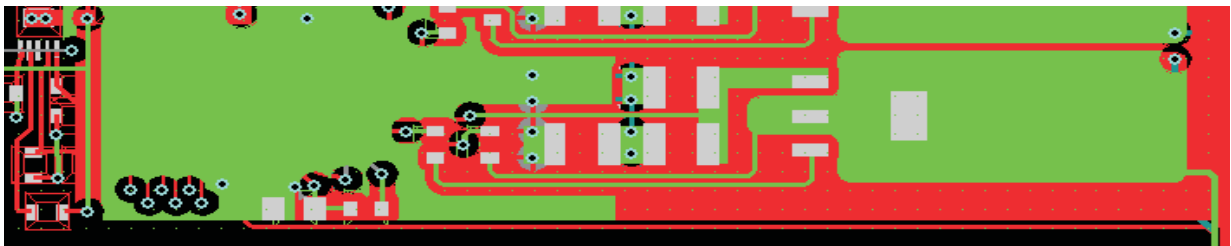


Figure 10. Bottom Layer

2.6 *TPS23851*

The TPS23851 power controller is not a power device, but will still dissipate approximately 350 mW due to quiescent current. For both this reason and supply decoupling integrity, the TPS23851 should have surface copper plane under and around the device, tied to VEE.

2.7 *Miscellaneous*

R1.7 is recommended to satisfy creepage and clearance recommendations at the SENSE4 pin (TSSOP-38 pin 23, SSOP-36 pin 22) only.

3 Example Board Layout

A typical board layout is shown below. This example is for a 24-port solution using six TPS23851 devices. Power FETs are distributed on the front and backside of the board. Top and Bottom and three inner signal copper layers are used. Port protection components are located along the bottom close to the connections to the external ports/magnetics. The input power and signal connections are along the top just above the TPS23851's. The power MOSFETs and sense resistors are closer to the middle.

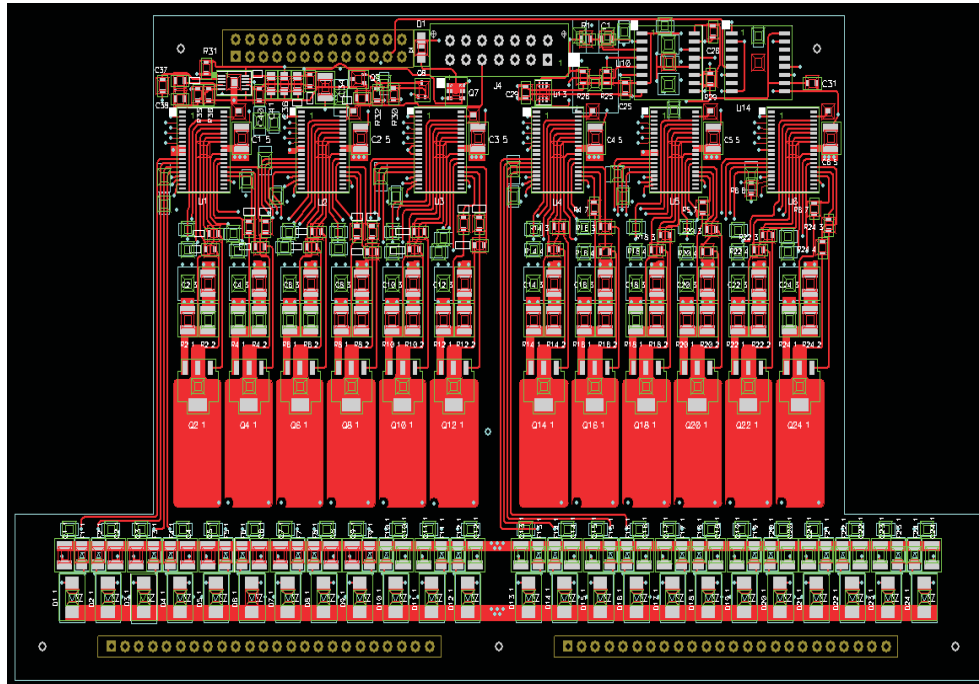


Figure 11. Top Layer

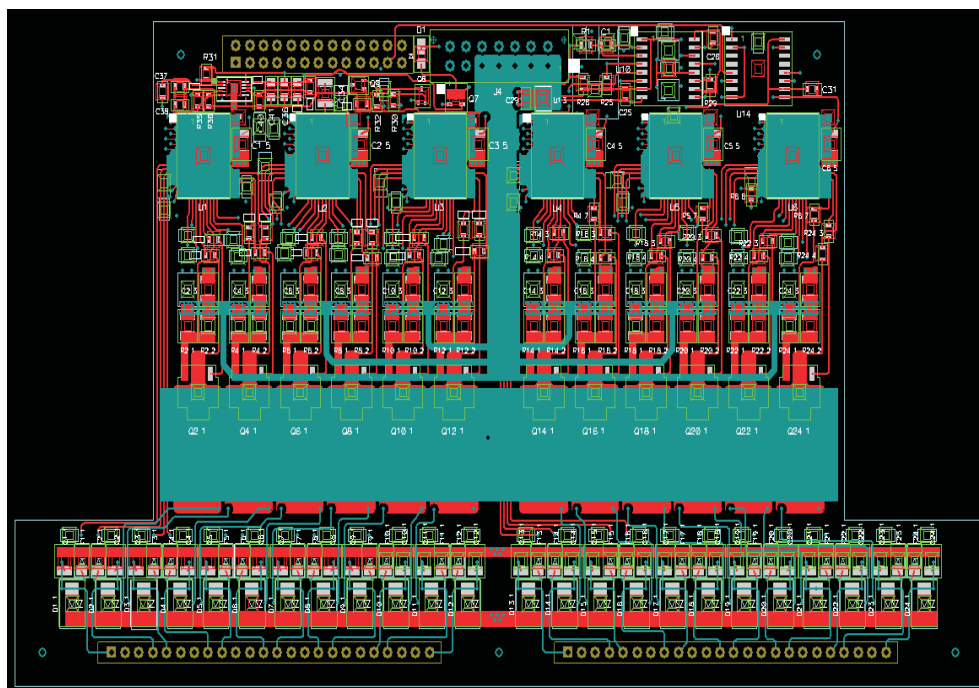


Figure 12. Top and Internal 1 Layers

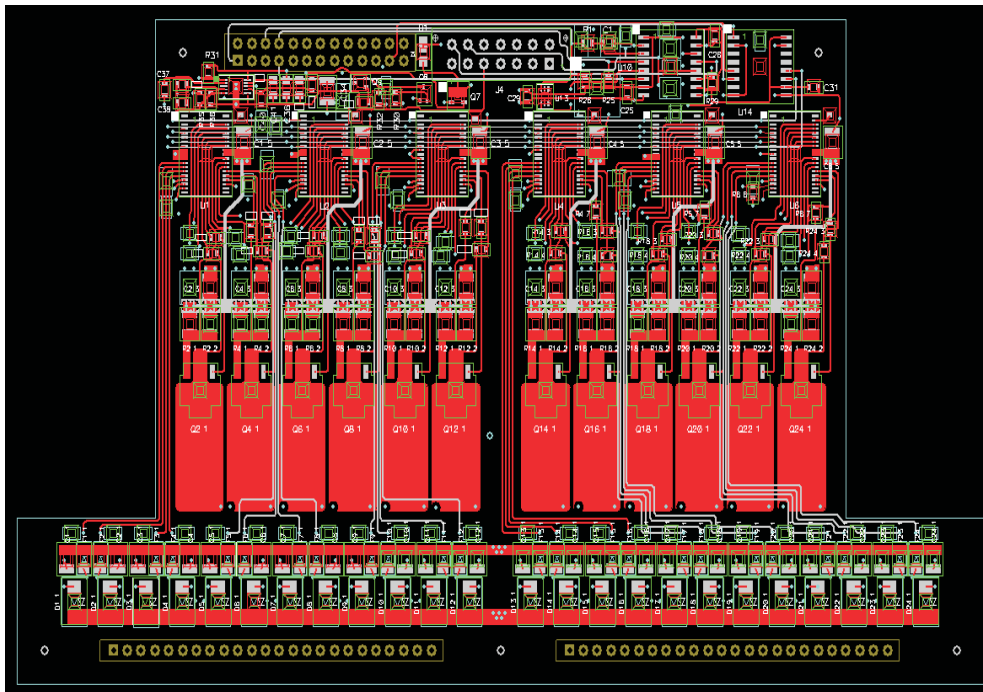


Figure 13. Top and Internal 2 Layers

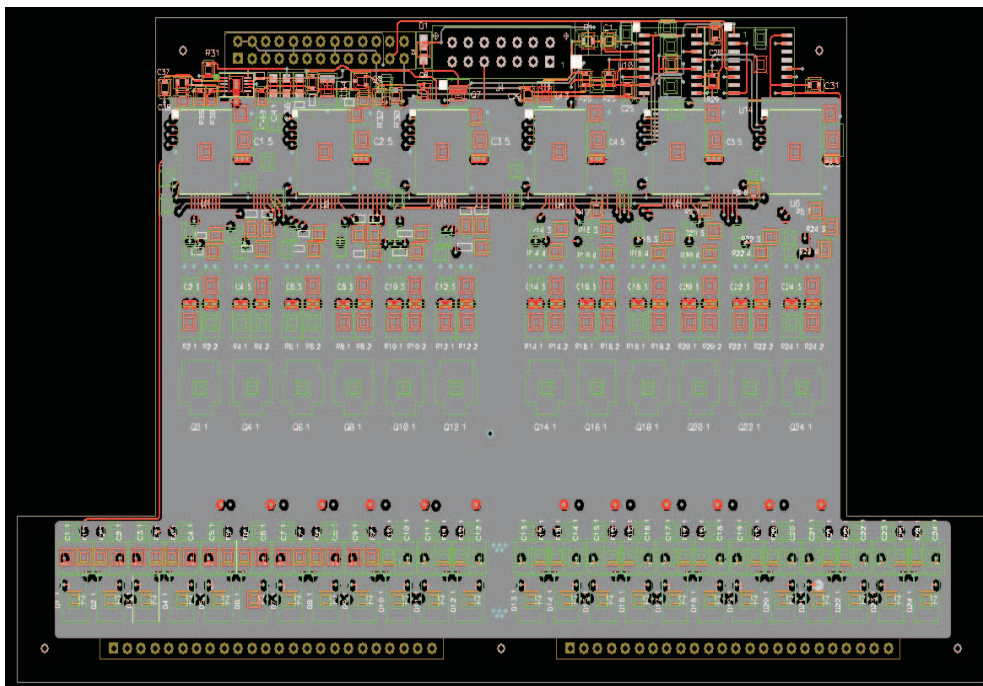


Figure 14. Top and Internal 3 Layers

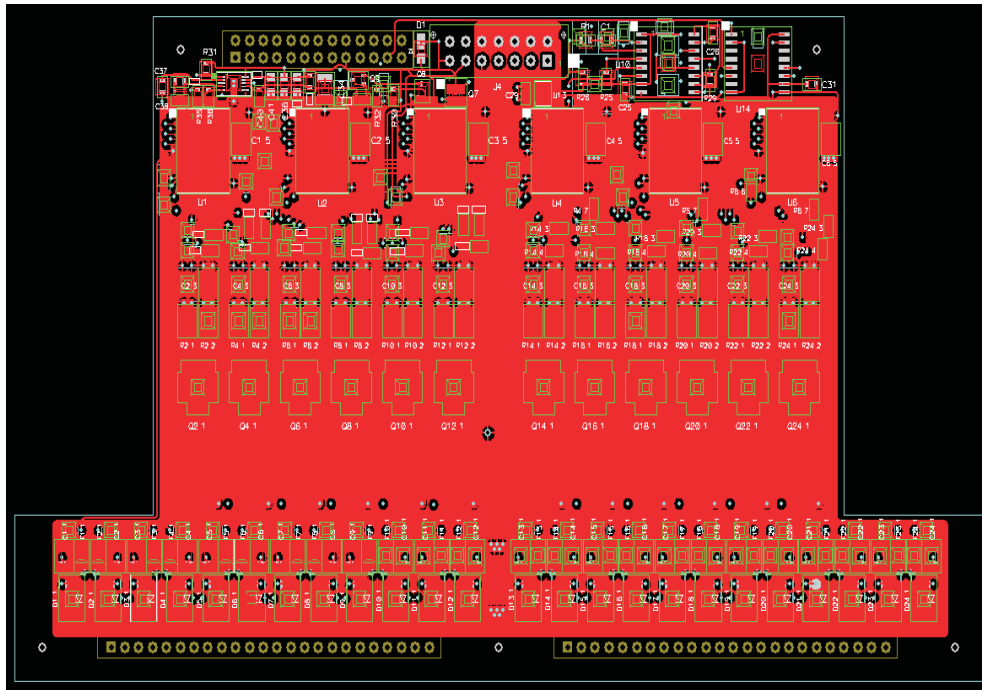


Figure 15. Top and Internal 4 Layers

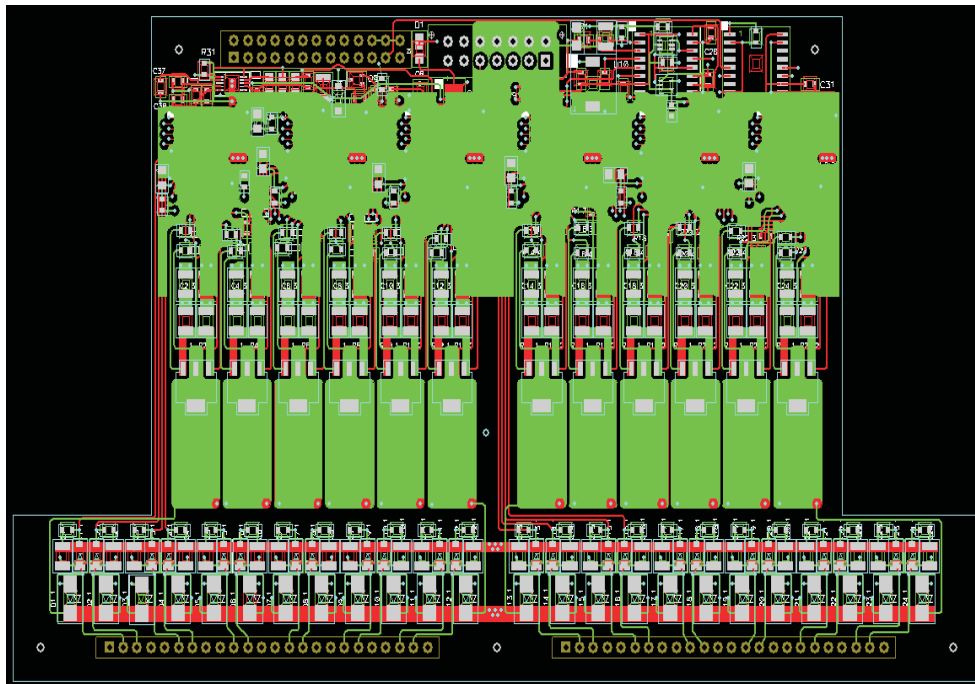


Figure 16. Top and Bottom Layers

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