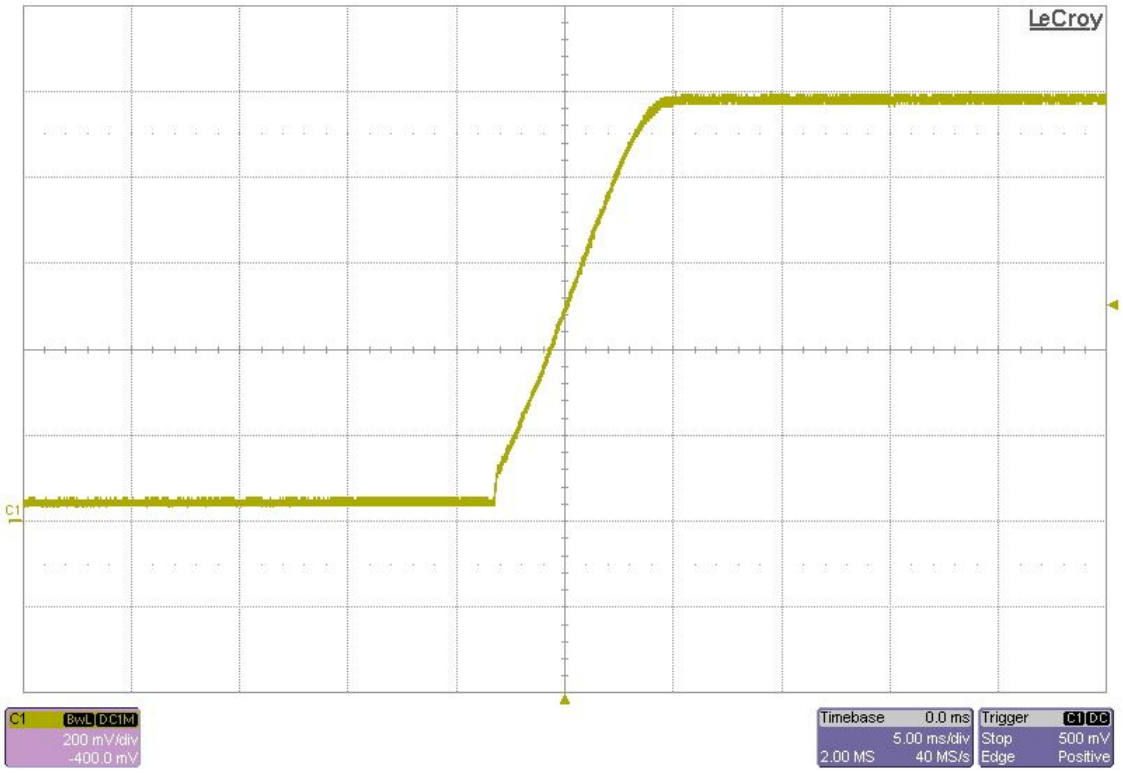
Abstract:

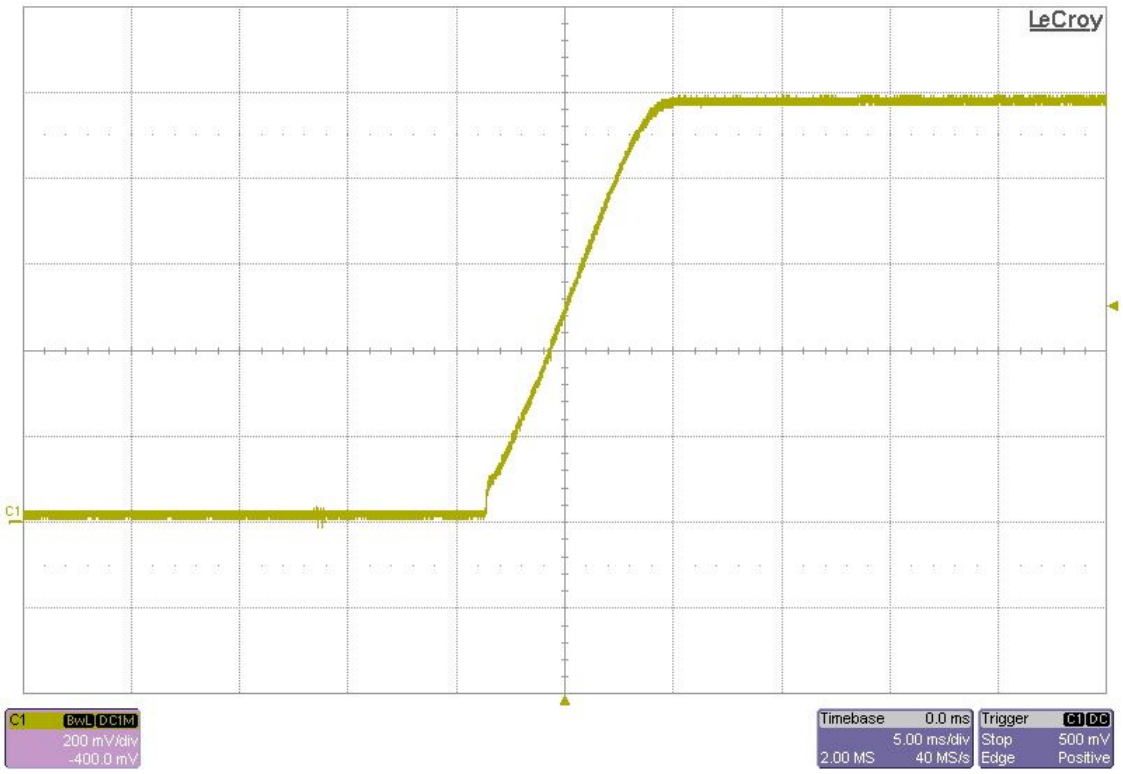
All the equations used to calculate component values in the PMP7303 design are located in the “Design Procedures” section of the TPS40322 Datasheet. The datasheet of the LM10010 details how to design the feedback network of the system.

1 Startup

Input voltage = 10V
Output voltage = 1V
Load current = 20A

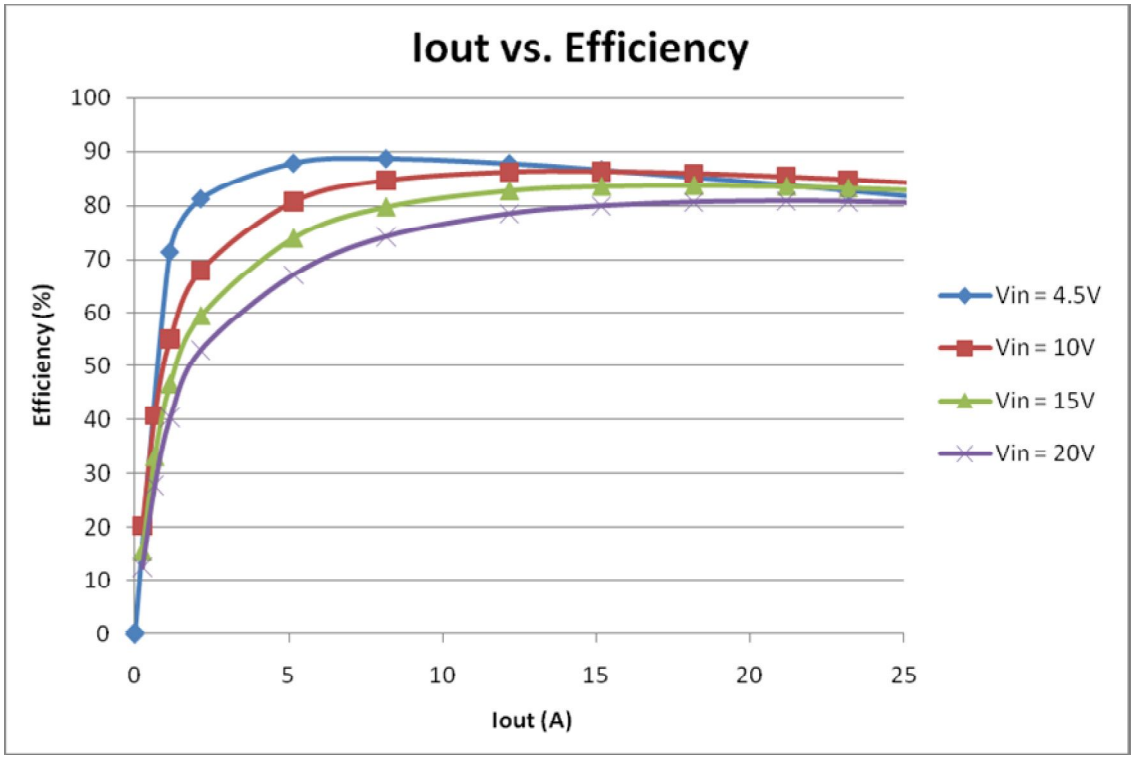


Input voltage = 10V
Output voltage = 1V
Load current = 0A



2 Efficiency

The efficiency is shown in the figure below.



VIN	IVIN	VOUT	ILOAD	EFFI%
0.00	0.000	0.995	0.000	0.00
4.50	0.100	0.995	0.002	0.53
4.50	0.352	0.995	1.133	71.32
4.50	0.583	0.995	2.138	81.18
4.50	1.297	0.995	5.147	87.77
4.50	2.035	0.995	8.154	88.58
4.50	3.066	0.995	12.161	87.70
4.50	3.875	0.995	15.166	86.55
4.50	4.716	0.995	18.173	85.21
4.50	5.591	0.995	21.179	83.76
4.50	6.196	0.995	23.182	82.73
4.50	6.821	0.995	25.191	81.67

VIN	IVIN	VOUT	ILOAD	EFFI%
10.00	0.115	0.994	0.235	20.33
10.00	0.155	0.994	0.637	40.81
10.00	0.205	0.994	1.137	55.04
10.00	0.313	0.995	2.138	67.88
10.00	0.636	0.997	5.147	80.64
10.00	0.960	0.997	8.154	84.62
10.00	1.406	0.997	12.161	86.17
10.00	1.751	0.996	15.167	86.26
10.00	2.106	0.996	18.172	85.91
10.00	2.472	0.996	21.178	85.29
10.00	2.722	0.996	23.182	84.77
10.00	2.979	0.996	25.191	84.19

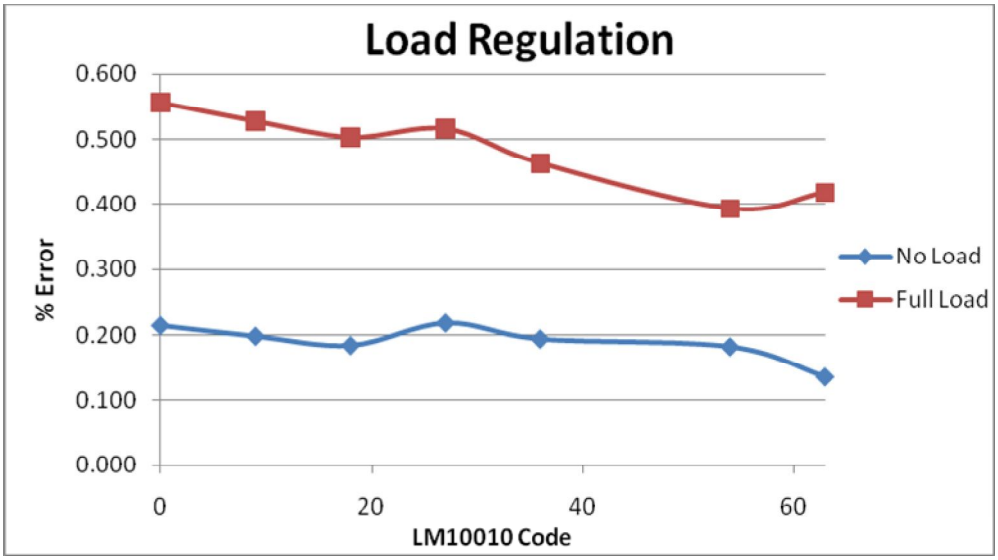
PMP7303 Test Results

VIN	IVIN	VOUT	ILOAD	EFFI%
15.00	0.100	0.994	0.235	15.52
15.00	0.127	0.994	0.638	33.20
15.00	0.161	0.994	1.138	46.77
15.00	0.238	0.995	2.139	59.58
15.00	0.464	1.002	5.148	74.03
15.00	0.682	1.001	8.154	79.83
15.00	0.979	1.000	12.160	82.84
15.00	1.208	1.000	15.167	83.65
15.00	1.444	0.999	18.172	83.83
15.00	1.686	0.999	21.178	83.63
15.00	1.852	0.999	23.182	83.35
15.00	2.021	0.998	25.190	82.97

VIN	IVIN	VOUT	ILOAD	EFFI%
19.99	0.094	0.994	0.236	12.53
19.99	0.114	0.994	0.638	27.88
19.99	0.140	0.994	1.138	40.40
19.99	0.201	0.995	2.140	53.06
19.99	0.385	1.005	5.148	67.11
19.99	0.552	1.004	8.155	74.19
19.99	0.778	1.003	12.161	78.45
19.99	0.952	1.002	15.168	79.89
19.99	1.130	1.002	18.173	80.59
19.99	1.311	1.001	21.179	80.83
19.99	1.437	1.000	23.182	80.72
19.99	1.565	1.000	25.190	80.49

3 Load Regulation (DC Accuracy with LM10010)

The max error that can be tolerated in terms of Vout on the DSP was given to be 5%. The goal of the design was to keep the DC error to a max 2.5%, in order to allow for room to compensate for the AC error.
There are 4 main contributors to the final error seen on the output. They are: the error caused by the LM10010 (2%max), feedback voltage error, the error of resistors in the feedback network, and the load regulation error from the IC. If the compilation of these errors are more than the targeted 2.5%, they can be decreased by using higher precision resistors(.1% or .5%), choosing an IC to minimize the feedback voltage error as well as the load regulation error, and to use the LM10010.
Below shows the total DC error seen on the output of the PMP7303. The expected output voltage was calculated using the spreadsheet titled "LM10010_Error_Analysis_locked.xlsx". Please add the load regulation error to the "feedback Voltage error" input. The feedback network resistors were doubled in value and put in parallel to reduce the feedback error of the system. The resistors were precise to 1%. The IC, TPS40322, has a max load regulation error of 0.5% and a feedback voltage error of 1%.The load regulation of the output is shown in the graph below.



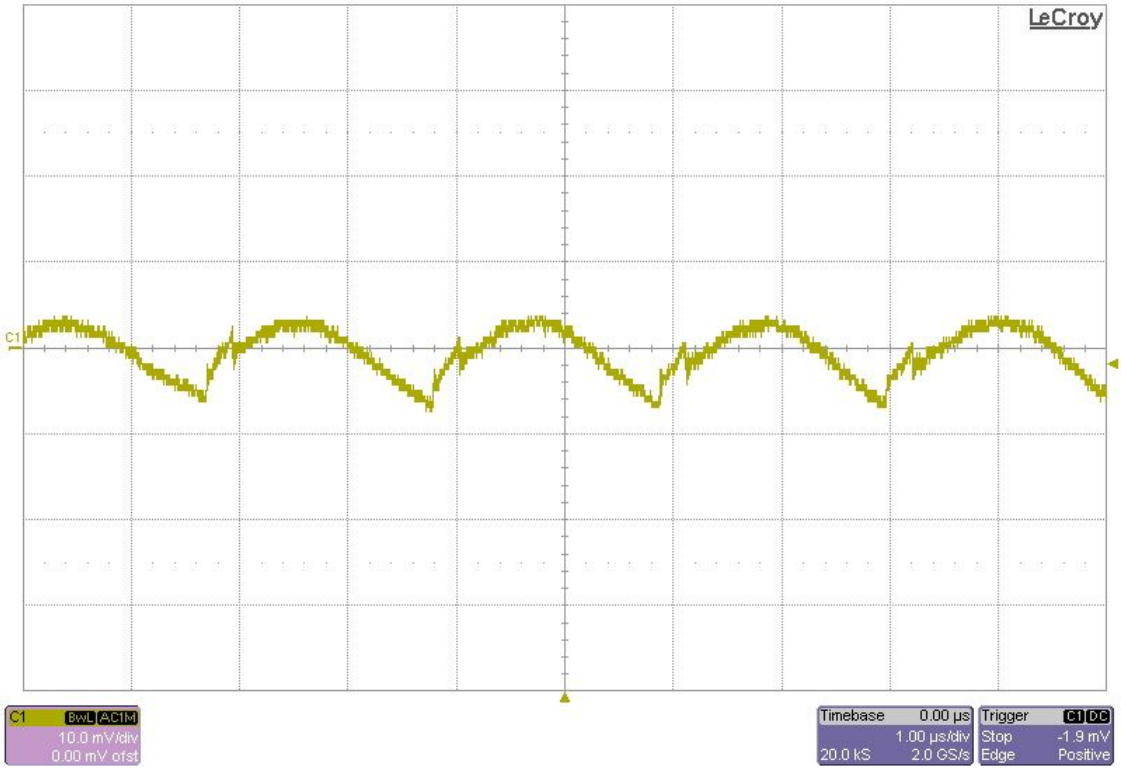
	LM10010 Code	Expected output voltage	Vout_act (no load)	%ERROR (No load)	Vout_act (full load)	%ERROR (Full load)
VIDA,B,C=0	0	0.7004	0.7019	0.214	0.7043	0.557
VIDA=1	9	0.7575	0.759	0.198	0.7615	0.528
VIDB=1	18	0.8146	0.8161	0.184	0.8187	0.503
VIDA,B=1	27	0.8717	0.8736	0.218	0.8762	0.516
VIDC=1	36	0.9287	0.9305	0.194	0.9330	0.463
VIDB,C=1	54	1.0429	1.0448	0.182	1.0470	0.393
VIDA,B,C=1	63	1.1000	1.1015	0.136	1.1046	0.418

Various VID codes (column 2) were used as input to the LM10010. Vout was measured with no load(Vout_act(no load)) and at full load (Vout_act (full load)) to show the load regulation error. Percent error shows the difference between the expected output voltage and the measured output voltage, both at no load and full load.

4 Output Ripple Voltage

The output ripple voltage is shown in the figure below.

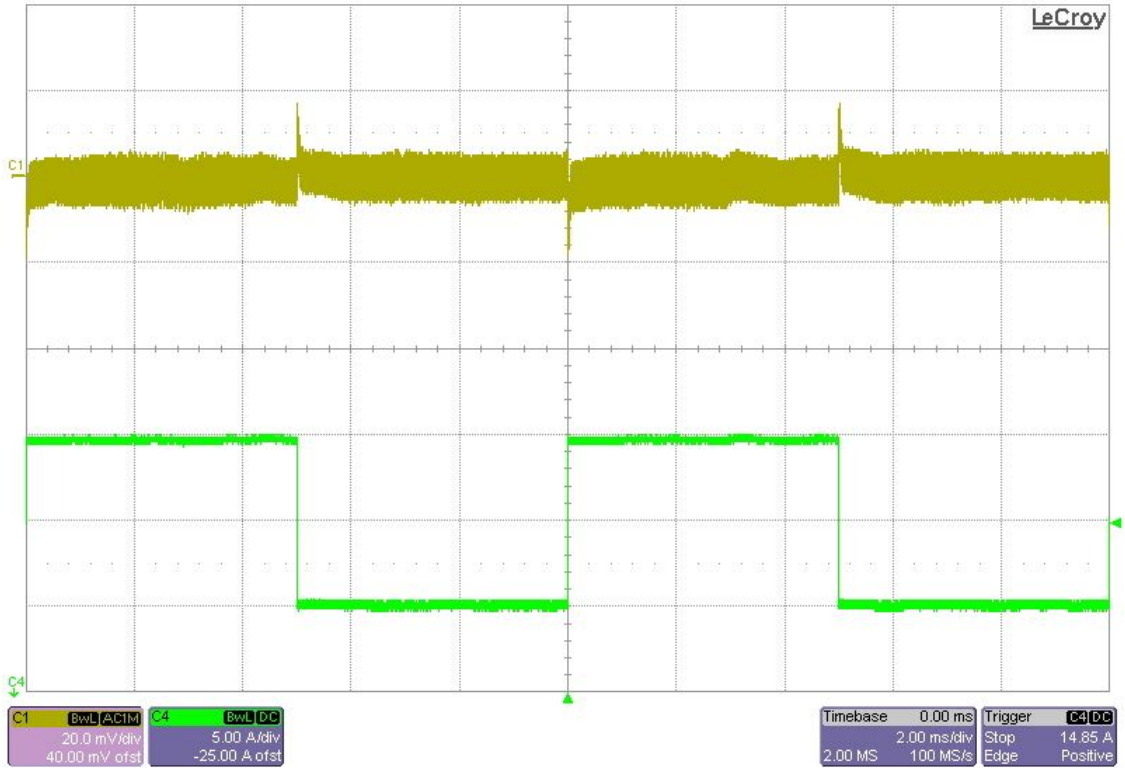
Input voltage = 10V
Output voltage = 1V
Load current = 25A

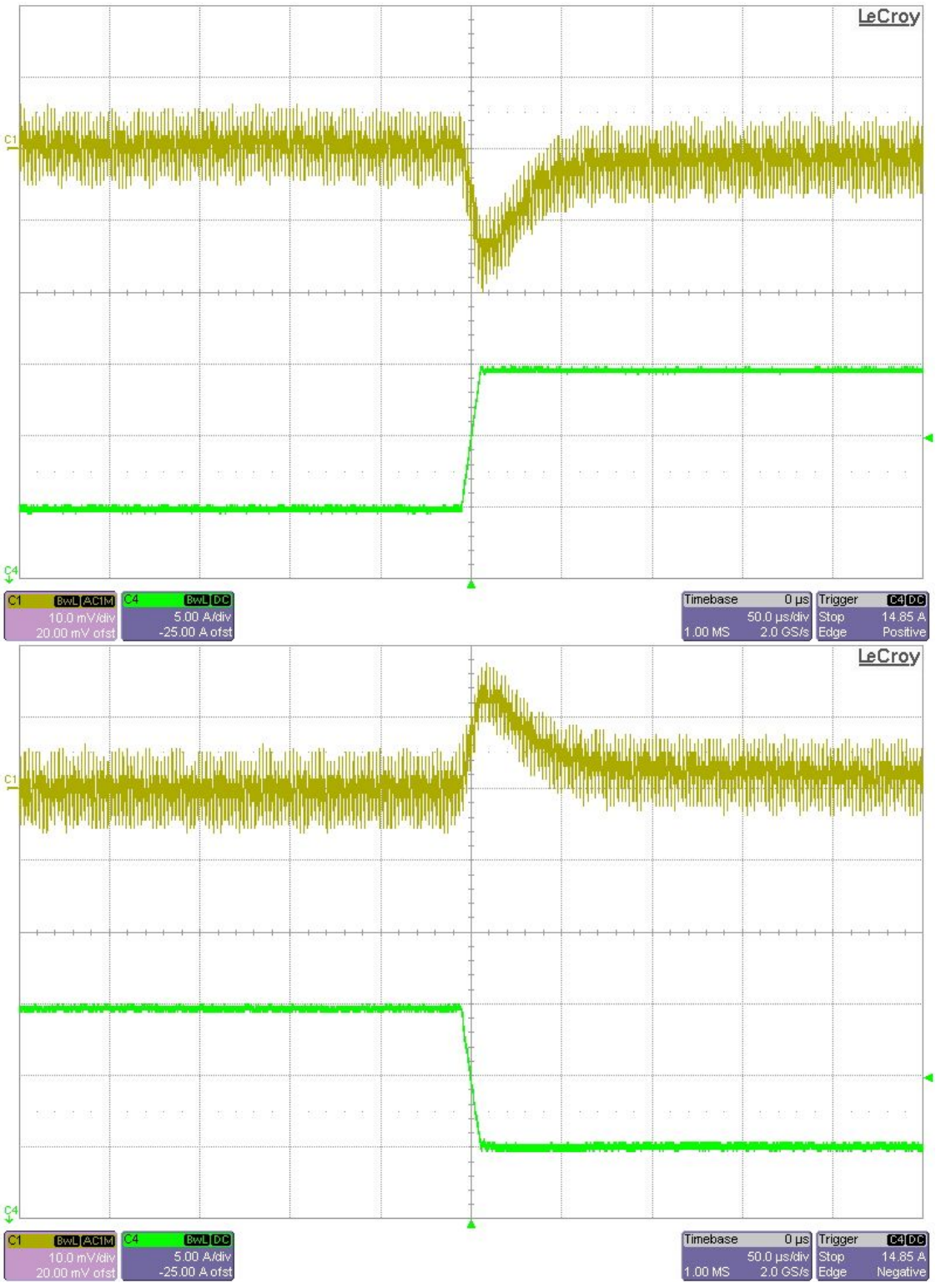


5 Load Transients

The figures below show output response to 10-20A load transients. The input voltage was set to 10V.

Channel 1 : Vout (AC coupled)
Channel 4 : Load current

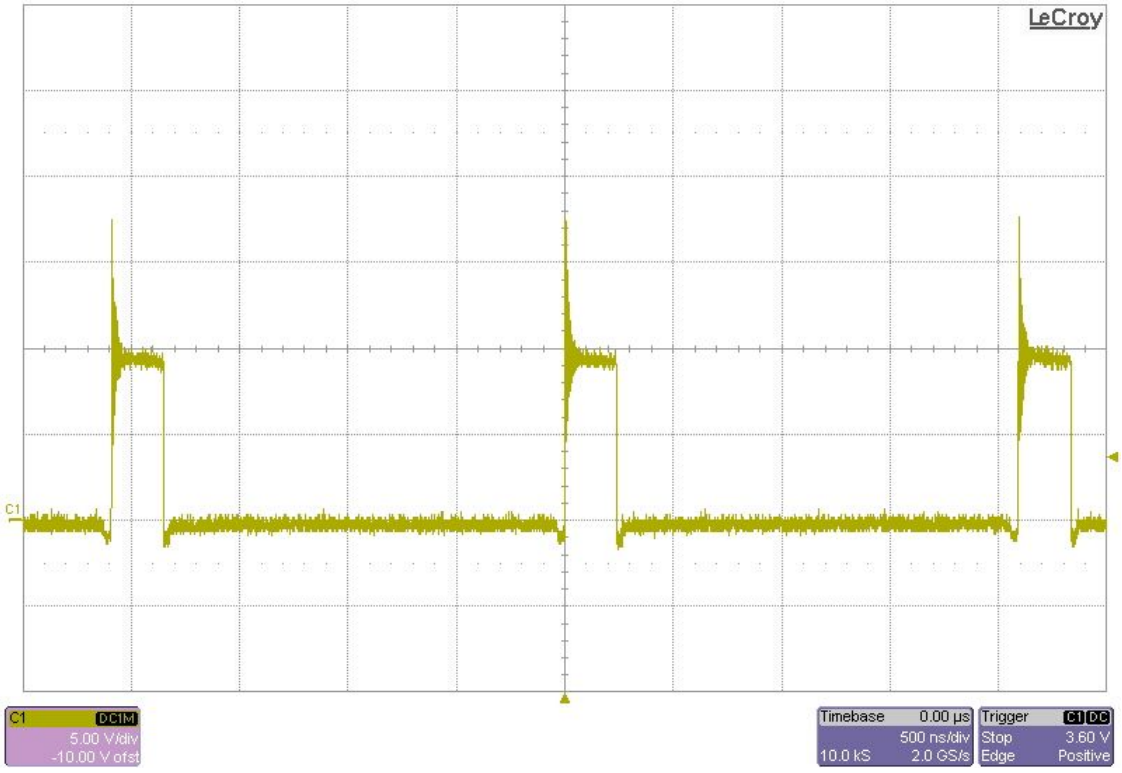



LeCroy
C1
C4
C1 BwL ACTM
10.0 mV/div
20.00 mV ofst
C4 BwL DC
5.00 A/div
-25.00 A ofst
Timebase 0 µs
50.0 µs/div
1.00 MS 2.0 GS/s
Trigger C4 DC
Stop 14.85 A
Edge Positive
LeCroy
C1
C4
C1 BwL ACTM
10.0 mV/div
20.00 mV ofst
C4 BwL DC
5.00 A/div
-25.00 A ofst
Timebase 0 µs
50.0 µs/div
1.00 MS 2.0 GS/s
Trigger C4 DC
Stop 14.85 A
Edge Negative

6 Switch Node Waveforms

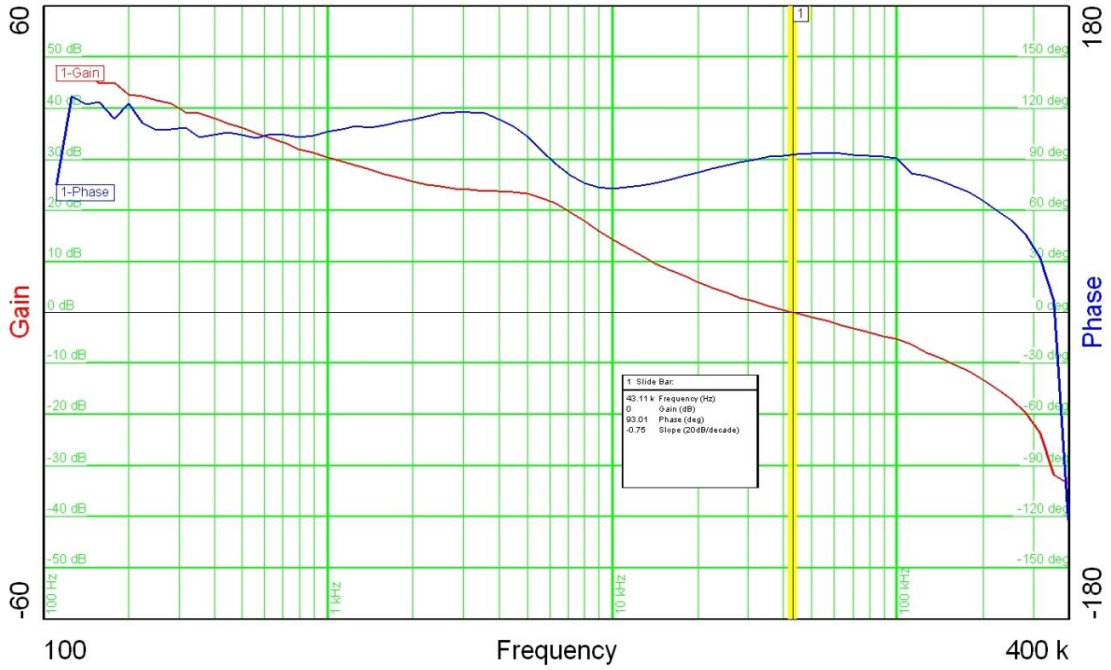
The following figures show the full bandwidth switch node waveforms at:

Input voltage = 10V
Output voltage = 1V
Load current = 25A (full BW)



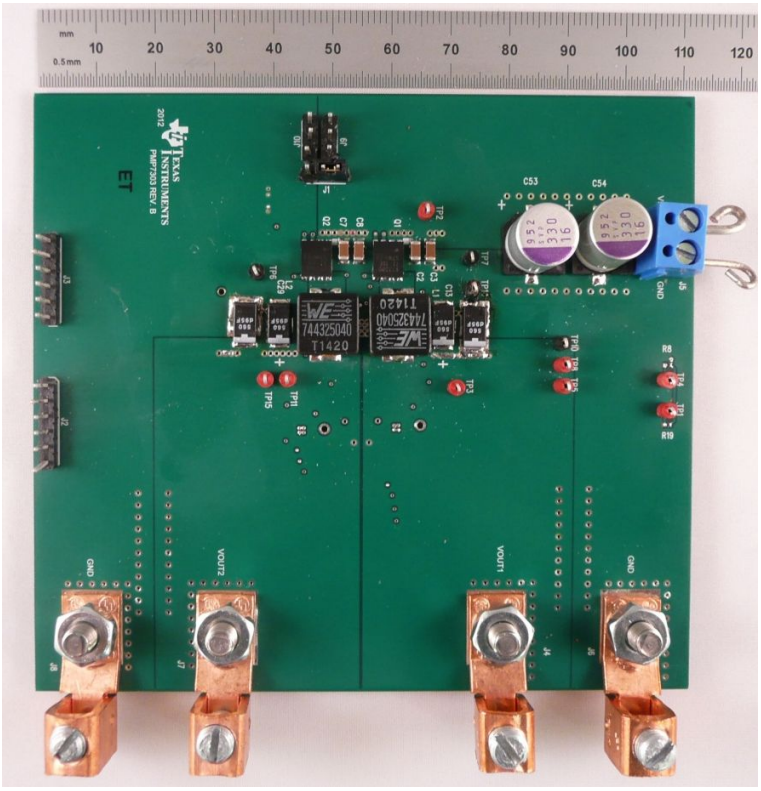
7 Control Loop Frequency Response

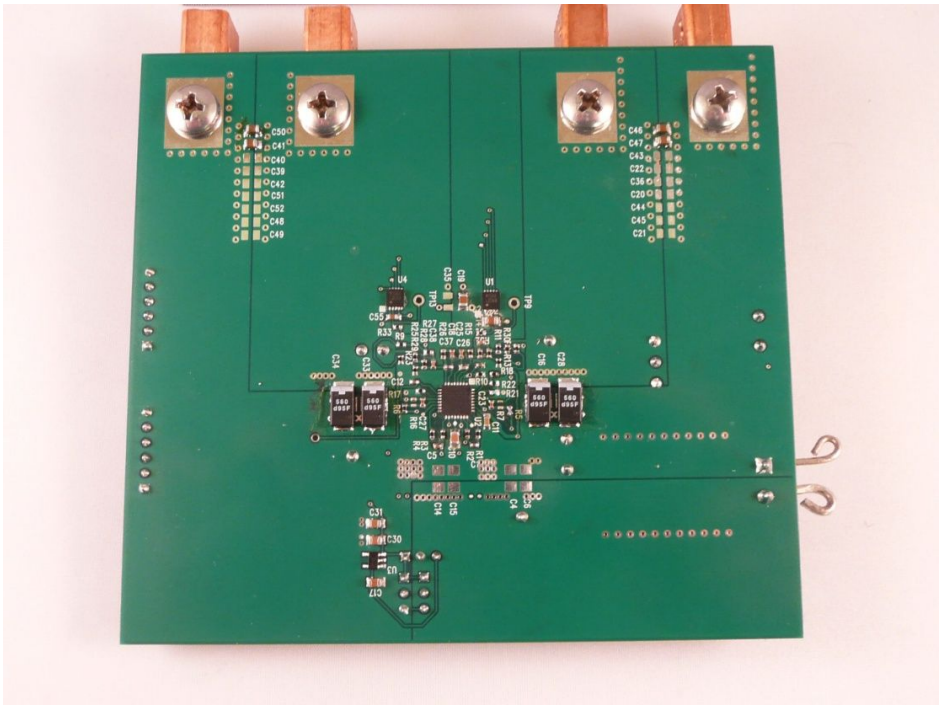
Input voltage = 10VDC
Output voltage = 1V
Load current = 25A
Phase margin = 93.01°
Bandwidth = 43.11kHz



8 Photo

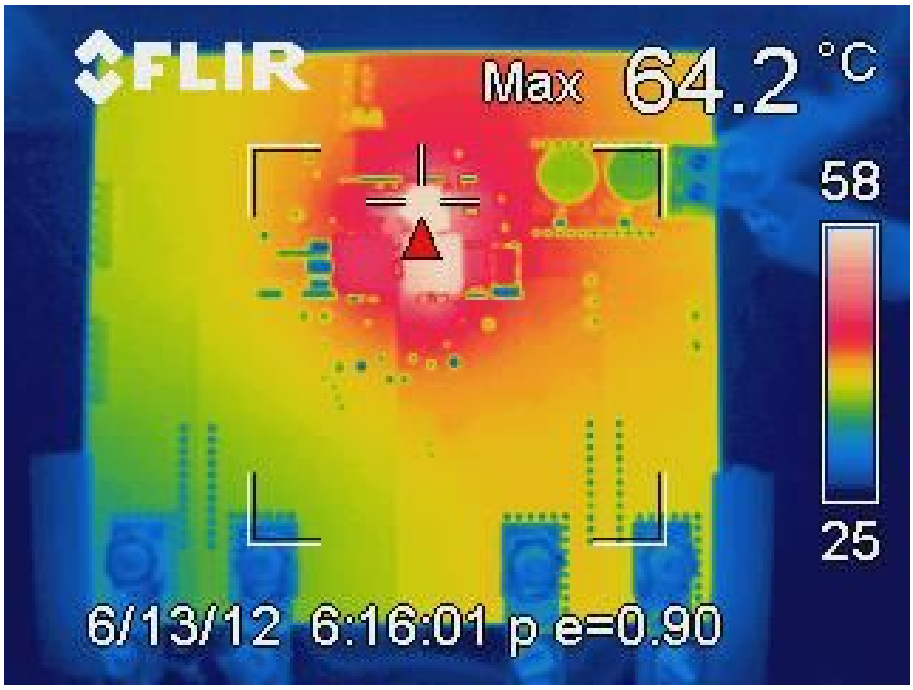
The images below show the top and bottom view, respectively, of the PMP7303 REVB prototype board.

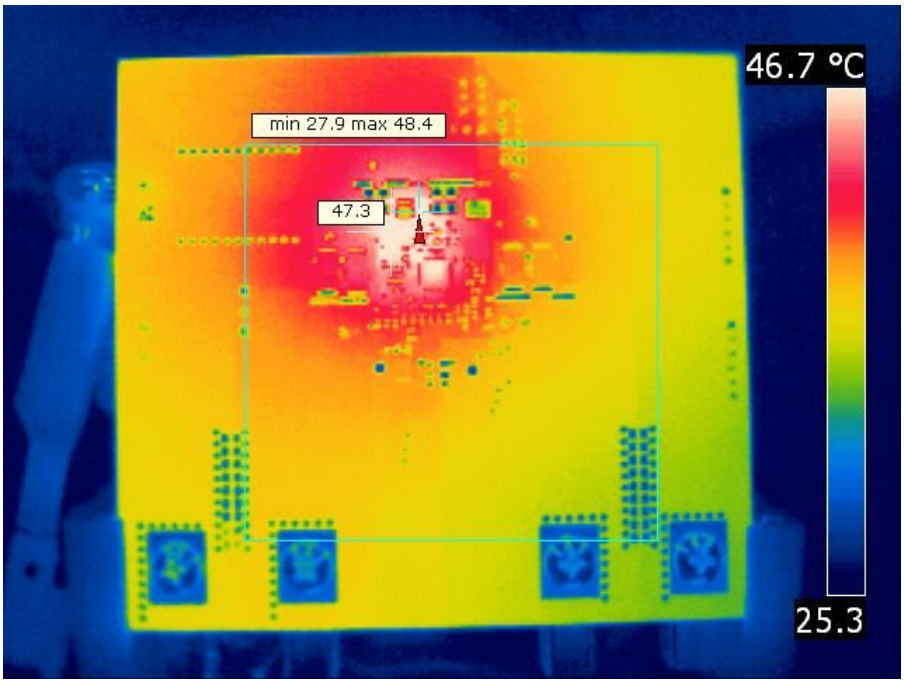




9 Thermal Analysis

The images below show the infrared images (top and bottom, respectively) taken from the FlexCam after 10min at full load (1V@25A). Input voltage = 10 VDC.





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