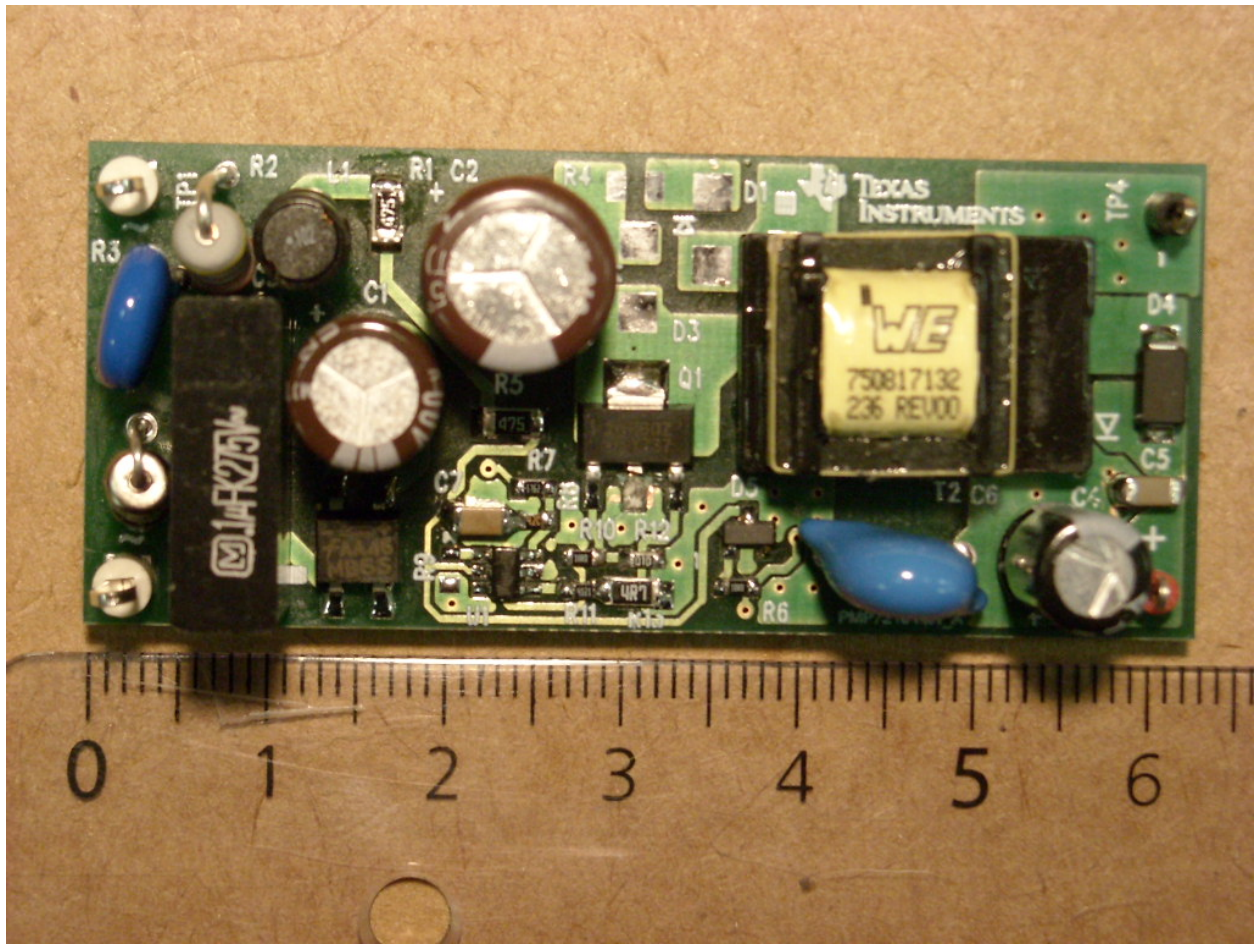


PHOTO OF THE PROTOTYPE:

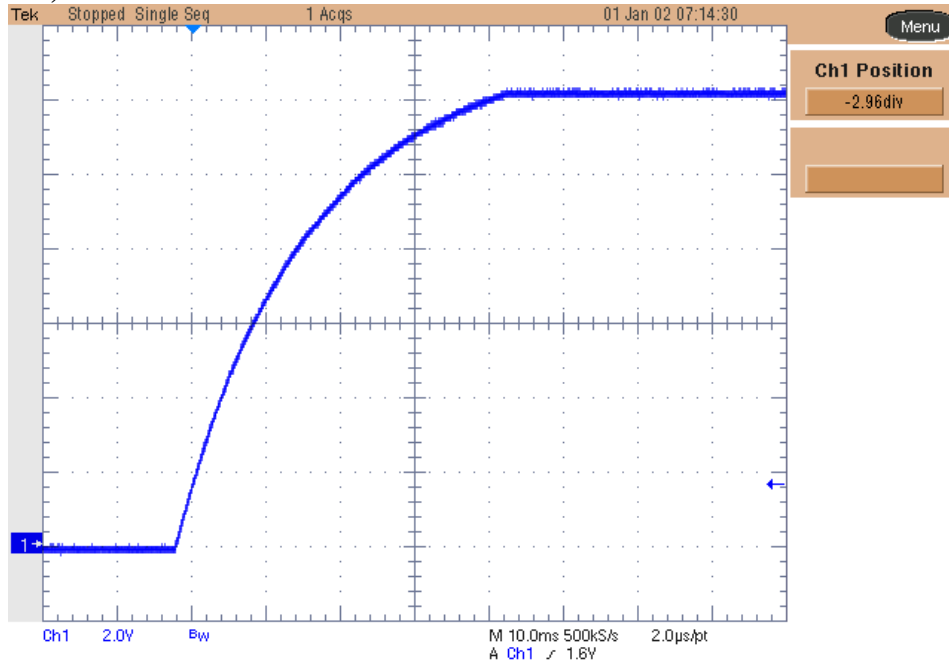


1 Startup

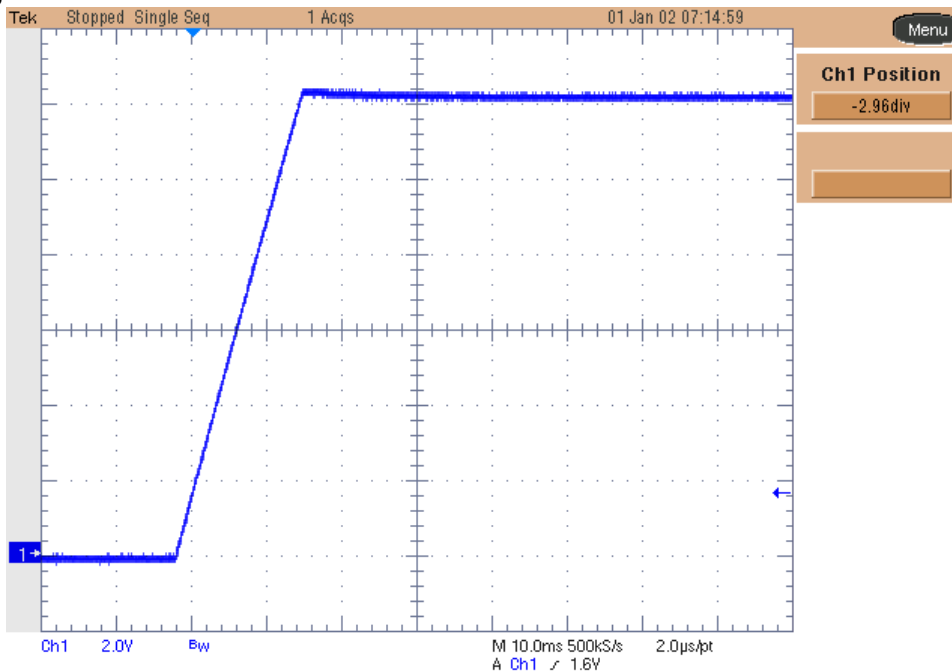
The output voltage behavior at startup is shown in the images below. The input voltage was set to 230Vac, 50Hz. The output fully loaded in the upper picture and unloaded for the bottom one.

Ch.1: Output voltage (2V/div, 10ms/div, DC coupling, 20MHz BWL)

I_{out} = 150mA;

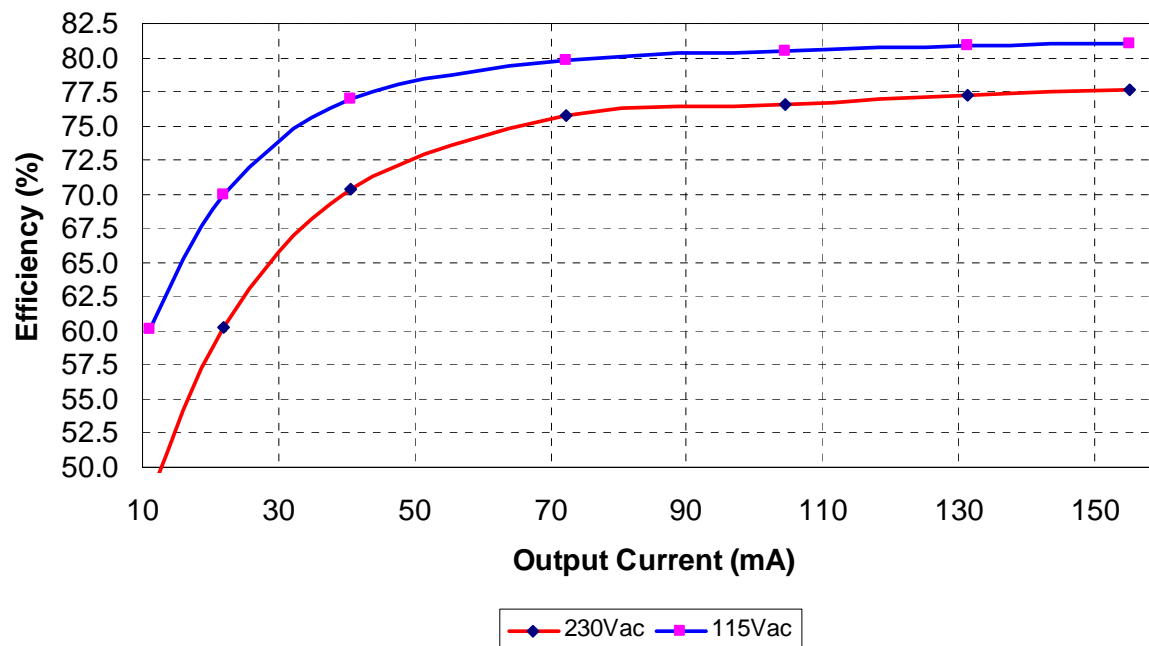


I_{out} = 0A;



2 Efficiency

The efficiency data are shown in the tables and graph below. A digital power meter Yokogawa WT210 has been used and the input AC voltage set to 115Vac, 60Hz and 230Vac, 50Hz.

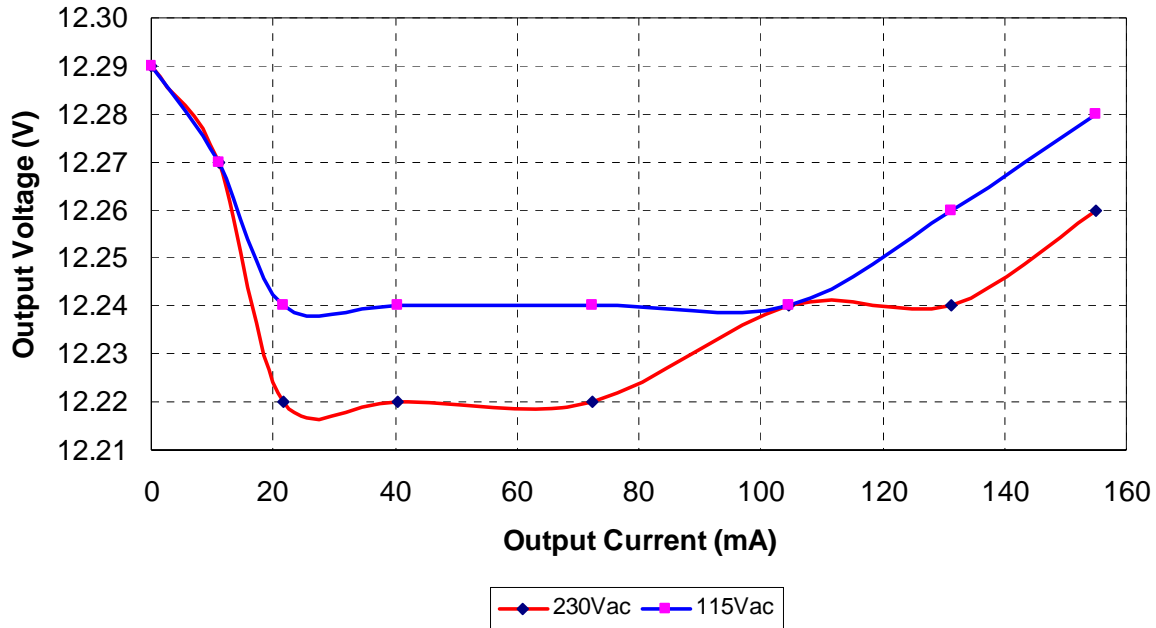


Iout (mA)	Vout (V)	Pout (W)	Pin (W)	Vin (Vac)	Ploss (W)	Eff (%)
0	12.29	0	0.0285	230	0.029	0.00
11.03	12.27	0.135	0.283	230	0.148	47.82
21.78	12.22	0.266	0.442	230	0.176	60.22
40.51	12.22	0.495	0.703	230	0.208	70.42
72.4	12.22	0.885	1.167	230	0.282	75.81
104.6	12.24	1.280	1.671	230	0.391	76.62
131.2	12.24	1.606	2.080	230	0.474	77.21
155.0	12.26	1.900	2.448	230	0.548	77.63

Iout (mA)	Vout (V)	Pout (W)	Pin (W)	Vin (Vac)	Ploss (W)	Eff (%)
0	12.29	0	0.0167	115	0.017	0.00
11.02	12.27	0.135	0.225	115	0.090	60.10
21.78	12.24	0.267	0.381	115	0.114	69.97
40.52	12.24	0.496	0.644	115	0.148	77.01
72.4	12.24	0.886	1.11	115	0.224	79.84
104.5	12.24	1.279	1.59	115	0.311	80.45
131.2	12.26	1.609	1.99	115	0.381	80.83
155.0	12.28	1.903	2.35	115	0.447	81.00

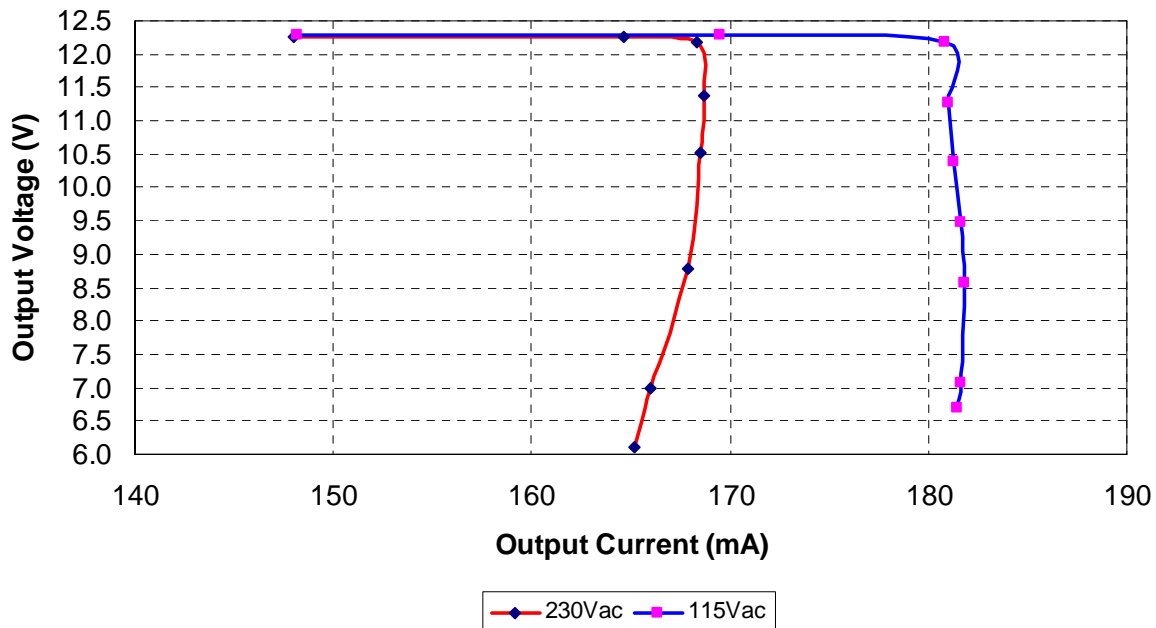
3 Output Voltage Regulation

The output voltage variation as function of load and input voltage is shown below:



4 Output Current Limit Behavior

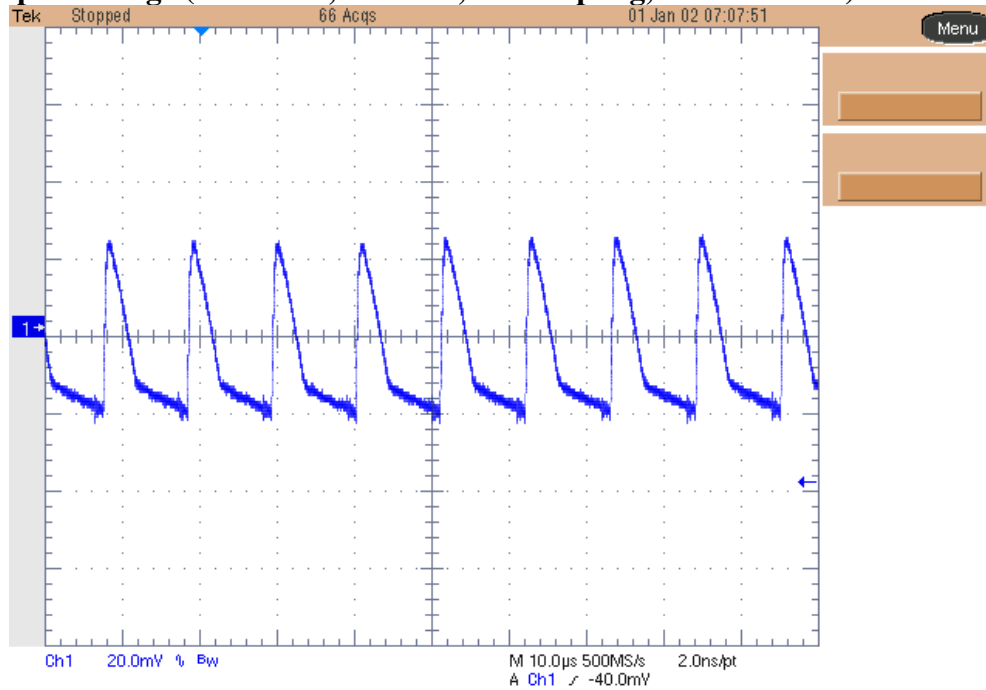
The output current limit behavior is shown below; a variable resistor has been connected to the output. The last two points show the converter's voltage before switching OFF.



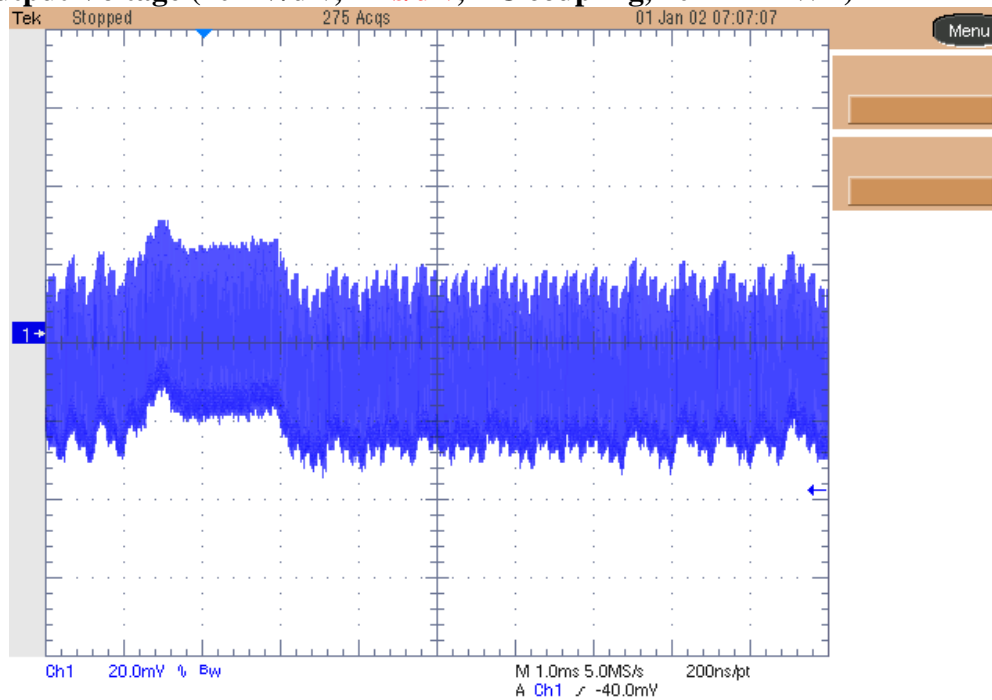
Output Ripple Voltage

The output ripple voltage is shown in the plots below. The input was set to 230Vac and the output fully loaded. The bottom picture shows the ripple variation due to dithering.

Ch.1: Output Voltage (20mV/div, 10us/div, AC coupling, 20MHz BWL)



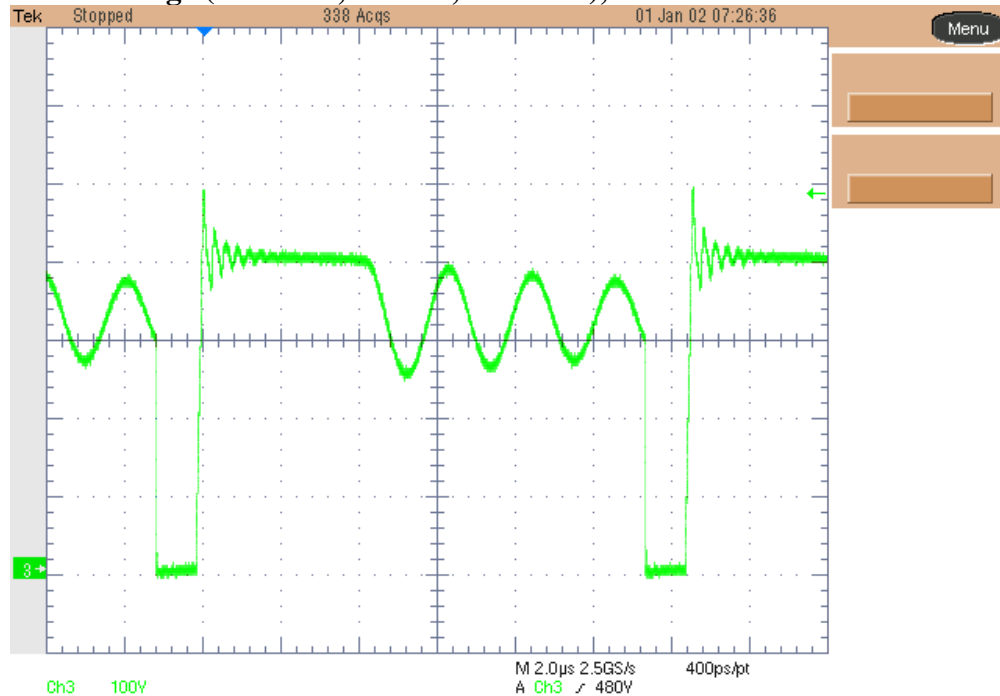
Ch.1: Output Voltage (20mV/div, 1ms/div, AC coupling, 20MHz BWL)



5 Switching Node Waveform

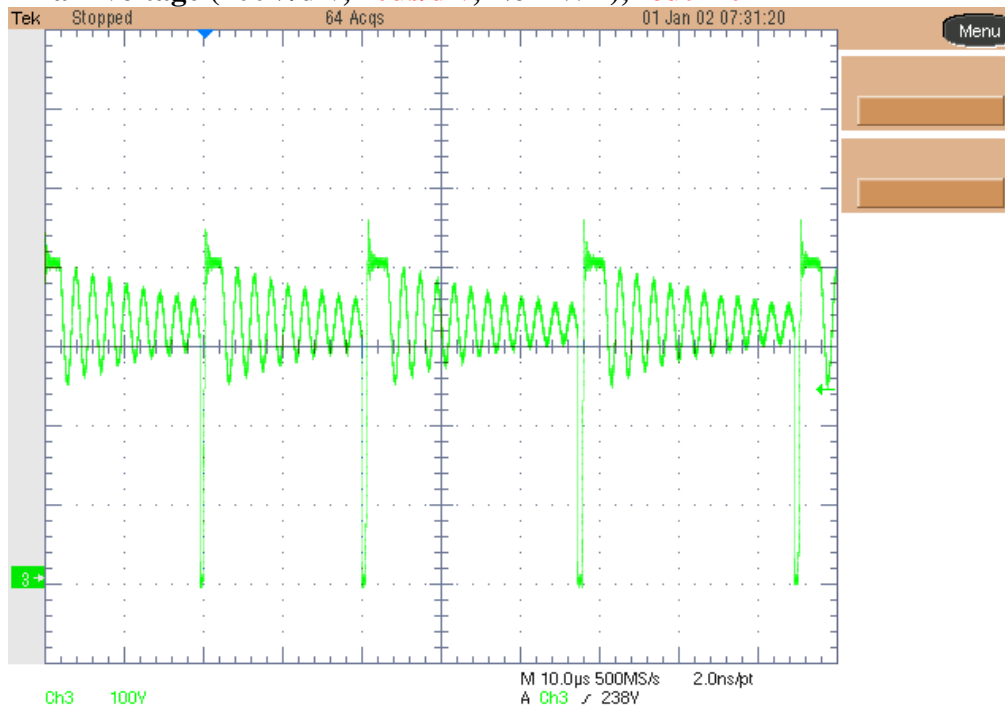
The images below show the peak voltage on the drain of the Mosfet Q1 with a 230Vac input at different loads, as well as the voltage on D4.

Ch3: Q1 Drain voltage (100V/div, 2us/div, No BWL), full load.

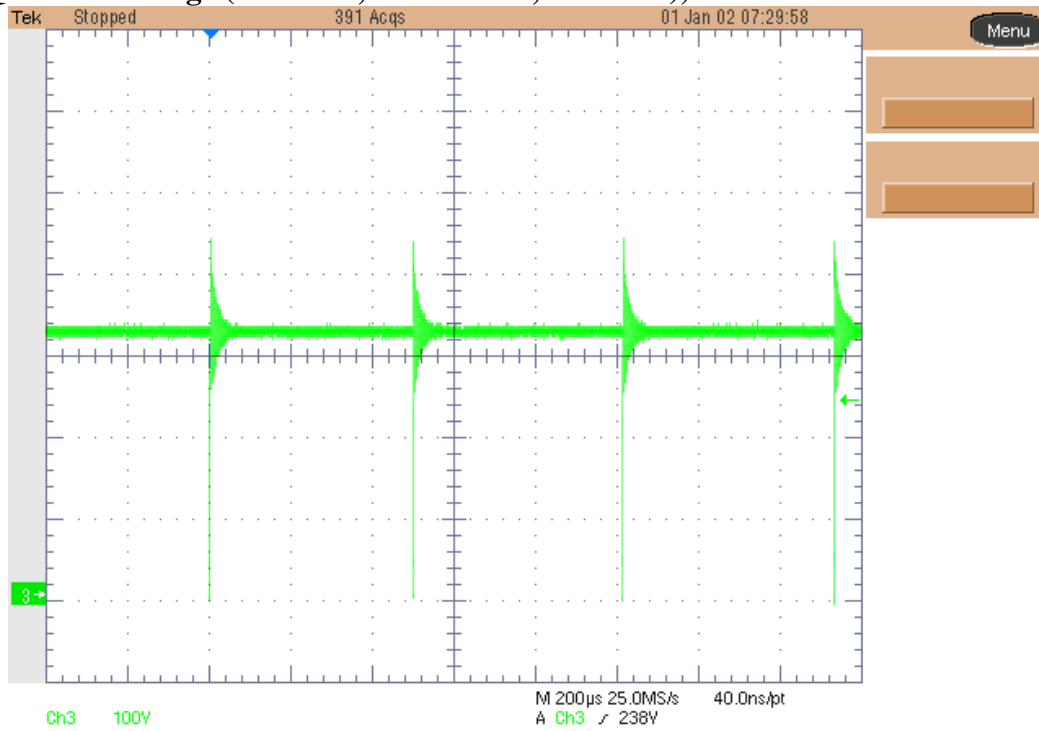


At light load, the converter reduces the switching frequency as shown in the picture below.

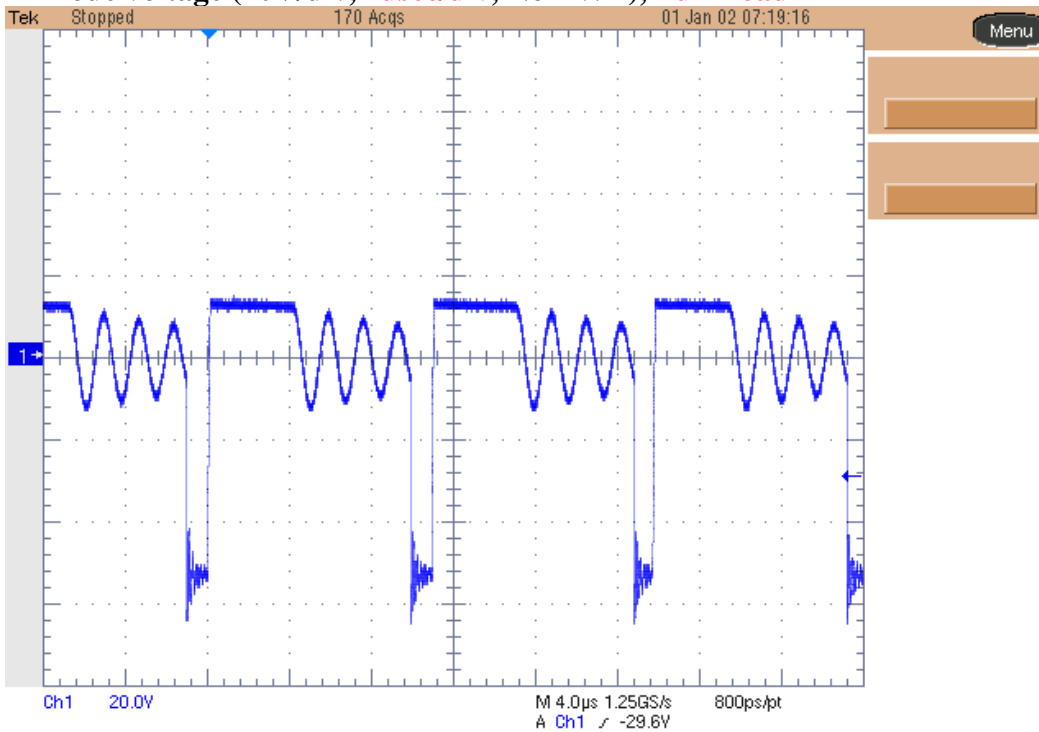
Ch3: Q1 Drain voltage (100V/div, 10us/div, No BWL), Iout=20mA



Ch3: Q1 Drain voltage (100V/div, 200usec/div, No BWL), No Load



Ch1: D4 Anode voltage (20V/div, 4usec/div, No BWL), Full Load

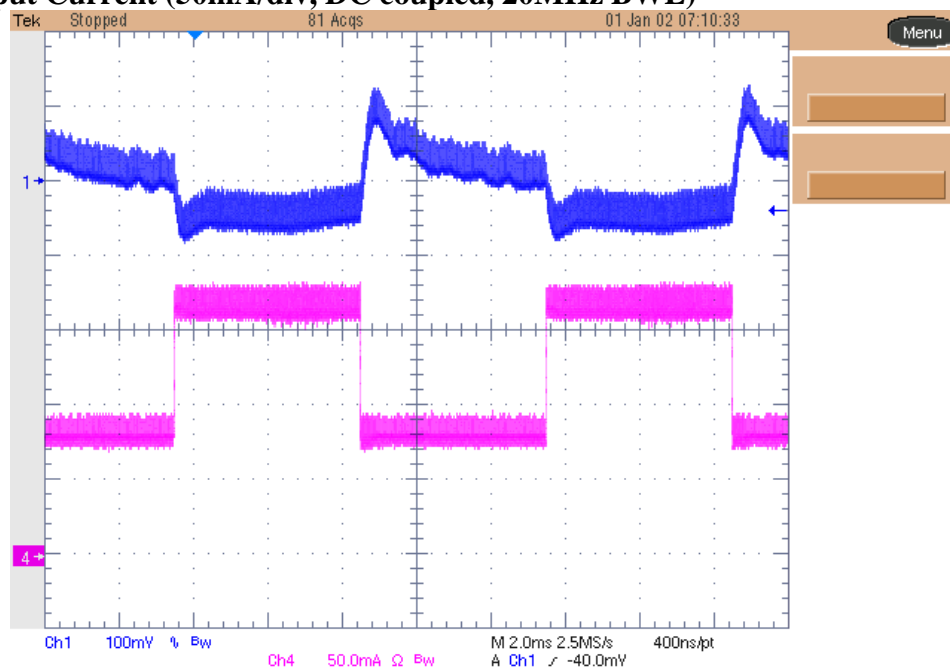


6 Transient Response

The images below show the transient response on the output voltage when the load has been switched between 50% and 100% of the nominal value (upper picture) and from 0% to 100% (bottom picture). The input voltage was set to 230Vac.

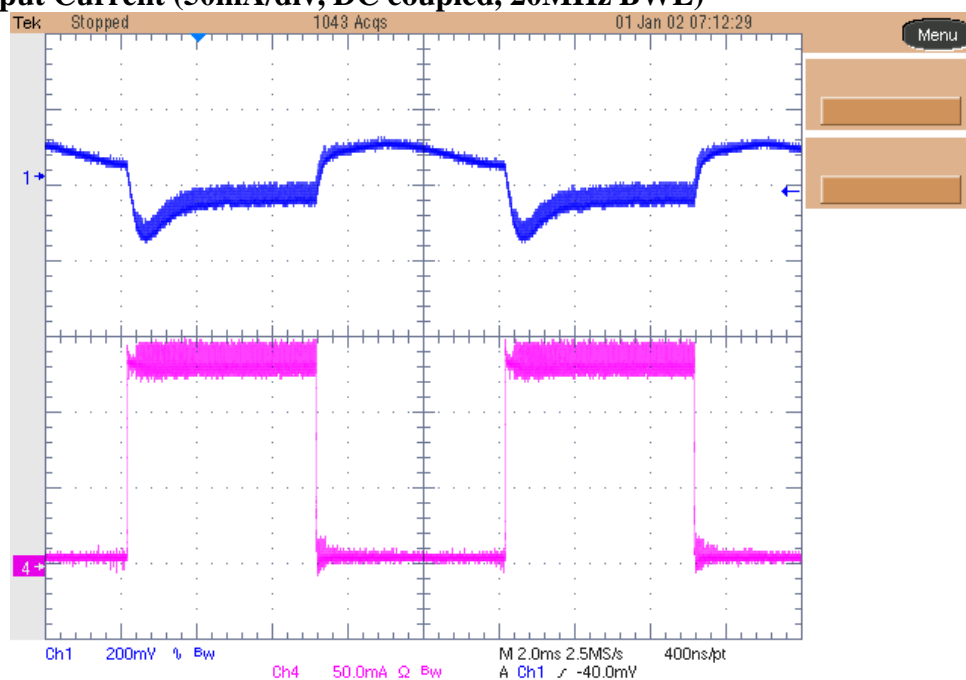
Ch1: Output Voltage (100mV/div, 2ms/div, AC coupled, 20MHz BWL).

Ch4: Output Current (50mA/div, DC coupled, 20MHz BWL)



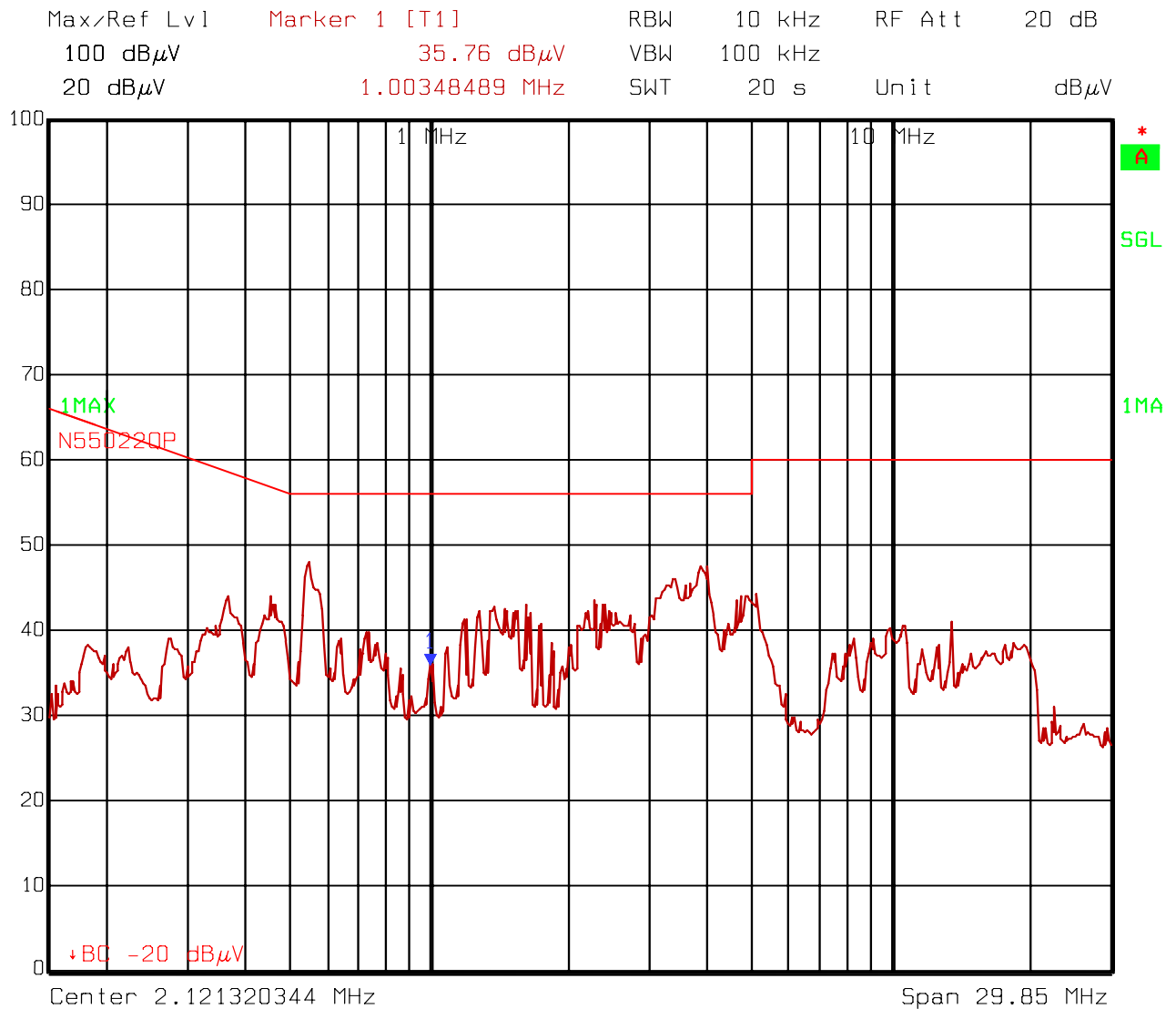
Ch1: Output Voltage (200mV/div, 2ms/div, AC coupled, 20MHz BWL).

Ch4: Output Current (50mA/div, DC coupled, 20MHz BWL)



7 EMI Measurement

The graph below shows the conducted emission EMI noise and the EN55022 Class-B Quasi-Peak limits (measurement from the worst case line). The load was connected to a LISN and an isolation transformer; the load was a power resistor, set to 80 Ohm (152mA load), while the input voltage was 230Vac. The receiver was set to Quasi-peak detector, 10 KHz bandwidth.



Title: FF1o1
 Date: 4.OCT.2012 15:09:24

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